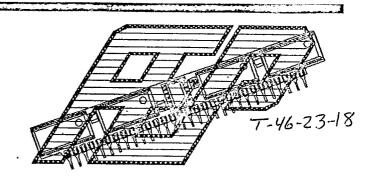
- >> 1,048,576 x 9 Organization
- >> 30 pin \$IP
- >> Low 0.510 inch stand-off height
- >> Optional PARITY CHECKER on board
- >> Single +5V power supply
- >> TTL compatible
- >> Pin for pin compatible with standard modules (without parity checker)
- >> Available in 1M x 8 organization



## 1 MEGAWORD BY 9 BIT LOW PROFILE DYNAMIC RAM MODULE WITH PARITY CHECKER

#### **DESCRIPTION:**

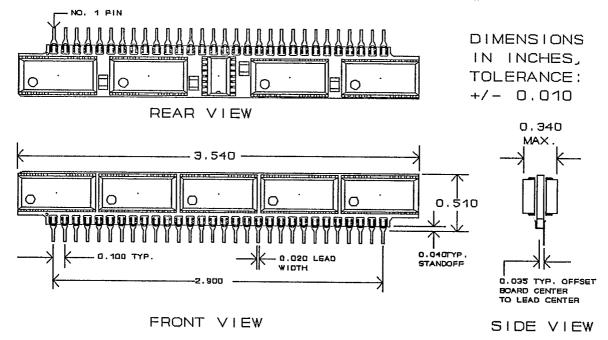
The AEPDX1M9L is a low profile 1 megaword by 9 bit dynamic random access memory module in a 30 pin single inline package format. Physically it consists of an FR4 PC material substrate mounted with nine 1M x 1 SOJ (small outline J-leaded package) ICs, the 74F280 parity checker, four 0.18 microfarad capacitors, and 30 edge clip I/O pins.

The module can use any of the 1M  $\times$  1 SOJs available from multiple manufacturers in both NMOS and low power CMOS technologies and with a variety of access speeds.

Power dissipation is also determined by the ICs used but is typically 50 milliwatts in standby and 2.5 to 3.5 watts when active (ratings for the CMOS version without the parity checker). A single 5V power supply is required.

Variations available are a 1M  $\times$  9 without the parity checker (making it compatible with standard 1M  $\times$  9 modules); a 1M  $\times$  8 (by omitting the 9th DRAM IC and the parity checker); or any of these with 90 degree lead pins, allowing them to be mounted on their sides thus giving a 0.350 stand-off height.

# SPECIFICATION DRAWING 1Mx9 LOW PROFILE DRAM WITH PARITY CHECKER - 30 PIN SIP



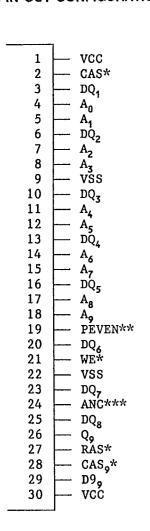


#### 1 MEGABYTE x 9 LOW PROFILE DYNAMIC RAM MODULE

### SIP PIN OUT CONFIGURATION

### **FUNCTIONAL DIAGRAM**

T-46-23-18



- \* ACTIVE WHEN LOW
- \*\* NO CONNECT WHEN OPTIONAL PARITY CHECKER IS OMITTED.
- \*\*\* ANC FOR NEXT GENERATION 4Mx9 MODULE.

