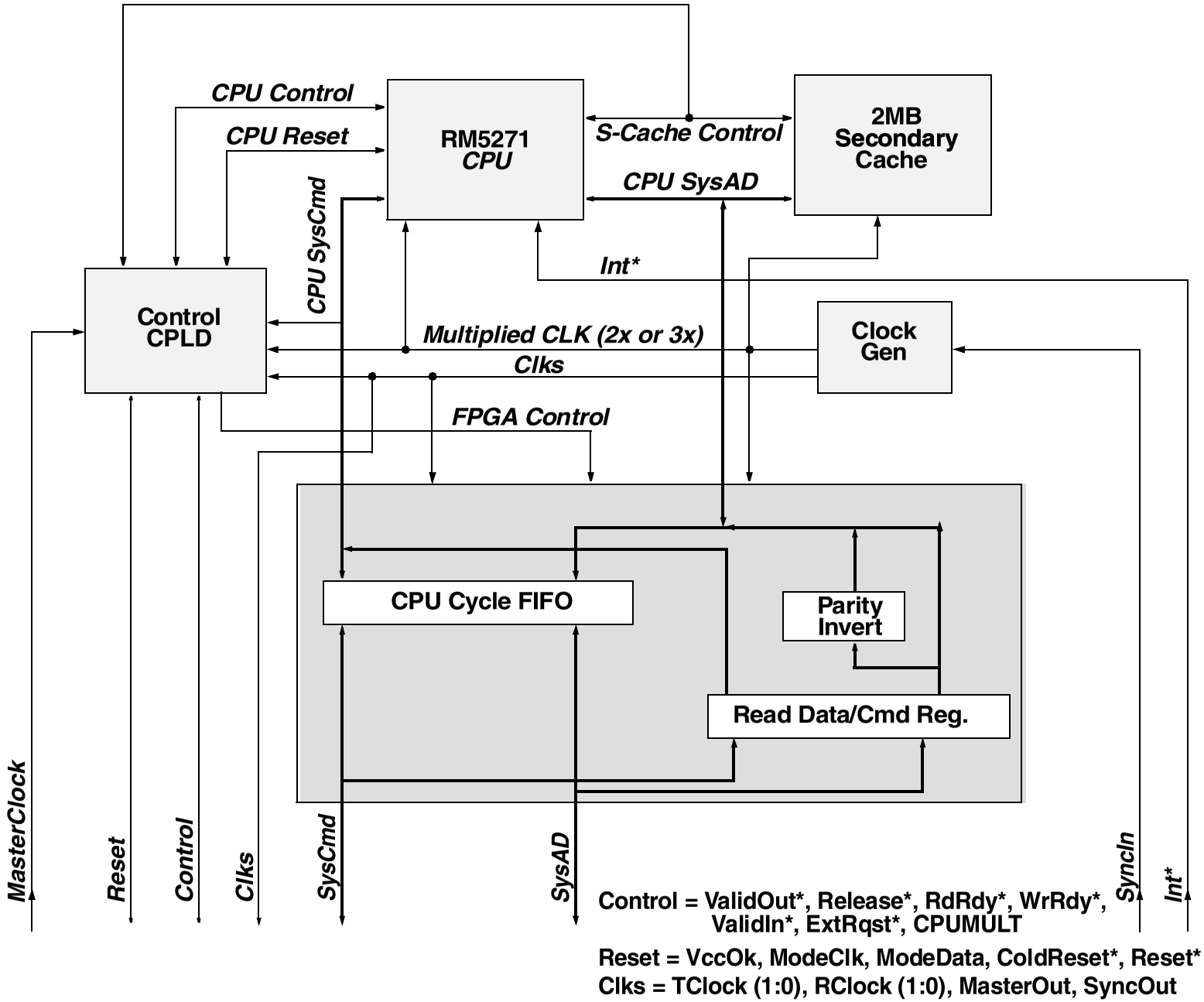
ACT-5271SC Multichip Module
Microprocessor with 2MB Secondary Cache

Features

- Footprint Compatible with Aeroflex's original ACT-4431SC 1MB Secondary Cache MCM in the 280 lead Ceramic Quad Flat Pack (CQFP)
- QED RM5271 Dual Issue superscalar microprocessor - can issue one integer and one floating-point instruction per cycle
  - Max system clock – 25MHz, Max Secondary Cache (SC) clock 75MHz, Max pipeline 150MHz
- High performance system interface compatible with R4400
  - Internal PLL generates selectable 2x/3x SC bus speed operation vs external system bus speed
  - Generates R4400 style system clocks
  - CPU cycle rate buffering FIFO implemented in FPGA
  - 64-bit multiplexed system address/data bus for optimum price/performance
  - High performance write protocols maximize uncached write bandwidth
  - Operates at processor clock multipliers 2, 2.5 & 3
- Integrated on-chip Primary Caches
  - 32KB instruction - 2 way set associative
  - 32KB data - 2 way set associative
  - Virtually indexed, physically tagged
  - Write-back and write-through on per page basis
  - Pipeline restart on first double for data cache misses
- Integrated in-module Secondary Cache
  - 2MB shared write-through
  - 4-128K x 36 Synchronous SRAM and 1-64K x 18 Tag RAM
- Integrated memory management unit
  - Fully associative joint TLB (shared by I and D translations)
  - 48 dual entries map 96 pages
  - Variable page size (4KB to 16MB in 4x increments)
- High-performance floating point unit
  - Single cycle repeat rate for common single precision operations and some double precision operations
  - Two cycle repeat rate for double precision multiply and double precision combined multiply-add operations
  - Single cycle repeat rate for single precision combined multiply-add operation
- MIPS IV instruction set
  - Floating point multiply-add instruction increases performance in signal processing and graphics applications
  - Conditional moves to reduce branch frequency
  - Index address modes (register + register)
- Embedded application enhancements
  - Specialized DSP integer Multiply-Accumulate instruction and 3 operand multiply instruction
  - I and D cache locking by set
  - Optional dedicated exception vector for interrupts



ACT-5271SC SIMPLIFIED BLOCK DIAGRAM

Description

The ACT-5271SC MCM consists of a QED RM5271 MIPS microprocessor with 2 MByte of shared, write-through Secondary Cache. The MCM translates the R4400 style clocking, bus and modebit information to what the RM5271 expects. This is accomplished by means of a PLL clock generator, a control CPLD and an FPGA based cycle FIFO.

Pinout Compatibility

The ACT-5271SC was designed as a high performance upgrade replacement for the ACT-4431SC. The 280 lead flatpack package outline was retained and the pinout is compatible, with the following exceptions:

- The reassignment of twenty-six - 3.3 volt supply pins to a core voltage of 2.5 volts.
- VccP, the quiet PLL supply is now 2.5 volts
- Ten previously unused pins are now used for test modes and programmable device configuration. They are pins 171-175, 177, 183, 184, 195 and 196. They should remain no connects (NC) at the board level.
- Certain special R4400 and ACT-4431SC function signals are not available and are no connects (NC) within the module substrate. These signals include IO_IN, IO_OUT, Status[7:0], IVDErrb, IVDAckb, 256K/1MB and FaultB.
- The JTAG port does not support complete boundary scan for the module. The JTAG is used to initialize the CPLD, which is one component in a chain of four.

Clocking and Speeds

The design is tailored towards replacing an ACT-4431SC device running with a 50 MHz MasterClock (100 MHz Pipeline Clock) and a TClock/RClock divisor of 4 (25 MHz). In order to mitigate the speed limitation of a 25 MHz SysAD bus, the ACT-5271SC utilizes a PLL clock multiplier and CPU cycle FIFO to run the RM5271 and the Secondary Cache connected to its SysAD bus at a higher rate. For a 25 MHz external bus, the cache bus can run at 50 MHz or 75 MHz (2x or 3x). The RM5271 pipeline can be 2, 2.5 or 3 times the cache speed.

Specifically, the R4400 style MasterClock is buffered and output as MasterOut. ModeClock is a divide by 256 of MasterOut. MasterClock is also divided by 2 to produce RClock, TClock and SyncOut. TClock and SyncOut are delayed from RClock by one buffer. SyncIn feeds the internal PLL multiplier circuit which drives the RM5271's SysClock and Secondary Cache RAMs at 2x or 3x. The RM5271's pipeline frequency is then determined by the modebit settings generated by the internal CPLD. The two Secondary Cache multiplier variations are selectable at module pin 195, for experimentation purposes.

Start up Sequence

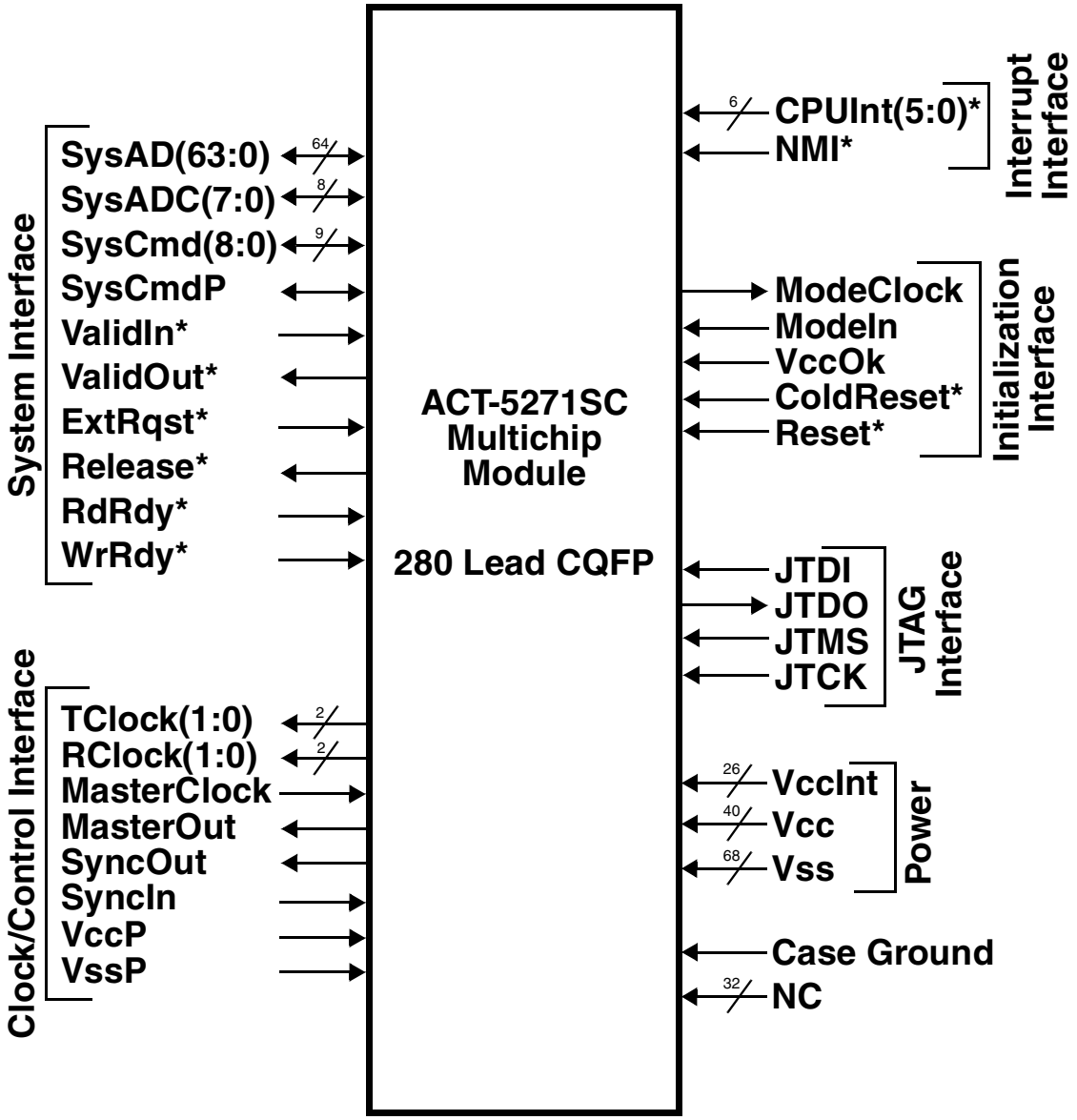
The process begins with the SRAM based FPGAs loading from an on-module serial EEPROM when VDDOK is asserted. At the same time, the standard R4400 startup sequence is followed via ModeClock, ModeIn, ColdResetB up to when ResetB is deasserted The RM5271 will, in turn, start its initialization when the internal PLL is Locked and ColdResetB is deasserted. The CPUs resetb is released with ResetB after checking to see that the FPGAs have configured. The actual mode bit stream sent to the RM5271 is created by the internal CPLD with a few pertinent bits stripped off the incoming stream: Endianness and Secondary Cache enable. For this design, the interface XmitDatPat is fixed at DDDD.

Cycle FIFO

The FIFO, implemented in an FPGA, accepts RM5271 CPU read and write cycle information direct from the CPU SysAD bus at the CPU clock rate and retransmits it to the MCM SysAD at the board's clock rate. Since the RM5271 does not normally output parity information on the address phase or the command bus, the parity information is added to the data captured from the CPU before it is entered into the FIFO. For Read data, if bad data is indicated by the Command bus (bit 5), the parity output to the RM5271 is inverted for that item, and all remaining ones in the case of a burst. Read cycles that hit in the Secondary Cache are not entered into the FIFO.

For additional Detail Information regarding the operation of the Quantum Effect Devices (QED) RISCMark™ RM5271SC™, 64-Bit Superscalar Microprocessor see the latest QED datasheet (Revision 1.3 2/2000).

ACT-5271SC Symbolic Pinouts



Absolute Maximum Rating[1]

Symbol	Parameter	Limits	Units
V_{TERM}	Terminal Voltage with respect to V_{SS}	-0.5[2] to +3.9	V
V_{IN}	Input Voltage Range	-0.5[2] to Vcc+0.5	V
T_{BIAS}	Case Operating Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Power Dissipation	10	W
$Ø_{JC}$	Thermal Resistance (Junction to Case)	2.5	°C/W
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Note 1: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2: V_{IN} minimum = -2.0V for pulse width less than 15ns. V_{IN} should not exceed 3.9 Volts.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{SS}	Supply Ground		0	V
V_{CC}	Supply Voltage	3.1	3.5	V
V_{CC}Int	Supply Voltage for RM5271 Core	2.4	2.6	V
V_{CC}P	Quiet V_{CC} for PLL	2.4	2.6	V
V_{IH}	High Level Input Voltage	2.0	Vcc + 0.5	V
V_{IL}	Low Level Input Voltage	-0.5	+0.66	V
T_C	Case Operating Temperature	-55	125	°C

Note: V_{CC} I/O should not exceed VccInt by greater than 1.2V during the power-up sequence.

Note: Applying a logic high state to any I/O pin before VccInt becomes stable is not recommended.

Note: As specified in IEEE 1149.1 (JTAG), the JTMS pin must be held low during reset to avoid entering JTAG test mode. Refer to the RM5200 Family Users Manual, Appendix F.

Pin Descriptions

System Interface:

SysAD(63:0)	I/O	**System address/data bus**: A 64 bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	I/O	**System address/data check bus:** An 8 bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmd(8:0)	I/O	**System command/identifier bus :** A 9 bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	**System command /data identifier bus parity**: Unused on Input, zero on output.
ValidIn*	I	**Valid Input:** An external agent asserts ValidIn* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	**Valid Output**: The processor asserts ValidOut* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ExtRqst*	I	**External Request:** An external agent asserts ExtRqst* to request the use of the system interface. The processor grants the request by asserting Release*.
Release*	O	**Release Interface:** In response to the assertion of ExtRqst*, the processor asserts Release* to signal the requesting device that the system interface is available.
RdRdy*	I	**Read ready:** The external agent asserts RdRdy*to indicate that it can accept processor read.
WrRdy*	I	**Write ready:** An external agent asserts WrRdy* when it can accept a processor write request.

Clock/Control Interface:

TClock(1:0)	O	**Transmit clocks** : Two identical transmit clocks that establish the system interface frequency.
RClock(1:0)	O	**Receive clocks:** Two identical receive clocks that establish the system interface frequency.
MasterClock	I	**Master clock:** Master clock input supplied by system.
MasterOut	O	**Master clock out**: Clock output buffered MasterClock.
SyncOut	O	**Synchronization clock out:** Synchronization clock output must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	I	**Synchronization clock in**: Synchronization clock input.
VccP	I	**Quiet Vcc for the PLL**: Quiet Vcc for the internal phase lock loop.
VssP	I	**Quiet Vss for the PLL**: Quiet Vss for the internal phase lock loop.

Pin Descriptions

Interrupt Interface: These signals comprise the interface used by external agents to interrupt the RM5271 processor.

CPUInt(5:0)	I	**Interrupt**: Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	I	**Nonmaskable interrupt**: Nonmaskable interrupt ORed with bit 6 of the interrupt register.

Initialization Interface: These signals comprise the interface by which an external agent initializes the RM5271 operating parameters.

ColdReset*	I	**Cold Reset:** This signal must be asserted for a power on reset or a cold reset.
ModeClock	O	**Boot Mode Clock:** Serial boot-mode data clock output at the MasterClock frequency divided by 256.
ModeIn	I	**Boot mode data in:** Serial boot-mode data input.
Reset*	I	**Reset:** This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initate a warm reset.
VccOk	I	**Vcc is OK:** When asserted, this signal tells the RM5271 that the 3.3 Volt power supply has been above 3.15 Volts for more than 100 milliseconds & will remain stable . Assertion of VccOK starts initialization sequence.

JTAG Interface:

JTDI	I	**JTAG data in:** Data is serial, scanned in thru this pin.
JTCK	I	**JTAG clock input:** On the rising edge of JTCK, both JTDI and JTMS are sampled.
JTDO	O	**JTAG data out:** Data is serial, scanned out thru this pin.
JTMS	I	**JTAG:** Test mode select.

Power:

VccInt	I	Supply voltage for RM5271 core.
Vcc	I	Supply voltage.
Vss	I	Supply ground.

ACT-5271SC Microprocessor CQFP Pinouts – "F10"

Pin #	Function	Pin #	Function	Pin #	Function
1	TClock0	48	Vss	95	Vss
2	Vss	49	VssP	96	SysAD59
3	SysAD45	50	Vcc	97	**VccInt
4	Vss	51	NC	98	SysAD27
5	TClock1	52	Vss	99	Vss
6	Vss	53	VccP	100	NC
7	SysAD13	54	**VccInt	101	Vcc
8	Vss	55	NC	102	SysAD58
9	SysAD14	56	Vss	103	Vss
10	Vcc	57	NC	104	SysAD26
11	JTMS	58	Vcc	105	Vcc
12	**VccInt	59	NC	106	NC
13	SysAD46	60	**VccInt	107	Vss
14	Vcc	61	SysADC7	108	SysAD57
15	JTDO	62	Vcc	109	**VccInt
16	**VccInt	63	SysADC3	110	SysAD25
17	SysAD15	64	**VccInt	111	Vss
18	Vcc	65	VccOk	112	NC
19	SysAD47	66	Vcc	113	Vcc
20	Vss	67	SysAD63	114	SysAD56
21	NC	68	Vss	115	Vss
22	Vcc	69	MasterOut	116	SysAD24
23	JTDI	70	Vss	117	**VccInt
24	Vss	71	SysAD31	118	NC
25	SysADC1	72	Vcc	119	Vss
26	**VccInt	73	SysAD30	120	SysADC6
27	SysADC5	74	Vcc	121	Vcc
28	Vcc	75	SysAD62	122	SysADC2
29	NC	76	Vss	123	Vss
30	**VccInt	77	SyncOut	124	NMI*
31	NC	78	Vss	125	Vcc
32	Vcc	79	SysAD29	126	SysAD55
33	JTCK	80	Vss	127	Vss
34	Vss	81	RClock1	128	SysAD23
35	SyncIn	82	Vss	129	**VccInt
36	Vss	83	Sys AD61	130	Release*
37	NC	84	Vss	131	Vss
38	Vss	85	RClock0	132	SysAD22
39	NC	86	Vss	133	Vcc
40	Vss	87	Vcc	134	SysAD54
41	MasterClock	88	Reset*	135	Vss
42	Vss	89	**VccInt	136	ModeIn
43	NC	90	SysAD60	137	**VccInt
44	Vcc	91	Vss	138	RdRdy*
45	NC	92	SysAD28	139	Vss
46	**VccInt	93	Vcc	140	SysAD53
47	NC	94	ColdReset*	141	SysAD21

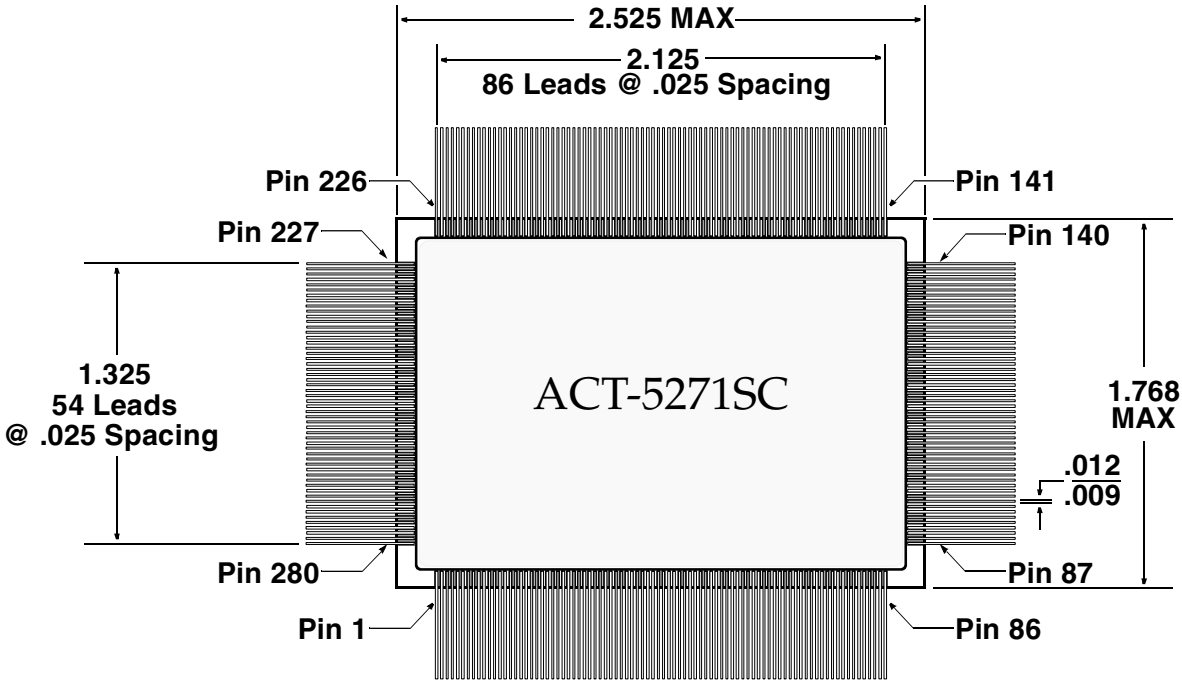
** These 26 VccInt pins may be 1.8V in future higher performance modules.

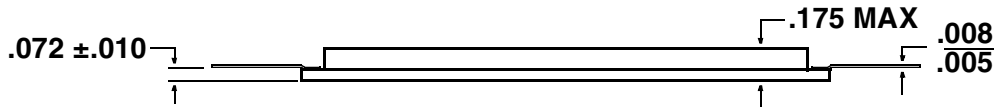
ACT-5271SC Microprocessor CQFP Pinouts – "F10"

Pin #	Function	Pin #	Function	Pin #	Function
142	Vss	189	CPUInt4	236	Vss
143	ExtRqst*	190	**VccInt	237	SysCmd3
144	Vcc	191	CPUInt5	238	Vcc
145	SysAD52	192	Vss	239	SysAD7
146	Vss	193	**VccInt	240	Vss
147	ValidOut*	194	NC (256K/1MB)	241	SysAD39
148	Vcc	195	NC (CPUMULT)	242	Vcc
149	SysAD20	196	NC (Prog_FPGA)	243	SysCmd4
150	Vss	197	NC	244	Vss
151	SysAD19	198	CASE GROUND	245	SysADC0
152	**VccInt	199	Vss	246	Vcc
153	SysAD51	200	SysAD32	247	SysADC4
154	Vss	201	Vcc	248	Vss
155	ValidIn*	202	SysAD0	249	SysCmd5
156	Vcc	203	Vss	250	**VccInt
157	SysAD18	204	SysAD1	251	SysAD8
158	Vss	205	**VccInt	252	Vss
159	SysAD50	206	SysAD33	253	SysAD40
160	**VccInt	207	Vss	254	Vcc
161	CPUInt0	208	SysAD34	255	SysCmd6
162	Vss	209	Vcc	256	Vss
163	SysAD49	210	SysAD2	257	SysAD9
164	Vcc	211	Vss	258	**VccInt
165	SysAD17	212	SysCmd0	259	SysAD41
166	Vss	213	**VccInt	260	Vss
167	SysAD16	214	SysAD35	261	SysCmd7
168	Vcc	215	Vss	262	Vcc
169	SysAD48	216	SysAD3	263	SysAD10
170	Vss	217	Vcc	264	Vss
171	NC (SP_SER_EN)	218	SysAD4	265	SysAD42
172	NC (SP_OE)	219	Vss	266	**VccInt
173	NC (SP_CE)	220	SysCmd1	267	SysCmd8
174	NC (SP_CCCK)	221	Vcc	268	Vss
175	NC (SP_DATA)	222	SysAD36	269	SysAD11
176	NC	223	Vss	270	Vcc
177	NC (ISP_EN)	224	SysCmd2	271	SysAD43
178	Vss	225	**VccInt	272	Vss
179	CPUInt1	226	SysAD5	273	SysCmdP
180	Vcc	227	SysAD37	274	**VccInt
181	CPUInt2	228	Vss	275	SysAD12
182	Vss	229	ModeClock	276	Vss
183	NC (IN_P5064)	230	Vcc	277	SysAD44
184	NC (DCD_SEL)	231	WrRdy*	278	Vcc
185	CPUInt3	232	Vss	279	NC
186	NC	233	SysAD6	280	Vss
187	NC	234	**VccInt		
188	Vss	235	SysAD38		

** These 26 VccInt pins may be 1.8V in future higher performance modules.

Package Information – "F10" – CQFP 280 Leads





(Dimensions are in inches)

Note: Outside ceramic tie bars not shown for clarity. Contact factory for details

Sample Ordering Information

Part Number	Screening	Speed (MHz)	Package
ACT-5271SC-150F10C	Commercial Temperature	150	280 Lead CQFP
ACT-5271SC-150F10I	Industrial Temperature		
ACT-5271SC-150F10T	Military Temperature		
ACT-5271SC-150F10M	Military Screening		

Part Number Breakdown

ACT– 5271 SC – 150 F10 M

Aeroflex Circuit Technology

Base Processor Type

Cache Style

SC = Secondary Cache

Maximum Pipeline Freq.

150 = 150MHz

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *

Package Type & Size

Surface Mount Package

F10 = 2.525" x 1.768" x 280 Lead CQFP

* **Screened to the individual test methods of MIL-STD-883**

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