AAT3244
300mA Adjustable Dual CMOS Low Voltage LDO Linear Regulator

PowerLinear™

General Description

The AAT3244 is a dual, low input voltage, low dropout (LDO) linear regulator with two Power OK (POK) outputs. Two integrated regulators provide high power outputs of 300mA from an input voltage range of 1.8V to 5.5V.

Two POK pins provide open drain signals when their respective regulator is within regulation. The AAT3244 has independent voltage inputs and enable pins for increased design flexibility. The device features a very low quiescent current (typically 85µA) and low dropout voltages (200mV at full load), making it ideal for portable applications where battery life is critical.

The AAT3244 is available in a space-saving, Pb-free 12-pin TSOPJW package and is capable of operation over the -40°C to +85°C temperature range.

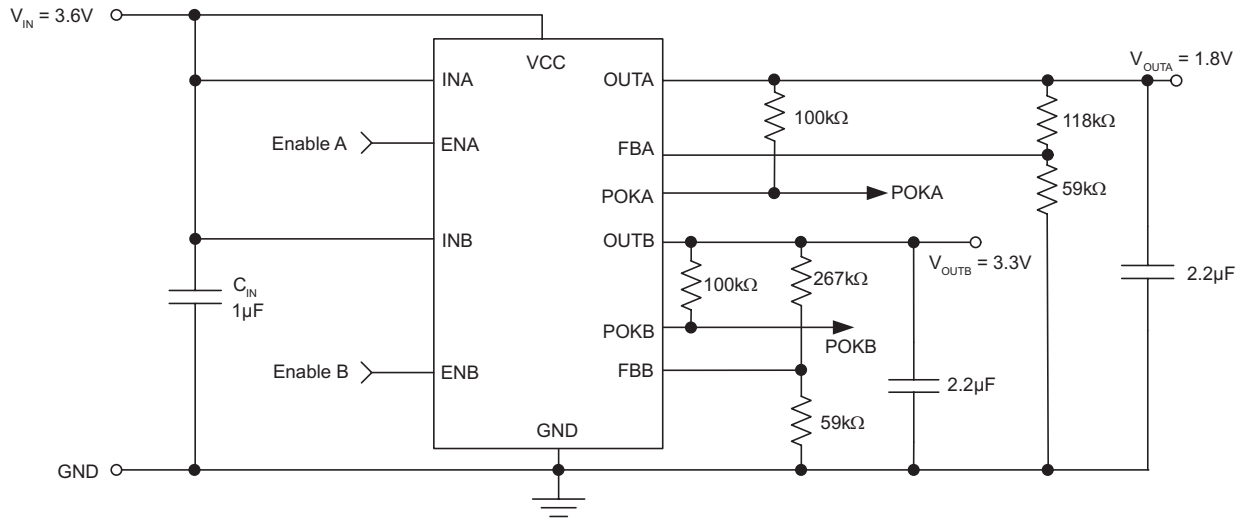
Features

- Low Input Voltage
  - 1.8V to 5.5V
- Ultra-Low Adjustable Output Voltage
  - 3.6V to 0.6V
- High Output Current
  - 300mA per LDO
- Low Dropout Voltage
  - Typ 200mV @ 300mA
- Low 85µA Quiescent Current (Both LDOs On)
- High Output Accuracy: ±1.5%
- Independent Input Supply and Enable Pins
- Over-Temperature Protection
- 12-Pin TSOPJW Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor/DSP Core/IO Power
- PDAs and Handheld Computers

Typical Application

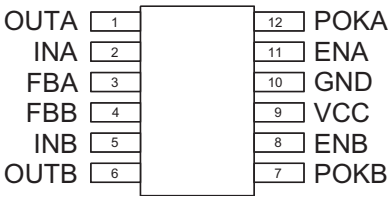


Pin Descriptions

Pin #	Symbol	Function
1	OUTA	300mA regulator output pin; should be closely decoupled with a low equivalent series resistance (ESR) ceramic capacitor.
2	INA	Input voltage pin for LDOA; should be closely decoupled.
3	FBA	Feedback input pin for LDOA. This pin is connected to OUTA. It is used to see the output of LDOA to regulate to the desired value via an external resistor divider.
4	FBB	Feedback input pin for LDOB. This pin is connected to OUTB. It is used to see the output of LDOB to regulate to the desired value via an external resistor divider.
5	INB	Input voltage pin for LDOB; should be closely decoupled.
6	OUTB	300mA regulator output pin; should be closely decoupled with a low ESR ceramic capacitor.
7	POKB	Power OK pin with open drain output. It is pulled low when the OUTB pin is outside the regulation window of ±10%. Place a pull-up resistor between POKB and OUTB.
8	ENB	Enable pin for LDOB. Active high. V_{EN} must be less than or equal to V_{CC}.
9	VCC	Input bias supply. Connect to an "always ON" supply voltage between 2.7V and 5.5V.
10	GND	Ground connection pin.
11	ENA	Enable pin for LDOA. Active high. V_{EN} must be less than or equal to V_{CC}.
12	POKA	Power OK pin with open drain output. It is pulled low when the OUTA pin is outside the regulation window of ±10%. Place a pull-up resistor between POKA and OUTA.

Pin Configuration

TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{CC}, V_{IN}	Input Voltage, LDO Input Voltage to GND	6.0	V
V_{FB}	FB to GND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation (T_A = 25°C)	625	mW
θ_{JA}	Thermal Resistance[2]	160	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

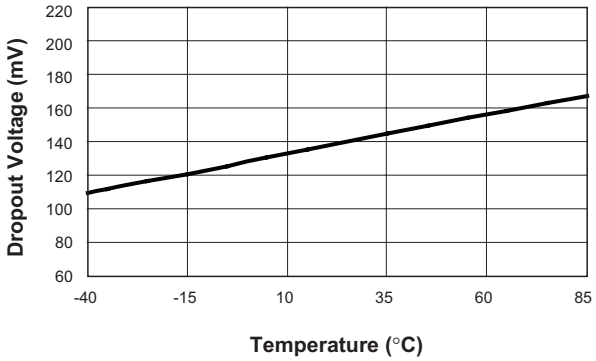
V_{CC} = V_{INA} = V_{INB} = 3.6V; T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
Bias Power Supply							
V_{CC}	Bias Power Supply Input			2.7		5.5	V
I_Q	Quiescent Current	V_{ENA} = V_{ENB} = V_{IN}; I_{LOAD} = 0			85	160	µA
I_{SHDN}	Shutdown Current	V_{ENA} = V_{ENB} = GND				1.0	µA
UVLO	Under-Voltage Lockout Voltage	V_{CC} Rising				2.6	V
		Hysteresis			200		mV
LDOA, LDOB; I_{OUT} = 300mA							
V_{IN}	Input Voltage			1.8		5.5	V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 300mA	T_A = 25°C	-2.0		2.0	%
			T_A = -40°C to +85°C	-3.5		3.5	
V_{FB}	Feedback Voltage			0.594	0.6	0.606	V
V_{DO}	Dropout Voltage[2]	I_{OUT} = 300mA			200	300	mV
$\Delta V_{OUT}/V_{OUT}/\Delta V_{IN}$	Line Regulation[3]	V_{IN} = V_{OUT} + 1.0V to 5.0V				0.09	%/V
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.5		V_{CC}	V
t_{EN}	Turn-On Enable Time				100		µs
V_{POK}	Power OK Trip Threshold	V_{OUT} Rising, T_A = 25°C		80		98	% of V_{OUT}
V_{POKHYS}	Power OK Hysteresis				1.0		% of V_{OUT}
$V_{POK(LO)}$	Power OK Output Voltage Low	I_{SINK} = 1mA				0.4	V
I_{POK}	POK Output Leakage Current	V_{POK} < 5.5V, V_{OUT} in Regulation				1.0	µA
I_{OUT}	Output Current	$V_{IN(MIN)}$ = 2.5V		300			mA
I_{SD}	Shutdown Current	V_{IN} = 5V				1.0	µA
T_{SD}	Over-Temperature Shutdown Threshold				140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				15		°C

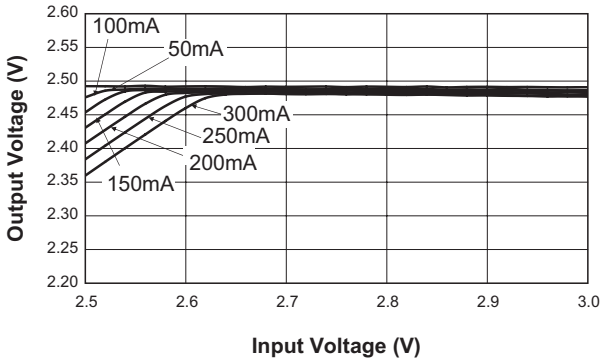
1. The AAT3244 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.
3. C_{IN} = 10µF.
4. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)}$ = $V_{OUT(MAX)}$ + $V_{DO(MAX)}$ as long as V_{IN} ≥ 1.8V.

Typical Characteristics

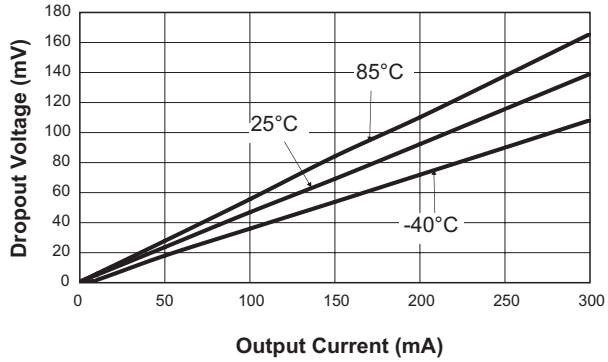
Dropout Voltage vs. Temperature
(V_{OUT} = 2.5V; I_{OUT} = 300mA)



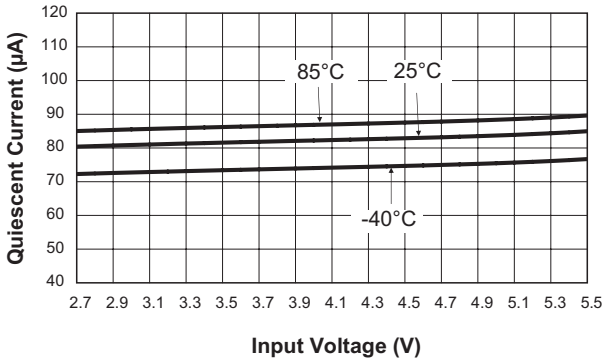
Output Voltage vs. Input Voltage
(V_{OUT} = 2.5V)



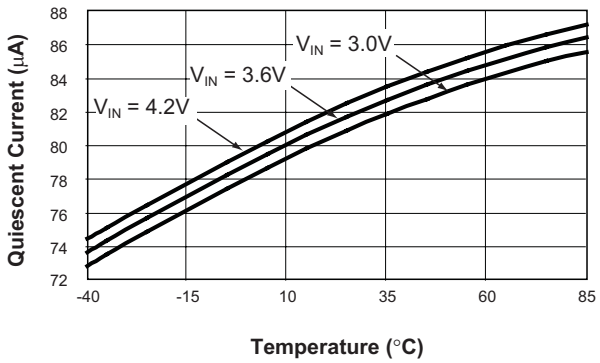
Dropout Voltage vs. Output Current
(V_{OUT} = 2.5V)



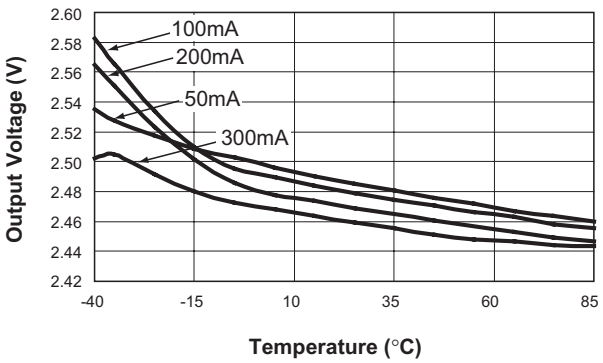
Quiescent Current vs. Input Voltage
(V_{OUT} = 2.5V)



Quiescent Current vs. Temperature
(V_{OUT} = 2.5V)

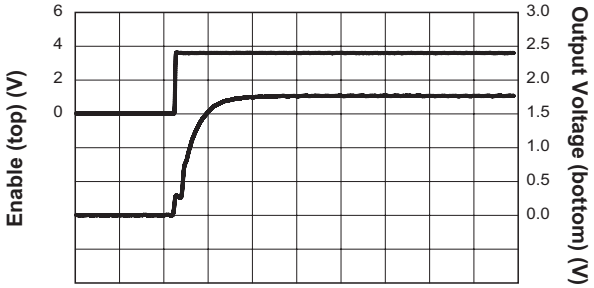


Output Voltage vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 2.5V)



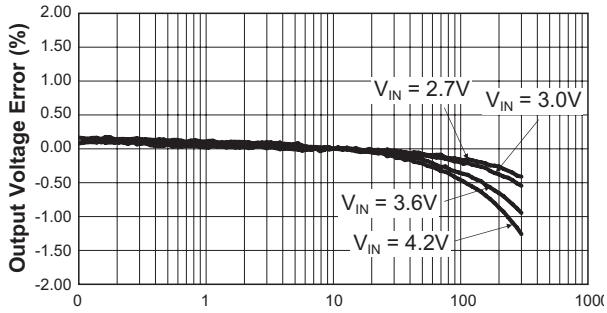
Typical Characteristics

Turn-On Time
(V_{OUT} = 1.8V)



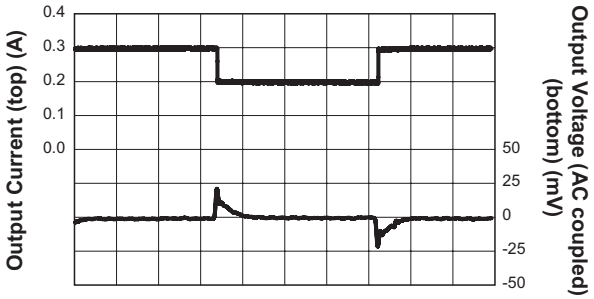
Time (50µs/div)

Load Regulation
(V_{OUT} = 2.5)



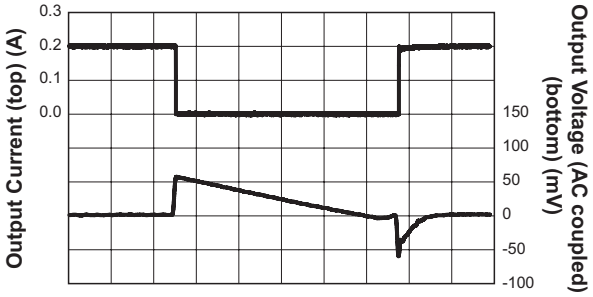
Output Current (mA)

Load Transient
(200mA–300mA; V_{OUT} = 1.8V)



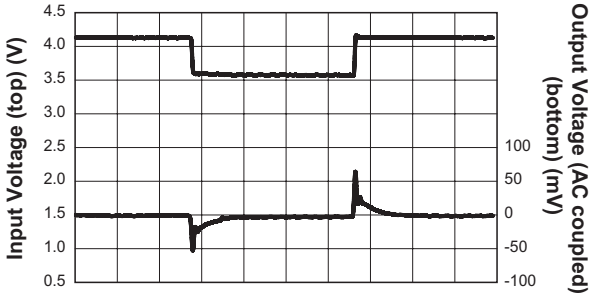
Time (50µs/div)

Load Transient
(1mA–200mA; V_{OUT} = 1.8V)



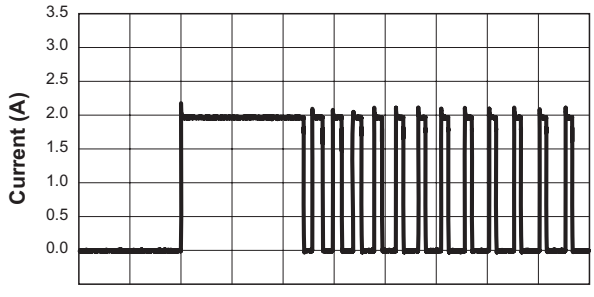
Time (50µs/div)

Line Transient
(3.6V– 4.2V; V_{OUT} = 1.8V)



Time (50µs/div)

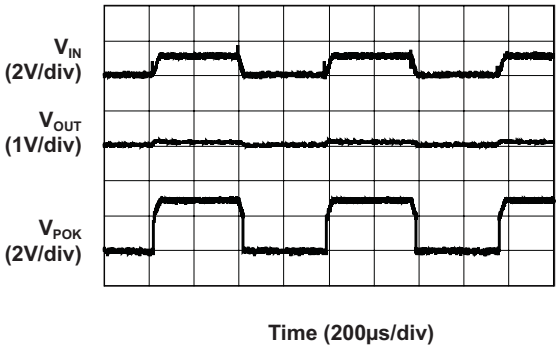
Over-Current Protection



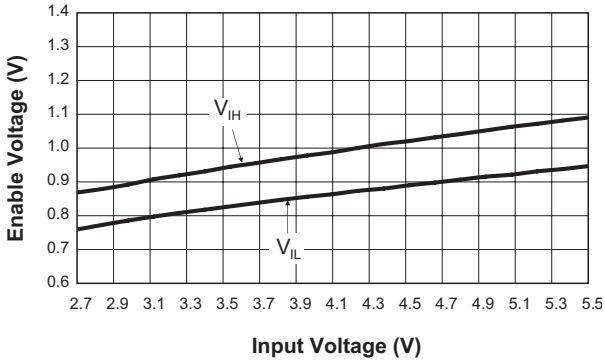
Time (50ms/div)

Typical Characteristics

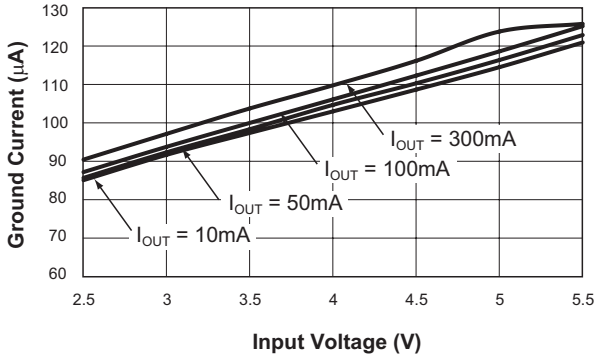
POK Output Response



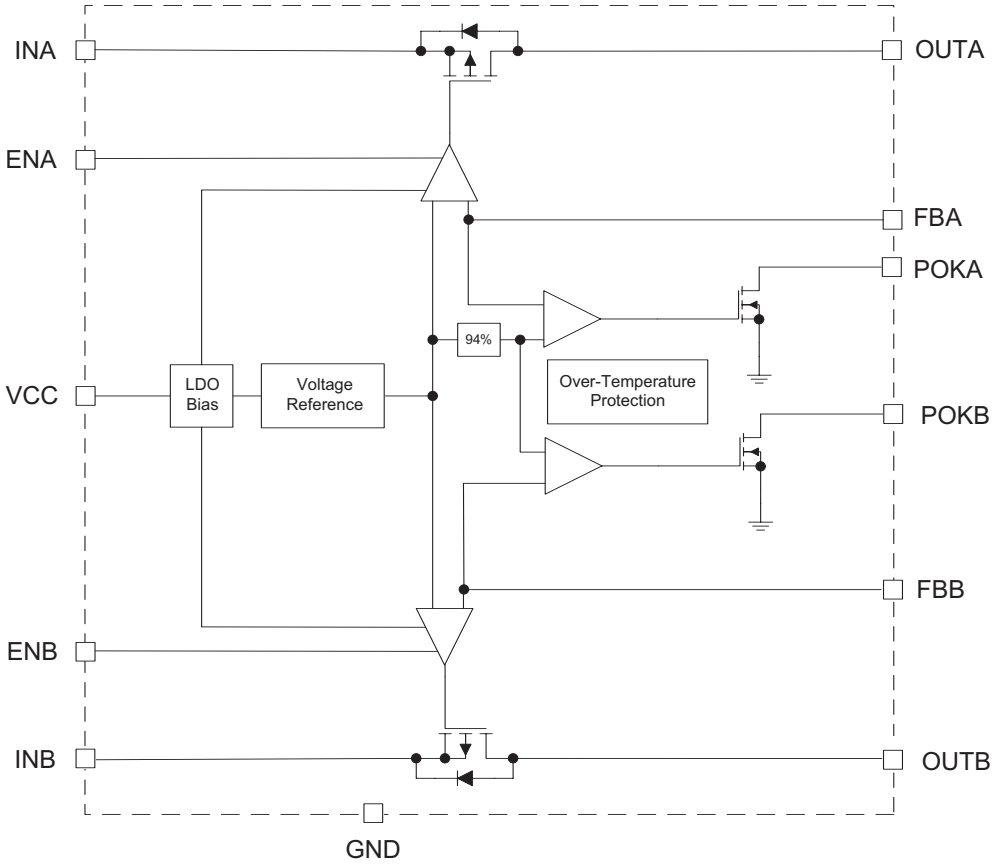
Enable Threshold Voltage vs. Input Voltage



Ground Current vs. Input Voltage



Functional Block Diagram



Functional Description

The AAT3244 is a high performance, low input voltage, dual LDO linear regulator. Both LDOA and LDOB are capable of delivering 300mA of current, within power dissipation limits. The LDOs are designed to operate with low-cost ceramic capacitors. For added flexibility, both regulators have independent input voltages operating from 1.8V to 5.5V, but share a common bias voltage, V_{CC}. The V_{CC} voltage should be tied to the highest system voltage available and should be available at all times. Each regulator has an independent enable pin. An external feedback pin for each LDO allows programming the output voltage from 3.6V to 0.6V. The regulators have thermal protection in case of adverse operating conditions.

A power OK comparator for each output is also integrated, which indicates when the output is within regulation. The POK is an open drain output and is held low when the AAT3244 is in shutdown mode.

Refer to the Thermal Considerations section of this datasheet for details on device operation at maximum output current loads.

Applications Information

To assure the maximum possible performance is obtained from the AAT3244, please refer to the following application recommendations.

Input Capacitor

A 1µF or larger capacitor is typically recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation; however, if the AAT3244 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation.

C_{IN} should be located as closely to the device supply pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}; however, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins OUT and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT3244 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications requiring low output noise and optimum power supply ripple rejection should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT3244. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance

ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature.

Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials

Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%. Capacitor area is another contributor to ESR. Capacitors

which are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size. Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

POK Output

The AAT3244 features integrated Power OK comparators which can be used as an error flag. The POK open drain output goes low when output voltage is 6% (typical) below its nominal regulation voltage. Additionally, any time one of the regulators is in shutdown, the respective POK output is pulled low. Connect a 100kΩ pull up resistor from POKA to either INA or OUTA, and POKB to either INB or OUTB.

Enable Function

The AAT3244 features an LDO regulator enable/ disable function. Each LDO has its own dedicated enable pin. These pins (ENA, ENB) are active high and are compatible with CMOS logic. To assure the LDO regulators will switch on,

$$1.5V \le V_{EN} \le V_{CC}$$

In shutdown, the AAT3244 will consume less than 1.0µA of current. If the enable function is not needed in a specific application, it may be tied to VCC to keep the LDO regulator in a continuously on state.

Thermal Protection

The AAT3244 has an internal thermal protection circuit which will activate when the device die temperature exceeds 140°C. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back approximately 15°C below the trip point.

No-Load Stability

The AAT3244 is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode.

Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the OUTA/B pins, possibly damaging the LDO regulator. In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will result in a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across INA/B to OUTA/B (connecting the cathode to INA/B and anode to OUTA/B). The Schottky diode forward voltage should be less than 0.45V.

Low Voltage Input Bias Considerations

The input voltage of both LDOs is designed to operate down to 1.8V input. However, to operate the LDO to its full potential, the AAT3244 requires a minimum bias voltage (V_{CC}) of 2.7V for all LDO input voltages between 1.8V and 2.7V. In portable systems utilizing single-cell Lithium-ion batteries, the VCC pin may be connected directly to the battery. In non-portable applications, the voltage can be connected to any supply from 2.7V to 5.5V. In the event that one of the input supplies is above 2.7V, this can also be connected to VCC, assuming that the supply will always be available.

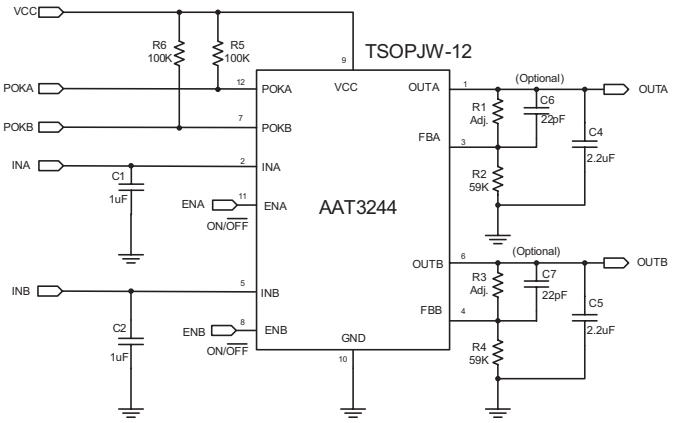


Figure 1: AAT3244 Schematic.

Adjustable Output Resistor Selection

Resistors R1, R2 and R3, R4 of Figure 1 program the outputs to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R2 and R4 is 59kΩ. Decreased resistor values are necessary to maintain noise immunity on the FB pin, resulting in increased quiescent current. Table 1 summarizes the resistor values for various output voltages.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2$$

With enhanced transient response for extreme pulsed load application, an external feed-forward capacitor, (C6 and C7 in Figure 1), can be added.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kΩ R1 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	267	1000
3.6	295	1105

Table 1. Adjustable Resistor Values For LDO Regulator.

Thermal Considerations and High Output Current Applications

The AAT3244 is designed to deliver continuous output load currents of 300mA under normal operating conditions and can supply up to 600mA during circuit start-up conditions. This is desirable for applications where there might be a brief high inrush current during a power-on event. The limiting characteristic for the maximum output load current safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account. The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the layout considerations section of this document. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT3244 are $T_{J(MAX)}$ (the maximum junction temperature for the device, which is 125°C) and θ_{JA} = 160°C/W (the package thermal resistance). Typically, maximum conditions are calculated at the maximum operating temperature of T_A = 85°C and under normal ambient conditions where T_A = 25°C. Given T_A = 85°C, the maximum package power dissipation is 250mW. At T_A = 25°C, the maximum package power dissipation is 625mW. The maximum continuous output current for the AAT3244 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator. To determine the maximum output current for a given output voltage, refer to the following equation. This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{D(MAX)} = [(V_{IN} - V_{OUTA})I_{OUTA} + (V_{IN} \cdot I_{GND})] + [(V_{IN} - V_{OUTB})I_{OUTB} + (V_{IN} \cdot I_{GND})]$$

This formula can be solved for I_{OUTA} to determine the maximum output current for LDOA:

$$I_{OUTA(MAX)} = \frac{P_{D(MAX)} - (2 \cdot V_{IN} \cdot I_{GND}) - (V_{IN} - V_{OUTB}) \cdot I_{OUTB}}{V_{IN} - V_{OUTA}}$$

The following is an example for a 2.5V output:

V_{OUTA} = 2.5V

V_{OUTB} = 1.5V

I_{OUTB} = 150mA

V_{IN} = 4.2V

I_{GND} = 125µA

$$I_{OUTA(MAX)} = \frac{625mW - (2 \cdot 4.2V \cdot 125\mu A) - (4.2 - 1.5) \cdot 150mA}{4.2 - 2.5}$$

$I_{OUTA(MAX)}$ = 129mA

From the discussion above, $P_{D(MAX)}$ was determined to equal 625mW at T_A = 25°C.

Therefore, with Regulator B delivering 150mA at 1.5V, Regulator A can sustain a constant 2.5V output at a 129mA load current at an ambient temperature of 25°C. Higher input-to-output voltage differentials can be obtained with the AAT3244, while maintaining device functions within the thermal safe operating area. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the LDO regulator in a duty-cycled mode.

For example, an application requires V_{IN} = 4.2V while V_{OUTA} = 1.5V at a 300mA load, V_{OUTB} = 1.5V at a 200mA load, and T_A = 25°C. To maintain this high input voltage and output current level, the LDO regulator must be operated in a duty-cycled mode.

Refer to the following calculation for duty-cycle operation:

I_{GND} = 125µA

I_{OUTA} = 300mA

I_{OUTB} = 200mA

V_{IN} = 4.2V

V_{OUT} = 1.5V

$P_{D(MAX)}$ is assumed to be 625mW

$$\%DC = \frac{100(P_{D(MAX)})}{[(V_{IN} - V_{OUTA})I_{OUTA} + (V_{IN} \cdot I_{GND})] + [(V_{IN} - V_{OUTB})I_{OUTB} + (V_{IN} \cdot I_{GND})]}$$

$$\%DC = \frac{100 \cdot 625mW}{[(4.2V - 1.5V)300mA + (4.2V \cdot 125\mu A)] + [(4.2V - 1.5V)200mA + (4.2V \cdot 125\mu A)]}$$

%DC = 46.3%

For a 300mA output current and a 2.7V drop across the AAT3244 at an ambient temperature of 25°C, the maximum on-time duty cycle for the device would be 46.3%.

Under-Voltage Lockout

Under-voltage lockout (UVLO) guarantees sufficient V_{CC} bias and proper operation of all internal circuits prior to activation.

Printed Circuit Board Layout Recommendations

The suggested PCB layout for the AAT3244 in a TSOPJW-12 package is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitors (C1and C2) should connect as closely as possible to input pins (Pin 2 and Pin 5) and GND (Pin 10).
2. The output traces of the feedback resistors (R1 and R3) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. Feedback resistors should be placed as closely as possible to the FB pin (Pin 3 and Pin 4) to minimize the length of the high impedance feedback trace.
4. The resistance of the trace from the load returns to GND (Pin 10) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. The feedback node is connected directly to the non-inverting input of the error amplifier, thus any noise or ripple from the divider resistors will be subsequently amplified by the gain of the error amplifier. This effect can increase noise seen on the LDO regulator output, as well as reduce the maximum possible power supply ripple rejection. For low output noise and highest possible power supply ripple rejection performance, it is critical to connect the divider resistors (R2 and R4) and output capacitors (C4 and C5) directly to the LDO regulator ground pin. This method will eliminate any load noise or ripple current feedback through the LDO regulator.

Evaluation Board Layout

The AAT3244 evaluation layout follows the recommend printed circuit board layout procedures and can be used as an example for good application layouts (See Figures 2 and 3).

Note: Board layout shown is not to scale.

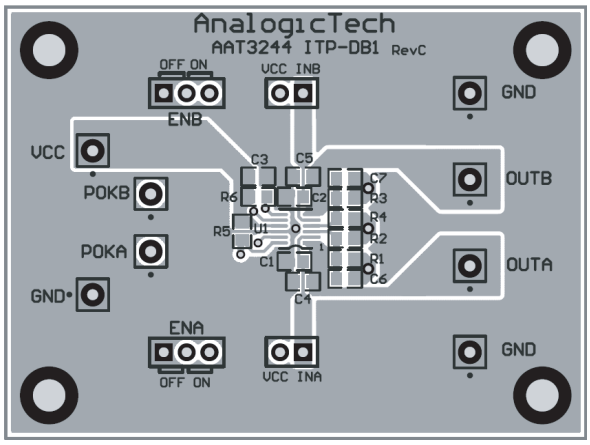


Figure 2: AAT3244 Evaluation Board Top Side Layout.

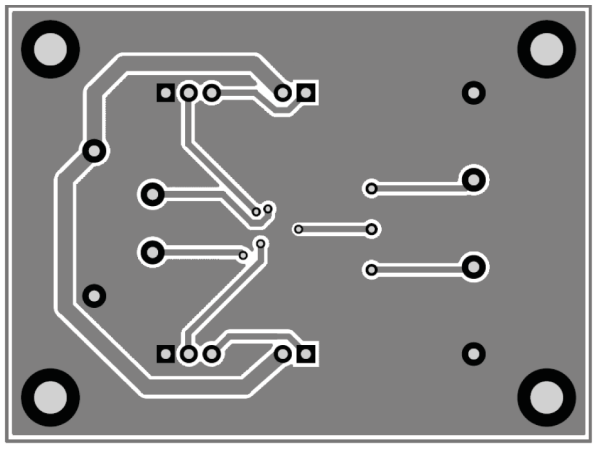


Figure 3: AAT3244 Evaluation Board Bottom Side Layout.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	LDO A	LDO B		
TSOPJW-12	0.6V	0.6V	WTXYY	**AAT3244ITP-AA-T1**

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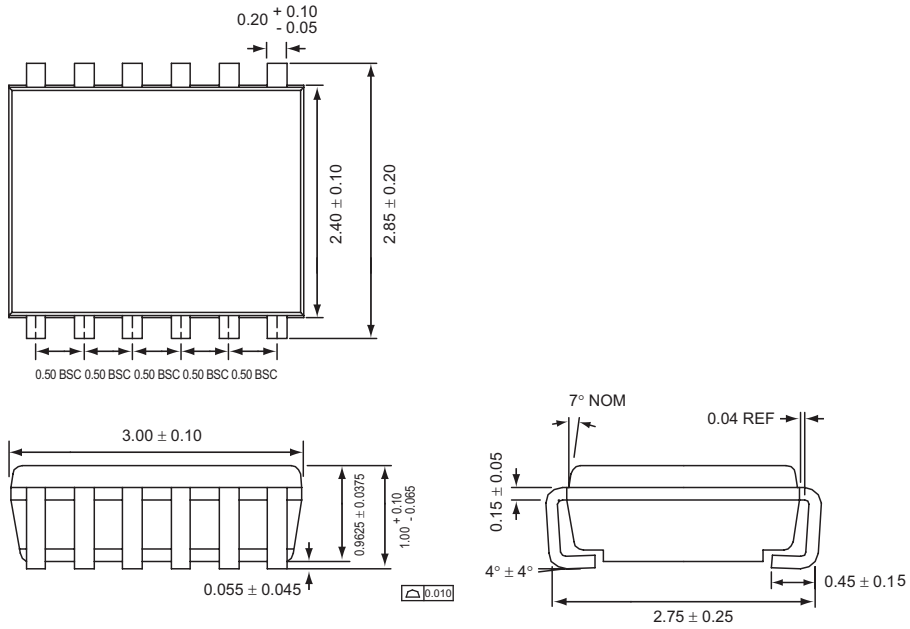
Legend	
Voltage	Code
Adjustable (0.6V)	A

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

TSOPJW-12



All dimensions in millimeters.

Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611