8-bit μP-compatible D/A converter

5018

FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to ± $^1/_2$ LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 68000 and many other μPs

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

DESCRIPTION

The 5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature coefficient.

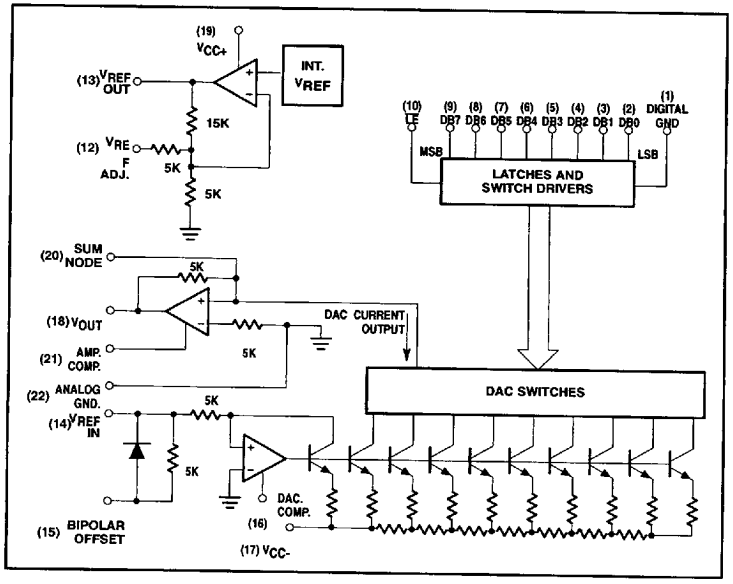
The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

ORDERING INFORMATION

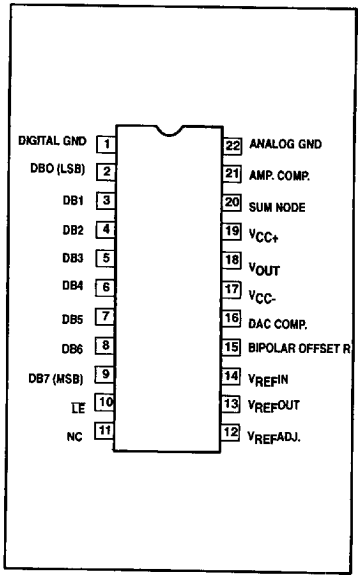
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
22-Pin Ceramic DIP	5018/BWA	GDIP1-T22

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING[1]	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_I	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF}OUT$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation	1000	mW

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS[2]	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution		8	8	8	8		8	Bits
	Monotonicity		8	8	8	8		8	Bits
ΔFS	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		+11.4	+15		+11.4	+15		V
$V_{CC}-$	Negative supply voltage		-11.4	-15		-11.4	-15		V
V_{IH}	Logic "1" input voltage	Pin 1 = GND	2.0			2.0			V
V_{IL}	Logic "0" input voltage	Pin 1 = GND			0.8			0.8	V
I_{IH}	Logic "1" input current	Pin 1 = GND, 2V < V_1 < 18V		0.1	10			10	μA
I_{IL}	Logic "0" input current	Pin 1 = GND, -5V < v_1 < 0.8V		-2.0	-10			-10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN}$ = 5.000V	9.50	9.961	10.50				V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN}$ = 5.000V	4.5 -5.25	4.961 -5.000	5.5 -4.75				V V
V_{ZS}	Zero scale voltage	Bipolar operation	-30	5	+30	-30		+30	mV
I_{SC}	Output short circuit current	V_O = 0V		15	40				mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V_{CC}-$ = -15V, 13.5V ≤ $V_{CC}+$ ≤ 16.5V external $V_{REF\ IN}$ = 5.000V		0.001	0.01			0.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (-)	$V_{CC}+$ = -15V, -13.5V ≤ $V_{CC}-$ ≤ -16.5V, external $V_{REF\ IN}$ = 5.000V		0.001	0.01			0.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN}$ = 5.000V					20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient						5		ppm/°C
I_{REF}	Reference output current[9]	$V_{REF\ OUT}$ = 0V			3				mA
I_{REFSC}	Reference short circuit current			15	30				mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V_{CC}-$ = -15V 13.5V ≤ $V_{CC}+$ ≤ 16.5V, I_{REF} = 1.0mA		0.003	0.01			0.01	%FR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (-)	$V_{CC}+$ = -15V, -13.5V ≤ $V_{CC}-$ ≤ 16.5V, I_{REF} = 1.0 mA		0.003	0.01			0.01	%FR/%VS
V_{REF}	Reference voltage	I_{REF} = 1.0mA	4.9	5.0	5.25				V

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta Y_{REF}/\Delta T$	Reference voltage temperature coefficient	I_{REF} = 1.0mA					60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	I_{REF} = 1.0mA	4.15	5.0	5.85				kΩ
I_{CC}+ I_{CC}-	Positive supply current Negative supply current	V_{CC}+ = 15V V_{CC}- = -15V		7 -10	14 -15			14 -15	mA mA
P_D	Power dissipation	I_{REF} = 1.0mA, V_{CC} = ±15V		255	435			435	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC}+ = +15V, V_{CC}- = -15V, unless otherwise specified.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = 55°C, +125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{SLH}	Setting time[4]	± 1/2 LSB	Input	All bits low-to-high[3]		1.8					μs
t_{SHL}	Setting time[5]	± 1/2 LSB	Input	All bits high-to-low		2.3					μs
t_{PLH}	Propagation delay[4]	Output	Input	All bits switched low-to-high		300					ns
t_{PHL}	Propagation delay[5]	Output	Input	All bits switched high-to-low		150					ns
t_{PLSB}	Propagation delay[4, 5]	Output	Input	1 LSB change[3, 4]		150					ns
t_{PLH}	Propagation delay[6]	Output	$\overline{CE}$	Low-to-High transition		300					ns
t_{PHL}	Propagation delay[7]	Output	$\overline{CE}$	High-to-Low transition		150					ns
t_S	Setup time[3, 8]	$\overline{CE}$	Input		100						ns
t_H	Hold time[3, 8]	Input	$\overline{CE}$		50						ns
t_{PW}	Latch enable pulse width[3, 8]				150						ns

NOTES:

1. Operation beyond limits in the table may impair the useful life of the device.
2. Refer to Figure 1.
3. Refer to Figure 2.
4. See Figure 5.
5. See Figure 6.
6. See Figure 7.
7. See Figure 8.
8. See Figure 9.
9. For reference currents > 3mA, use of an external buffer is required.

TEST CONFIGURATIONS AND WAVEFORM DEFINITIONS

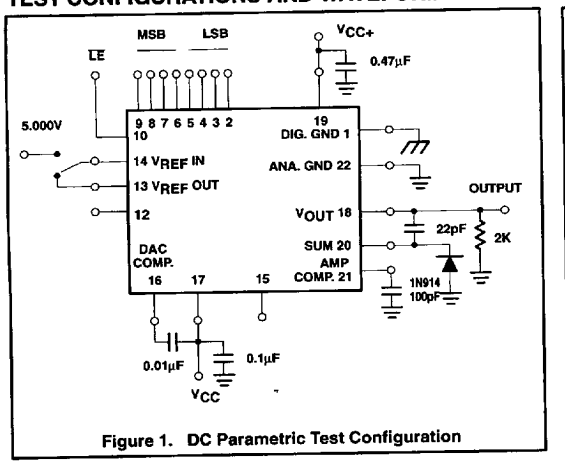


Figure 1. DC Parametric Test Configuration

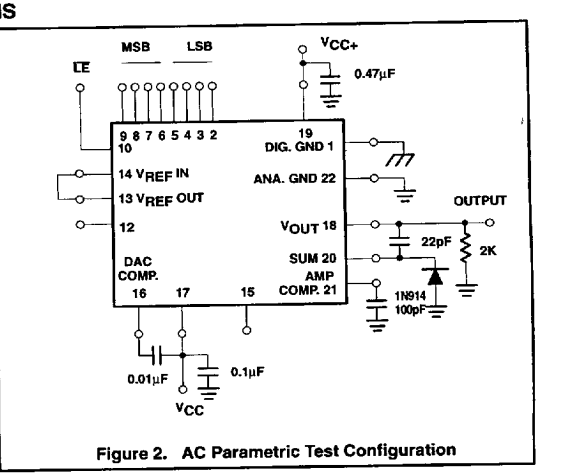


Figure 2. AC Parametric Test Configuration

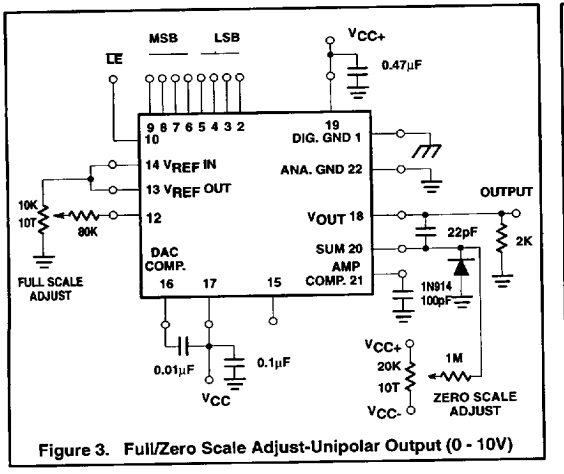


Figure 3. Full/Zero Scale Adjust-Unipolar Output (0 - 10V)

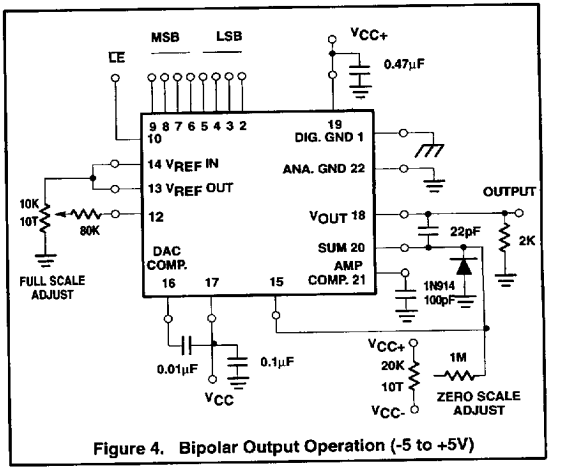


Figure 4. Bipolar Output Operation (-5 to +5V)

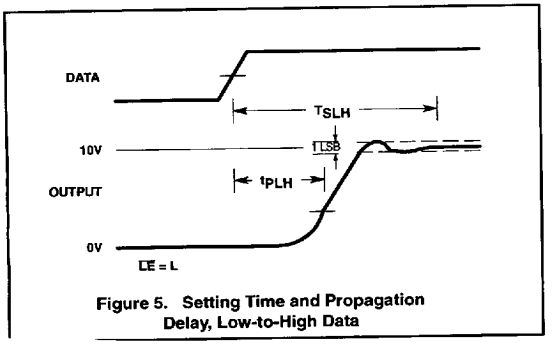


Figure 5. Setting Time and Propagation Delay, Low-to-High Data

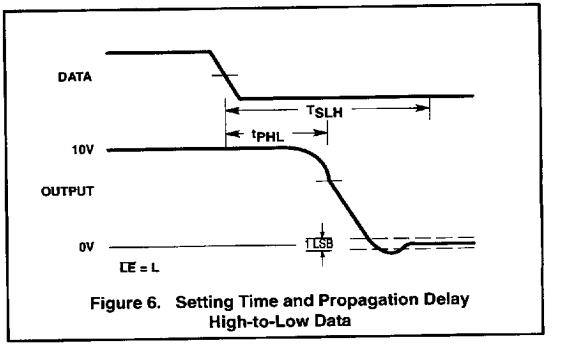


Figure 6. Setting Time and Propagation Delay High-to-Low Data

TEST WAVEFORM DEFINITIONS

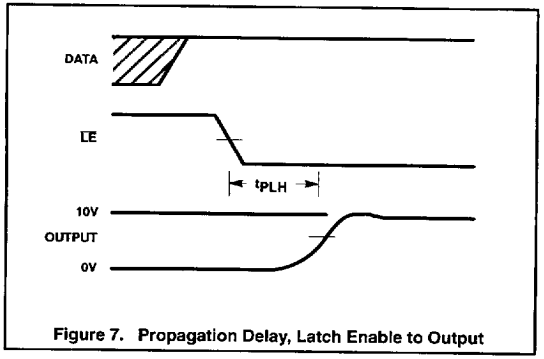


Figure 7. Propagation Delay, Latch Enable to Output

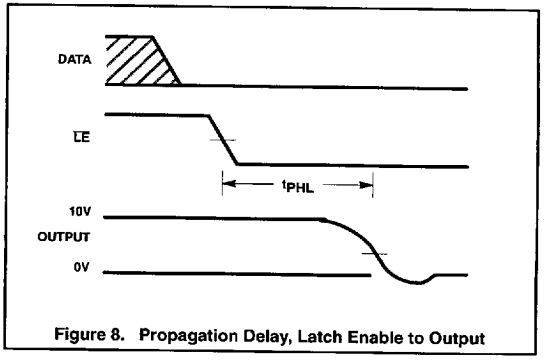


Figure 8. Propagation Delay, Latch Enable to Output

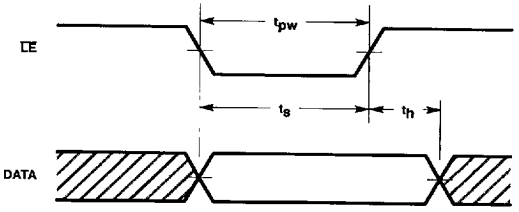


Figure 9. Latch Enable Pulse Width, Setup and Hold Times