National Semiconductor

10145A
16 x 4 Register File (Random Access Memory)

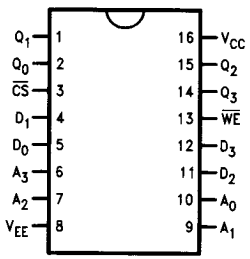
General Description

The 10145A is a high-speed 64-bit Random Access Memory organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select (CS) and Write Enable (WS) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Connection Diagram

16-Pin Ceramic Dual-in-Line Package



TL/D/9742–2

Top View

Order Number 10145ADC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select
A_0–A_3	Address
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enables
Q_0–Q_3	Data Outputs