

PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M
PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M
STANDARD HIGH-SPEED PAL® CIRCUITS

D2705, FEBRUARY 1984—REVISED AUGUST 1989

- Choice of Operating Speeds
 High Speed, A Devices . . . 25 MHz
 Half Power, A-2 Devices . . . 16 MHz

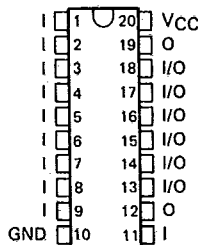
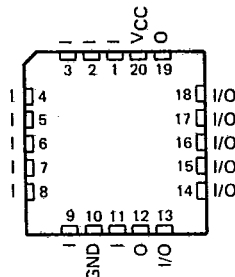
- Choice of Input/Output Configuration

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

TEXAS INSTR (ASIC/MEMORY)

25E D

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

J OR W PACKAGE
(TOP VIEW)FK PACKAGE
(TOP VIEW)**description**

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

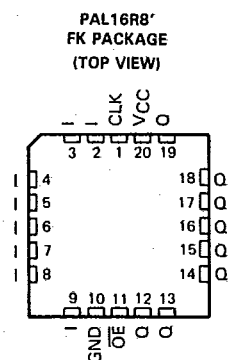
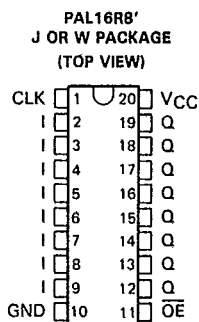
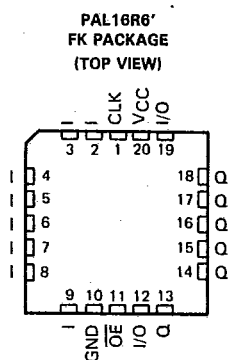
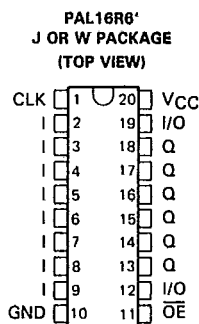
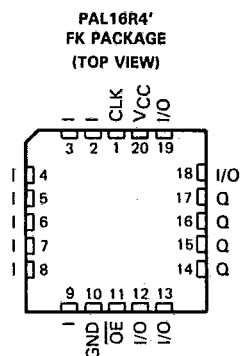
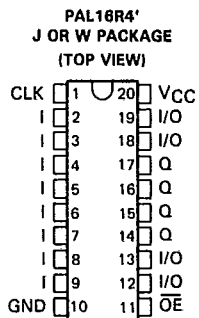
**TEXAS
INSTRUMENTS**

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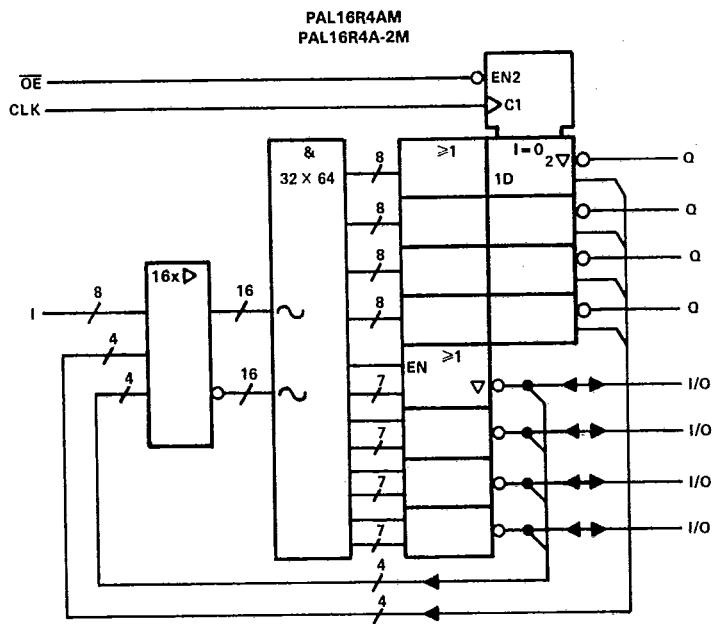
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STANDARD HIGH-SPEED PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D



functional block diagrams (positive logic)

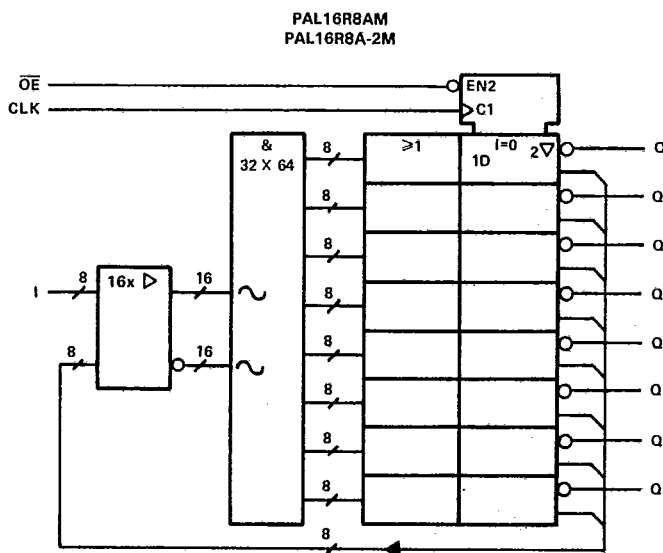
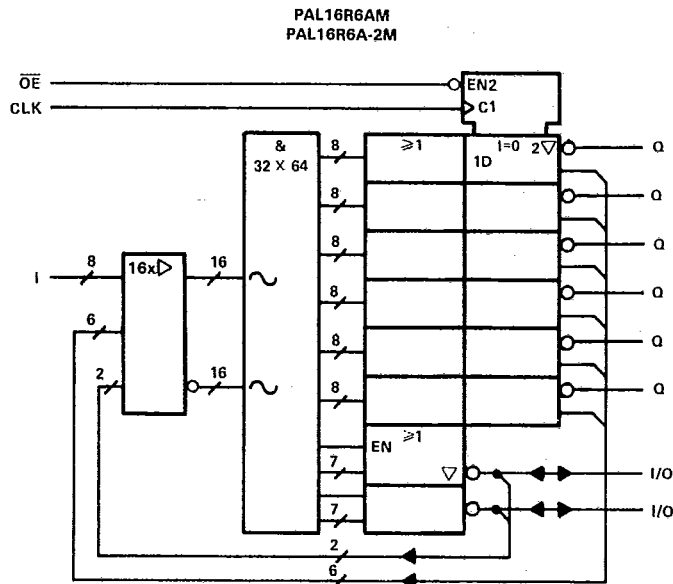


~ denotes fused inputs

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STANDARD HIGH-SPEED PAL® CIRCUITS

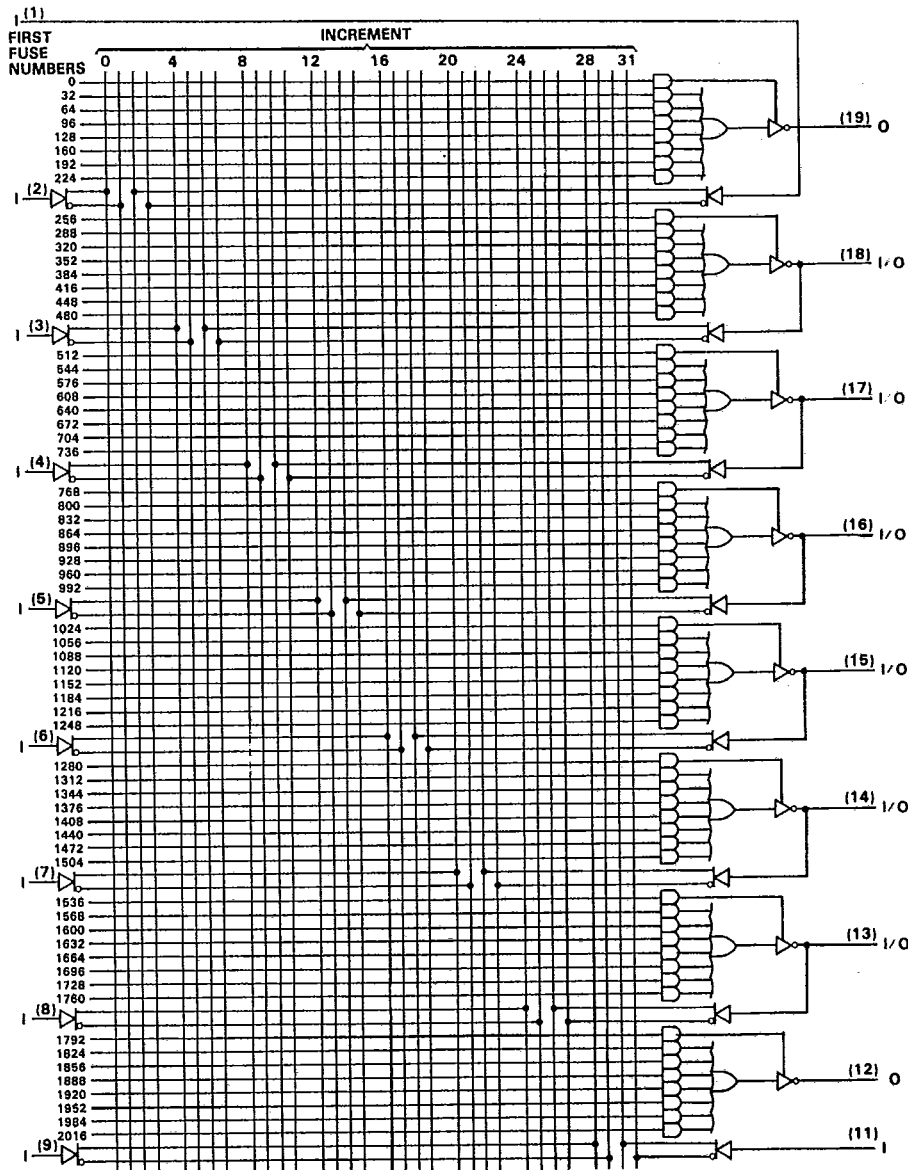
TEXAS INSTR (ASIC/MEMORY) 25E D

functional block diagrams (positive logic)



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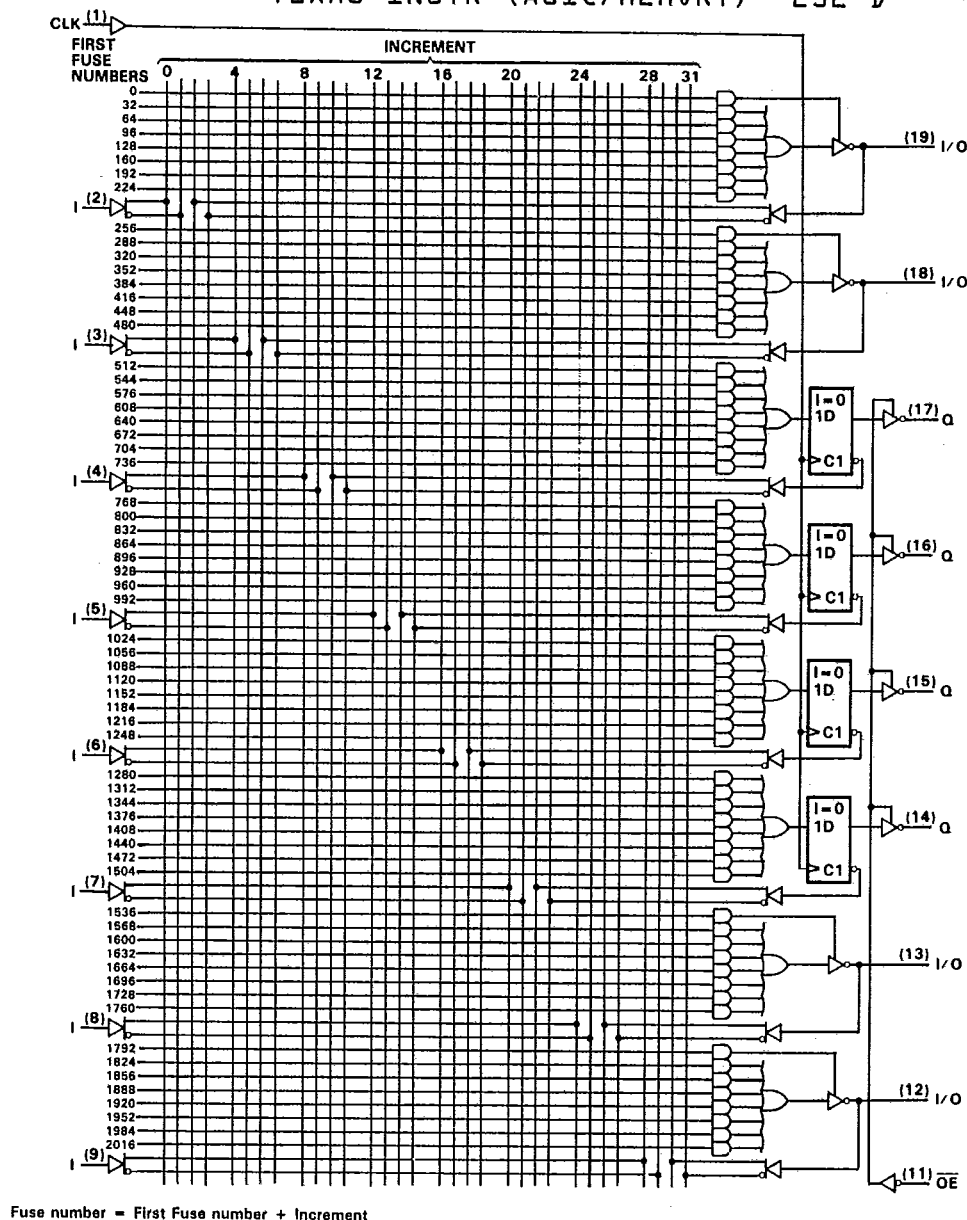
TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

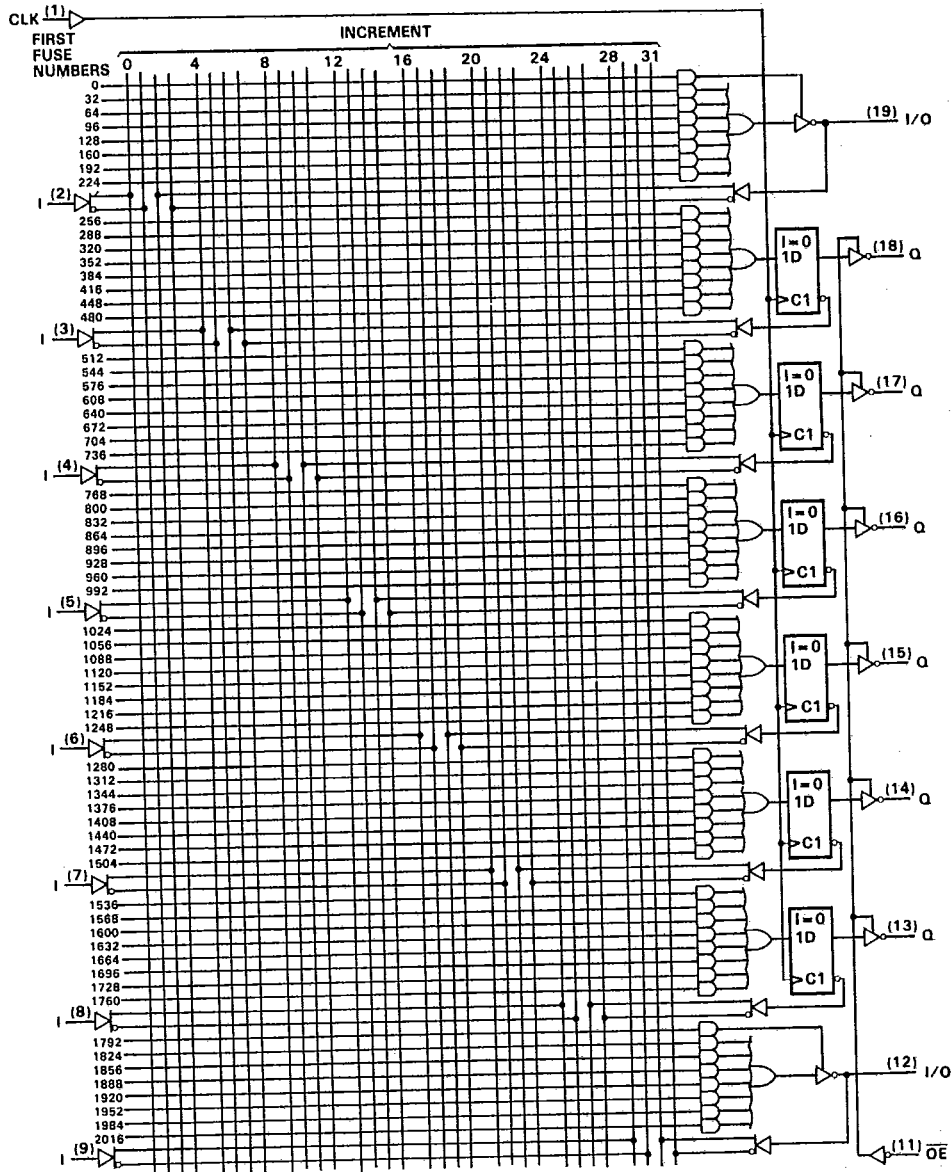
PAL16R4AM, PAL16R4A-2M
STANDARD HIGH-SPEED PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D



PAL16R6AM, PAL16R6A-2M
STANDARD HIGH-SPEED PAL® CIRCUITS

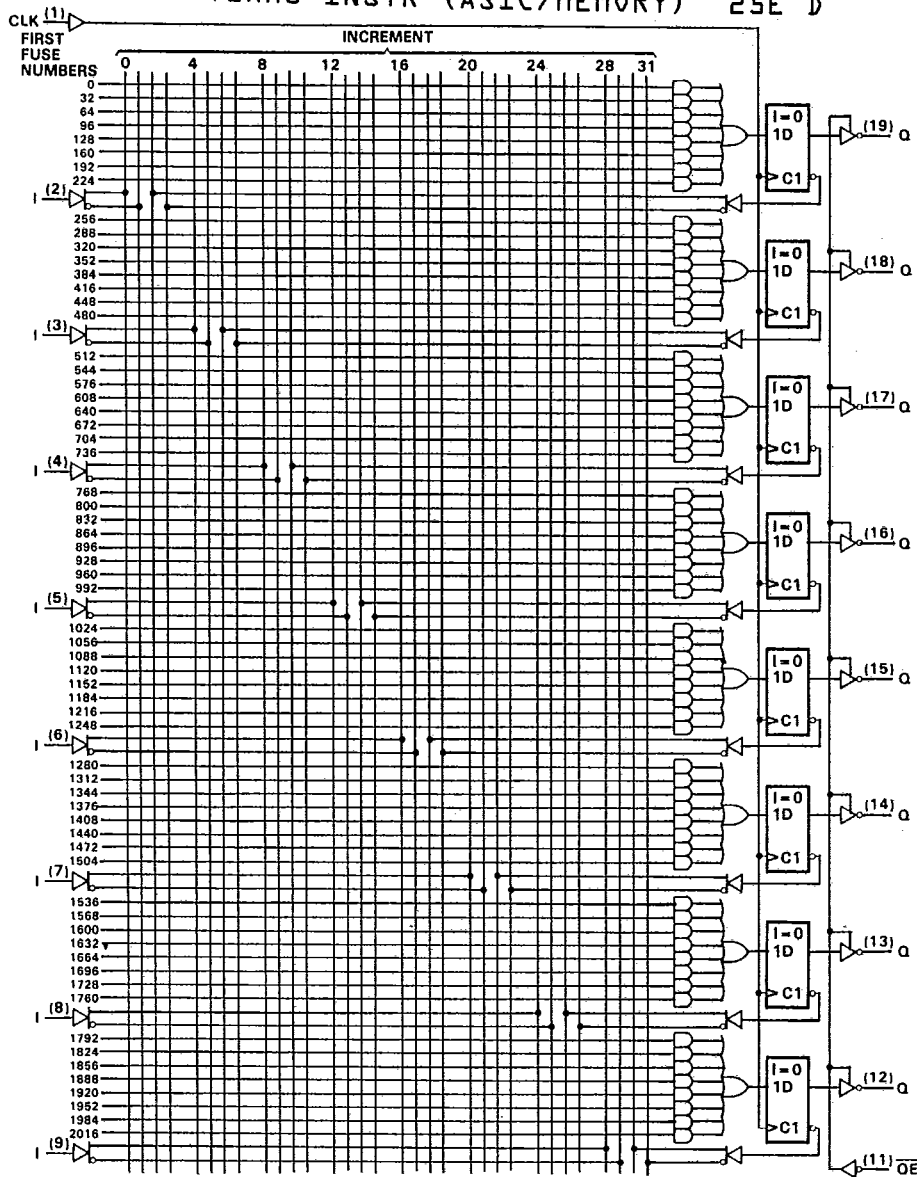
TEXAS INSTR (ASIC/MEMORY) 25E D



Fuse number = First Fuse number + Increment

PAL16R8AM, PAL16R8A-2M
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STANDARD HIGH-SPEED PAL® CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to a disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	OE input		5.5	V
		All others		5.5	
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	-55		125	°C

TEXAS INSTR (ASIC/MEMORY) 25E D

PAL16L8AM, PAL16R4AM, PAL16R6AM, PAL16R8AM
STANDARD HIGH-SPEED PAL® CIRCUITS

TEXAS INSTR (ASIC/MEMORY) 25E D

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2 mA	2.4	3.2		V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = -12 mA		0.25	0.4	V
I _{OZH}	Outputs I/O ports V _{CC} = 5.5 V, V _O = 2.7 V		20		μA
			100		
I _{OZL}	Outputs I/O ports V _{CC} = 5.5 V, V _O = 0.4 V		-20		μA
			-100		
I _I	V _{CC} = 5.5 V, V _I = 5.5 V		0.2		mA
I _{IH}	I/O ports All others V _{CC} = 5.5 V, V _I = 2.7 V		100		μA
			25		
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		mA
	OE input All others		-0.1		
I _{OS} ‡	V _{CC} = 5.5 V, V _O = 0.5 V	-30		-250	mA
I _{CC}	V _{CC} = 5.5 V, V _I = 0 V, Outputs open		75	180	mA

timing requirements

	MIN	MAX	UNIT
f _{clock} Clock frequency	0	25	MHz
t _w Pulse duration (see Note 2)			
	Clock high	15	ns
	Clock low	20	
t _{su} Setup time, input or feedback before CLK†	25		ns
t _h Hold time, input or feedback after CLK†	0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{max}				25	45		MHz
t _{pd}	I, I/O,	O, I/O			15	30	ns
t _{pd}	CLK†	Q			10	20	ns
t _{en}	OE‡	Q			15	25	ns
t _{dis}	OE‡	Q			10	25	ns
t _{en}	I, I/O	O, I/O			14	30	ns
t _{dis}	I, I/O	O, I/O			13	30	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

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TEXAS INSTR (ASIC/MEMORY) 25E D

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2 mA	2.4	3.2		V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4	V
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			20	μA
				100	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V			-20	μA
				-100	
I _I	V _{CC} = 5.5 V, V _I = 5.5 V			0.2	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			100	μA
				25	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2	mA
				-0.1	
I _{OS} ‡	V _{CC} = 5.5 V, V _O = 0.5 V	-30		-250	mA
I _{CC}	V _{CC} = 5.5 V, V _I = 0 V, Outputs open		75	90	mA

timing requirements

	MIN	MAX	UNIT
f _{clock} Clock frequency	0	16	MHz
t _w Pulse duration, (see Note 2)			ns
	Clock high	25	
	Clock low	25	
t _{su} Setup time, input or feedback before CLK†	35		ns
t _h Hold time, input or feedback after CLK†	0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}				16	25		MHz
t _{pd}	I, I/O,	O, I/O			25	40	ns
t _{pd}	CLK†	Q			11	35	ns
t _{en}	OE†	Q			20	35	ns
t _{dis}	OE†	Q			11	30	ns
t _{en}	I, I/O	O, I/O			25	40	ns
t _{dis}	I, I/O	O, I/O			25	35	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

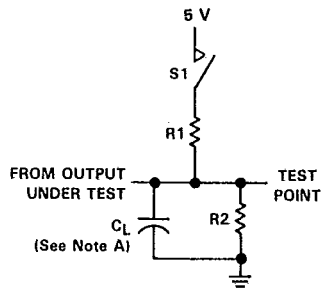
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

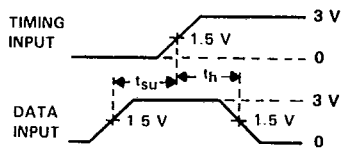
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

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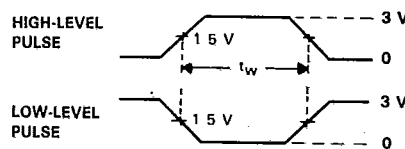
PARAMETER MEASUREMENT INFORMATION



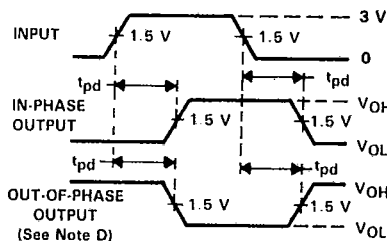
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



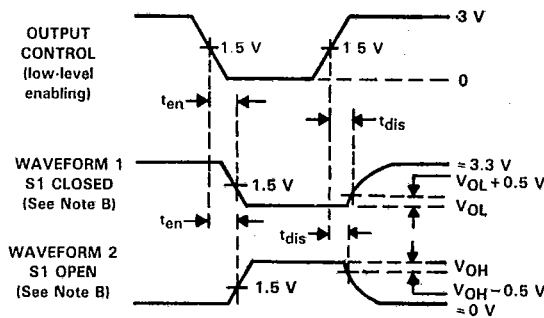
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} 5 pF for t_{dis} .
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 1

TEXAS INSTR (ASIC/MEMORY) 25E D