Integrated Circuit Systems, Inc.

ICS950901

Programmable Timing Control Hub™ for P4™

Recommended Application:

VIA P4X266 chipset with PC133 or DDR memory.

Output Features:

- 2 - Pair of differential CPU clocks @ 3.3V
- 1 - Pair of differential push pull CPU_CS clocks @ 2.5V
- 3 - AGP @ 3.3V
- 9 - PCI @ 3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V
- 1 - REF @ 3.3V, 14.318MHz

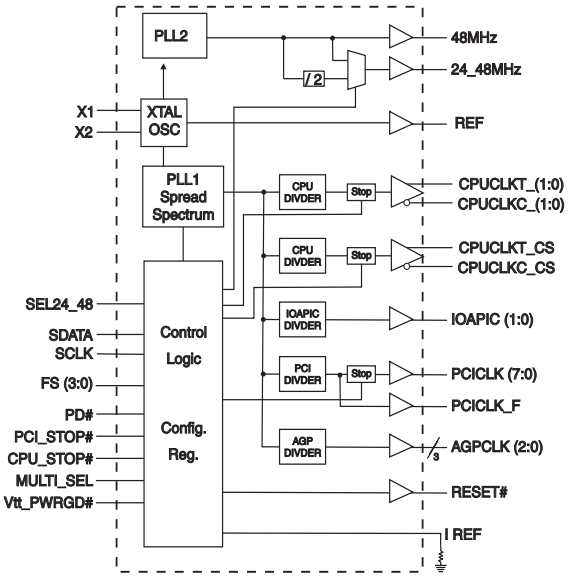
Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- For DDR and or PC133 SDRAM system use ICS93718 as the memory buffer.
- Uses external 14.318MHz crystal.

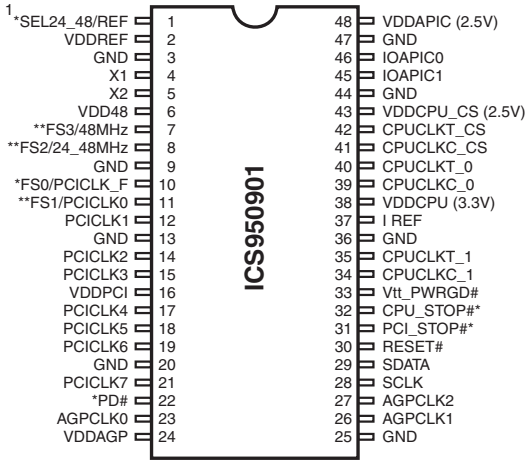
Key Specifications:

- CPU_CS - CPU0: <±250ps
- CPU_CS - AGP: <±250ps
- PCI - PCI: <500ps
- CPU - PCI: Min = 1.0ns, Typ = 2.0ns, Max = 4.0ns

Block Diagram



Pin Configuration



48-Pin 300-mil SSOP

1. These outputs have 2X drive strength.

* These inputs have a internal Pull-up resistor of 120K to VDD

** These inputs have a internal pull-down to GND

Frequency Table

FS3	FS2	FS1	FS0	CPUCLK MHz	AGP MHz	PCICLK MHz
0	0	0	0	66.67	66.66	33.33
0	0	0	1	100.00	66.67	33.33
0	0	1	0	133.33	66.67	33.33
0	0	1	1	200.00	66.66	33.33
0	1	0	0	100.90	67.27	33.63
0	1	0	1	103.00	68.67	34.33
0	1	1	0	107.00	71.33	35.67
0	1	1	1	110.00	73.33	36.67
1	0	0	0	133.90	66.95	33.48
1	0	0	1	137.33	68.66	34.33
1	0	1	0	140.00	70.00	35.00
1	0	1	1	142.66	71.33	35.67
1	1	0	0	145.33	72.66	36.33
1	1	0	1	146.66	73.33	36.67
1	1	1	0	153.33	76.66	38.33
1	1	1	1	160.00	80.00	40.00

General Description

The **ICS950901** is a single chip clock solution for desktop designs using the VIA P4X266 chipset with PC133 or DDR memory. with PC133 or DDR memory. When used with a fanout buffer such as the ICS93712, ICS93715 or the ICS93718 provides all the necessary clock signals for such a system.

The **ICS950901** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	SEL24_48	IN	Selects either 24 or 48MHz output.
	REF	OUT	3.3V, 14.318MHz reference clock output.
2, 6, 16, 24, 38	VDD	PWR	3.3V power supply.
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2.
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF).
7	FS3	IN	Logic input frequency select bit. Input latched at power on.
	48MHz	OUT	3.3V Fixed 48MHz clock output..
8	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24_48MHz	OUT	Selectable 24 or 48MHz output.
3, 9, 13, 20, 25, 36, 44, 47	GND	PWR	Ground pins for 3.3V supply.
10	FS0	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK_F	OUT	3.3V Free running PCI clock output
11	FS1	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK0	OUT	3.3V PCI clock output.
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
21, 19, 18, 17, 15, 14	PCICLK (7:2)	OUT	3.3V PCI clock outputs.
27, 26, 23	AGP (2:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
28	SCLK	IN	Clock pin for I^2C circuitry 5V tolerant.
29	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant.
30	RESET#	OUT	Real time system reset signal for frequency value or watchdog timmer timeout. This signal is active low.
33	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS (3:0) is valid and ready to be sampled (active low).
34, 39	CPUCLKC_(1:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
35, 40	CPUCLKT_(1:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
37	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
41	CPUCLKC_CS	OUT	Complementory"" clocks of differential pair CPU outputs. These are 2.5V push-pull outputs.
42	CPUCLKT_CS	OUT	True"" clocks of differential pair CPU outputs. These are 2.5V push-pull outputs.
43	VDDCPU_CS (2.5V)	PWR	Power for CPUCLK_CS outputs 2.5V.
45, 46	IOAPIC (1:0)	OUT	2.5V clock outputs
48	VDDAPIC (2.5V)	PWR	Power for APIC clocks 2.5V.

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General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

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Byte 0: Functionality and frequency select register (Default=0)

Bit		Description								PWD
	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	AGPCLK MHz	PCICLK MHz	Spread %	
		FS3	FS2	FS1	FS0					
	0	0	0	0	0	66.67	66.66	33.33	+/- 0.30% Center Spread	
	0	0	0	0	1	100.00	66.67	33.33	+/- 0.30% Center Spread	
	0	0	0	1	0	133.33	66.67	33.33	+/- 0.30% Center Spread	
	0	0	0	1	1	200.00	66.66	33.33	+/- 0.30% Center Spread	
	0	0	1	0	0	100.90	67.27	33.63	+/- 0.30% Center Spread	
	0	0	1	0	1	103.00	68.67	34.33	+/- 0.30% Center Spread	
	0	0	1	1	0	107.00	71.33	35.67	+/- 0.30% Center Spread	
	0	0	1	1	1	110.00	73.33	36.67	+/- 0.30% Center Spread	
	0	1	0	0	0	133.90	66.95	33.48	+/- 0.30% Center Spread	
	0	1	0	0	1	137.33	68.66	34.33	+/- 0.30% Center Spread	
	0	1	0	1	0	140.00	70.00	35.00	+/- 0.30% Center Spread	
	0	1	0	1	1	142.66	71.33	35.67	+/- 0.30% Center Spread	
	0	1	1	0	0	145.33	72.66	36.33	+/- 0.30% Center Spread	
	0	1	1	0	1	146.66	73.33	36.67	+/- 0.30% Center Spread	
Bit (2,7:4)	0	1	1	1	0	153.33	76.66	38.33	+/- 0.30% Center Spread	Note 1
	0	1	1	1	1	160.00	80.00	40.00	+/- 0.30% Center Spread	
	1	0	0	0	0	66.67	66.66	33.33	0 to - 0.6% Down Spread	
	1	0	0	0	1	100.00	66.67	33.33	0 to - 0.6% Down Spread	
	1	0	0	1	0	133.33	66.67	33.33	0 to - 0.6% Down Spread	
	1	0	0	1	1	200.00	66.66	33.33	0 to - 0.6% Down Spread	
	1	0	1	0	0	66.67	66.66	33.33	+/- 0.50% Center Spread	
	1	0	1	0	1	100.00	66.67	33.33	+/- 0.50% Center Spread	
	1	0	1	1	0	133.33	66.67	33.33	+/- 0.50% Center Spread	
	1	0	1	1	1	200.00	66.66	33.33	+/- 0.30% Center Spread	
	1	1	0	0	0	201.00	67.00	33.50	+/- 0.30% Center Spread	
	1	1	0	0	1	203.00	67.67	33.83	+/- 0.30% Center Spread	
	1	1	0	1	0	205.00	68.33	34.17	+/- 0.30% Center Spread	
	1	1	0	1	1	207.00	69.00	34.50	+/- 0.30% Center Spread	
	1	1	1	0	0	209.00	69.67	34.83	+/- 0.30% Center Spread	
	1	1	1	0	1	211.00	70.33	35.17	+/- 0.30% Center Spread	
	1	1	1	1	0	213.00	71.00	35.50	+/- 0.30% Center Spread	
	1	1	1	1	1	215.00	71.67	35.83	+/- 0.30% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2,7:4									0
Bit 1	0 - Normal 1 - Spread spectrum enable									1
Bit 0	0 - Watch dog safe frequency will be selected by latch inputs 1 - Watch dog safe frequency will be programmed by Byte 10 bit (4:0)									0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

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Byte 1: CPU Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	-	1	(Reserved)
Bit6	10	1	PCICLK_F (Active/Inactive)
Bit5	-	1	(Reserved)
Bit4	-	0	(Reserved)
Bit3	-	0	(Reserved)
Bit2	35, 34	1	CPUCLKT/C1 (Active/Inactive)
Bit1	40, 39	1	CPUCLKT/C0 (Active/Inactive)
Bit0	42, 41	1	CPUCLKT/C_CS (Active/Inactive)

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	21	1	PCICLK7 (Active/Inactive)
Bit6	19	1	PCICLK6 (Active/Inactive)
Bit5	18	1	PCICLK5 (Active/Inactive)
Bit4	17	1	PCICLK4 (Active/Inactive)
Bit3	15	1	PCICLK3 (Active/Inactive)
Bit2	14	1	PCICLK2 (Active/Inactive)
Bit1	12	1	PCICLK1 (Active/Inactive)
Bit0	11	1	PCICLK0 (Active/Inactive)

Byte 3: Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	-	1	Reserved
Bit6	1	1	SEL 24_48, 0=24Mhz 1=48MHz
Bit5	-	1	(Reserved)
Bit4	46	1	IOAPIC 0
Bit3	45	1	IOAPIC 1
Bit2	23	1	AGPCLK 0
Bit1	26	1	AGPCLK 1
Bit0	27	1	AGPCLK 2

Byte 4: Frequency Select Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	Latched FS3#
Bit 6	-	X	Latched FS2#
Bit 5	-	X	Latched FS1#
Bit 4	-	X	Latched FS0#
Bit 3	7	1	48MHz (Active/Inactive)
Bit 2	8	1	24_48MHz (Active/Inactive)
Bit 1	-	0	Reserved
Bit 0	1	1	REF (Active/Inactive)

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Byte 5: Peripheral Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	X	-	(Reserved)
Bit 6	X	-	(Reserved)
Bit 5	X	-	(Reserved)
Bit 4	X	-	(Reserved)
Bit 3	X	-	(Reserved)
Bit 2	X	-	(Reserved)
Bit 1	X	-	(Reserved)
Bit 0	X	-	(Reserved)

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Name	PWD	Description
Bit 7	Revision ID Bit3	X	Revision ID values will be based on individual device's revision
Bit 6	Revision ID Bit2	X	
Bit 5	Revision ID Bit1	X	
Bit 4	Revision ID Bit0	X	
Bit 3	Vendor ID Bit3	0	(Reserved)
Bit 2	Vendor ID Bit2	0	(Reserved)
Bit 1	Vendor ID Bit1	0	(Reserved)
Bit 0	Vendor ID Bit0	1	(Reserved)

Byte 7: Revision ID and Device ID Register

Bit	Name	PWD	Description
Bit 7	Device ID7	1	Device ID values will be based on individual device "01h" in this case.
Bit 6	Device ID6	0	
Bit 5	Device ID5	0	
Bit 4	Device ID4	1	
Bit 3	Device ID3	1	
Bit 2	Device ID2	0	
Bit 1	Device ID1	1	
Bit 0	Device ID0	0	

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

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Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 8 • 290ms = 2.3 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	0	
Bit 3	WD3	1	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I²C programing.
Bit 6	WD Enable	0	Watchdog Enable bit. This bit will over write WDEN latched value. 0 = disable, 1 = Enable.
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	1	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

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Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	CPU 0/1 Div 3	0	CPU 0/1 clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	CPU 0/1 Div 2	1	
Bit 5	CPU 0/1 Div 1	0	
Bit 4	CPU 0/1 Div 0	1	
Bit 3	CPU_CS Div 3	0	CPU_CS clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU_CS Div 2	1	
Bit 1	CPU_CS Div 1	0	
Bit 0	CPU_CS Div 0	1	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP Div 3	0	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	AGP Div 2	1	
Bit 5	AGP Div 1	0	
Bit 4	AGP Div 0	1	
Bit 3	APIC Div 3	0	IOAPIC clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 2	APIC Div 2	1	
Bit 1	APIC Div 1	0	
Bit 0	APIC Div 0	1	

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Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP_INV	0	AGP Phase Inversion bit
Bit 6	APIC_INV	0	APIC Phase Inversion bit
Bit 5	CPU 0/1_INV	0	CPU 0/1 Phase Inversion bit
Bit 4	CPU_CS_INV	0	CPU_CS Phase Inversion bit
Bit 3	PCI Div 3	1	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 2	PCI Div 2	0	
Bit 1	PCI Div 1	0	
Bit 0	PCI Div 0	1	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/9	/18	/36	/72

Byte 18: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	CPU_Skew 1	1	These 2 bits delay the CPUCLKC/T_CS with respect to CPUCLKC/T (1:0) 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 6	CPU_Skew 0	0	
Bit 5	CPU_Skew 1	1	These 2 bits delay the CPUCLKC/T (1:0) clock with respect to CPUCLKC/T_CS 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 4	CPU_Skew 0	0	
Bit 3	AGPCLK	1	Group Skew Control
Bit 2	AGPCLK	0	Group Skew Control
Bit 1	AGPCLK	1	Group Skew Control
Bit 0	AGPCLK	0	Group Skew Control

Byte 19: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	IOAPIC	1	Group Skew Control
Bit 6	IOAPIC	0	
Bit 5	IOAPIC	0	
Bit 4	IOAPIC	0	
Bit 3	PCICLK (7:0)	1	
Bit 2	PCICLK (7:0)	0	
Bit 1	PCICLK (7:0)	0	
Bit 0	PCICLK (7:0)	0	

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Byte 20: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	PCI_Skew 3	1	These 4 bits can change the CPU to PCI (7:0) skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of Bits (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 6	PCI_Skew 2	0	
Bit 5	PCI_Skew 1	0	
Bit 4	PCI_Skew 0	0	
Bit 3	PCIF_Skew 3	1	These 4 bits can change the CPU to PCIF skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of Bit (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 2	PCIF_Skew 2	0	
Bit 1	PCIF_Skew 1	0	
Bit 0	PCIF_Skew 0	0	

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	PCIF_1_Slew 1	0	PCIFclock slew rate control bits.
Bit 6	PCIF_1_Slew 0	1	01 = strong:11 = normal; 10 = weak
Bit 5	PCIF_0_Slew 1	0	PCI clock slew rate control bits.
Bit 4	PCIF_0_Slew 0	1	01 = strong: 11 = normal; 10 = weak
Bit 3	AGP (2:1)_Slew 1	0	AGP (2:1) clock slew rate control bits.
Bit 2	AGP (2:1)_Slew 1	1	01 = strong: 11 = normal; 10 = weak
Bit 1	AGP_0_Slew 1	0	AGP_0 clock slew rate control bits.
Bit 0	AGP_0_Slew 0	1	01 = strong: 11 = normal; 10 = weak

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	REF Slew 1	0	REF clock slew rate control bits.
Bit 6	REF Slew 0	1	01 = strong: 11 = normal; 10 = weak
Bit 5	PCI (7:4) Slew 1	0	PCI (6:4) clock slew rate control bits.
Bit 4	PCI (7:4) Slew 0	1	01 = strong: 11 = normal; 10 = weak
Bit 3	PCI (3:1) Slew 1	0	PCI (3:1) clock slew rate control bits.
Bit 2	PCI (3:1) Slew 0	1	01 = strong: 11 = normal; 10 = weak
Bit 1	PCI0 Slew 1	0	PCI0 clock slew rate control bits.
Bit 0	PCI0 Slew 0	1	01 = strong: 11 = normal; 10 = weak

Byte 23: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	
Bit 5	Reserved	X	Reserved
Bit 4	Reserved	X	
Bit 3	48-24 Slew 1	0	48-24 clock slew rate control bits.
Bit 2	48-24 Slew 0	1	01 = strong: 11 = normal; 10 = weak
Bit 1	48-24 Slew 1	0	48-24 clock slew rate control bits.
Bit 0	48-24 Slew 0	1	01 = strong: 11 = normal; 10 = weak

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters.

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V + - 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{ih}		2		V_{DD}+0.3	V
Input Low Voltage	V_{il}		V_{SS}-0.3		0.8	V
Input High Current	I_{ih}	V_{in} = V_{DD}	-5		5	mA
Input Low Current	I_{il1}	V_{in} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{in} = 0 V; Inputs with no pull-up resistors	-200			mA
Operating	$I_{DD3.3OP}$	C_l = 0 pF; Select @ 66M			100	mA
Supply Current		C_l = Full load @ 133.3 MHz		181	280	mA
Power Down		I_{REF}=2.32mA		13	20	mA
Supply Current	$I_{DD3.3PD}$	I_{REF}= 5mA			37	mA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Pin Inductance	L_{pin}				7	nH
	C_{IN}	Logic Inputs			5	pF
Input Capacitance$_1$	C_{out}	Output pin capacitance			6	pF
	C_{INX}	X_1 & X_2 pins	27		45	pF
Transition Time$_1$	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time$_1$	T_s	From 1st crossing to 1% target Freq.			3	ms
Clk Stabilization$_1$	T_{STAB}	From V_{DD} = 3.3V to 1% target Freq.			3	ms
	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	ns
Delay	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	ns

$_1$ Guarenteed by design, not 100% tested in production.

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Electrical Characteristic - CPUCLKC/T

TA = 0 - 70º C; VDD = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output						
Impedance	Z_o	$V_o = V_x$	3000			Ω
Output High Voltage	V_{oh}	V_r = 475W +1%; I_{REF}=2.32mA; Ioh = 6*IREF		0.71	1.2	V
Output High Current	I_{oh}			-13.92		mA
Rise Time$_1$	t_r	V_{ol} = 20%, V_{oh} = 80%, 0.175 - 0.525 V	175	263	700	ps
Differential Crossover	V_x		45	50	55	%
Duty Cycle$_1$	d_t	V_t = 50%	45	51	55	%
Skew1, CPU to CPU	t_{sk}	V_t = 50%		55	150	ps
Jitter, Cycle-to-cycle$_1$	$t_{jcyc-cyc}$	$V_t = V_x$		105	200	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKTC_CS

T_A = 0 - 70º C; V_{DD} = 2.5V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{oh2b}	I_{oh} = -12.0 mA	2			V
Output Low Voltage	V_{ol2b}	I_{ol} = 12 mA			0.4	V
Output High Current	I_{oh2b}	V_{oh} = 1.7 V			-19	mA
Output Low Current	I_{ol2b}	V_{ol} = 0.7 V	19			mA
Rise Time	t_{r2B}	V_{ol} = 0.4 V, V_{oh} = 2.0 V		0.75	1.6	ns
Differential Crossover	V_x		45	50	55	%
Duty Cycle	d_{t2B}	V_t = 1.25 V, Typ: crossing	45	50.9	55	%
Skew	t_{sk2B}	V_t = 1.25 V			175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$	V_t = 1.25 V		155	250	ps
Jitter, One Sigma	t_{j1s2B}	V_t = 1.25 V			150	ps
Jitter, Absolute	t_{jabs2B}	V_t = 1.25 V	-250		250	ps

1Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{01}			33.33		MHz
Output Impedance	R_{DSN1}	Vo = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{oh1}	I_{oh} = -1 mA	2.4			V
Output Low Voltage	V_{ol1}	I_{ol} = 1 mA			0.55	V
Output High Current	I_{oh1}	V_{OH}@ MIN = 1.0 V, V_{OH}@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{ol1}	V_{OL}@ MIN = 1.95 V, V_{OL}@ MAX= 0.4 V	30		38	mA
Rise Time	t_{r1}	V_{ol} = 0.4 V, V_{oh} = 2.4 V	0.5	1.91	2	ns
Fall Time	t_{f1}	V_{oh} = 2.4 V, V_{ol} = 0.4 V	0.5	1.68	2	ns
Duty Cycle	d_{t1}	V_t = 1.5 V	45	49.7	55	%
Skew	t_{sk1}	V_t = 1.5 V		332	500	ps
Jitter	$t_{jcyc-cyc}$	V_t = 1.5 V		116	250	ps

$_1$Guarenteed by design, not 100% tested in production.

Electrical Characteristics - AGP

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}	V_o = V_{DD}*(0.5)	12		55	Ω
Output Impedance	R_{DSN1}	V_o = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{oh} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{ol} = 1 mA			0.55	V
Output High Current	I_{OH1}	V_{OH}@ MIN = 1.0 V, V_{OH}@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	V_{OL}@ MIN = 1.95 V, V_{OL}@ MAX= 0.4 V	30		38	mA
Rise Time	t_{r1}	V_{ol} = 4 V, V_{oh} = 2.4 V	0.5	1.16	2	ns
Fall Time	t_{f1}	V_{oh} = 2.4 V, V_{ol} = 0.4 V	0.5	1.22	2	ns
Duty Cycle	d_{t1}	V_t = 1.5 V	45	51.8	55	%
Skew	t_{sk1}	V_t = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$	V_t = 1.5 V		84	500	ps

$_1$Guarenteed by design, not 100% tested in production.

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Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{oh4b}	I_{oh} = -12 mA	2			V
Output Low Voltage	V_{ol4b}	I_{ol} = 12 mA			0.4	V
Output High Current	I_{oh4b}	V_{oh} = 1.7 V			-19	mA
Output Low Current	I_{ol4b}	V_{ol} = 0.7 V	19			mA
Rise Time$_1$	T_{r4B}	V_{ol} = 0.4 V, V_{OH} = 2.0 V		1.16	2	ns
Fall Time$_1$	T_{f4B}	V_{oh} = 2.0 V, V_{OL} = 0.4 V		1.09	2	ns
Duty Cycle$_1$	D_{t4B}	V_t = 1.25 V	45	49.9	55	%
Jitter, One Sigma$_1$	T_{j1s4B}	V_t = 1.25 V			0.5	ns
Jitter, Absolute$_1$	T_{jabs4B}	V_t = 1.25 V	-1		1	ns
Jitter, Cycle to Cycle	Normal	V_t = 1.25 V		89	250	ps

$_1$Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O	V_o = V_{DD}*(0.5)		48		MHz
Output Impedance	R_{DSN1}	V_o = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{oh} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{ol} = 1 mA			0.55	V
Output High Current	I_{OH1}	V_{OH}@ MIN = 1.0 V, V_{OH}@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	V_{OL}@ MIN = 1.95 V, V_{OL}@ MAX= 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}	V_{ol} = 0.4 V, V_{oh} = = 2.4 V	0.5	1.32	1	ns
48DOT Fall Time	t_{f1}	V_{oh} = 2.4 V, V_{ol} = 0.4 V	0.5	1.28	1	ns
VCH 48 USB Rise Time	t_r	V_{ol} = 0.4 V, V_{oh} = 2.4 V	1	1.32	2	ns
VCH 48 USB Fall Time	t_{f1}	V_{oh} = 2.4 V, V_{ol} = 0.4 V	1	1.26	2	ns
48 DOT to 48 USB Skew	t_{skew1}	V_t = 1.5 V		0.3	1	ns
Duty Cycle	d_{t1}	V_t = 1.5 V	45	52.7	55	%
Jitter	$t_{jcyc-cyc}$	V_t = 1.5 V		119	350	ps

$_1$Guarenteed by design, not 100% tested in production

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Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{o1}					MHz
Output Impedance	R_{dsp1}	$V_o = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{oh1}	I_{oh} = -1 mA	2.4			V
Output Low Voltage	V_{ol1}	I_{ol} = 1 mA			0.4	V
Output High Current	I_{oh1}	V_{OH}@ MIN = 1.0 V, V_{OH}@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{ol1}	V_{OL}@ MIN = 1.95 V, V_{OL}@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}	V_{ol} = 0.4 V, V_{oh} = 2.4 V	1	0.89	4	ns
Fall Time	t_{f1}	V_{oh} = 2.4 V, V_{OL} = 0.4 V	1	0.72	4	ns
Duty Cycle	d_{t1}	V_t = 1.5 V	45	54.6	55	%
Jitter	$t_{jcyc-cyc}$	V_t = 1.5 V		234	500	ps

$_1$Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH\ @MIN}$= 1.0V , $V_{OH@\ MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL\ @MIN}$= 1.2V , $V_{OL@\ MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

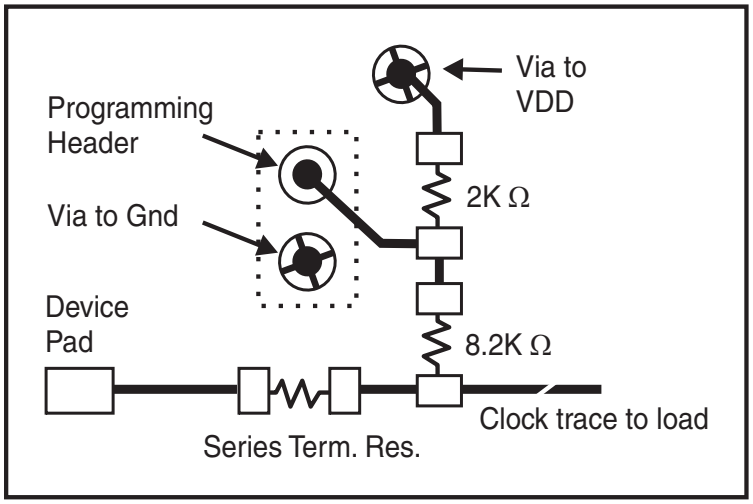

Fig. 1

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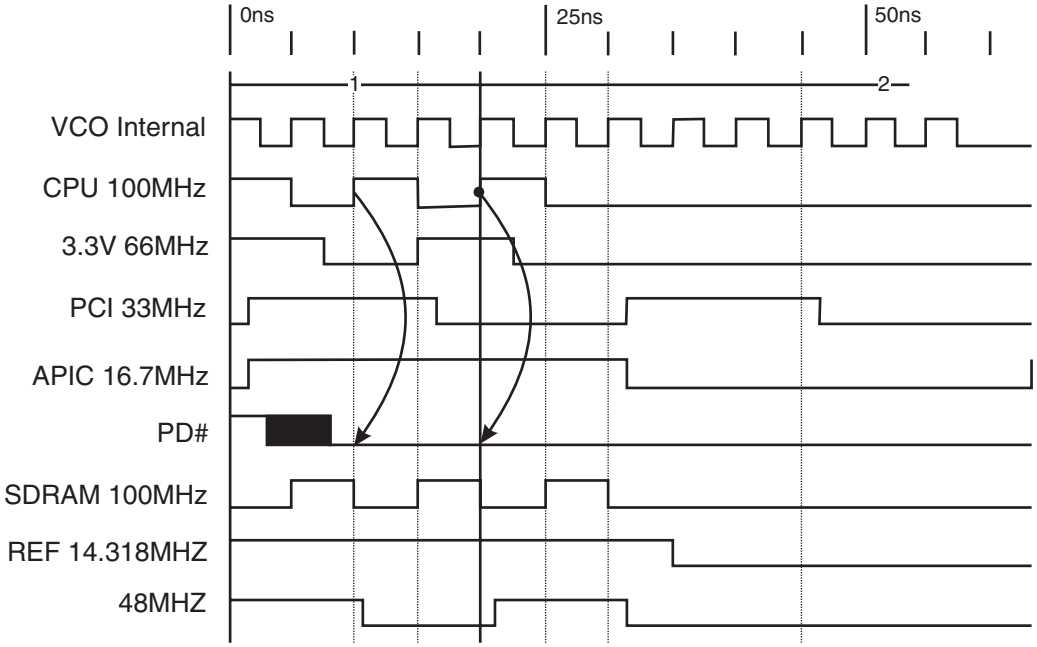
Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

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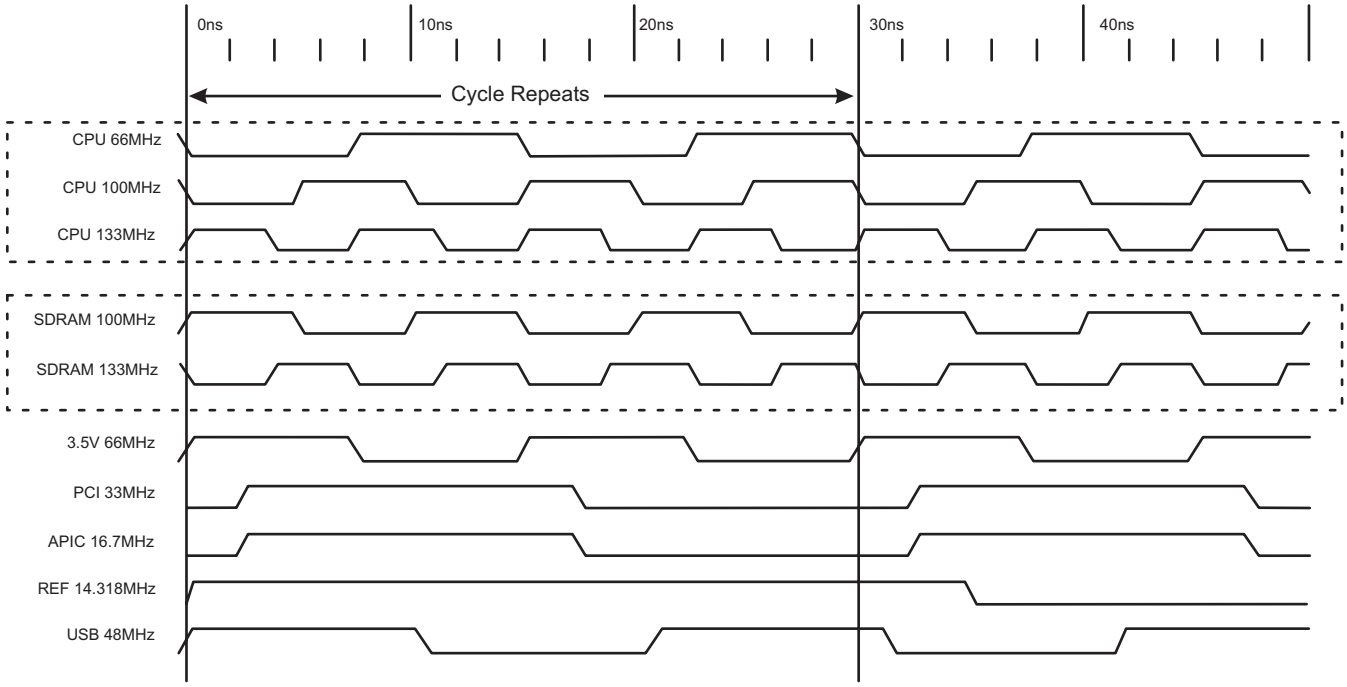
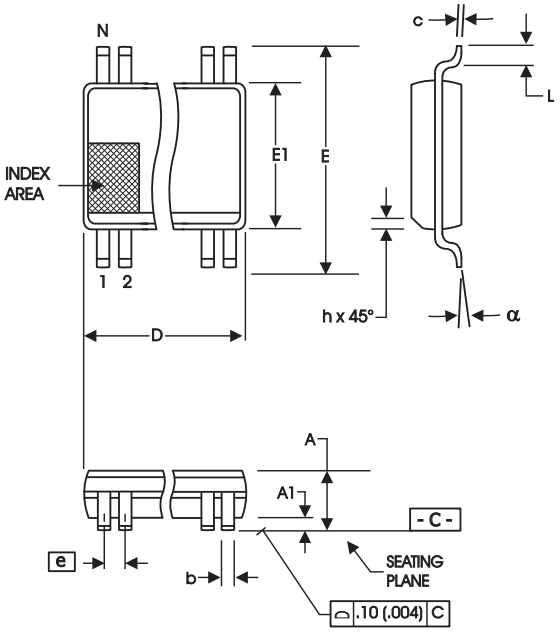


Group Offset Waveforms

Third party brands and names are the property of their respective owners.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950901yFLFT

Example:

ICS XXXX y F LF - T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

Registered Company

9001

For more information on Integrated Circuit Systems Inc. or any of our products please visit our web site at:
http://www.icst.com

Revision History

Rev.	Issue Date	Description	Page #
F	5/25/2005	Added LF Ordering Information.	19

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