12-BIT 20MSPS ADC BW1009L

GENERAL DESCRIPTION

The BW1009L is a CMOS 12-bit analog-to-digital converter (ADC). It converts the analog input signal into 12bit binary digital codes at a maximum sampling rate of 20MHz.

The device is a monolithic ADC with an on-chip, high-performance, sample-and-hold Amplifier (SHA) and current reference. The structure allows both differential and single-ended input.

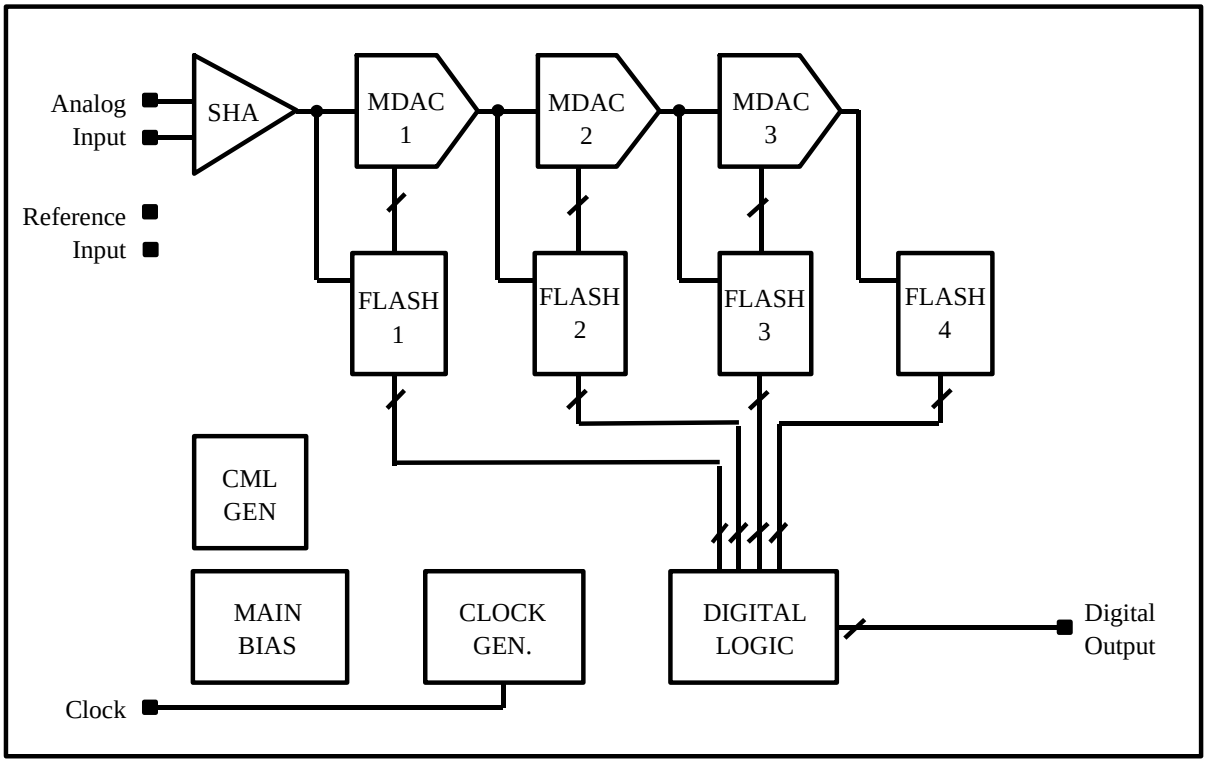
TYPICAL APPLICATIONS

High Definition TV (HDTV)
Video Applications
CCD Imaging (Copiers, Scanners, Cameras)
Medical Imaging
Digital Communications

FEATURES

- **Resolution : 12-bit**
- **Maximum Conversion Rate : 20MHz**
- **Package Type : 48TSSOP**
- **Power Supply : 3.3V**
- **Power Consumption : 150mW (typical)**
- **Reference Voltage : 2V, 1V (dual reference)**
- **Input Range : 0.5V ~ 2.5V ($2.0V_{P-P}$)**
- **Differential Linearity Error : ±1.0 LSB**
- **Integral Linearity Error : ±2.0 LSB**
- **Signal to Noise & Distortion Ratio : 62dB**
- **Digital Output : CMOS Level**
- **Operating Temperature Range : 0°C ~ 70°C**

FUNCTIONAL BLOCK DIAGRAM



Ver 1.6 (Apr. 2002)

CORE PIN DESCRIPTION

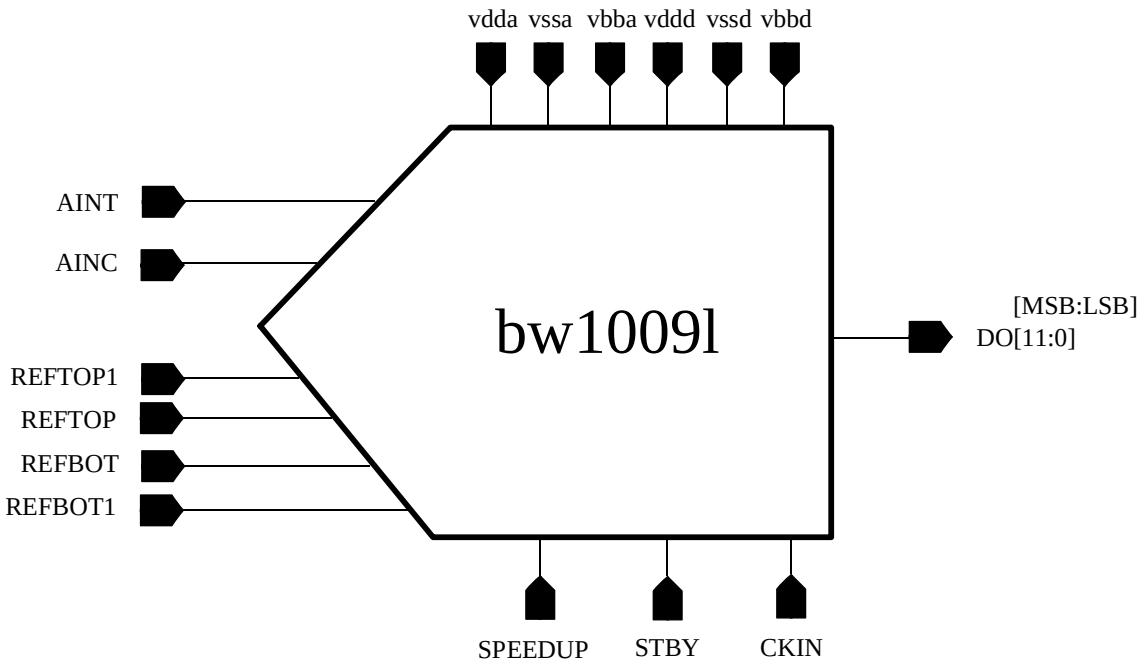
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
REFTOP1	AI	piar50_bb	Reference Top Sense (2.0V)
REFTOP	AI	pia_bb	Reference Top Force (2.0V)
REFBOT	AI	pia_bb	Reference Bottom Force (1.0V)
REFBOT1	AI	piar50_bb	Reference Bottom Sense (1.0V)
VDDA	AP	vdda	Analog Power (3.3V)
VBBA	AG	vbba	Analog Sub Bias
VSSA	AG	vssa	Analog Ground
AINT	AI	piar50_bb	Analog Input + (Input Range : 1.0V ~ 2.0V)
AINC	AI	piar50_bb	Analog Input – (Input Range : 1.0V ~ 2.0V)
SPEEDUP	DI	picc_bb	VDD=Speed up, Normal (≤20MHz) GND=Speed down (≤15MHz)
STBY	DI	picc_bb	VDD=power saving (standby), GND=normal
CKIN	DI	picc_bb	Sampling Clock Input
D[11:0]	DO	poa_bb	Digital Output
VBBD	DG	vbba	Digital Sub Bias
VSSD	DG	vssd	Digital GND
VDDD	DP	vddd	Digital Power (3.3V)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

- AB : Analog Bidirection
- DB : Digital Bidirection



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	4.5	V
Analog Input Voltage	AINT/AINC	VSS to VDD	V
Digital Input Voltage	CKIN	VSS to VDD	V
Reference Voltage	REFTOP/REFBOT/ REFTOP1/REFBOT1	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTES

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDD VDDA VDDR	3.15	3.3	3.45	V
Reference Input Voltage	REFTOP REFBOT		2.0 1.0		V
Analog Input Voltage	AINT AINC	0.5	- 1.5	2.5	V
Operating Temperature	Toper	0	-	70	°C

NOTES

It is strongly recommended that all the supply pins (VDDA, VDDD, VDDR) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Differential Nonlinearity	DNL	-	±0.8	±1	LSB	REFTOP=2V REFBOT=1V
Integral Nonlinearity	INL	-	±1.2	±2	LSB	REFTOP=2V REFBOT=1V
Offset Voltage	OFF	-	-	30	LSB	REFTOP=2V REFBOT=1V

(Converter Specifications : VDDA=VDDD=VDDR=3.3V, VSSA=VSSD=VSSR=0V,
Toper=25 °C, REFTOP=2V, REFBOT=1V unless otherwise specified)

AC ELECTRICAL CHARACTERISTICS

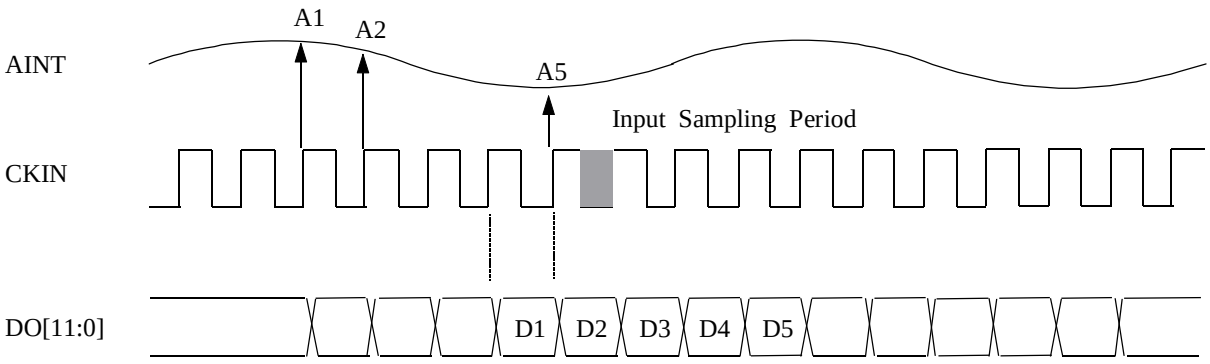
Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Maximum Conversion Rate	fc	-	-	20	MHz	AIN=AINT-AINC
Dynamic Supply Current	IVDD	-	45	55	mA	fc=20MHz (without system load)
Total Harmonic Distortion	THD	-	-68	-62	LSB	AIN=1MHz
Signal-to-Noise & Distortion Ratio	SNDR	58	62	-	dB	AIN=1MHz

(Conversion Specifications : VDDA=VDDD=VDDR=3.3V, VSSA=VSSD=VSSR=0V,
Toper=25 °C, REFTOP=2V, REFBOT=1V unless otherwise specified)

I/O CHART

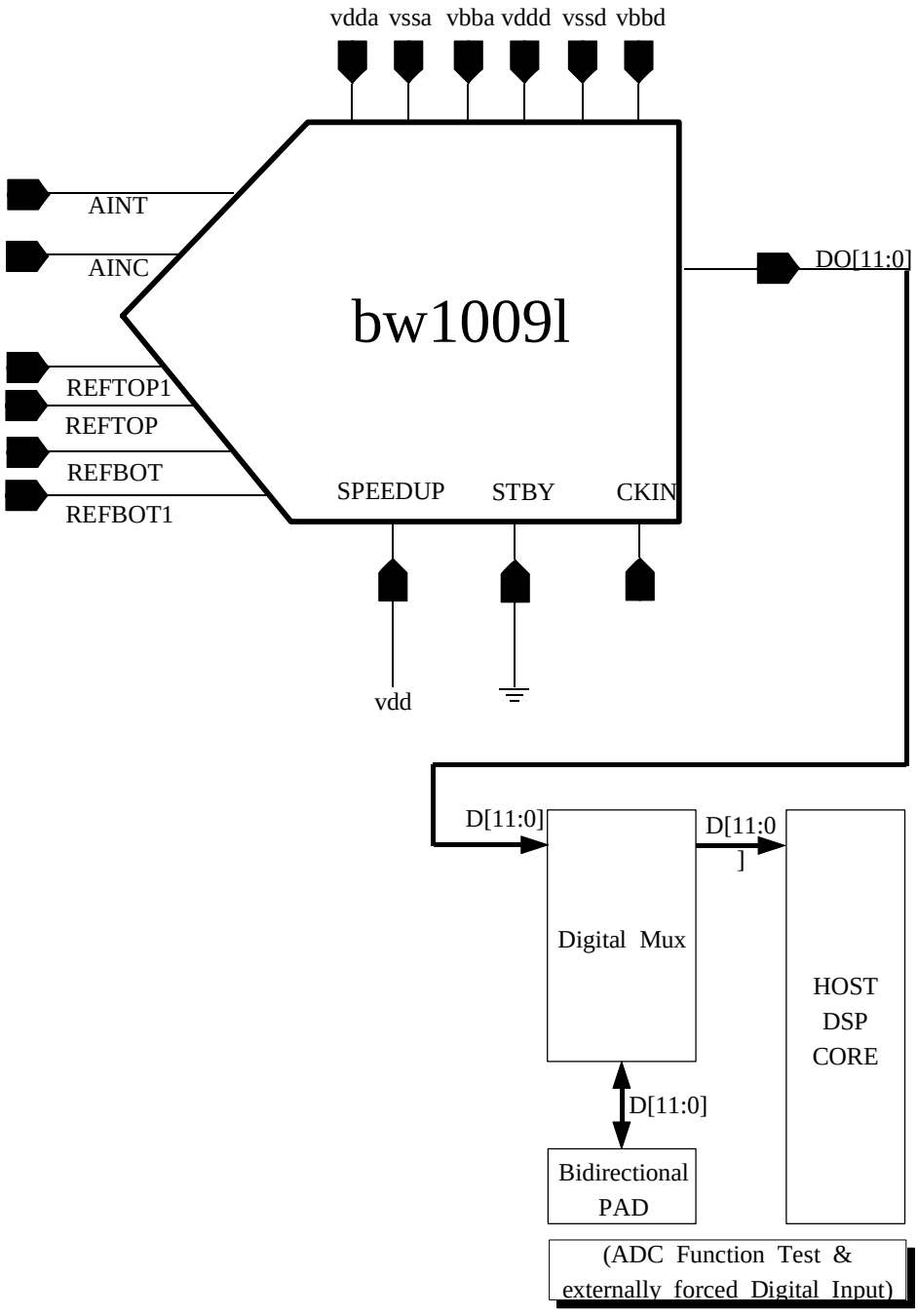
Index	AINT Input (V)	AINC Input (v)	Digital Output	
0	0.5000 ~ 0.5005	1.5	0000 0000 0000	1LSB=0.488mV REFTOP=2.0V REFBOT=1.0V
1	0.5005 ~ 0.5010	1.5	0000 0000 0001	
2	0.5010 ~ 0.5015	1.5	0000 0000 0010	
~	~		~	
2047	1.4995 ~ 1.5000	1.5	0111 1111 1111	
2048	1.5000 ~ 1.5005	1.5	1000 0000 0000	
2049	1.5005 ~ 1.5010	1.5	1000 0000 0001	
~	~		~	
4093	2.4985 ~ 2.4990	1.5	1111 1111 1101	
4094	2.4990 ~ 2.4995	1.5	1111 1111 1110	
4095	2.4995 ~ 2.5000	1.5	1111 1111 1111	

TIMING DIAGRAM



CORE EVALUATION GUIDE

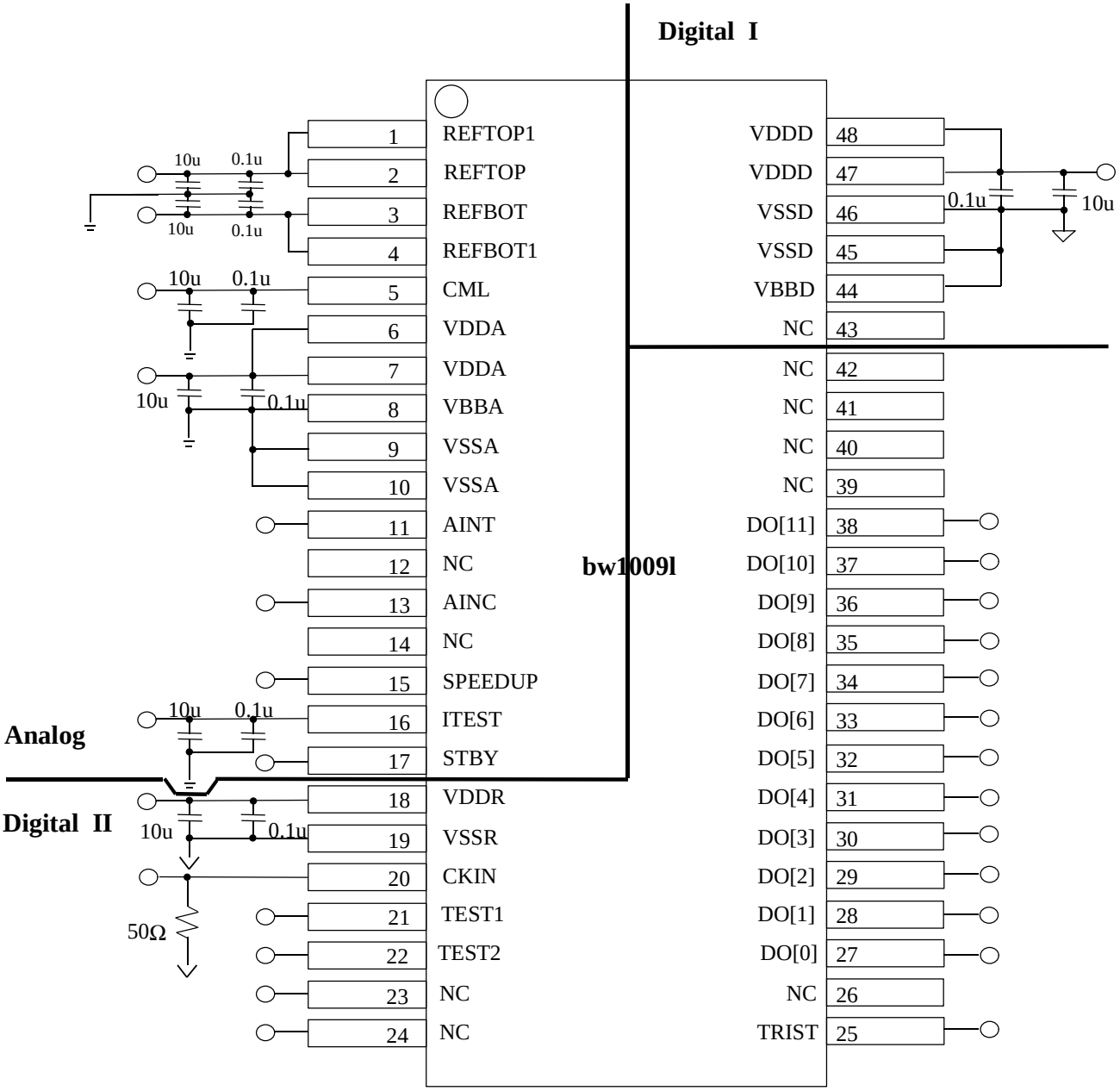
1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased internally through resistor divider.



PACKAGE CONFIGURATION

NOTES

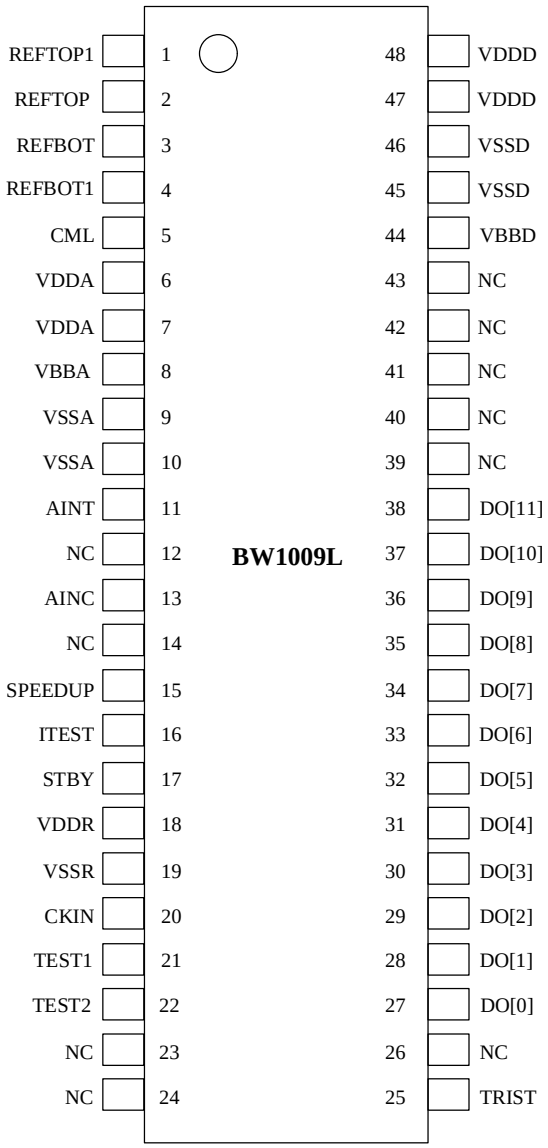
1. NC denotes "No Connection".



PACKAGE PIN DESCRIPTION

No.	NAME	I/O TYPE	PIN DESCRIPTION
1	REFTOP1	AI	Reference Top Sense (2.0V)
2	REFTOP	AI	Reference Top Force (2.0V)
3	REFBOT	AI	Reference bottom Force (1.0V)
4	REFBOT1	AI	Reference bottom Sense (1.0V)
5	CML	AB	Internal Bias Point
6, 7	VDDA	AP	Analog Power (3.3V)
8	VBBA	AG	Analog Sub Bias
9, 10	VSSA	AG	Analog Ground
11	AINT	AI	Analog Input +
13	AINC	AI	Analog Input –
15	SPEEDUP	DI	VDD=Normal (≤20MHz) GND=Speed Down (≤15MHz)
16	ITEST	AB	open=use internal bias circuit
17	STBY	DI	VDD=Power saving (Standby), GND=Normal
18	VDDR	PP	PAD Power (3.3V)
19	VSSR	PG	PAD Ground
20	CKIN	DI	Sampling Clock Input
21	TEST1	AO	Monitoring (TEST) Cell Pin1, GND=Normal
22	TEST2	AO	Monitoring (TEST) Cell Pin2, GND=Normal
25	TRIST	DI	Tristate Buffer Input VDD=High Impedance, GND=Normal
27	DO[0]	DO	Digital Output (LSB)
28~37	DO[1:10]	DO	Digital Output
38	DO[11]	DO	Digital Output (MSB)
44	VBBD	DG	Digital Sub Bias
45, 46	VSSD	DG	Digital GND
47, 48	VDDD	DP	Digital Power (3.3V)

CONFIGURATION



NOTES

1. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively

USER GUIDE

1. Input Range

   - If you want to using the single-ended input, you should use he input range as below.

     AINT : 0.5V ~ 2.5V,

     AINC : 1.5V.

   - If you want to using the differential input, you should use the input range as below.

     AINT : 1.0V ~ 2.0V,

     AINC : 1.0V ~ 2.0V.

   AIN : AINT - AINC

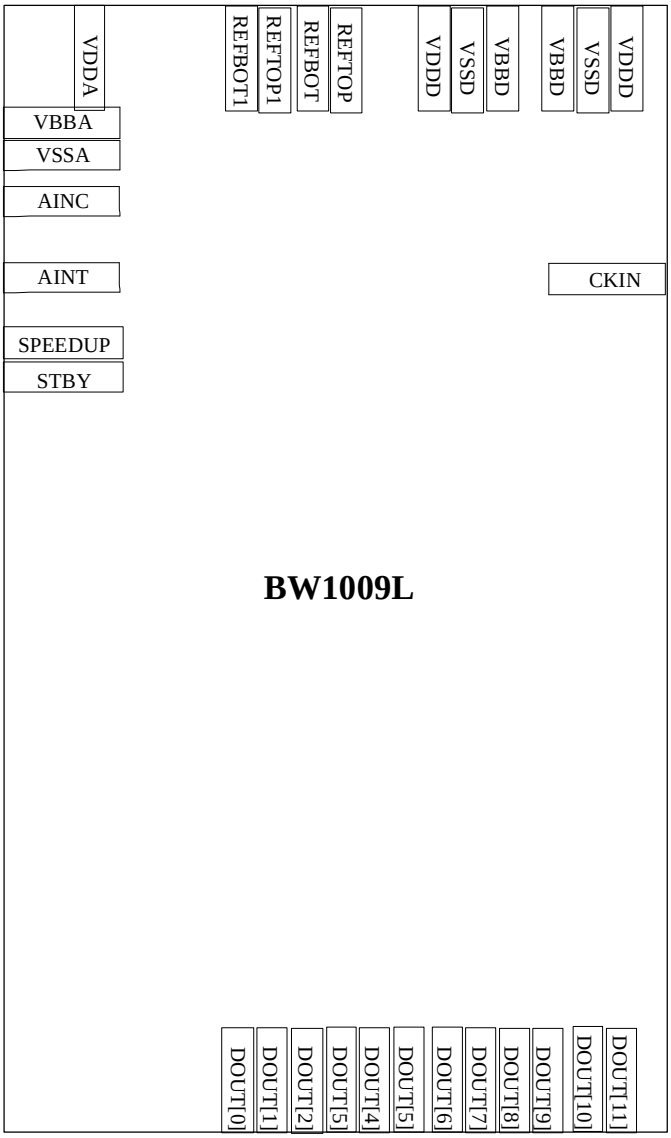
2. Speed Up

   The initial target speed of BW1009L is 20MHz.

   If you want speed down (about 15MHz), you should connect the SPEEDUP port to 'LOW'.

   And it can save the total power consumption about 10 ~ 15%.

PHANTOM CELL INFORMATION



Pin Name	Pin Usage	Pin Layout Guide
VDDA	External	- Do not merge the analog powers with another power from other blocks. - Use good power and ground source on board.
VSSA	External	
VBBA	External	
VDDD	External	
VSSD	External	
VBBD	External	
AINT, AINC	External/Internal	- Do not overlap with digital lines. - Maintain the shortest path to pads.
REFTOP, REFTOP1	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFBOT, REFBOT1	External/Internal	
SPEEDUP	External/Internal	- Separate from all other analog signals
CKIN	External/Internal	
STBY	External/Internal	
ADO[11]	External/Internal	- Separated from the analog clean signals if possible.
ADO[10]	External/Internal	
ADO[9]	External/Internal	
ADO[8]	External/Internal	
ADO[7]	External/Internal	
ADO[6]	External/Internal	
ADO[5]	External/Internal	
ADO[4]	External/Internal	
ADO[3]	External/Internal	
ADO[2]	External/Internal	
ADO[1]	External/Internal	
ADO[0]	External/Internal	

FEEDBACK REQUEST

ADC Specification

Parameter	Min	Typ	Max	Unit	Remarks
Supply voltage				V	
Reference Input voltage				V	
Analog Input voltage				Vpp	
Operating temperature				°C	
Integral non-linearity error				LSB	
Differential non-linearity error				LSB	
Offset voltage error (Bottom)				mV	
Offset voltage error (Top)				mV	
Maximum conversion rate				MSPS	
Dynamic supply current				mA	
Power dissipation				mW	
Signal-to-noise ratio				dB	
Digital output format (Provide detailed description & timing diagram)					

- What do you want to choose as power supply voltages? For example, the analog VDD needs to be 5V. the digital VDD can be 3.3V/5V.
- What resolution do you need for ADC?
- How about conversion speed (data in $\rightarrow$ data out)?
- How many cycles do exist during the latency of ADC (pipelined delay)?
- What's the input range? And then what do you need between single input and differential input?
- Can the bus interface be compatible with TTL?
- Could you explain external/internal pin configurations as required?

Specially requested function list :

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0		Original version published (preliminary)	
ver 1.1			
ver 1.2			
ver 1.3			
ver 1.4			
ver 1.5	1999.07	Release the formal datasheet	
ver 1.6	02.04.29	Add the pin information to the phantom cell information	