Am29050™

RISC Microprocessor with On-Chip Floating-Point Unit

**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- Full 32-bit, three-bus architecture
- 55 million instructions per second (MIPS) sustained at 40 MHz
- On-chip double-precision floating-point arithmetic unit
- 80-megaflop peak floating-point execution at 40 MHz
- 40-, 33-, 25-, and 20-MHz operating frequencies
- CMOS technology/TTL compatible
- 4-Gbyte virtual address space with demand paging
- Concurrent instruction and data accesses
- Burst-mode access support
- Advanced debugging support

- 64-entry Memory Management Unit (MMU) with region mapping
- 1024-byte branch target cache
- 4-entry physical address cache
- Demultiplexed and pipelined address, instruction, and data buses
- 192 general-purpose registers
- Three-address instruction architecture
- On-chip byte-alignment support allows optional byte/half-word accesses
- Pin and bus compatibility with Am29000® and Am29005™ microprocessors
- Binary compatibility with all 29K™ microprocessors and microcontrollers

SIMPLIFIED BLOCK DIAGRAM

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GENERAL DESCRIPTION

The Am29050 RISC microprocessor is a high-performance, general-purpose, 32-bit microprocessor implemented in CMOS technology. It supports a variety of applications by virtue of a flexible architecture and rapid execution of simple instructions that are common to a wide range of tasks.

The Am29050 microprocessor meets the demanding requirements of floating-point intensive embedded applications such as X terminals, signal processing, and digital communications. Because it excels at complex math operations required for fast matrix transformations, the Am29050 microprocessor provides graphics and imaging applications with fast 3D performance and gives printers the highest performance page description language (PDL) possible.

The Am29050 microprocessor instruction set has been influenced by the results of high-level language, optimizing compiler research. It is appropriate for a variety of languages because it efficiently executes operations that are common to all languages. Consequently, the Am29050 microprocessor is an ideal target for high-level languages such as C, FORTRAN, Pascal, Ada, and COBOL.

The processor is available in a 169-lead pin grid array (PGA) package. The PGA has 141 signal pins, 27 power and ground pins, and 1 alignment pin.

RELATED AMD PRODUCTS

29K Family Devices

Part No.	Description
Am29000®	32-bit RISC microprocessor
Am29005™	Low-cost 32-bit RISC microprocessor with no MMU and no branch target cache
Am29030™	32-bit RISC microprocessor with 8-Kbyte instruction cache
Am29035™	32-bit RISC microprocessor with 4-Kbyte instruction cache
Am29040™	32-bit RISC microprocessor with 8-Kbyte instruction cache and 4-Kbyte data cache
Am29200™	32-bit RISC microcontroller
Am29205™	Low-cost 32-bit RISC microcontroller with 16-bit bus interface
Am29240™	32-bit RISC microcontroller with 4-Kbyte instruction cache and 2-Kbyte data cache
Am29243™	32-bit RISC data microcontroller with instruction and data caches and DRAM parity
Am29245™	Low-cost 32-bit RISC microcontroller with 4-Kbyte instruction cache

29K FAMILY DEVELOPMENT SUPPORT PRODUCTS

Contact your local AMD representative for information on the complete set of development support tools. The following software and hardware development products are available on several hosts:

■ Optimizing compilers for common high-level languages

■ Assembler and utility packages

■ Source- and assembly-level software debuggers

■ Target-resident development monitors

■ Simulators

■ Demonstration and evaluation systems

THIRD-PARTY DEVELOPMENT SUPPORT PRODUCTS

The Fusion29K® Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD Fusion29K Partners include
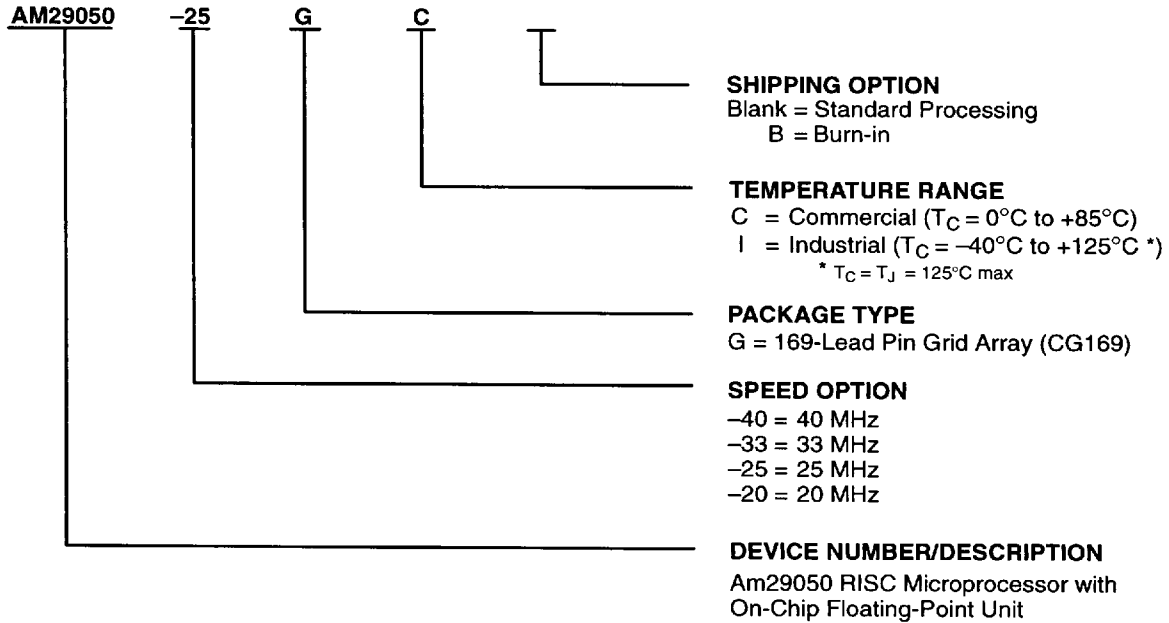
■ Silicon products

■ Emulators

■ Hardware and software debuggers

■ Modeling/simulation tools

■ Software development tools

■ Real-time operating systems (RTOS)

■ Application-specific hardware and software

■ Board-level products

■ Manufacturing and prototyping support

■ Custom support and training

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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. Valid order numbers are formed by a combination of the elements below.

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AM29050      -25      G      C
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SHIPPING OPTION
Blank = Standard Processing
B = Burn-in

TEMPERATURE RANGE
C = Commercial (T_C = 0°C to +85°C)
I = Industrial (T_C = –40°C to +125°C *)
     * $T_C = T_J$ = 125°C max

PACKAGE TYPE
G = 169-Lead Pin Grid Array (CG169)

SPEED OPTION
–40 = 40 MHz
–33 = 33 MHz
–25 = 25 MHz
–20 = 20 MHz

DEVICE NUMBER/DESCRIPTION
Am29050 RISC Microprocessor with
On-Chip Floating-Point Unit

Valid Combinations		Comments
AM29050–40 AM29050–33 AM29050–25 AM29050–20	GC	With heat sink With heat sink Without heat sink Without heat sink
AM29050–33 AM29050–25 AM29050–20	GI	With heat sink Without heat sink Without heat sink

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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LOGIC SYMBOL

Logic symbol diagram for Am29050 Microprocessor with the following inputs on the left: BREQ, PEN, IRDY, IERR, IBACK, DRDY, DERR, DBACK, CDA, WARN, INTR2–INTR0 (4), CNTL1–CNTL0 (2), RESET, TEST, INCLK, TRAP1–TRAP0 (2), I31–I0 (32), PWRCLK, SYSCLK, D31–D0; and the following outputs on the right: BGRT, BINV, R/W, SUP/US, LOCK, MPGM1–MPGM0 (2), IREQ, PDA, DBREQ, DREQT1–DREQT0 (2), MSERR, OPT2–OPT0 (3), STAT2–STAT0 (3), IREQT, PIA, IBREQ, A31–A0 (32).

KEY FEATURES AND BENEFITS

The Am29050 microprocessor extends the 29K Family of processors with a high-performance, pipelined, on-chip floating-point unit. The floating-point unit performs IEEE-compatible, single-precision and double-precision arithmetic at a peak rate of 80 million floating-point operations per second (MFLOPS) at 40 MHz. The Am29050 microprocessor also has features to improve the performance of loads and branches, allowing sustained integer performance of 55 million instructions per second (MIPS) at 40 MHz.

The Am29050 microprocessor provides a powerful upgrade to the Am29000 microprocessor. It can be used in existing Am29000 processor applications without hardware or software modifications, bringing a dramatic increase in performance to floating-point-intensive applications, particularly graphics and laser-printer applications.

Added features include a pipelined floating-point arithmetic unit, region mapping for virtual-to-physical address translation, a monitor mode for debugging supervisor code, and instruction breakpoints for enhanced debugging. Specific performance enhancements to the Am29000 microprocessor include a larger branch target cache, a physical address cache, an early address generator, and instruction forwarding logic.

On-Chip Floating-Point Arithmetic Unit

An on-chip floating-point unit performs single- and double-precision floating-point operations in accordance with the IEEE Standard for Binary Floating-Point Arithmetic (ANSI/IEEE Standard 754-1985). This unit also performs integer multiplications. An independent divide/square root unit interactively computes floating-point divisions and square roots in parallel with other operations. A 64-bit register file port is dedicated to the writing of floating-point results. These results can be written without interfering with integer operations.

Multiple concurrent operations can be supported, the principal limitation being resource contention. Most of the time, floating-point operations are performed in parallel with integer operations and other floating-point operations.

Memory Management

The Am29050 microprocessor incorporates a Memory Management Unit (MMU) that accepts a 32-bit virtual byte address and translates it to a 32-bit physical byte address in a single cycle. The MMU is not dedicated to any particular address-translation architecture. Address translation is performed either by the Translation Look-Aside Buffer (TLB) or by one of the two region mapping units.

The TLB maps virtual regions of fixed size into physical regions of the same size. The TLB is an associative table that contains the most recently used address translations for the processor. TLB entries are modified directly by processor instructions. A TLB entry consists of 64 bits and appears as two word-length TLB registers that can be inspected and modified by instructions.

In addition to page-by-page address translation, the Am29050 microprocessor supports translation for variable-sized regions. The region mapping units map virtual regions of variable size ranging from 64 Kbyte to 2 Gbyte into regions of physical memory. Each region mapping unit consists of two protected special-purpose registers. Any virtual address not mapped by the region mapping units is translated by the TLB.

Branch Target Cache

The branch target cache on the Am29050 microprocessor allows fast access to instructions fetched nonsequentially. This keeps the instruction pipeline full until the processor can establish a new instruction-prefetch stream from the external instruction memory. A branch instruction can execute in a single cycle if the branch target is in the branch target cache.

The branch target cache is a 1-Kbyte storage array that contains blocks of instructions from recently taken branches. To improve the proportion of successful searches, the branch target cache is organized as a two-way set-associative memory. The branch target cache can be configured under software control to cache either two or four instructions for each branch. Each of the two sets in the branch target cache contains 128 instructions, and the 128 instructions are further divided either into 32 blocks of four instructions each or into 64 blocks of two instructions each.

System Interface

The Am29050 microprocessor channel consists of the following 32-bit buses and related controls:

- An instruction bus that transfers instructions into the processor.
- A data bus that transfers data to and from the processor.
- An address bus that provides addresses for both instruction and data accesses. The address bus also is used to transfer data to a coprocessor.

The channel performs accesses and data transfers to all external devices and memories, including instruction and data memories, instruction caches, data caches, input/output devices, bus converters, and coprocessors.

The channel defines three different access protocols: simple, pipelined, and burst-mode. For simple accesses, the Am29050 microprocessor holds the address valid throughout the entire access. This is appropriate for high-speed devices that can complete

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an access in one cycle, and for low-cost devices that are accessed infrequently (such as read-only memories containing initialization routines). Pipelined and burst-mode accesses provide high performance with other types of devices and memories.

The Am29050 microprocessor determines whether an access is simple, pipelined, or burst-mode on a transfer-by-transfer (i.e., generally device-by-device) basis. However, an access that begins as a simple access may be converted to a pipelined or burst-mode access at any time during the transfer. This relaxes the timing constraints on the channel-protocol implementation, since addressed devices do not have to respond immediately to a pipelined or burst-mode request.

Except for the shared address bus, the channel maintains a strict division between instruction and data accesses. In the most common situation, the system supplies the processor with instructions using burst-mode accesses, with instruction addresses transmitted to the system only when a branch occurs. Data accesses can occur simultaneously without interfering with instruction transfer.

The Am29050 microprocessor contains arbitration logic to support other masters on the channel. A single external master can arbitrate directly for the channel, while multiple masters can arbitrate using a daisy chain or other method that requires no additional arbitration logic. However, to increase arbitration performance in a multiple-master configuration, an external channel arbiter should be used. This arbiter works in conjunction with the processor's arbitration logic.

Clocks

The Am29050 microprocessor generates and distributes a system clock at its operating frequency. This clock is specially designed to reduce skews between the system clock and the processor's internal clocks. The internal clock-generation circuitry requires a single-phase oscillator signal at twice the processor operating frequency.

For systems in which processor-generated clocks are not appropriate, the Am29050 microprocessor also can accept a clock from an external clock generator.

The processor decides between these two clocking arrangements based on whether the power supply to the clock-output driver is tied to +5 V or to Ground.

Master/Slave Operation

Each Am29050 microprocessor output has associated logic that compares the signal on the output with the signal that the processor is providing internally to the output driver. The processor signals situations where the output of any enabled driver does not agree with its input.

For a single processor, the output comparison detects short circuits in output signals, but does not detect open

circuits. It is possible to connect a second processor in parallel with the first, where the second processor has its outputs disabled due to the Test mode. The second processor detects open-circuit signals, as well as provides a check of the outputs of the first processor.

Debugging and Testing

The Am29050 microprocessor provides debugging and testing features for both software and hardware.

Software debugging on the Am29050 microprocessor is supported by the trace facility, hardware breakpoints, and the monitor mode.

The trace facility guarantees exactly one trap after the execution of any instruction in a program being tested. The trace trap allows a debug routine to follow the execution of instructions, and to determine the state of the processor and system at the end of each instruction.

The Am29050 microprocessor provides two hardware instruction breakpoints that can suspend execution of the current program on a specified instruction access. Suspension either forces a trace trap or forces a halt if the system is under emulator control.

Monitor mode allows debugging of operating-system routines and interrupt and trap handlers. Monitor mode can also be used by an external hardware debugger.

The Am29050 microprocessor also supports the direct attachment of a hardware-development system such as an in-circuit emulator. This attachment is made directly to the processor in the system under development, without removing the processor from the system. A test/development interface makes it possible for the hardware-development system to inspect and modify the internal state (e.g., general-purpose register contents, TLB entries, etc.) of the Am29050 microprocessor. In addition, the Am29050 microprocessor can be used to access other system devices and memories on behalf of the hardware-development system.

The test/development interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor. The Halt, Step, Reset, and Load Test Instruction modes allow the hardware-development system to control the operation of the Am29050 microprocessor. The hardware-development system can supply the processor with instructions on the instruction bus using the Load Test Instruction mode. Internal processor state can be inspected and modified via the data bus.

Coprocessor Attachment

A coprocessor for the Am29050 microprocessor attaches directly to the processor channel. However, this attachment has features that are different than those of other channel devices. The coprocessor interface on the Am29050 microprocessor supports a high operand-

transfer rate and the overlap of coprocessor operations with other processor operations, including other external accesses.

The coprocessor is assigned a special address space on the channel. This permits the transfer of operands and other information on the address bus without interfering with normal addressing functions. Since both the address bus and data bus are used for data transfer, the Am29050 microprocessor can transfer 64 bits of information to the coprocessor in one cycle.

Pin, Bus, and Binary Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. The Am29050 microprocessor provides compatibility on several levels. The processor is pin, bus, and binary compatible with the Am29000 and Am29005 processors. Pin and bus compatibility ensures a convenient upgrade path for embedded applications. In addition, the processor is binary compatible with the other members of the 29K family (the Am29030, Am29035, and Am29040 microprocessors, and the Am29200, Am29205, Am29240, Am29243, and Am29245 microcontrollers).

Complete Development and Support Environment

A complete development and support environment is vital for reducing a product's time-to-market. Advanced Micro Devices has created a standard development environment for the 29K Family of processors. In addition, the Fusion29K program's third-party support organization provides the most comprehensive customer/partner program in the embedded processor market.

Advanced Micro Devices offers a complete set of hardware and software tools for design, integration, debugging, and benchmarking. These tools, which are available now for the 29K Family, include the following:

- High C® 29K optimizing C compiler with assembler, linker, ANSI library functions, and 29K Family architectural simulator
- XRAY29K™ source-level debugger
- MiniMON29K™ debug monitor
- A complete family of demonstration and development systems

In addition, Advanced Micro Devices has developed a standard host interface (HIF) specification for operating system services, the Universal Debug Interface (UDI) for seamless connection of debuggers to ICEs and target hardware, and extensions for the UNIX common object file format (COFF).

This support is augmented by a staff of factory support and field application engineers, an engineering hotline, and an on-line technical bulletin board.

PERFORMANCE OVERVIEW

The Am29050 microprocessor provides a significant margin of performance over other processors in its class, since the majority of processor features were defined with the maximum achievable performance in mind. This section describes the features of the Am29050 microprocessor from the point of view of system performance.

Instruction Set Overview

All 29K Family members employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands can be contained in any of the general-purpose registers, and the results can be stored into any of the general-purpose registers.

The Am29050 microprocessor also provides four double-precision floating-point accumulator registers for use with the floating-point multiply-accumulate and multiply-sum operations. Instructions are provided for writing and reading the accumulator registers directly.

The Am29050 microprocessor instruction set contains 125 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous.

All instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, stores, and certain floating-point instructions.

Instruction Execution

The Am29050 microprocessor uses an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands, and provide a 32-bit result.

Floating-point operations are performed in an on-chip floating-point unit. The floating-point unit performs 32-bit, single-precision and 64-bit, double-precision computations.

The performance degradation of load and store operations is minimized in the Am29050 microprocessor by overlapping them with instruction execution, by taking advantage of pipelining, and by organizing the flow of external data onto the processor so that the impact of external accesses is minimized.

Early Loads

The early load feature of the Am29050 microprocessor speeds up the execution of load operations by making the physical address of the load instruction available at the end of the decode cycle of the load instruction. At the

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beginning of the next cycle, when the load enters the execute stage, the physical address appears on the channel. In effect, early loads reduce the memory access time by one cycle.

Early loads can occur in two different ways. Either the physical address of the load is available in the four-entry physical address cache, or, when an address computation immediately precedes the load instruction, the computed physical address can be forwarded directly to the channel.

Pipelining

The Am29050 microprocessor utilizes a four-stage pipeline for integer operations, allowing it to execute one integer instruction every clock cycle. The processor can complete an instruction on every cycle, even though four cycles are required from the beginning of an instruction to its completion.

Floating-point operations are pipelined to a depth determined by the operation latency and are overlapped with integer operations. A floating-point operation and an integer operation can complete at the same time without stalling the pipeline.

Instruction operations are overlapped with operand fetch and result write-back to the register file. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays which might arise from these dependencies.

Pipeline interlocks are implemented by processor hardware, including those required for floating-point operations. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

Register File

The on-chip register file containing 192 general-purpose registers allows most instruction operands to be fetched without the delay of an external access. The register file incorporates several features that aid the retention of data required by an executing program. Because of the number of general-purpose registers, the frequency of external references for the Am29050 microprocessor is significantly lower than the frequency of references in processors having only 16 or 32 registers.

Four-port access to the register file allows two 64-bit source-operands to be fetched in one cycle while two previously computed results are written; one write port is for integer operations, and the other port is for floating-point operations. Four 64-bit internal buses prevent contention in the routing of operands. All operand fetches and result write-backs for instruction execution can be performed in a single cycle.

The registers allow efficient procedure linkage by caching a portion of a compiler's run-time stack. On the average,

procedure calls and returns can be executed 5 to 10 times faster (on a cycle-by-cycle basis) than in processors that require the implementation of a run-time stack in external memory (with the attendant loading and storing of registers on procedure call and return).

Protection

The Am29050 microprocessor offers three mutually exclusive modes of execution that restrict or permit accesses to certain processor registers and external storage locations. Supervisor and user modes are for normal program execution, and monitor mode is used for debugging. All system-protection features of the Am29050 microprocessor are based on the difference between these modes.

Memory access protection is provided by the MMU. Six protection bits determine whether or not an access is permitted to the page associated with the entry. For the same virtual page, the access authority of programs executing in supervisor mode can be different from the authority of programs executing in user mode.

The register file can be configured to restrict accesses to supervisor-mode programs on a bank-by-bank basis using a register bank protect register.

Data Formats

The Am29050 microprocessor defines a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for single- and double-precision floating-point, word-integer (signed and unsigned), word-logical, word-boolean, half-word integer (signed and unsigned), and byte data (signed and unsigned).

Word-boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the most significant bit values 1 and 0, respectively. Other data formats, such as character strings, are supported by instruction sequences.

Separate Address, Instruction, and Data Buses

The Am29050 microprocessor incorporates two 32-bit buses for instruction and data transfers, and a third address bus that is shared between instruction and data accesses. This bus structure allows simultaneous instruction and data transfers, even though the address bus is shared. The channel achieves the performance of four separate 32-bit buses at a much reduced pin count.

The address bus is pipelined, so that it can be released before an instruction or data transfer is completed. This allows a subsequent access to begin before the first has completed and allows the processor to have two accesses in progress simultaneously.

Support of Burst Devices and Memories

Burst-mode accesses provide high transfer rates for instructions and data at sequential addresses. For such accesses, the address of the first instruction or datum is sent, and subsequent requests for instructions or data at sequential addresses do not require additional address transfers. These instructions or data are transferred until either party involved in the transfer terminates the access.

Burst-mode accesses can occur at the rate of one access per cycle after the first address has been processed. At 40 MHz, the maximum achievable transfer bandwidth for either instructions or data is 160 Mbyte/s.

Burst-mode accesses may occur to input/output devices, if the system design permits.

Interface to Fast Devices and Memories

The processor can be interfaced to devices and memories that complete accesses within one cycle. The channel protocol takes maximum advantage of such devices and memories by allowing data to be returned to the processor during the cycle in which the address is transmitted. This allows a full range of memory-speed trade-offs to be made within a particular system.

Branch Target Cache Memory

In general, the Am29050 microprocessor meets its instruction bandwidth requirements via instruction prefetching. However, instruction prefetching is ineffective when a branch occurs. The Am29050 microprocessor therefore incorporates a 64- or 128-entry (configurable at run time) branch target cache array to supply instructions for a branch—if this branch has been taken previously—while a new prefetch stream is established.

If branch-target instructions are in the branch target cache, branches execute in a single cycle. This has a very positive effect on processor performance, due to the amount of time the processor could otherwise be idle waiting for the new instruction stream.

The branch target cache in the Am29050 microprocessor eliminates the branch latency for 80% of all successful branches on the average.

Branching

Branch conditions in the Am29050 microprocessor can be based on Boolean data contained in general-purpose registers, as well as on arithmetic condition codes.

The Am29050 microprocessor executes branches in a single cycle, for those cases where the target of the branch is in the branch target cache. The single-cycle branch is unusual for a pipelined processor, and is due to processor hardware which allows much of the branch instruction operation to be performed early in the execution of the branch. Single-cycle branching

has a dramatic effect on performance, since successful branches typically represent 15% to 25% of a processor's instruction mix.

The techniques used to achieve single-cycle branching also minimize the execution time of branches in those cases where the target is not in the branch target cache. To keep the pipeline operating at the maximum rate, the instruction following the branch, referred to as the delay instruction, is executed regardless of the outcome of the branch. An optimizing compiler can define a useful instruction for the delay instruction in approximately 90% of branch instructions, thereby increasing the performance of branches.

Memory Management

A 64-entry Translation Look-Aside Buffer (TLB) and two Region Mapping registers on the Am29050 microprocessor perform virtual-to-physical address translation, avoiding the cycle that would be required to transfer the virtual address to an external TLB. A number of enhancements improve the performance of address translation:

■ Pipelining—The operation of the TLB is pipelined with other processor operations.

■ Early Address Translation—Address translations for load, store, and branch instructions occur during the cycle in which these instructions are executed. This allows the physical address to be transferred externally in the next cycle.

■ Region Mapping—The region mapping registers permit efficient mapping of large, contiguous regions of memory. This is useful for code libraries and large data structures; these can appear in a virtual address space without paging overhead.

■ Task Identifiers—Task identifiers allow TLB entries to be matched to different processes, so that TLB invalidation is not required during task switches.

■ Least-Recently Used Hardware—This hardware allows immediate selection of a TLB set to be replaced.

■ Software Reload—Software reload allows the operating system to use a page-mapping scheme that is best matched to its environment. Paged-segmented, one-level-page mapping, two-level-page mapping, or any other user-defined page-mapping scheme can be supported. Because Am29050 microprocessor instructions execute at an average rate of nearly one instruction per cycle, software reload has a performance approaching that of hardware TLB reload.

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Interrupts and Traps

When the Am29050 microprocessor takes an interrupt or trap, it does not automatically save its current state information in memory. This feature greatly improves the performance of temporary interruptions such as TLB reload or other simple operating-system calls or interrupts that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state saved—can be tailored to the needs of a particular system.

Interrupts and traps are dispatched through a 256-entry vector area that directs the processor to a routine to handle a given interrupt or trap. The vector area can be relocated in memory by the modification of a processor register. There can be multiple vector areas in the system, though only one is active at any given time.

The vector area is either a table of pointers to the interrupt and trap handlers, or a segment of instruction memory (possibly read-only memory) containing the handlers themselves. The choice between the two possible vector area definitions is determined by the cost/performance trade-offs made for a particular system.

CONNECTION DIAGRAM

169-Lead PGA
Bottom View
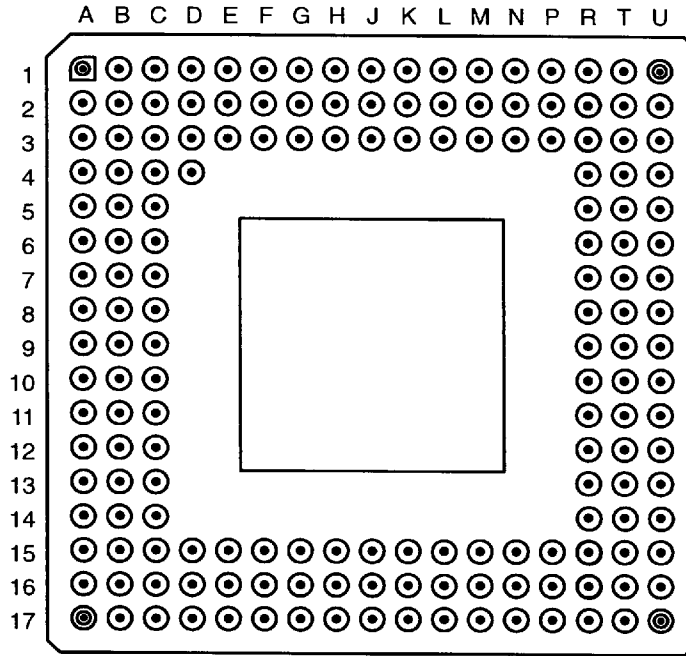
Note: Pinout observed from pin side of package.

Am29050 Microprocessor

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PGA PIN DESIGNATIONS
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	GND	C10	GND	J16	A16	R12	STAT2
A2	I1	C11	GND	J17	A14	R13	GND
A3	I0	C12	D22	K1	I26	R14	OPT0
A4	D2	C13	D26	K2	I25	R15	A2
A5	D4	C14	V_{CC}	K3	GND	R16	A6
A6	D6	C15	D30	K15	V_{CC}	R17	A7
A7	D9	C16	D31	K16	A12	T1	INCLK
A8	D11	C17	A29	K17	A13	T2	$\overline{BREQ}$
A9	D12	D1	I11	L1	I27	T3	$\overline{DERR}$
A10	D14	D2	I10	L2	I28	T4	$\overline{IRDY}$
A11	D16	D3	I7	L3	V_{CC}	T5	$\overline{WARN}$
A12	D18	D4♦	PIN169	L15	V_{CC}	T6	$\overline{INTR2}$
A13	D20	D15	A31	L16	A10	T7	$\overline{INTR0}$
A14	D21	D16	A28	L17	A11	T8	$\overline{BINV}$
A15	D25	D17	A26	M1	I29	T9	$\overline{BGRT}$
A16	D27	E1	I13	M2	I30	T10	$\overline{DREQ}$
A17	GND	E2	I12	M3	GND	T11	$\overline{LOCK}$
B1	I6	E3	V_{CC}	M15	GND	T12	MSERR
B2	I5	E15	GND	M16	A0	T13	STAT0
B3	I3	E16	A27	M17	A1	T14	SUP/$\overline{US}$
B4	D0	E17	A23	N1	I31	T15	OPT1
B5	D1	F1	I16	N2	$\overline{TEST}$	T16	A3
B6	D5	F2	I15	N3	SYSCLK	T17	A4
B7	D8	F3	I14	N15	GND	U1	GND
B8	D10	F15	A25	N16	MPGM1	U2	$\overline{PEN}$
B9	D13	F16	A24	N17	MPGM0	U3	$\overline{IERR}$
B10	D15	F17	A21	P1	CNTL1	U4	$\overline{IBACK}$
B11	D17	G1	I19	P2	CNTL0	U5	$\overline{INTR3}$
B12	D19	G2	I18	P3	PWRCLK	U6	$\overline{INTR1}$
B13	D23	G3	I17	P15	A5	U7	$\overline{TRAP0}$
B14	D24	G15	A22	P16	A8	U8	$\overline{IBREQ}$
B15	D28	G16	A20	P17	A9	U9	$\overline{IREQ}$
B16	D29	G17	A19	R1	$\overline{RESET}$	U10	$\overline{PIA}$
B17	A30	H1	I20	R2	$\overline{CDA}$	U11	R/$\overline{W}$
C1	I9	H2	I22	R3	$\overline{DRDY}$	U12	DREQT1
C2	I8	H3	I21	R4	$\overline{DBACK}$	U13	DREQT0
C3	I4	H15	GND	R5	GND	U14	STAT1
C4	I2	H16	A18	R6	V_{CC}	U15	IREQT
C5	GND	H17	A17	R7	$\overline{TRAP1}$	U16	OPT2
C6	D3	J1	I23	R8	GND	U17	GND
C7	D7	J2	I24	R9	$\overline{DBREQ}$		
C8	V_{CC}	J3	GND	R10	$\overline{PDA}$		
C9	V_{CC}	J15	A15	R11	V_{CC}		

♦**Note:** *Pin Number D4 is the alignment pin and is electrically connected to the package lid.*

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PGA PIN DESIGNATIONS
(Sorted by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	M16	D5	B6	GND	K3	INCLK	T1
A1	M17	D6	A6	GND	N15	$\overline{INTR0}$	T7
A2	R15	D7	C7	GND	R5	$\overline{INTR1}$	U6
A3	T16	D8	B7	GND	U1	$\overline{INTR2}$	T6
A4	T17	D9	A7	GND	R13	$\overline{INTR3}$	U5
A5	P15	D10	B8	GND	R8	$\overline{IRDY}$	T4
A6	R16	D11	A8	GND	M3	$\overline{IREQ}$	U9
A7	R17	D12	A9	GND	U17	IREQT	U15
A8	P16	D13	B9	I0	A3	$\overline{LOCK}$	T11
A9	P17	D14	A10	I1	A2	MPGM0	N17
A10	L16	D15	B10	I2	C4	MPGM1	N16
A11	L17	D16	A11	I3	B3	MSERR	T12
A12	K16	D17	B11	I4	C3	OPT0	R14
A13	K17	D18	A12	I5	B2	OPT1	T15
A14	J17	D19	B12	I6	B1	OPT2	U16
A15	J15	D20	A13	I7	D3	$\overline{PDA}$	R10
A16	J16	D21	A14	I8	C2	$\overline{PEN}$	U2
A17	H17	D22	C12	I9	C1	$\overline{PIA}$	U10
A18	H16	D23	B13	I10	D2	PIN169	D4♦
A19	G17	D24	B14	I11	D1	PWRCLK	P3
A20	G16	D25	A15	I12	E2	R/$\overline{W}$	U11
A21	F17	D26	C13	I13	E1	$\overline{RESET}$	R1
A22	G15	D27	A16	I14	F3	STAT0	T13
A23	E17	D28	B15	I15	F2	STAT1	U14
A24	F16	D29	B16	I16	F1	STAT2	R12
A25	F15	D30	C15	I17	G3	SUP/$\overline{US}$	T14
A26	D17	D31	C16	I18	G2	SYSCLK	N3
A27	E16	$\overline{DBACK}$	R4	I19	G1	$\overline{TEST}$	N2
A28	D16	$\overline{DBREQ}$	R9	I20	H1	$\overline{TRAP0}$	U7
A29	C17	$\overline{DERR}$	T3	I21	H3	$\overline{TRAP1}$	R7
A30	B17	$\overline{DRDY}$	R3	I22	H2	V_{CC}	C14
A31	D15	$\overline{DREQ}$	T10	I23	J1	V_{CC}	L15
$\overline{BGRT}$	T9	DREQT0	U13	I24	J2	V_{CC}	C8
$\overline{BINV}$	T8	DREQT1	U12	I25	K2	V_{CC}	C9
$\overline{BREQ}$	T2	GND	E15	I26	K1	V_{CC}	E3
$\overline{CDA}$	R2	GND	H15	I27	L1	V_{CC}	K15
CNTL0	P2	GND	M15	I28	L2	V_{CC}	L3
CNTL1	P1	GND	C10	I29	M1	V_{CC}	R6
D0	B4	GND	A1	I30	M2	V_{CC}	R11
D1	B5	GND	A17	I31	N1	$\overline{WARN}$	T5
D2	A4	GND	C5	$\overline{IBACK}$	U4		
D3	C6	GND	C11	$\overline{IBREQ}$	U8		
D4	A5	GND	J3	$\overline{IERR}$	U3		

♦**Note:** Pin Number D4 is the alignment pin and is electrically connected to the package lid.

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PIN DESCRIPTIONS

Although certain outputs are described as being three-state or bidirectional outputs, all outputs (except MSERR) may be placed in a high-impedance state by the Test mode. The three-state and bidirectional terminology in this section is for those outputs (except SYSCLK) that are disabled when the processor grants the channel to another master.

A31–A0
Address Bus (three-state outputs, synchronous)

The address bus transfers the byte address for all accesses except burst-mode accesses. For burst-mode accesses, it transfers the address for the first access in the sequence.

BGRT
Bus Grant (output, synchronous)

This output signals to an external master that the processor is relinquishing control of the channel in response to BREQ.

BINV
Bus Invalid (output, synchronous)

This output indicates that the address bus and related controls are invalid. It defines an idle cycle for the channel.

BREQ
Bus Request (input, synchronous)

This input allows other masters to arbitrate for control of the processor channel.

CDA
Coprocessor Data Accept (input, synchronous)

This signal allows the coprocessor to indicate the acceptance of operands or operation codes. For transfers to the coprocessor, the processor does not expect a DRDY response; an active level on CDA performs the function normally performed by DRDY. CDA may be active whenever the coprocessor is able to accept transfers.

CNTL1–CNTL0
CPU Control (inputs, asynchronous)

These inputs control the processor mode:

CNTL1	CNTL0	Mode
0	0	Load Test Instruction
0	1	Step
1	0	Halt
1	1	Normal

D31–D0
Data Bus (bidirectional, synchronous)

The data bus transfers data to and from the processor for load and store operations.

DBACK
Data Burst Acknowledge (input, synchronous)

This input is active whenever a burst-mode data access has been established. It may be active even though no data are currently being accessed.

DBREQ
Data Burst Request (three-state output, synchronous)

This signal is used to establish a burst-mode data access and to request data transfers during a burst-mode data access. DBREQ may be active even though the address bus is being used for an instruction access. This signal becomes valid late in the cycle, with respect to DREQ.

DERR
Data Error (input, synchronous)

This input indicates that an error occurred during the current data access. For a load, the processor ignores the content of the data bus. For a store, the access is terminated. In either case, a Data Access Exception trap occurs. The processor ignores this signal if there is no pending data access.

DRDY
Data Ready (input, synchronous)

For loads, this input indicates that valid data is on the data bus. For stores, it indicates that the access is complete, and that data need no longer be driven on the data bus. The processor ignores this signal if there is no pending data access.

DREQ
Data Request (three-state output, synchronous)

This signal requests a data access. When it is active, the address for the access appears on the address bus.

DREQT1–DREQT0
Data Request Type (three-state outputs, synchronous)

These signals specify the address space of a data access, as follows (the value "x" is a "don't care"):

DREQT1	DREQT0	Mode
0	0	Instruction/data memory access
0	1	Input/output access
1	x	Coprocessor transfer

An interrupt/trap vector request is indicated as a data memory read. If required, the system can identify the vector fetch by the STAT2–STAT0 outputs. DREQT1–DREQT0 are valid only when $\overline{\text{DREQ}}$ is active.

I31–I0
Instruction Bus (inputs, synchronous)

The instruction bus transfers instructions to the processor.

$\overline{\text{IBACK}}$
Instruction Burst Acknowledge (input, synchronous)

This input is active whenever a burst-mode instruction access has been established. It may be active even though no instructions are currently being accessed.

$\overline{\text{IBREQ}}$
Instruction Burst Request (three-state output, synchronous)

This signal is used to establish a burst-mode instruction access and to request instruction transfers during a burst-mode instruction access. $\overline{\text{IBREQ}}$ may be active even though the address bus is being used for a data access. This signal becomes valid late in the cycle with respect to $\overline{\text{IREQ}}$.

$\overline{\text{IERR}}$
Instruction Error (input, synchronous)

This input indicates that an error occurred during the current instruction access. The processor ignores the content of the instruction bus, and an Instruction Access Exception trap occurs if the processor attempts to execute the invalid instruction. The processor ignores this signal if there is no pending instruction access.

INCLK
Input Clock (input)

When the processor generates the clock for the system, this is an oscillator input to the processor at twice the processor's operating frequency. In systems where the clock is not generated by the processor, this signal must be tied High or Low, except in certain master/slave configurations.

$\overline{\text{INTR3}}$–$\overline{\text{INTR0}}$
Interrupt Request (inputs, asynchronous)

These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{\text{INTR0}}$ has the highest priority, and the interrupt caused by $\overline{\text{INTR3}}$ has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register. $\overline{\text{INTR0}}$ cannot be masked with the Interrupt Mask field.

$\overline{\text{IRDY}}$
Instruction Ready (input, synchronous)

This input indicates that a valid instruction is on the instruction bus. The processor ignores this signal if there is no pending instruction access.

$\overline{\text{IREQ}}$
Instruction Request (three-state output, synchronous)

This signal requests an instruction access. When it is active, the address for the access appears on the address bus.

IREQT
Instruction Request Type (three-state output, synchronous)

This signal specifies the address space of an instruction request when $\overline{\text{IREQ}}$ is active:

IREQT	Mode
0	Instruction/data memory access
1	Instruction read-only memory access

$\overline{\text{LOCK}}$
Lock (three-state output, synchronous)

This output allows the implementation of various channel and device interlocks. It may be active only for the duration of an access, or active for an extended period of time under control of the Lock bit in the Current Processor Status.

The processor does not relinquish the channel (in response to $\overline{\text{BREQ}}$) when $\overline{\text{LOCK}}$ is active.

MPGM1–MPGM0
MMU Programmable (three-state outputs, synchronous)

These outputs reflect the value of two PGM bits in the Translation Look-Aside Buffer or Region Mapping Unit entry associated with the access. If no address translation is performed, these signals are both Low.

MSERR
Master/Slave Error (output, synchronous)

This output shows the result of the comparison of processor outputs with the signals provided internally to the off-chip drivers. If there is a difference for any enabled driver, this line is asserted.

OPT2–OPT0
Option Control (three-state outputs, synchronous)

These outputs reflect the value of bits 18–16 of the load or store instruction that begins an access. Bit 18 of the

instruction is reflected on OPT2, bit 17 on OPT1, and bit 16 on OPT0.

The standard definitions of these signals (based on DREQT) are as follows (the value "x" is a "don't care"):

DREQT1	DREQT0	OPT2	OPT1	OPT0	Meaning
0	x	0	0	0	Word-length access
0	x	0	0	1	Byte access
0	x	0	1	0	Half-word access
0	0	1	0	0	Instruction ROM access (as data)
0	0	1	1	0	In-circuit emulator access
—All Others—					Reserved

During an interrupt/trap vector fetch, the OPT2–OPT0 signals indicate a word-length access (000). Also, the system should return an entire aligned word for a read, regardless of the indicated data length.

The Am29050 microprocessor does not explicitly prevent a store to the instruction ROM. OPT3–OPT0 are valid only when $\overline{\text{DREQ}}$ is active.

$\overline{\text{PDA}}$
Pipelined Data Access
(three-state output, synchronous)

If $\overline{\text{DREQ}}$ is not active, this output indicates that a data access is pipelined with another in-progress data access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of $\overline{\text{DREQ}}$.

$\overline{\text{PEN}}$
Pipeline Enable (input, synchronous)

This signal allows devices that can support pipelined accesses (i.e., that have input latches for the address and required controls) to signal that a second access may begin while the first is being completed.

$\overline{\text{PIA}}$
Pipelined Instruction Access
(three-state output, synchronous)

If $\overline{\text{IREQ}}$ is not active, this output indicates that an instruction access is pipelined with another in-progress instruction access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of $\overline{\text{IREQ}}$.

$\text{R}/\overline{\text{W}}$
Read/Write (three-state output, synchronous)

This signal indicates whether data is being transferred from the processor to the system, or from the system to the processor. $\text{R}/\overline{\text{W}}$ is valid only when the address bus is valid. $\text{R}/\overline{\text{W}}$ will be High when $\overline{\text{IREQ}}$ is active.

$\overline{\text{RESET}}$
Reset (input, asynchronous)

This input places the processor in the Reset mode.

STAT2–STAT0
CPU Status (outputs, synchronous)

These outputs indicate the state of the processor's execution stage on the previous cycle. They are encoded as follows:

STAT2	STAT1	STAT0	Condition
0	0	0	Halt or Step Modes
0	0	1	Pipeline Hold Mode
0	1	0	Load Test Instruction Mode, Halt/Freeze
0	1	1	Wait Mode
1	0	0	Interrupt Return
1	0	1	Taking Interrupt or Trap
1	1	0	Non-sequential Instruction Fetch
1	1	1	Executing Mode

$\text{SUP}/\overline{\text{US}}$
Supervisor/User Mode
(three-state output, synchronous)

This output indicates the program mode for an access.

SYSCLK
System Clock (bidirectional)

This is either a clock output with a frequency that is half that of INCLK, or an input from an external clock generator at the processor's operating frequency.

$\overline{\text{TEST}}$
Test Mode (input, asynchronous)

When this input is active, the processor is in Test mode. All outputs and bidirectional lines, except MSERR, are forced to the high impedance state.

$\overline{\text{TRAP1}}$–$\overline{\text{TRAP0}}$
Trap Request (inputs, asynchronous)

These inputs generate prioritized trap requests. The trap caused by $\overline{\text{TRAP0}}$ has the highest priority. These trap requests are disabled by the DA bit of the Current Processor Status Register.

$\overline{\text{WARN}}$
Warn (input, asynchronous, edge-sensitive)

A high-to-low transition on this input causes a non-maskable $\overline{\text{WARN}}$ trap to occur. This trap bypasses the normal trap vector fetch sequence and is useful in situations where the vector fetch may not work (e.g., when data memory is faulty).

SPECIAL PINS

The following pins are not signal pins, but are named in Am29050 microprocessor documentation because of their special role in the processor and system.

PWRCLK
Power Supply for SYSCLK Driver

This pin is a power supply for the SYSCLK output driver. It isolates the SYSCLK driver and is used to determine whether or not the Am29050 microprocessor generates the clock for the system. If power (+5 V) is applied to this pin, the Am29050 microprocessor generates a clock on the SYSCLK output. If this pin is grounded, the Am29050 microprocessor accepts a clock generated by the system on the SYSCLK input.

PIN169
Alignment pin

In the PGA package, this pin is used to indicate proper pin-alignment of the Am29050 microprocessor and is used by an in-circuit emulator to communicate its presence to the system.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Voltage on any Pin
    with Respect to GND ...... −0.5 V to V_{CC} +0.5 V
Maximum V_{CC} .... 6.0 V DC

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) and Industrial (I) Devices

Case Temperature (T_C) .... 0°C to +85°C **(C)**
Case Temperature (T_C) * .... −40°C to +125°C **(I)**
Supply Voltage (V_{CC}) .... +4.75 V to +5.25 V
* measured "instant on" ($T_C=T_J$)

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL Operating Ranges

Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage		−0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILSYSCLK}$	SYSCLK Input Low Voltage		−0.5	0.8	V
$V_{IHSYSCLK}$	SYSCLK Input High Voltage		V_{CC}−0.8	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except SYSCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for All Outputs except SYSCLK	I_{OH} = −400 μA	2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} −0.45 V		±10	μA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} −0.45 V		±10	μA
I_{CCOP}	Operating Power Supply Current	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{RESET}$ active with externally supplied SYSCLK		38	mA/MHz
V_{OLC}	SYSCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	SYSCLK Output High Voltage	I_{OHC} = −20 mA	V_{CC} −0.6		V

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance			15	pF
C_{INCLK}	INCLK Input Capacitance			20	pF
C_{SYSCLK}	SYSCLK Capacitance	fC = 1 MHz (see Note)		90	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note: *Not 100% tested.*

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SWITCHING CHARACTERISTICS over COMMERCIAL Operating Range

No.	Parameter Description	Test Conditions[1]	40 MHz		33 MHz		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK) Period (T)	Note 2	25	100	30	100	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 14	0.5T–1	0.5T+1	0.5T–1	0.5T+1	ns
2	SYSCLK High Time when used as input	Notes 14, 17			15		ns
3	SYSCLK Low Time when used as input	Notes 14, 17			14		ns
4	SYSCLK Rise Time	Note 3		3		4	ns
5	SYSCLK Fall Time	Note 3		3		4	ns
6	Synchronous SYSCLK Output Valid Delay	Notes 4, 13	2	12	2	13	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	Notes 13, 19	2	13	2	14	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 5, 15, 16	1	20	1	20	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 6, 13	0	8	2	10	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 6, 15, 16	1	20	1	20	ns
9	Synchronous Input Setup Time	Note 8	8		10		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		3.5		4		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		8		11		ns
10	Synchronous Input Hold Time	Note 7	2.5		3.0		ns
11	Asynchronous Input Minimum Pulse Width	Note 9	T+10		T+10		ns
12	INCLK Period		12.5	50	15	50	ns
12A	INCLK to SYSCLK Delay		1.5	7	2	8	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		1.5	7	2	8	ns
13	INCLK Low Time	Note 18	3		4.25		ns
14	INCLK High Time	Note 18	3		4.25		ns
15	INCLK Rise Time	Note 18		3.25		3.25	ns
16	INCLK Fall Time	Note 18		3.25		3.25	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 10	0	4	1	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 11	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 13	0	6.0	0	6	ns
20	Three-State Synchronous SYSCLK Output Invalid Delay for D31–D0	Notes 12, 15, 16	3	20	3	20	ns

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SWITCHING CHARACTERISTICS over COMMERCIAL Operating Range

No.	Parameter Description	Test Conditions[1]	25 MHz		20 MHz		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK) Period (T)	Note 2	40	100	50	100	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 14	0.5T−1	0.5T+1	0.5T−1	0.5T+1	ns
2	SYSCLK High Time when used as input	Note 14	19		22		ns
3	SYSCLK Low Time when used as input	Note 14	17		19		ns
4	SYSCLK Rise Time	Note 3		5		5	ns
5	SYSCLK Fall Time	Note 3		5		5	ns
6	Synchronous SYSCLK Output Valid Delay	Notes 4, 13	2	14	2	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	Notes 13, 19	2	18	2	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 5, 15, 16	3	30	3	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 6, 13	2	14	2	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 6, 15, 16	3	30	3	30	ns
9	Synchronous Input Setup Time	Note 8	12		15		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		6		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		13		16		ns
10	Synchronous Input Hold Time	Note 7	3.5		4		ns
11	Asynchronous Input Minimum Pulse Width	Note 9	T+10		T+10		ns
12	INCLK Period		20	50	25	50	ns
12A	INCLK to SYSCLK Delay		2	10	2	12	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	10	2	12	ns
13	INCLK Low Time		6.75		9.25		ns
14	INCLK High Time		6.75		9.25		ns
15	INCLK Rise Time			3.25		3.25	ns
16	INCLK Fall Time			3.25		3.25	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 10	1	7	1	8	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 11	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 13	0	7	0	9	ns
20	Three-State Synchronous SYSCLK Output Invalid Delay for D31–D0	Notes 12, 15, 16	3	20	3	25	ns

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SWITCHING CHARACTERISTICS over INDUSTRIAL Operating Range

| No.	Parameter Description	Test Conditions[1]	33 MHz		Unit
			Min	Max	
1	System Clock (SYSCLK) Period (T)	Note 2	30	100	ns
1A	SYSCLK at 1.5V to $\overline{SYSCLK}$ at 1.5V when used as an output	Note 14	0.5T–1	0.5T+1	ns
2	SYSCLK High Time when used as input	Note 14	15		ns
3	SYSCLK Low Time when used as input	Note 14	14		ns
4	SYSCLK Rise Time	Note 3		3	ns
5	SYSCLK Fall Time	Note 3		3	ns
6	Synchronous SYSCLK Output Valid Delay	Notes 4, 13	2	13	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	Notes 13, 19	2	14	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 5, 15, 16	1	20	ns
8	Synchronous $\overline{SYSCLK}$ Output Valid Delay	Notes 6, 13	2	10	ns
8A	Three-State $\overline{SYSCLK}$ Synchronous Output Invalid Delay	Notes 6, 15, 16	1	20	ns
9	Synchronous Input Setup Time	Note 8	10		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		4		ns
9B	Synchronous Input Setup Time for $\overline{DRDY}$		11		ns
10	Synchronous Input Hold Time	Note 7	3		ns
11	Asynchronous Input Minimum Pulse Width	Note 9	T+10		ns
12	INCLK Period		15	50	ns
12A	INCLK to SYSCLK Delay		2	8	ns
12B	INCLK to $\overline{SYSCLK}$ Delay		2	8	ns
13	INCLK Low Time		4.25		ns
14	INCLK High Time		4.25		ns
15	INCLK Rise Time			3.25	ns
16	INCLK Fall Time			3.25	ns
17	INCLK to Deassertion of $\overline{RESET}$ (for phase synchronization of SYSCLK)	Note 10	1	5	ns
18	$\overline{WARN}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 11	4T		ns
19	$\overline{BINV}$ Synchronous Output Valid Delay from $\overline{SYSCLK}$	Note 13	0	6	ns
20	Three-State Synchronous SYSCLK Output Invalid Delay for D31–D0	Notes 12, 15, 16	3	20	ns

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SWITCHING CHARACTERISTICS over INDUSTRIAL Operating Range

No.	Parameter Description	Test Conditions[1]	25 MHz		20 MHz		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK) Period (T)	Note 2	40	100	50	100	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 14	0.5T−1	0.5T+1	0.5T−1	0.5T+1	ns
2	SYSCLK High Time when used as input	Note 14	19		22		ns
3	SYSCLK Low Time when used as input	Note 14	17		19		ns
4	SYSCLK Rise Time	Note 3		4		4	ns
5	SYSCLK Fall Time	Note 3		4		4	ns
6	Synchronous SYSCLK Output Valid Delay	Notes 4, 13	2	14	2	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	Notes 13, 19	2	18	2	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 5, 15, 16	3	30	3	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 6, 13	2	14	2	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 6, 15, 16	3	30	3	30	ns
9	Synchronous Input Setup Time	Note 8	12		15		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		6		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		13		16		ns
10	Synchronous Input Hold Time	Note 7	3.5		4		ns
11	Asynchronous Input Minimum Pulse Width	Note 9	T+10		T+10		ns
12	INCLK Period		20	50	25	50	ns
12A	INCLK to SYSCLK Delay		2	10	2	12	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	10	2	12	ns
13	INCLK Low Time		6.75		9.25		ns
14	INCLK High Time		6.75		9.25		ns
15	INCLK Rise Time			3.25		3.25	ns
16	INCLK Fall Time			3.25		3.25	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 10	1	7	1	8	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 11	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 13	0	7	0	9	ns
20	Three-State Synchronous SYSCLK Output Invalid Delay for D31–D0	Notes 12, 14, 15	3	20	3	25	ns

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Notes:

1. Test conditions: All inputs/outputs are TTL compatible for V_{IH}, V_{IL}, V_{OH}, and V_{OL} unless otherwise noted. All output timing specifications are for 80 pF of loading. All setup, hold, and delay times are measured relative to SYSCLK or INCLK unless otherwise noted. All input Low levels must be driven to 0.45 V and all input High levels must be driven to 2.4 V except SYSCLK.

2. AC measurements made relative to 1.5 V, except where noted.

3. SYSCLK rise and fall times measured between 0.8 V and (V_{CC} − 1.0 V).

4. Synchronous Outputs relative to SYSCLK rising edge include: A31–A0, $\overline{BGRT}$, R/$\overline{W}$, SUP/$\overline{US}$, $\overline{LOCK}$, MPGM1–MPGM0, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, DREQT1–DREQT0, $\overline{PDA}$, OPT2–OPT0, STAT2–STAT0, and MSERR.

5. Three-state Synchronous Outputs relative to SYSCLK rising edge include: A31–A0, R/$\overline{W}$, SUP/$\overline{US}$, $\overline{LOCK}$, MPGM1–MPGM0, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, DREQT1–DREQT0, $\overline{PDA}$, and OPT2–OPT0.

6. Synchronous Outputs relative to SYSCLK falling edge ($\overline{SYSCLK}$): $\overline{IBREQ}$, $\overline{DBREQ}$.

7. Synchronous Inputs include: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{DERR}$, $\overline{DBACK}$, $\overline{CDA}$, I31–I0, $\overline{DRDY}$, and D31–D0.

8. Synchronous Inputs include: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{DERR}$, $\overline{DBACK}$, and $\overline{CDA}$.

9. Asynchronous Inputs include: $\overline{WARN}$, $\overline{INTR3}$–$\overline{INTR0}$, $\overline{TRAP3}$–$\overline{TRAP0}$, and CNTL1–CNTL0.

10. $\overline{RESET}$ is an asynchronous input on assertion/deassertion. As an option to the user, $\overline{RESET}$ deassertion can be used to force the state of the internal divide-by-two flip-flop to synchronize the phase of SYSCLK (if internally generated) relative to $\overline{RESET}$/INCLK.

11. $\overline{WARN}$ has a minimum pulse width requirement upon deassertion.

12. To guarantee Store/Load with one-cycle memories, D31–D0 must be asserted relative to SYSCLK falling edge from an external drive source.

13. Refer to Capacitive Output Delay table when capacitive loads exceed 80 pF.

14. When used as an input, SYSCLK presents a 90-pF max load to the external driver. When SYSCLK is used as an output, timing is specified with an external load capacitance of ≤ 200 pF. For frequencies ≤ 33 MHz, the measurement point is 1.5 V. For frequencies > 33 MHz, the measurement point is 2.5 V.

15. Three-State Output Inactive Test Load. Three-State Synchronous Output Invalid Delay is measured as the time to a ±500 mV change from prior output level.

16. When a three-state output makes a synchronous transition from a valid logic level to a high-impedance state, data are guaranteed to be held valid for an amount of time equal to the lesser of the minimum Three-State Synchronous Output Invalid Delay and the minimum Synchronous Output Valid Delay.

17. SYSCLK is not available as an input at 40 MHz.

18. Performance guaranteed by design for 40 MHz part.

19. All unused outputs should be terminated.

■ 0257525 0051027 373 ■
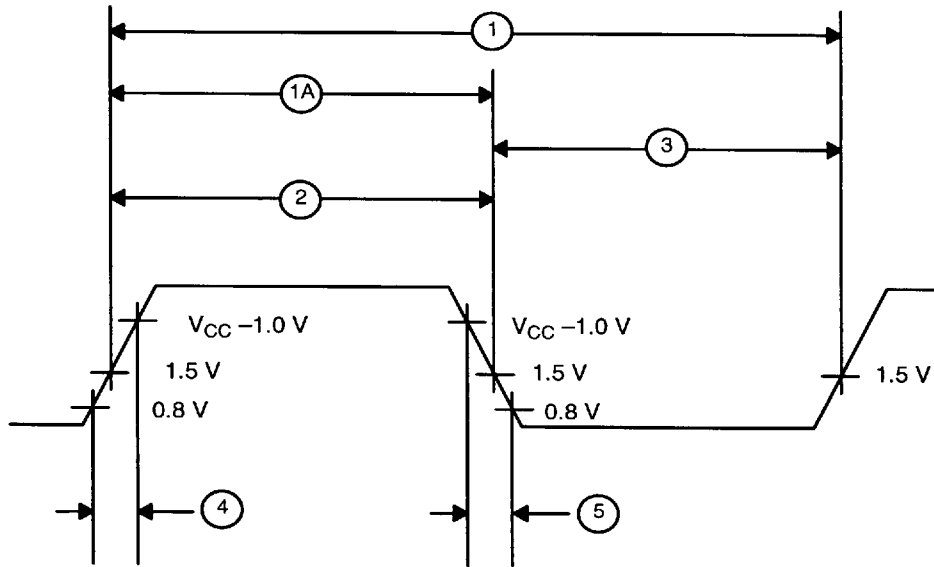
SWITCHING WAVEFORMS

Relative to SYSCLK

■ 0257525 0051028 20T ■
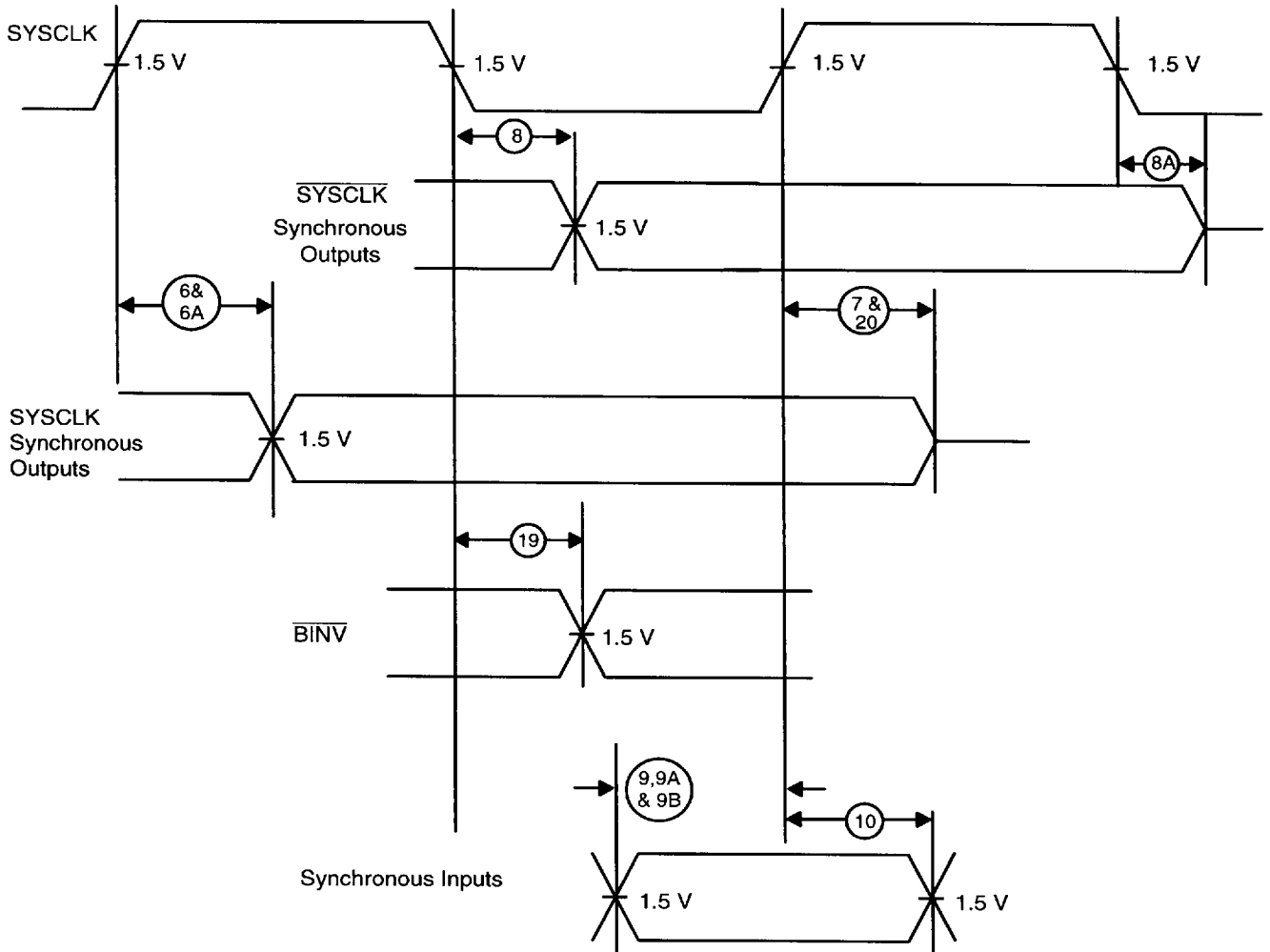
SWITCHING WAVEFORMS (continued)
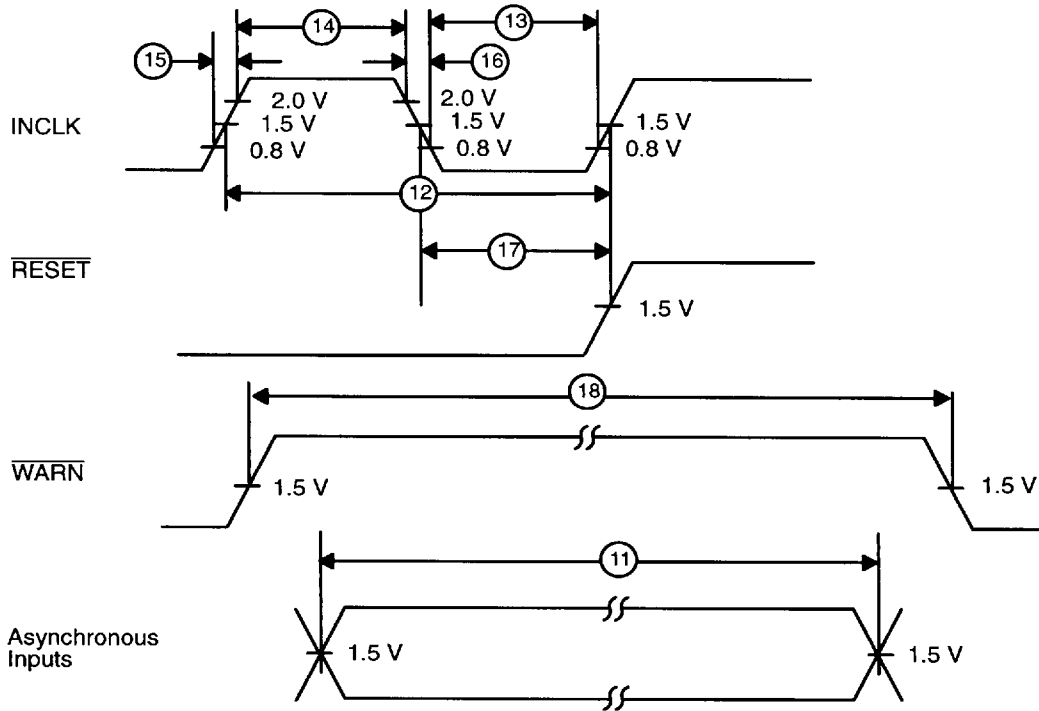
INCLK and Asynchronous Inputs

■ 0257525 0051029 146 ■

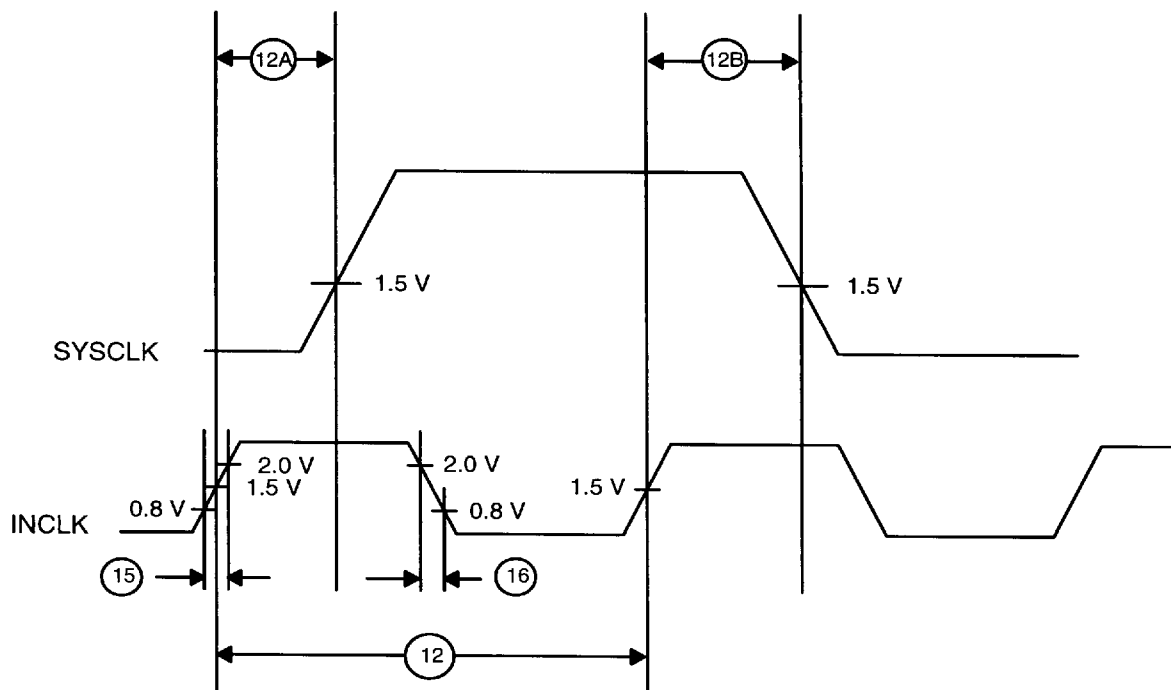## SWITCHING WAVEFORMS (continued)

SYSCLK Definition for 33 MHz and Below


INCLK to SYSCLK Delay

CAPACITIVE OUTPUT DELAYS

For loads greater than 80 pF

This table describes the additional output delays for capacitive loads greater than 80 pF. Values in the Maximum Additional Delay column should be added to the value listed in the Switching Characteristics table. For loads less than or equal to 80 pF, refer to the delays listed in the Switching Characteristics table. Delay values are based on model simulation and are not guaranteed.

No.	Parameter Description	Total External Capacitance	Maximum Additional Delay
6	Synchronous SYSCLK Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +3 ns +4 ns +6 ns +7 ns

SWITCHING TEST CIRCUIT

V_L

$I_{OL} = 3.2$ mA

$V_{REF} = 1.5$ V

C_L

Am29050
Pin Under Test

$I_{OH} = 400 \mu A$

V_H
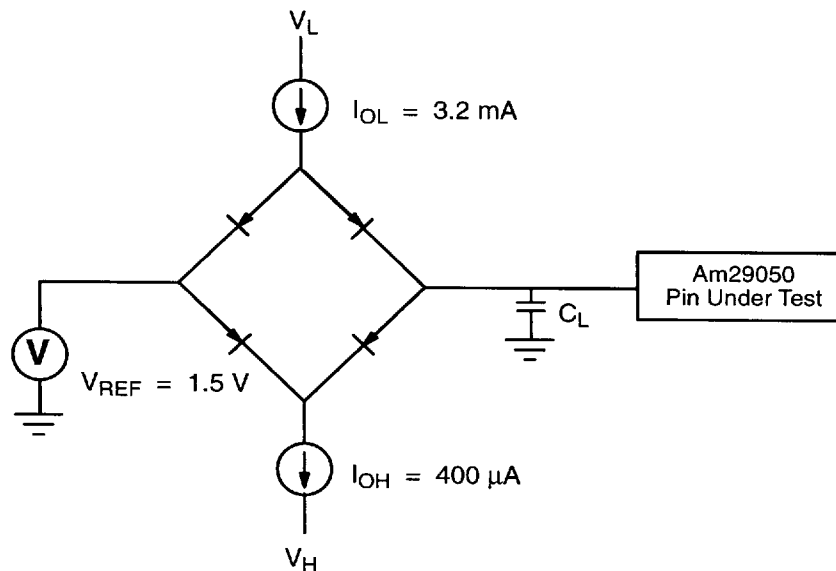
C_L is guaranteed to 80 pF. For capacitive loading greater than 80 pF, refer to the Capacitive Output Delay table.

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THERMAL CHARACTERISTICS
Pin Grid Array (PGA) Package

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Thermal Resistance — °C/Watt
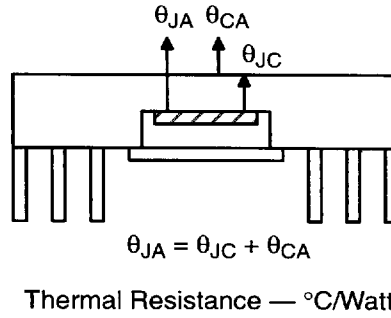
Parameter	Airflow — ft./min. (m/sec)				
	0 (0)	150 (0.76)	300 (1.53)	480 (2.45)	700 (3.58)
θ_{JC} Junction-to-Case	2.4	2.4	2.4	2.4	2.4
θ_{CA} Case-to-Ambient (no Heatsink)	14.7	12.9	11.4	10.0	8.8
θ_{CA} Case-to-Ambient (with omnidirectional 3-fin Heatsink)	8.6	6.6	3.7	2.1	1.2

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PHYSICAL DIMENSIONS
CGX 169
Ceramic Pin Grid Array

1.740 / 1.780   —A—
1.600 BSC

—B—

1.740 / 1.780   1.600 BSC

∅b1= 0.080 Max

Lid Outline
Cavity Down PGA

Index Corner

0.000 BSC (4x)

0.003 Min (4x)
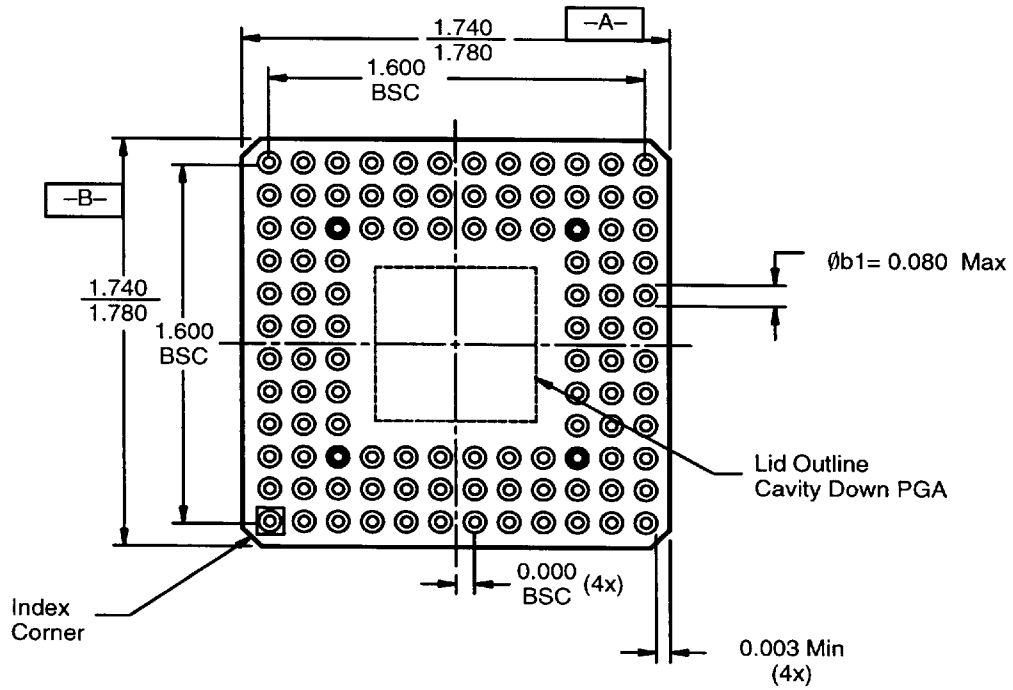
View of PGA Pin Matrix for Both Small and Large Outline

Base Plane   —C—   Heatsink Option

Lid

0.420 Max

0.120 / 0.140
0.025 / 0.055
0.105 / 0.195
0.080 / 0.140
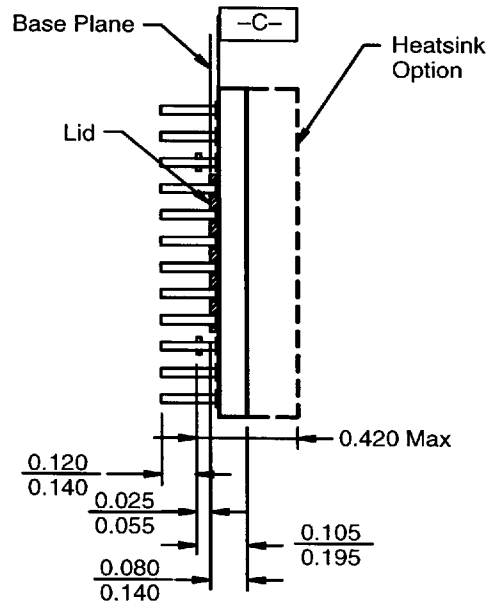
Side View of a Cavity-Down PGA

Notes:

1. All measurements are in inches unless otherwise noted.

2. Not to scale. For reference only.

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