REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE 91-01-21

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, UV ERASABLE PROGRAMMABLE LOGIC DEVICE MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90611

SHEET 1 OF 17 1

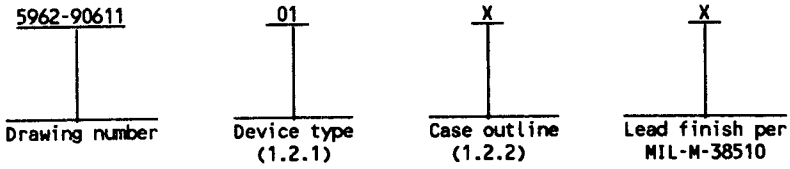
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number(PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	t_{PD}
01		32-Macrocell EPLD	35 ns
02		32-Macrocell EPLD	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-15 (28-lead, 1.485" x .310" x .230"), dual-in-line package 2/
Y	C-J7 (28-lead, .458" x .458" x .180"), J-leaded chip carrier 2/

1.3 Absolute maximum ratings.

Supply voltage to ground potential	-2.0 V dc to +7.0 V dc
DC Input voltage	-2.0 V dc to +7.0 V dc
Maximum power dissipation 3/	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outline X and Y	See Mil-M-38510, appendix C
Junction temperature (T_j)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Endurance	25 erase/write cycles (minimum)
Data retention	10 years, (minimum)

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short circuit test; (e.g., I_{OS}).
4/ When the thermal resistance for this case is specified in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.2 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.2 V, I_{OL} = 8.0 mA, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Input high voltage 1/ 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 1/ 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND	1, 2, 3	All	-10	10	uA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-40	40	uA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V and 4.5 V V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	mA
Power supply current 2/ 4/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = V_{CC} to GND $f = 1/t_{PD1}$	1, 2, 3	All		225	mA
Power supply current 4/ (standby)	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} to GND	1, 2, 3	All		200	mA
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0.0 V, T_A = 25°C, f = 1MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 2/	C_{OUT}		4	All		12	pF
Functional tests		See 4.3.1d	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics							
Dedicated input to combinatorial output delay 6/	t_{PD1}	See figure 4 5/	9, 10, 11	01		35	ns
				02		25	
I/O input to combinatorial output delay 7/	t_{PD2}		9, 10, 11	01		35	ns
				02		25	
Dedicated input to combinatorial output delay with expander delay 2/ 8/	t_{PD3}		9, 10, 11	01		60	ns
				02		40	
I/O input to combinatorial output delay with expander delay 2/ 9/	t_{PD4}		9, 10, 11	01		60	ns
				02		40	
Input to output enable delay 2/ 10/	t_{EA}		9, 10, 11	01		35	ns
				02		25	
Input to output disable delay 2/ 10/	t_{ER}		9, 10, 11	01		35	ns
				02		25	
Synchronous clock input to output delay	t_{CO1}		9, 10, 11	01		23	ns
				02		15	
Synchronous clock to local feedback to combinatorial output 2/ 11/	t_{CO2}		9, 10, 11	01		46	ns
				02		30	
Any input or feedback setup time to synchronous clock input	t_S		9, 10, 11	01	21		ns
				02	15		
Input hold time from synchronous clock input	t_H		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Synchronous clock input high time 2/	t_{WH}	See figure 4 5/	9, 10, 11	01	10		ns
				02	8		
Synchronous clock input low time 2/	t_{WL}		9, 10, 11	01	10		ns
				02	8		
Asynchronous clear width 12/	t_{RW}		9, 10, 11	01	33		ns
				02	28		
Asynchronous clear recovery time 12/	t_{RR}		9, 10, 11	01	35		ns
				02	25		
Asynchronous clear to registered output delay 12/	t_{RO}		9, 10, 11	01		33	ns
				02		28	
Asynchronous preset width 12/	t_{PW}		9, 10, 11	01	33		ns
				02	28		
Asynchronous preset recovery time 12/	t_{PR}		9, 10, 11	01	38		ns
				02	25		
Asynchronous preset to registered output delay 12/	t_{PO}		9, 10, 11	01		33	ns
				02		28	
Synchronous clock to local feedback input 2/ 13/	t_{CF}		9, 10, 11	01		13	ns
				02		7	
External synchronous clock period ($t_{CO1} + t_S$)	t_P		9, 10, 11	01	44		ns
				02	30		
External maximum frequency ($1/(t_{CO1} + t_S)$ 14/	f_{MAX1}		9, 10, 11	01	22.7		MHz
				02	33.3		
Maximum frequency with internal only feedback $1/(t_{CF} + t_S)$ 2/ 15/	f_{MAX2}		9, 10, 11	01	29.4		MHz
				02	45.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data path maximum frequency, least of $1/(t_{WL} + t_{WH})$, $(1/(t_{S1} + t_H))$ or $(1/(t_{CO1})$ 12/ 16/	f_{MAX3}	See figure 4 5/	9, 10, 11	01	43.4		MHz
				02	62.5		
Maximum register toggle frequency $1/(t_{WH} + t_{WL})$ 12/ 17/	f_{MAX4}		9, 10, 11	01	50.0		MHz
				02	62.5		
Output data stable time from synchronous clock input 12/ 18/	t_{OH}		9, 10, 11	All	2		ns
External Asynchronous Switching Characteristics							
Asynchronous clock input to output delay	t_{ACO1}	See figure 4 5/	9, 10, 11	01		35	ns
				02		25	
Asynchronous clock input to local feedback to combinatorial output 2/ 19/	t_{ACO2}		9, 10, 11	01		62	ns
				02		46	
Dedicated input or feedback setup time to asynchronous clock input	t_{AS}		9, 10, 11	01	15		ns
				02	12		
Input hold time from asynchronous clock input	t_{AH}		9, 10, 11	01	17.5		ns
				02	12		
Asynchronous clock input high time 2/	t_{AWH}		9, 10, 11	01	30		ns
				02	11		
Asynchronous clock input low time 2/	t_{AWL}		9, 10, 11	01	30		ns
				02	11		
Asynchronous clock to local feedback input 2/ 20/	t_{ACF}		9, 10, 11	01		27	ns
				02		21	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
External asynchronous clock period ($t_{ACO1} + t_{AS}$) or ($t_{AWH} + t_{AWL}$) 2/	t_{AP}	See figure 4 5/	9, 10, 11	01	50		ns
				02	37		
External maximum frequency in asynchronous mode ($1/(t_{AP})$ 2/ 21/	f_{MAXA1}		9, 10, 11	01	20.0		MHz
				02	27.0		
Maximum internal asynchronous frequency ($1/(t_{ACF} + t_{AS})$ 2/ 22/	f_{MAXA2}		9, 10, 11	01	16.6		MHz
				02	25.0		
Data path maximum frequency in asynchronous mode 2/ 23/	f_{MAXA3}		9, 10, 11	01	16.6		MHz
				02	40.0		
Maximum asynchronous register toggle frequency $1/(t_{AWH} + t_{AWL})$ 2/ 24/	f_{MAXA4}		9, 10, 11	01	16.6		MHz
				02	45.0		
Output data stable time from asynchronous clock input 12/ 25/	t_{AOH}		9, 10, 11	All	14		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.
4/ Measured with device programmed with manufacturers test pattern and shall be made available upon request.
5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A.
6/ This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function (see figure 4).
7/ This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
8/ This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

TABLE I. Electrical performance characteristics - Continued

9/ This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10/ Transition is measured ± 0.5 V from steady state voltage on the output from the 1.5 V level on the input with the load on figure 3, circuit B.
11/ This specification is a measure of the delay from synchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes that no expanders are used in the logic of the combinatorial output and the register is synchronously clocked (see figure 4).
12/ Values guaranteed by design and are not tested.
13/ This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register setup time, t_S, is the minimum internal period for an internal state machine configuration.
14/ This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
15/ This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO1}$. This specification assumes no expander logic is used.
16/ This frequency indicates the maximum frequency at which the device may operate in the data path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
17/ This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
18/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.
19/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input.
20/ This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register set up time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path (see figure 4).
21/ This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data input path.
22/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$. This specification assumes no expander logic is utilized.
23/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. If this frequency is less than $1/t_{ACO1}$ or $1/(t_{AH} + t_{AS})$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data path mode. Assumes no expander logic is used.
24/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to either a dedicated input or an I/O pin.
25/ This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

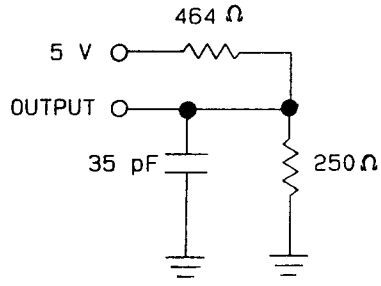
Device types	All	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	I	V_{CC}
2	I/CLK	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I
7	V_{CC}	I
8	GND	I
9	I/O	I/CLK
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I	I/O
14	I	V_{CC}
15	I	GND
16	I	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I
21	GND	I
22	V_{CC}	I
23	I/O	I
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I	I/O
28	I	GND

Figure 1. Terminal connections.

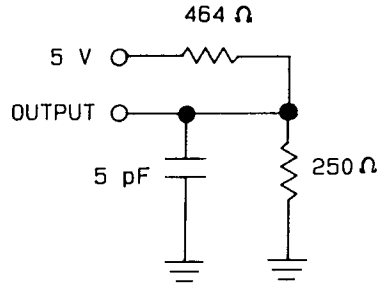
Truth table		
Input pins		Output pins
CP/I	I	I/O
X	X	Z

NOTES:
1. x = Don't care
2. z = High impedance

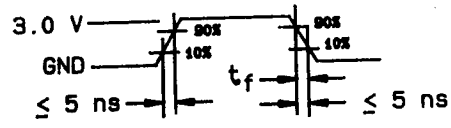
FIGURE 2. Truth table (unprogrammed).



Circuit A
Output load



Circuit B
Output load for t_{EA} and t_{ER}



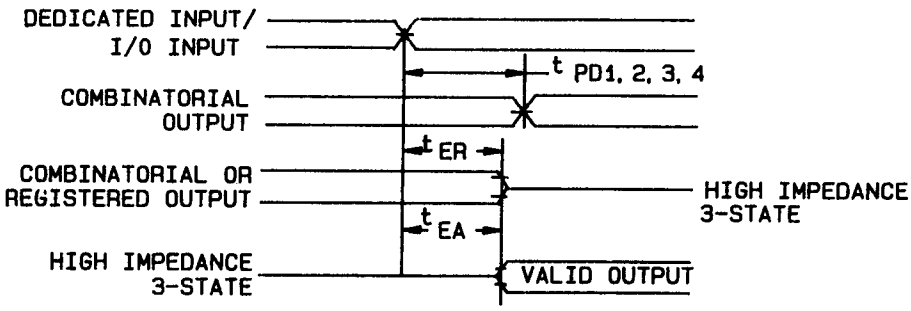
Input pulses

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

External Combinatorial



External synchronous

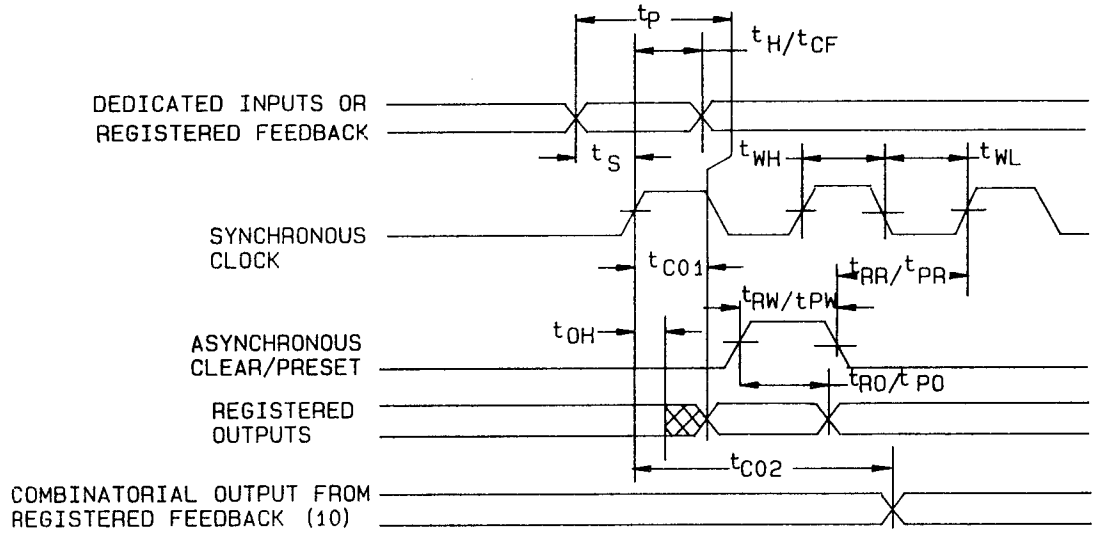


FIGURE 4. Switching waveforms.

External Asynchronous

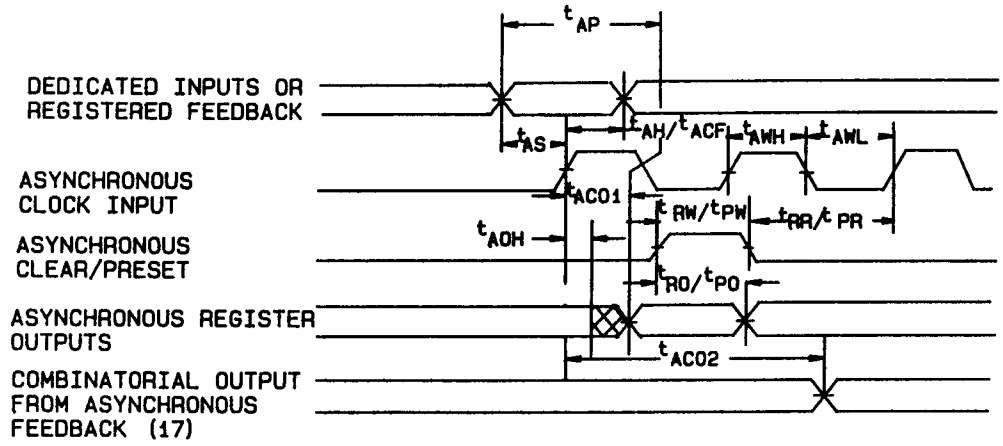


FIGURE 4. Switching waveforms - continued.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection groups A, B, C, or D (see 4.3herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at leâst 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPLD's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.5 herein) to the specified pattern (See 3.2.3.1 herein) or erased (see 4.4 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all logic array bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.)

Margin test method

(1) Program a minimum of 95% of the total number of cells, including the slowest programming cell (see 3.10.2).
(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at 150°C or for 8 hours at +200°C or for 2 hours at 300°C for unassembled devices only.
(3) Perform electrical test (see 4.2b) at 25°C including a margin test at Vm = 5.7 V and loose timing (i.e. = 1s).
(4) Erase (see 3.10.1).
(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.10.2).
(6) Perform electrical test (see 4.2b) at 25°C including a margin test at Vm = 5.7 V and loose timing (i.e. = 1s).
(7) Perform burn-in (see 4.2a).
(8) Perform electrical test (see 4.2b) at 25°C including a margin test at Vm = 5.7 V and loose timing (i.e. = 1).
(9) Repeat step 8 at t_c = +125°C and -55°C.
(10) Erase (see 3.10.1). Devices may be submitted for groups A, C and D testing prior to erasure provided devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
(11) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial characterization and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. See footnote 4 of table II.

e. All devices selected for testing shall be programmed per 3.2.3.1 herein.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1,2,3,4**,7, 8A, 8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 functional tests shall verify that no cells are programmed for unprogrammed devices, that the altered item drawing pattern exists for programmed devices, or that the devices comply with 3.2.3.1 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed per 3.2.3.1 herein. After completion of testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. A reprogrammability test shall be added to group C inspection prior to performing steady-state life test (see 4.3.2b). The devices devices to be submitted to the steady-state life testing shall be subjected to the following tests and examinations;

Each device in the sample shall be subjected to a minimum of 25 program and erase cycles.

(1) All devices selected for testing shall be programmed per 3.2.3.1 herein.

(2) Verify pattern (see 3.10.3).

(3) Erase (see 3.10.1).

(4) Verify pattern erasure (see 3.10.3).

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms. The intergrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of twentyfive Ws/cm^2. The erasure time with this dosage is approxi)ately 35 minutes using a ultraviolet lamp with a 12000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum intergrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 uW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made availible upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.