NEC
NEC Electronics Inc.

Description

The μPD23C1001E is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

Features
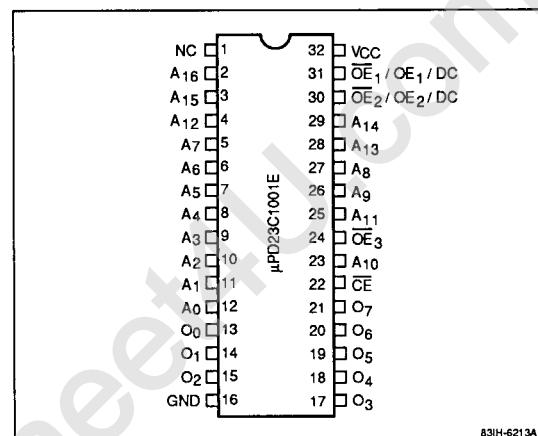
- 131,072-word by 8-bit organization
- Fast access time of 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1001EC	200 ns	32-pin plastic DIP

Pin Configuration

32-Pin Plastic DIP


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NC   [ 1        32 ] VCC
A16  [ 2        31 ] OE1 / OE1 / DC
A15  [ 3        30 ] OE2 / OE2 / DC
A12  [ 4        29 ] A14
A7   [ 5        28 ] A13
A6   [ 6        27 ] A8
A5   [ 7        26 ] A9
A4   [ 8        25 ] A11
A3   [ 9        24 ] OE3
A2   [ 10       23 ] A10
A1   [ 11       22 ] CE
A0   [ 12       21 ] O7
O0   [ 13       20 ] O6
O1   [ 14       19 ] O5
O2   [ 15       18 ] O4
GND  [ 16       17 ] O3
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83IH-6213A

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}_1$/OE_1/DC	Output enable 1 (Note 1)
$\overline{OE}_2$/OE_2/DC	Output enable 2 (Note 1)
$\overline{OE}_3$	Output enable 3
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{OE}_1$/OE_1/DC and $\overline{OE}_2$/OE_2/DC).

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Capacitance

T_A = 25°C; f = 1 MHz
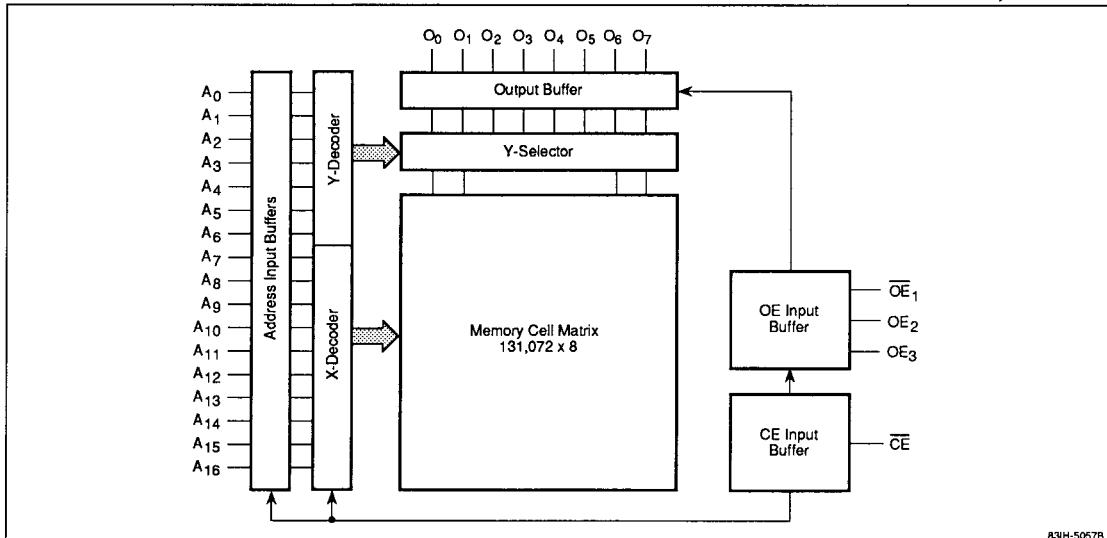
Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		15		pF
Output capacitance	C_O		15		pF

Truth Table

$\overline{CE}$	$\overline{OE}_1/OE_1/DC$	$\overline{OE}_2/OE_2/DC$	$\overline{OE}_3$	Outputs	Function
V_{IH}	X	X	X	High-Z	Standby
V_{IL}	I	X	X	High-Z	Active
V_{IL}	X	I	X	High-Z	Active
V_{IL}	X	X	V_{IH}	High-Z	Active
V_{IL}	A	A	V_{IL}	D_{OUT}	Read

Notes:

(1) I = Inactive

(2) A = Active

(3) X = "don't care"

Block Diagram

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0 V \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400 \mu A$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = +2.5 mA$
Input leakage current	I_{LI}	-10		10	μA	$V_I = 0 V$ to V_{CC}
Output leakage current	I_{LO}	-10		10	μA	$V_O = 0 V$ to V_{CC}; outputs disabled
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$ (active)
	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$ (standby)
	I_{CC3}			100	μA	$\overline{CE} \geq V_{CC} - 0.2 V$ (standby)

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0 V \pm 10\%$ (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Chip enable access time	t_{CE}			200	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

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Timing Waveform

Notes:

[1] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever becomes inactive first.

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