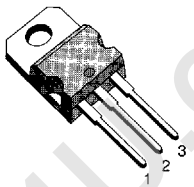
SGS-THOMSON
MICROELECTRONICS

STP53N05

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP53N05	50 V	< 0.025 Ω	53 A

- TYPICAL $R_{DS(on)}$ = 0.022 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

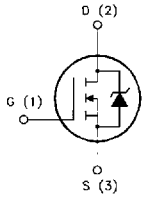


TO-220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	50	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	50	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	53	A
I_D	Drain Current (continuous) at T_c = 100 °C	37	A
I_{DM}(•)	Drain Current (pulsed)	212	A
P_{tot}	Total Dissipation at T_c = 25 °C	150	W
	Derating Factor	1	W/°C
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Case-sink	Typ	0.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	53	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 25 V)	450	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	110	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (T_c = 100 °C, pulse width limited by T_j max, $\delta < 1\%$)	37	A

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	50			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	2.9	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 26.5 A V_{GS} = 10V I_D = 26.5 A T_c = 100°C		0.022	0.025 0.05	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	53			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 26.5 A	17	22		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1700 630 200	2200 850 260	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 25 V I_D = 26.5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		50 110	70 160	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 53 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		460		A/µs
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 40 V I_D = 53 A V_{GS} = 10 V		50 14 25	70	nC nC nC

SWITCHING OFF

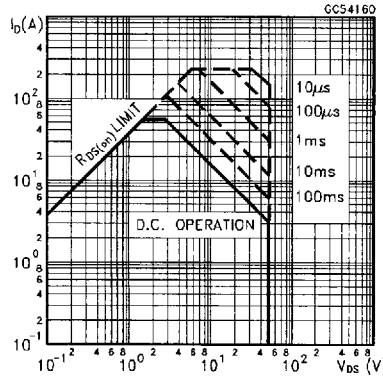
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 53 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		55 50 110	80 70 160	ns ns ns

SOURCE DRAIN DIODE

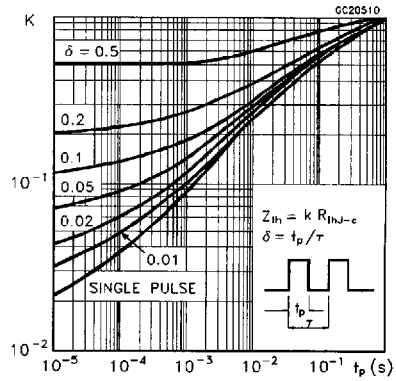
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				53 212	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 53 A V_{GS} = 0			2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 53 A di/dt = 100 A/µs V_{DD} = 30 V T_j = 150 °C (see test circuit, figure 5)		150 0.45 6		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

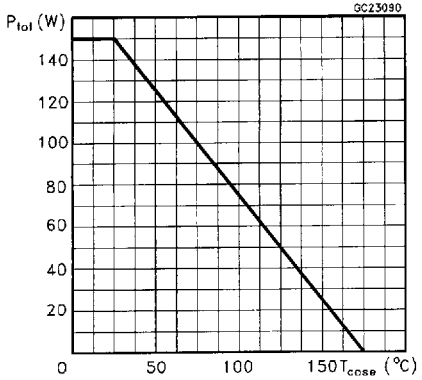
Safe Operating Areas



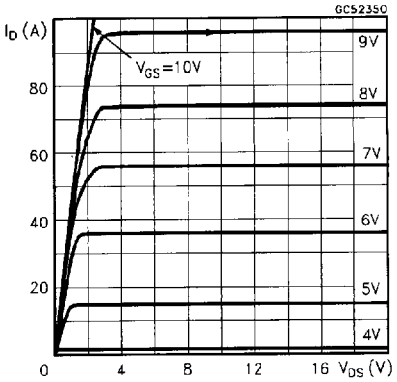
Thermal Impedance



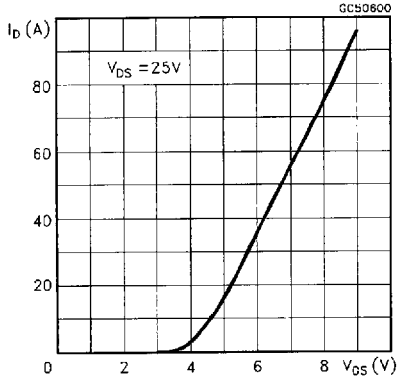
Derating Curve



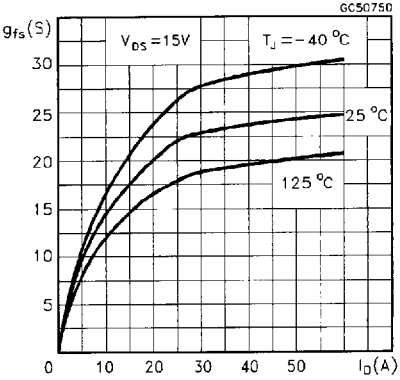
Output Characteristics



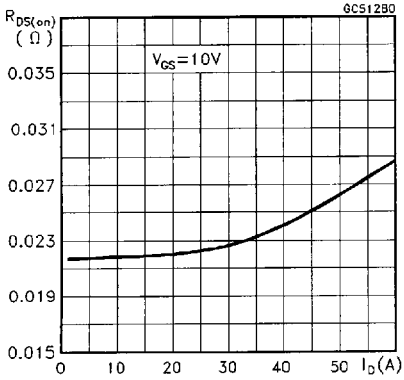
Transfer Characteristics



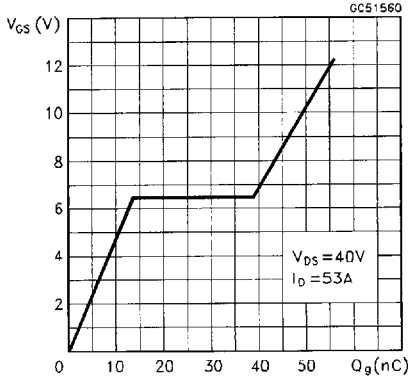
Transconductance



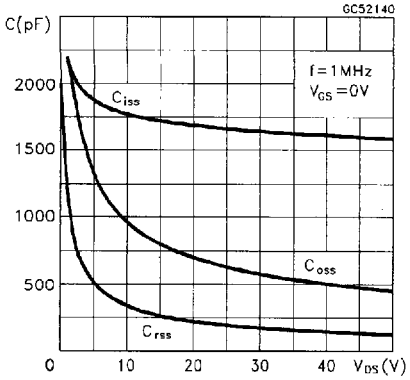
Static Drain-source On Resistance



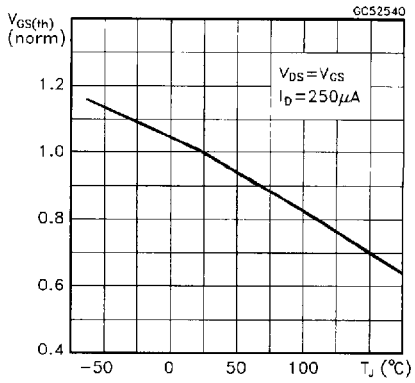
Gate Charge vs Gate-source Voltage



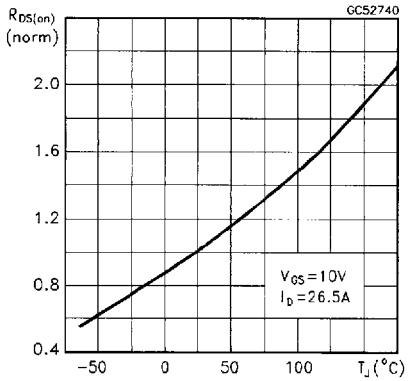
Capacitance Variations



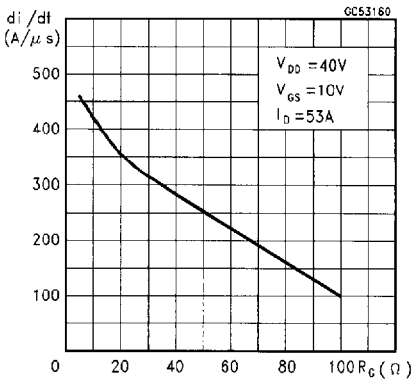
Normalized Gate Threshold Voltage vs Temperature



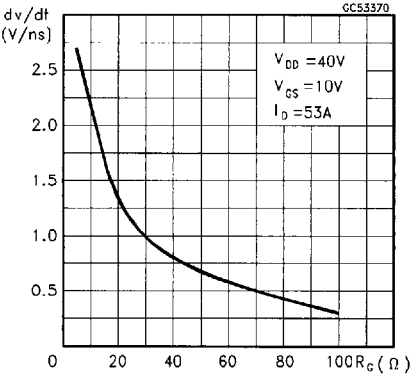
Normalized On Resistance vs Temperature



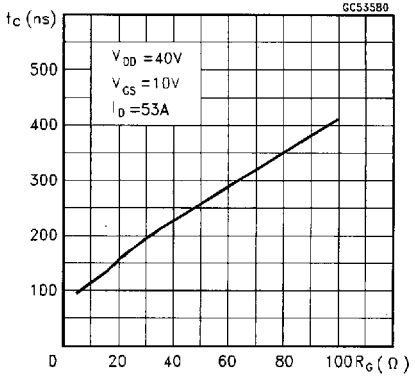
Turn-on Current Slope



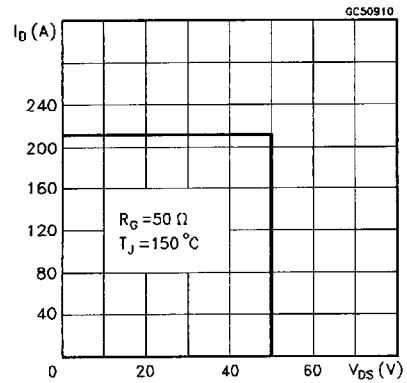
Turn-off Drain-source Voltage Slope



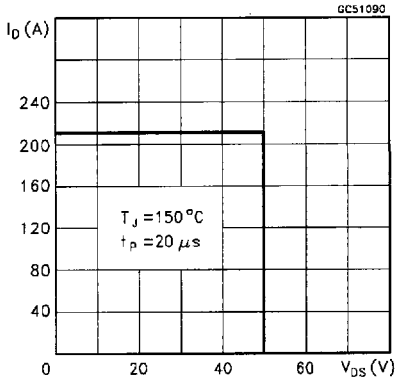
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

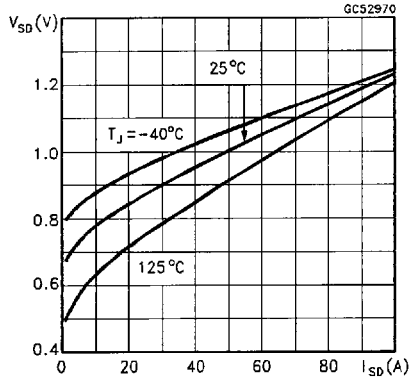


Fig. 1: Unclamped Inductive Load Test Circuits

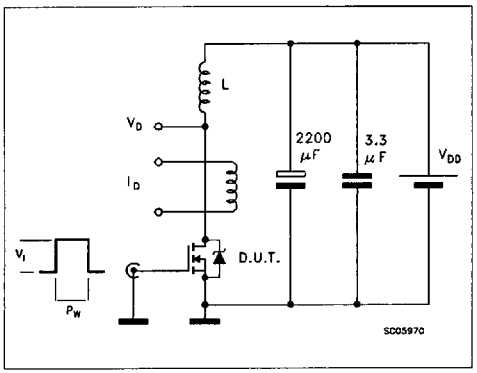


Fig. 2: Unclamped Inductive Waveforms

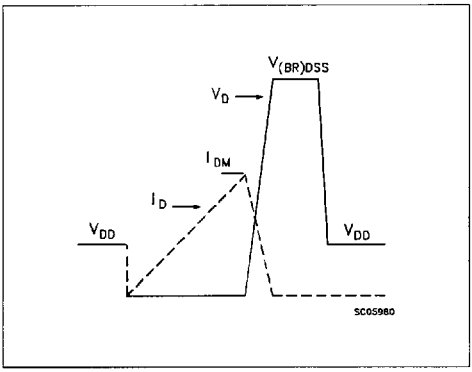


Fig. 3: Switching Times Test Circuits For Resistive Load

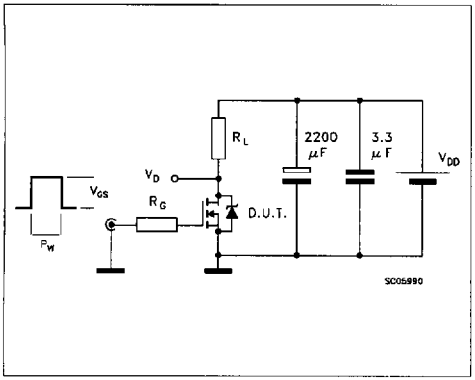


Fig. 4: Gate Charge Test Circuit

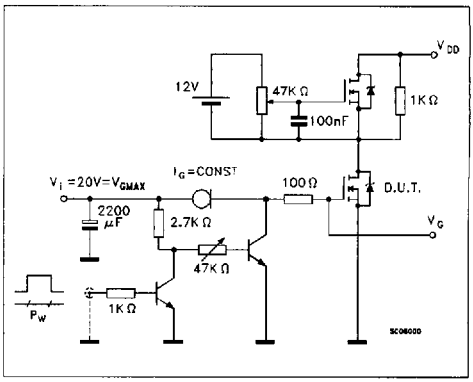


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times