HDTV Deserialiser GD14516A

Advance Information

The GD14516A High Definition TV Deserialiser is designed for point-to-point serial transmission systems for HDTV signals according to SMPTE292.

The device provides a fully integrated solution for:

- Clock recovery and data re-timing at 1485 Mbit/s
- Descrambler and NRZI decoder
- Frame Detector for SAV/EAV
- 1:20 DeMUX.

The Clock and Data Recovery Circuit consists of:

- a Bang-Bang Phase Detector (PD) with data re-timing
- Phase-Frequency Comparator (PFC),
- a Lock Detect Circuit (LCD) with Lock Alarm Output,
- a Tristatable Charge Pump
- a wide tuning range VCO.

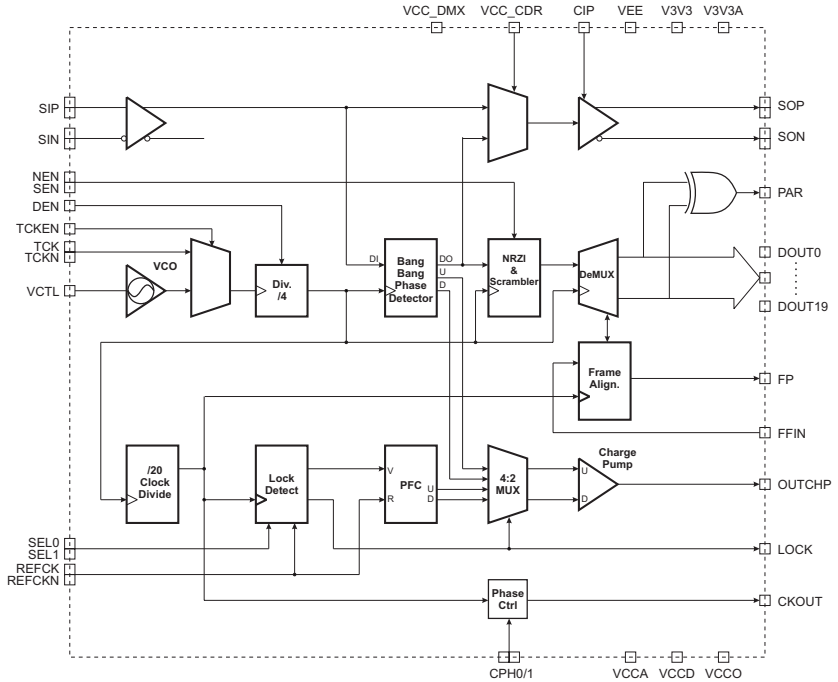
The VCO centre frequency is determined by the REFCK multiplied by 20. The loop filter time constant is determined by an external RC filter.

When in lock, the digital *Lock Detect Circuit* uses the incoming data to control the PLL. When not in lock, i.e. the VCO frequency is more than 500 ppm away from the REFCK frequency, the LDC switches to the local clock (REFCK) until the VCO frequency once more enters the ±500 ppm range. Then it switches back to the PD, comparing the VCO clock to the incoming data stream. The LDC continuously monitors the VCO frequency against the REFCK input, clearing LOCK if the VCO leaves the lock range.

A Frame Alignment circuit detects the EAV/SAV framing pattern and aligns data at the 20 bit output port. The frame alignment can be disabled to allow other coding schemes.

The high-speed data input is differential and compatible with PECL levels. It is connected via loop-through transmission lines to minimize stub related reflections. For repeater applications a re-timed 75 Ω cable driver output is provided, which also can be used to drive an optical module.

The GD14516A is packaged in a 68 pin leaded Multi Layer Ceramic (MLC) package with cavity down for easy cooling.



Features

- Nominal data-rate 1485 Mbit/s NRZI.
- Two operating ranges:
  - 1.2 -1.5 Gbit/s
  - 300 - 375 Mbit/s
- Timing and Alignment Jitter in accordance with SMPTE292.
- High-speed data input and output use Loop-through bondings to reduce reflections.
- Complete Clock/20 (Data Recovery) and Lock Acquisition on one IC.
- Digitally controlled capture and lock.
  - Full capture range with true Phase/Frequency detect between VCO-CLK and REFCK.
  - Bang-Bang Phase Detector between VCO-CLK and DATA.
  - Lock in range ±500 ppm or ±2000 ppm referred to REFCK.
  - Lock Alarm Output.
- End of Active Video (EAV) / Start of Active Video (SAV) detection and alignment of the parallel 20 bit output
- Re-timed differential 75 Ω cable driver output with external termination resistors.
- Supply operation: 5 V and 3.3 V.
- Power dissipation: 2500 mW typ.
- Power down modes for repeater applications.
- 68 pin Multi Layer Ceramic (MLC) leaded package with transmission lines.

Applications

- HDTV studio equipment.

Function Details

The Clock and Data Recovery (CDR) part of the GD14516A consists of:

- an Input Amplifier,
- a Voltage Controlled Oscillator (VCO),
- a Phase Detector
- a Loop Filter
- a Charge Pump
- a Phase-Frequency Comparator

The Charge Pump performs the transformation between the digital error signal of the Phase Detector and the voltage controlling the oscillator.

The true Phase-Frequency Comparator is used when acquiring lock and a Lock Detection circuit determines whether or not the PLL is locked onto incoming data. A divide by 4 option (DEN input) following the on-chip oscillator provides two tuning ranges for the VCO
1200 – 1500 MHz (DEN = “0”)
300 – 375 MHz (DEN = “1”)

When the CDR has acquired lock, the Frame Detect/Alignment circuit - if enabled - searches for an EAV/SAV framing pattern and aligns the parallel data outputs accordingly.

All logic blocks in the design are differentially coupled, i.e. both clocks and signals are differential. This in conjunction with the de-coupled power planes in the package, provide a low jitter content in the parallel output data.

The Phase Detector

The *Phase Detector* (PD) used in the CDR is designed to give minimum static phase error of the PLL. It is of the true digital type (Bang-Bang), producing a binary output. It samples data prior to, in the vicinity of and after any potential bit transition. When a transition has occurred the value of the sample in the vicinity of the transition tells whether the VCO clock leads or lags the incoming data and the phase detector produces a binary output accordingly. Hence the PLL is controlled by the bit transition point.

The output of the PD is binary with three values indicating whether the VCO must go UP or DOWN in frequency, if a bit transition has occurred, or stay, if not (consecutive “1"s or ”0"s). This information is fed into the Charge Pump, which transfers it into three output levels, sinking or sourcing current or tristating the output. The output of the Charge Pump is integrated and filtered outside the chip by two resistors and a capacitor. The initial values has been determined to 51 Ω and 100 nF in parallel with 2 µF, with a resistor of 1 kΩ connected in series with the Charge Pump output. These values can be altered to achieve the optimal characteristics for the application.

The Phase-Frequency Comparator

The *Phase-Frequency Comparator* (PFC) ensures predictable lock up conditions for the GD14516. It is used during acquisition, and serves as means to pull the VCO into the range of the data rate where the PD is capable of acquiring lock. The comparator is of the set-reset type, comparing the edges of the VCO frequency divided by 20 and the local reference clock (REFCK). The output of the PFC tells whether the VCO must be adjusted UP or DOWN, proportional to the phase error between the clocks. This information is fed into the Charge Pump, which provides sinking or sourcing current for the loop filter capacitor.

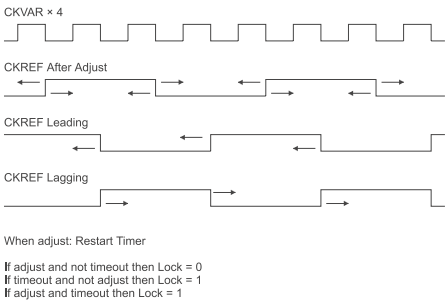


Figure 1. *Lock Detect Scheme.*

The REFCK input is configured as a differential input, but will also operate as single ended TTL input due to the internal 1.4 V DC-bias on the inverted input. Use external decoupling to set a clean threshold.

The Lock Detect Circuit

The *Lock Detect Circuit* (LDC) is the guarantee of a fast and reliable lock up. It monitors the difference between the divided VCO clock and the reference clock (REFCK), when the PLL is locked onto the incoming data by the PD. If the difference between the divided VCO clock and the clock reference is greater than ±500 ppm, the LDC considers the PLL to be out of lock, and switches to the PFC to pull the VCO frequency into the data rate range. The alarm lock output is set low.

When the LDC has monitored the VCO frequency to be within the Data Rate range over a period corresponding to ±500 ppm, it switches back to the PD and starts acquiring lock onto data. This way the recovered output clock is always kept within the ±500 ppm, regardless of the serial data line is active or not.

Frame Detector & Alignment

When the FFIN signal is high, the *Frame Detector & Alignment* (FDA) starts looking for EAV/SAV in the incoming data stream and aligns data whenever SAV/EAV is found regardless of the current alignment.

The 20 bit data outputs will be completely aligned by the FDA upon reception of the first EAV or SAV sequence and the FP output activated.

A parity output is provided for test purposes. This output is a synchronous XOR of the parallel output data.

Power Down

GD14516A has been designed to allow 2 Power Down modes as listed below.

Please note that in all modes the appropriate supply voltages should always be applied to the V_{3V3}, V_{CC} and V_{EE} pins:

CDR (V_{CC_CDR} = +5V, V_{CC_DMX} = 0V): Re-timed repeater without DeMUX, but serial input and output, CDR, VCO and Lock Detect are active.

Bypass (V_{CC_CDR} = 0V, V_{CC_DMX} = 0V): Repeater with only serial input and output active.

Normal (V_{CC_CDR} = +5V, V_{CC_DMX} = +5V): Standard mode of operation with all circuits active.

V_{CC_CDR} & V_{CC_DMX} require approximately 1 mA and can be switched by CMOS logic.

Applications

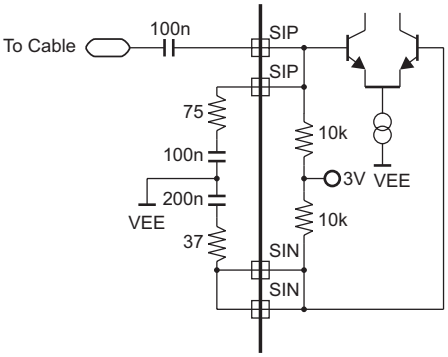


Figure 2. *Standard Input Configuration.*

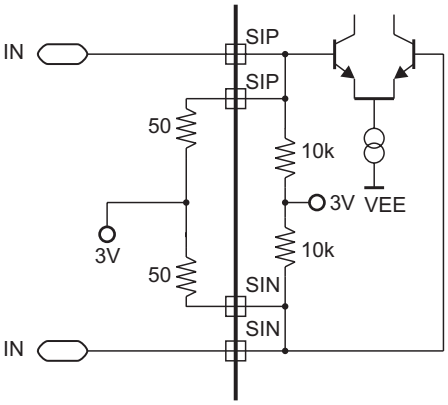


Figure 3. *PECL Input Configuration.*

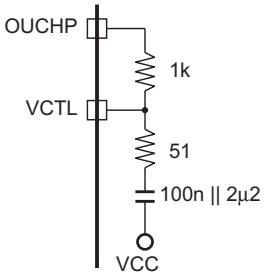


Figure 4. *Loop Filter*

Note: De-coupling should be made from VCC to VEE plane. Use 33 nF chip capacitors close to package pins.

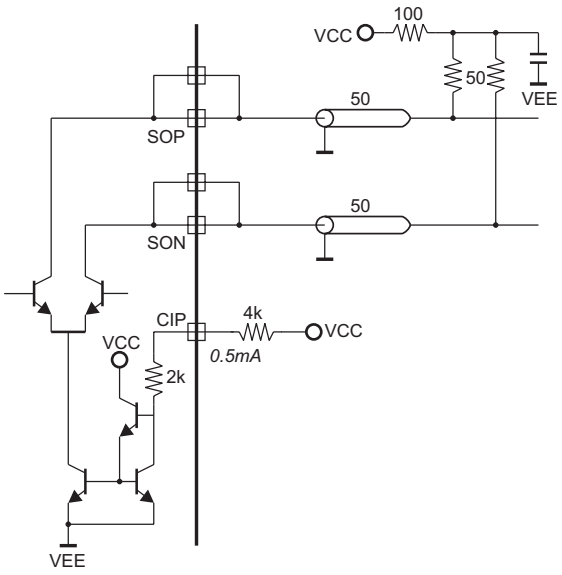


Figure 5. *Differential PECL Driver*

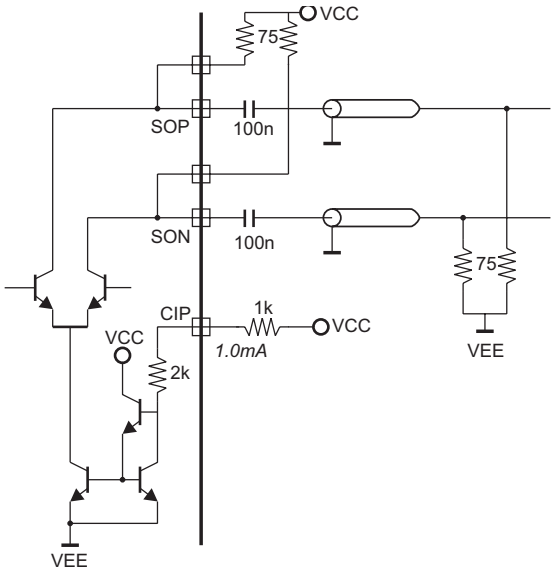


Figure 6. *Dual 75R Cable Driver*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
SIP SIN	29, 30 27, 28	Analog IN	Serial data input (differential). Compatible with PECL levels. Loop-back termination: Each input is connected to two pins, one for input and the other for the termination resistor. See Figures on page 3.
SOP SON	24, 25 22, 23	Open Collector	Re-timed differential serial data output. High speed Open Collector outputs to be used with 75 Ω cable or 50 Ω termination for optical transmitter. See Figures on page 3.
CIP	32	Analog IN	DC-Current control input for SOP, SON: 1mA current into CIP generates 25mA bias for the differential output stage. Maximum setting is 1.2mA => 30mA output stage bias. If CIP is pulled low, the output stage will turn off.
DOUT0, DOUT1 DOUT2, DOUT3 DOUT4, DOUT5 DOUT6, DOUT7 DOUT8, DOUT9 DOUT10, DOUT11 DOUT12, DOUT13 DOUT14, DOUT15 DOUT16, DOUT17 DOUT18, DOUT19	58, 59 61, 62 63, 64 66, 67 2, 3 5, 6 7, 8 10, 11 12, 13 15, 16	TTL OUT	Re-timed parallel data output from DeMUX. After frame synchronisation, bit 0 holds the first bit received (LSB).
CKOUT	57	TTL OUT	Regenerated output clock, VCO frequency divided by 20.
REFCK, REFCKN	44, 45	TTL IN	Reference clock input with frequency equal to data rate divided by 20, 74.25 MHz @ 1.485 Gbit/s. Internal 1.4 V DC-bias on REFCKN should be externally de-coupled or driven.
SEL0	46	TTL IN	Lock Detect Range select: “0” ±2000 ppm “1” ±500 ppm
SEL1	33		PLL override “0” PFC always used “1” Lock Detect Circuit selects PFC or PD
CPH0, CPH1	20, 19	TTL IN	Phase relation select between CKOUT and the loading of the parallel data. Data ready after CKOUT rising edge: CPH1 CPH0 1 1 T_{DEL} = 0° 0 0 T_{DEL} = 90° 1 0 T_{DEL} = 180° 0 1 T_{DEL} = 270°
FFIN	49	TTL IN	Enable alignment of the parallel outputs on each EAV/SAV.
PAR	53	TTL OUT	Parity (synchronuos XOR) of parallel output data.
FP	50	TTL OUT	EAV/SAV frame detect output. One pulse at 74.25 MHz indicates that a valid Frame Sequence has been detected.
LOCK	40	TTL OUT	CDR Lock alarm output. When low, the divided VCO frequency deviates more than ±500/±2000 ppm from REFCK.
VCTL	37	Analog IN	VCO control voltage input.
OUCHP	39	Analog OUT	Charge Pump output providing sink or source current for the integrating capacitor in the external loop filter.
TCKEN	36	TTL IN	Bypass VCO input for DC-functional and parametric testing only. Tie to VEE when not used. “0” Enable VCO, disable TCK,TCKN clock input. “1” Test mode: Disable VCO, enable TCK,TCKN clock input.
TCK, TCKN	41, 42	Analog IN	Test clock input, see TCKEN. Tie to VEE when not used.
SEN	56	TTL IN	Scrambler “0” Enable scrambler “1” Disable scrambler

Mnemonic:	Pin No.:	Pin Type:	Description:
NEN	54	TTL IN	NRZI Encoder “0” Enable NRZI “1” Bypass NRZI
DEN	47	TTL IN	Control of VCO divide by 4 “0” Disable divide by 4 “1” Enable divide by 4
VCC_DMX	17	PWR CTL	Power down DeMUX. VCC_CDR must be “1” “0” Disable DeMUX and parallel clock output “1” Enable DeMUX
VCC_CDR	34	PWR CTL	Power down re-timer “0” Power down (Async. Repeater) “1” Enable re-timer
V3V3	68	PWR	+3.3 V Power for data path.
V3V3A	51	PWR	+3.3 V Power for PFC and CDR.
VEE	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V Power.
VCCA	35	PWR	+5 V Power for VCO.
VCCD	18	PWR	+5 V Power for Cable driver
VCCO	1, 52	PWR	+5 V Power for TTL I/O.

Package Pinout

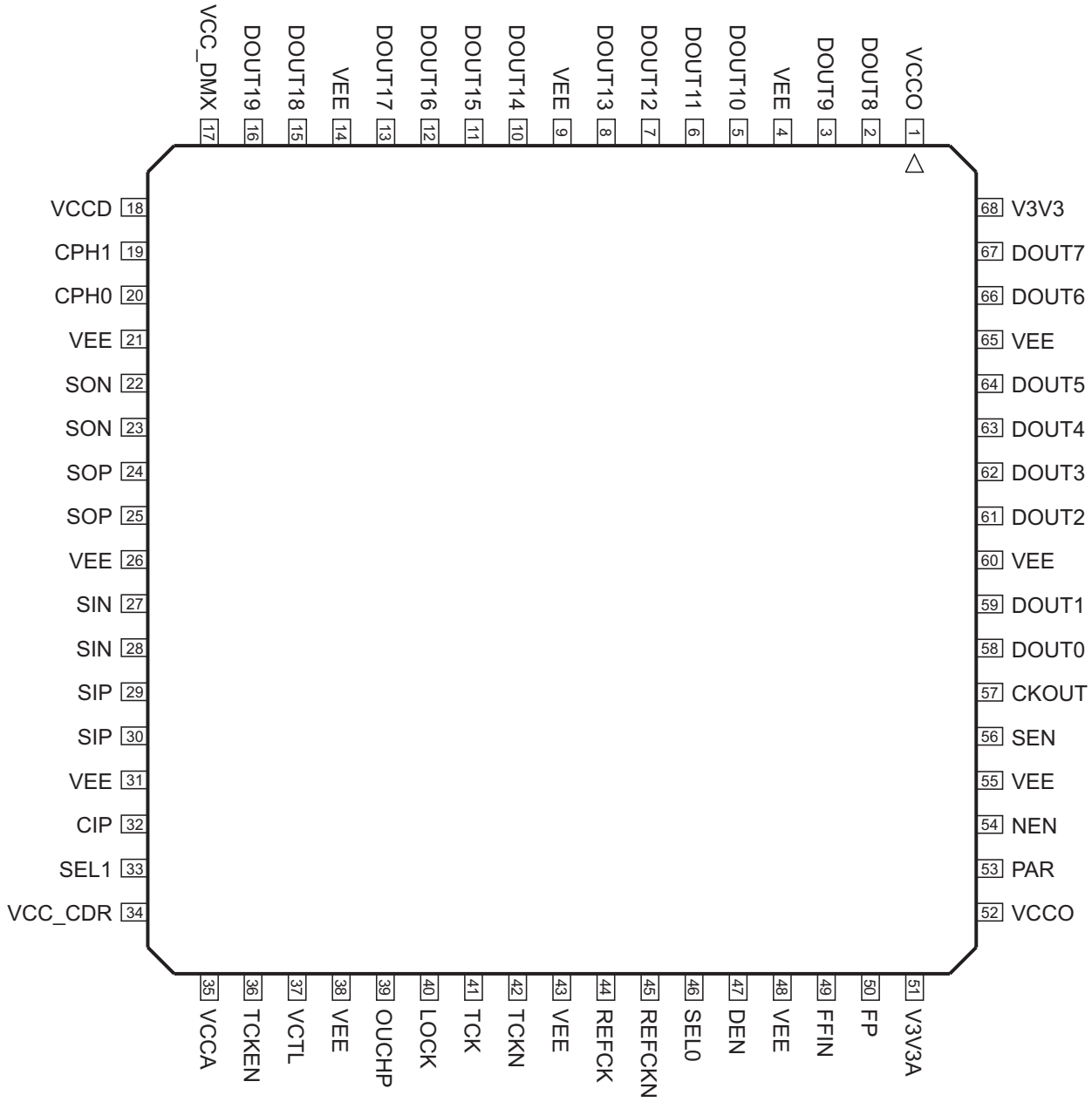


Figure 7. *Package 68 pin MLC, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{3V3} , V_{CC}	Positive Supply		V_{EE}-0.5		7	V
$V_{I\ max,CIP}$	Input Voltage for CIP		V_{EE}-0.5		V_{CC}+0.5	V
$I_{I\ max,CIP}$	Input Current for CIP		-1.0		3.0	mA
$V_{O\ max}$	Output Voltage		V_{EE}-0.5		V_{CC}+0.5	V
$I_{O\ max}$	Output Current				40	mA
$V_{I\ max}$	Input Voltage		V_{EE}-0.5		V_{CC}+0.5	V
$I_{I\ max}$	Input Current		-1.0		1.0	mA
T_O	Operating Temperature	Junction	-40		+125	°C
T_S	Storage Temperature		-65		+175	°C

Note: Temperature range specify only reliability regarding damage. Performance is only tested and quaranteed for the T_{CASE} as given below.

DC Characteristics

T_{CASE} = 0 °C to 70 °C, θ_{J-C} = 7 °C/W. Appropriate heat sinking is required.
All voltages in the table are referred to V_{EE}. V_{CC_CDR} = 5 V, V_{CC_DMX} = 5 V

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC} V_{CCA} V_{CCO}	5 V Supply Voltage		4.75	5.00	5.25	V
I_{CC}	Total current from V_{CC} , V_{CCA} , V_{CCO}			270		mA
V_{3v3}	3.3 V Core Supply Voltage		3.1	3.3	3.5	V
I_{3v3}	Current from V_{3v3}			350		mA
PD	Power Dissipation			2500		mW
$V_{C\ SIP/SIN}$	SIP/SIN Data Common Mode Voltage		V_{CC}-2.0		V_{CC}-0.5	V
$V_{I\ SIP/SIN}$	SIP/SIN Data Minimum Input Voltage SIP/SIN Data Maximum Input Voltage	Note 1		200	400 1000	mV_{P-P} mV_{P-P}
$V_{IIH\ TTL}$	TTL Input HI Voltage		2.0		4.0	V
$V_{IIL\ TTL}$	TTL Input LO Voltage				0.8	V
$I_{IH\ TTL}$	TTL Input HI Current	V_{IH} max			500	µA
$I_{IL\ TTL}$	TTL Input LO Current	V_{IL} min			-500	µA
$V_{OH\ TTL}$	TTL Output HI Voltage	Note 2	2.4			V
$V_{OL\ TTL}$	TTL Output LO Voltage	Note 2			0.5	V
$I_{OH\ SOP/SON}$	Open Collector Output HI Sink Current	Note 3	-20	-25	-30	mA
$I_{OL\ SOP/SON}$	Open Collector Output LO Sink Current	Note 3			-0.5	mA
V_{VCTL}	VCO Control Voltage	I_{VCTL}< 30 µA	0.5		V_{CC}-1.5	V
$I_{OH\ CPH}$	OUCHP Source Current (DC steady)	Note 4	500	1000		µA
$I_{OL\ CPH}$	OUCHP Sink Current (DC steady)	Note 4	-500	-1000		µA

Note 1: Data eye diagram in accordance with SMPTE292, terminated via loop-through to 75 Ω.
Note 2: R_{load} = 500 Ω to 1.4 V.
Note 3: R_{load} = 50 Ω to V_{CC}. Current into CIP=1 mA. Output logic level “1" corresponds to LO current.
Note 4: Output terminated to 2.5 V during test.

AC Characteristics

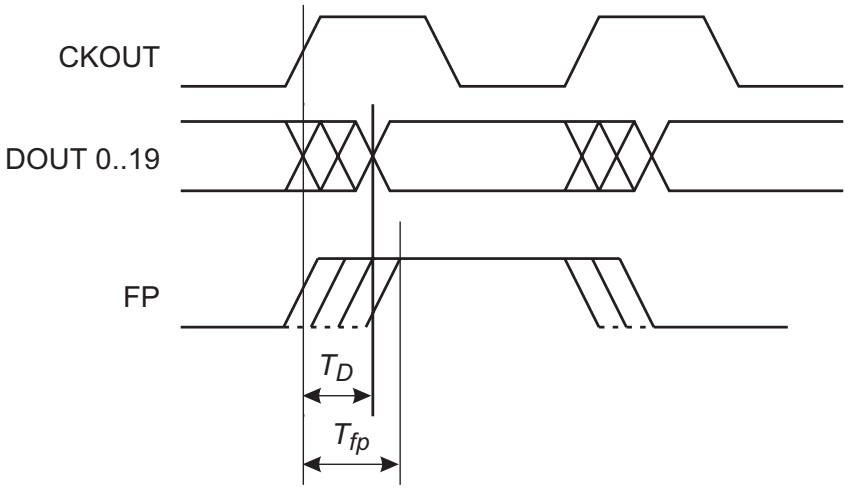


Figure 8. *Data Output Delay from CKOUT for CPH0/1 = 1,1*

T_{CASE} = 0 °C to 70 °C, V_{CC} = 5.0 V, V_{3V3} = 3.3 V

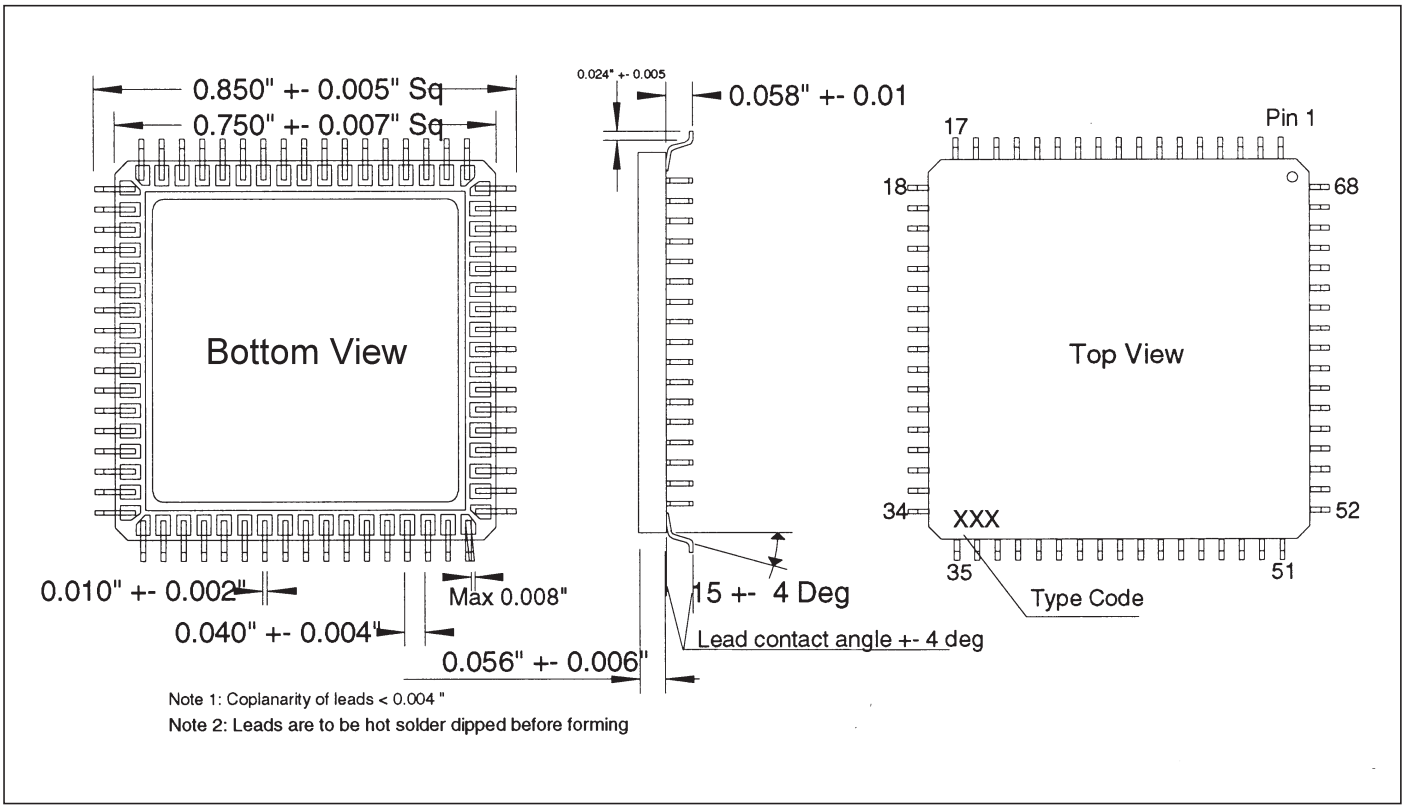
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Tol}	Jitter Tolerance	10Hz < F < 150MHz (Note1) 100kHz < F < 150MHz (Note1)	1.0 0.2			UI_{P-P} UI_{P-P}
J_{Trf}	Jitter Transfer	F < Loop bandwidth (Note 2)		0.1		dB
T_A	Acquisition Time	2^{23}-1 PRBS		5	50	µs
L_{CID}	Consecutive Identical Digits	# bits with no transitions	100			bits
D_C	Input Clock / REFCK Frequency Deviation	Note 3			±200	ppm
$C_{DUTY\ REFCK}$	REFCK Clock Duty Cycle	$V_{Thresh.}$= 1.4 V	40		60	%
$C_{DUTY\ CKOUT}$	Output Clock Duty Cycle	Note 4	45		55	%
$T_{TLH\ Clock}$	CKOUT Rise Time	20-80% (Note 4)		2000		ps
$T_{THL\ Clock}$	CKOUT Fall Time	80-20% (Note 4)		2000		ps
$T_{TLH\ Data}$	Output Data Rise Time	20-80% (Note 4)		2000		ps
$T_{THL\ Data}$	Output Data Fall Time	80-20% (Note 4)		2000		ps
T_D	DOUT from CKOUT	See figure	0	275		ps
T_{fp}	FP from CKOUT			1200		ps
$T_{TLH\ SON/SOP}$	SOP/SON Rise Time	1 m cable, 75 Ω load			270	ps
$T_{THL\ SON/SOP}$	SOP/SON Fall Time	1 m cable, 75 Ω load			270	ps
$N_{Serial\text{-}Parallel}$	no. of bits stored in pipe-lines		30		55	bits

Note 1: 1 UI = 673 ps; Measured according to RP184: Measurement of Jitter in Bit-Serial Digital Interfaces.
Note 2: Data Pattern 2^{23}-1 PRBS. Through careful filter design, loop peaking may be controlled which is the major contribute to Jitter Transfer.
Note 3: Maximum deviation between reference clock input and divided VCO clock when in lock.
Note 4: Threshold voltage = 1.4 V. Load = 500 Ω || 10pF to 1.4 V. For CKOUT Load = 500 Ω || 20 pF to 1.4 V.

Reference Standards

SMPTE 292M (May 7, 1996): Bit-Serial Digital Interface for HDTV.
SMPTE RP184 (December 1, 1996): Measurement of Jitter in Bit-Serial Digital Interfaces.

Package Outline



Ordering Information

To order, please specify as shown below:

Product Name:	Package Type:	Case Temperature Range:	Option:
GD14516A-68BA	68 pin Ceramic (MLC)	0..70 °C	

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