CD54/74HC4066
CD54/74HCT4066

High-Speed CMOS Logic

Quad Bilateral Switch

$V_{CC} = 14$
$GND = 7$

92CS-39851

FUNCTIONAL DIAGRAM

Type Features:

- *Wide analog-input-voltage range: 0-10 V*
- *Low "ON" resistance: 25 Ω @ V_{CC} = 4.5 V*
  15 Ω @ V_{CC} = 9 V
- *Fast switching and propagation delay times*
- *Low "OFF" leakage current*

The RCA CD54/74 HC/HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear "ON"-resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

The CD54HC4066 and CD54HCT4066 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4066 and CD74HCT4066 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Alternate Source: Phillps/Signetics*
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *CD54HC/CD74HC types:*
  2 V to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V & 10 V
- *CD54HCT/CD74HCT types:*
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
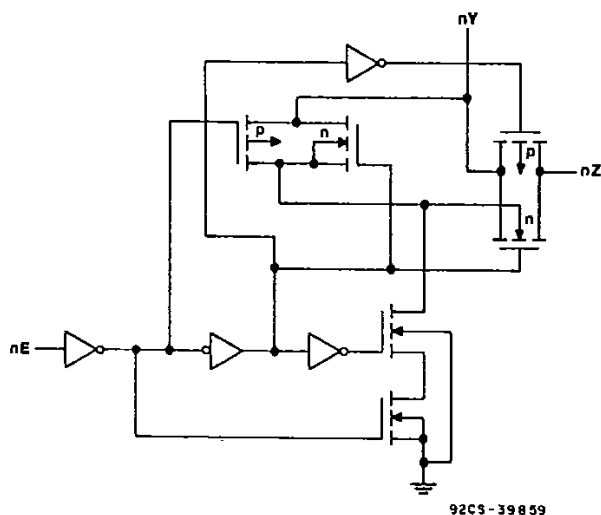 *CMOS input compatiblity*
  $I_1 \leq 1\ \mu A$ @ V_{OL}, V_{OH}

92CS-39859

Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

INPUT nE	SWITCH
L	off
H	on

H = HIGH Level
L = LOW Level

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
  (Voltages referenced to ground)
  HCT Types .... −0.5 to +7 V
  HC Types .... −0.5 to +10.5 V
DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < −0.5 V OR V_I > V_{CC} +0.5 V) .... ±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR V_O < −0.5 V OR V_O > V_{CC} +0.5 V) .... ±20 mA
• DC SWITCH CURRENT, I_O, (FOR V_I > −0.5 V OR V_I < V_{CC} + 0.5 V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
  For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
  For T_A = −55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
  For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
  For T_A = −40 to +70°C (PACKAGE TYPE M) .... 400 mW
  For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPE F, H .... −55 to +125°C
  PACKAGE TYPE E, M .... −40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
  Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
    with solder contacting lead tips only .... +300°C

• In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{on} values shown in the Electrical Characteristics Chart). No V_{CC} current will flow through R_L if the switch current flows into terminals 2, 3, 9 and 10.

```
1Y  — 1        14 — VCC
1Z  — 2        13 — 1E
2Z  — 3        12 — 4E
2Y  — 4        11 — 4Y
2E  — 5        10 — 4Z
3E  — 6         9 — 3Z
GND — 7         8 — 3Y
```

92CS - 39852
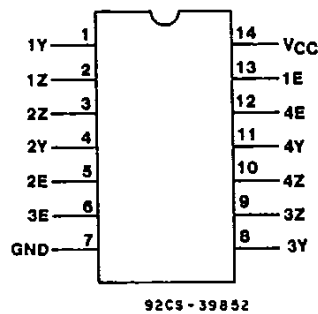
TERMINAL ASSIGNMENT

CD54/74HC4066
CD54/74HCT4066

RECOMMENDED OPERATING CONDITIONS: For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	10	V
CD54/74HCT Types	4.5	5.5	
DC Input Voltage, V_C, and Analog Switch Voltage, $V_{I/O}$	0	V_{CC}	
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f (Control Inputs)			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 9 V	0	250	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	HC CON-TROL V_I V	HC SW-ITCH V_{IS} V	HC V_{CC} V	74HC/54HC +25°C Min	Typ	Max	74HC -40/+85°C Min	Max	54HC -55/+125°C Min	Max	HCT CON-TROL V_I V	HCT SW-ITCH V_{IS} V	HCT V_{CC} V	74HCT/54HCT +25°C Min	Typ	Max	74HCT -40/+85°C Min	Max	54HCT -55/+125°C Min	Max	UNITS
High-Level Input Voltage V_{IH}	—	—	2	1.5	—	—	1.5	—	1.5	—	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—											
			9	6.3	—	—	6.3	—	6.3	—											
Low-Level Input Voltage V_{IL}	—	—	2	—	—	0.5	—	0.5	—	0.5	—	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35											
			9	—	—	2.7	—	2.7	—	2.7											
Input Leakage Current (Any Control) I_{IL}	V_{CC} or Gnd	—	10	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	—	5.5	—	—	±0.1	—	±1	—	±1	µA
Off-Switch Leakage Current I_Z	V_{IL}	V_{CC} or Gnd	10	—	—	±0.1	—	±1	—	±1	V_{IL}	V_{CC} or Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
"On" Resistance I_O = 1 mA (Fig. 2) R_{on}	V_{CC} or Gnd	V_{CC}	4.5	—	25	80	—	106	—	128	V_{CC} or Gnd	V_{CC}	4.5	—	25	80	—	106	—	128	Ω
			6	—	20	75	—	94	—	113			—	—	—	—	—	—	—	—	
			9	—	15	60	—	78	—	95			—	—	—	—	—	—	—	—	
	V_{CC} to Gnd	V_{CC}	4.5	—	35	95	—	118	—	142	V_{CC} to Gnd	V_{CC}	4.5	—	35	95	—	118	—	142	
			6	—	24	84	—	105	—	126			—	—	—	—	—	—	—	—	
			9	—	16	70	—	88	—	105			—	—	—	—	—	—	—	—	
"On" Resistance Between Any Two Switches ΔR_{on}	V_{CC}	—	4.5	—	1	—	—	—	—	—	V_{CC}	—	4.5	—	1	—	—	—	—	—	
			6	—	0.75	—	—	—	—	—			—	—	—	—	—	—	—	—	
			9	—	0.5	—	—	—	—	—			—	—	—	—	—	—	—	—	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	—	6	—	—	2	—	20	—	40	V_{CC} or Gnd	—	5.5	—	—	2	—	20	—	40	µA
			10	—	—	16	—	160	—	320											
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*	—	—	—	—	—	—	—	—	—	—	V_{CC}-2.1	—	4.5 to 5.5	—	100	360	—	450	—	490	µA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	1

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Time:	t_{PHL}	15	4	4	
Switch In to Out	t_{PLH}				ns
Switch Turn Off	t_{PHZ}, t_{PLZ}	15	12	14	
Switch Turn On	t_{PZH}, t_{PZL}	15	8	9	
Power Dissipation Capacitance*	C_{PD}	—	25	38	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o \quad \text{where:}$$

f_i = input frequency f_o = output frequency
C_L = load capacitance C_S = switch capacitance
V_{CC} = supply voltage

SWITCHING CHAARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time	t_{PLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Switch In to Out	t_{PHL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		9	—	8	—	—	—	11	—	—	—	13	—	—	
Switch Turn On Delay	t_{PZH}	2	—	100	—	—	—	125	—	—	—	150	—	—	
	t_{PZL}	4.5	—	20	—	24	—	25	—	30	—	30	—	36	ns
		9	—	12	—	—	—	15	—	—	—	18	—	—	
Switch Turn Off Delay		2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		9	—	24	—	—	—	30	—	—	—	36	—	—	
Input (Control) Capacitance	C_i	—	—	—	—	10	—	10	—	10	—	10	—	10	pF

T-51-11

CD54/74HC4066
CD54/74HCT4066

ANALOG CHANNEL CHARACTERISTICS - Typical Values at T_C = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 12)	Fig. 3 Notes 1 & 2		4.5	200	200	MHz
Cross Talk Between Any Two Switches (Fig. 13)	Fig. 4 Notes 2 & 3		4.5	-72	-72	dB
Total Harmonic Distortion	1 KHz, Fig. 5	V_{IS} = 4 Vpp	4.5	0.022	0.023	%
		V_{IS} = 8 Vpp	9	0.008	N/A	
Control to Switch Feedthrough Noise	Fig. 6		4.5	TBE	TBE	mV
			9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 13)	Fig. 7 Notes 2 & 3		4.5	-72	-72	dB
Switch Input Capacitance C_S	—		—	5	5	pF

Notes: 1. Adjust input level for 0 dBm at output, f = 1 MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS}.
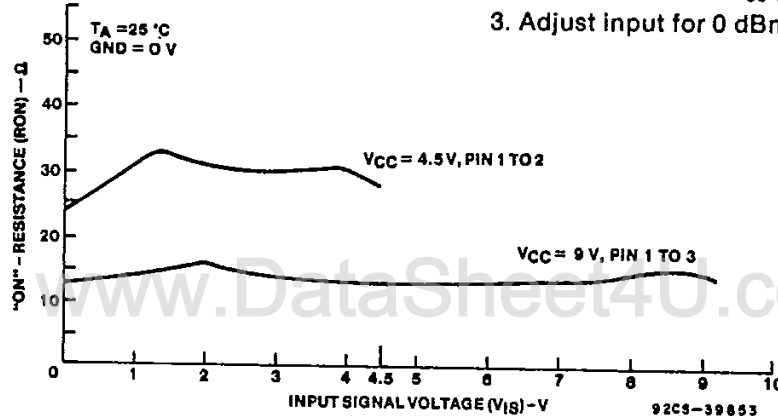
Fig. 2 - Typical "ON" resistance vs. input signal voltage.

ANALOG TEST CIRCUITS
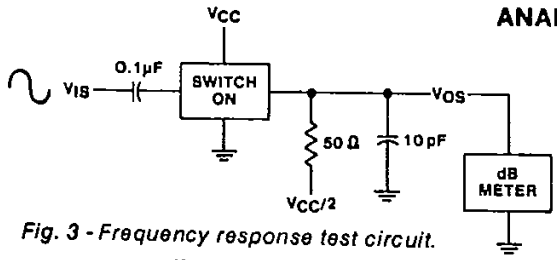
Fig. 3 - Frequency response test circuit.
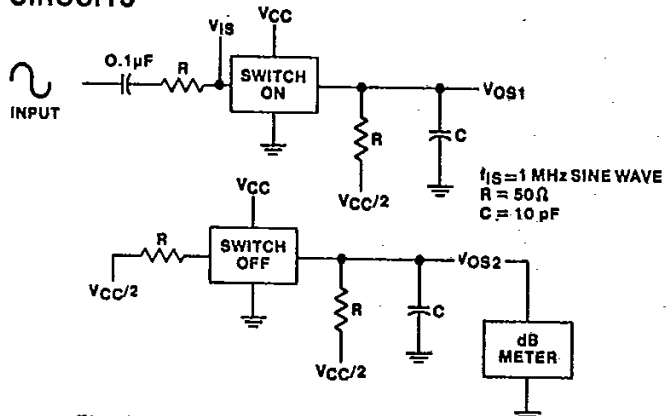
Fig. 4 - Crosstalk between two switches test circuit.
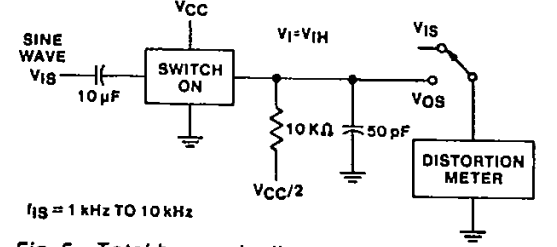
Fig. 5 - Total harmonic distortion test circuit.
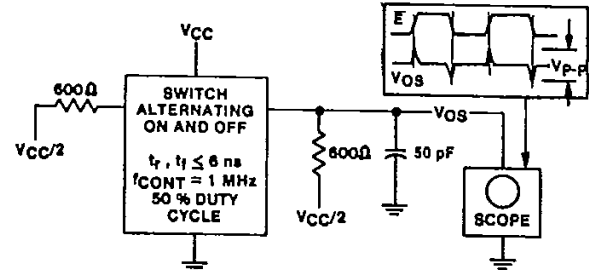
Fig. 6 - Control-to-switch feedthrough noise test circuit.
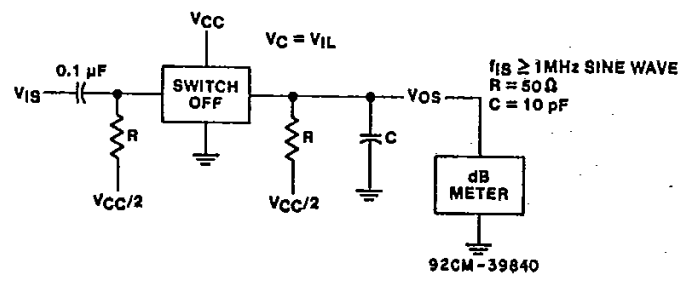
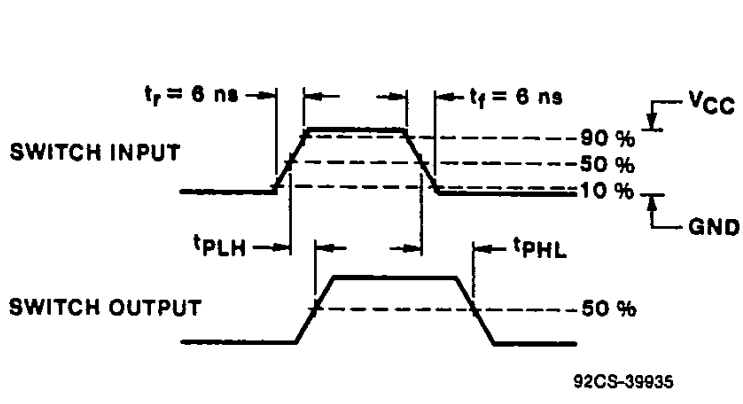Fig. 7 - Switch off signal feedthrough.
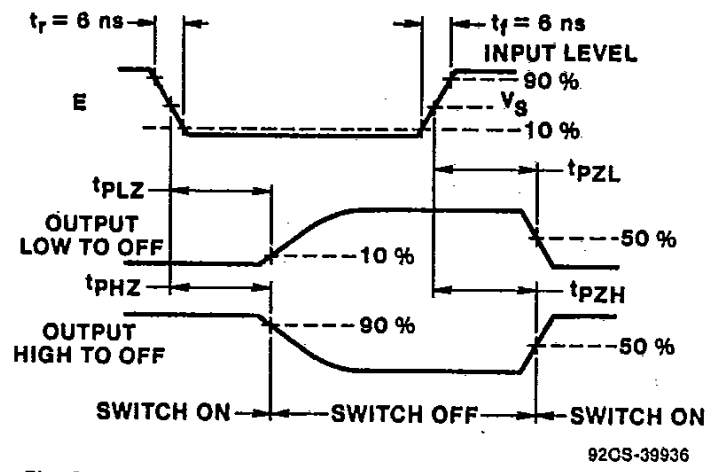
Fig. 8 - Switch propagation - delay times waveforms.

Fig. 9 - Switch turn-on and turn-off propagation delay times waveforms.

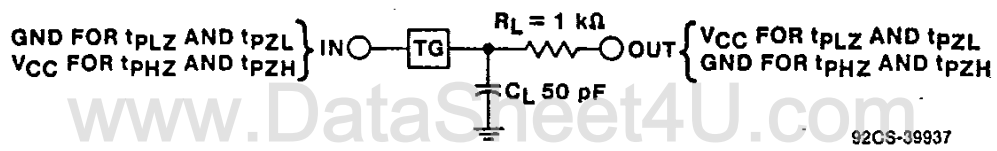|	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

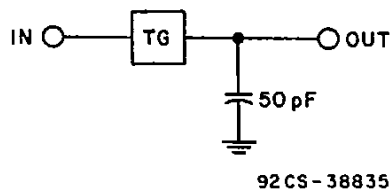Fig. 10 - Switch on/off propagation delay time test circuit.

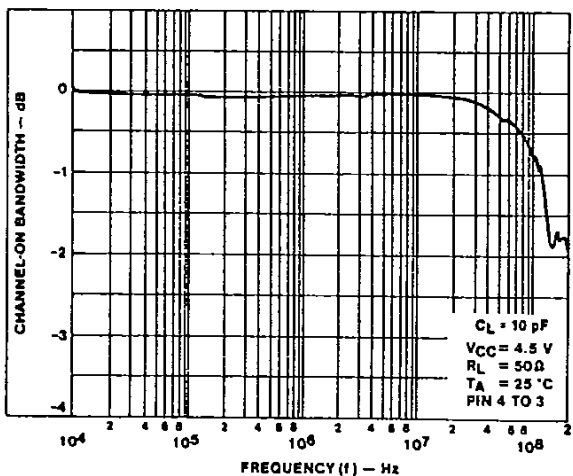Fig. 11 - Switch-in to switch-out propagation delay time test circuit.

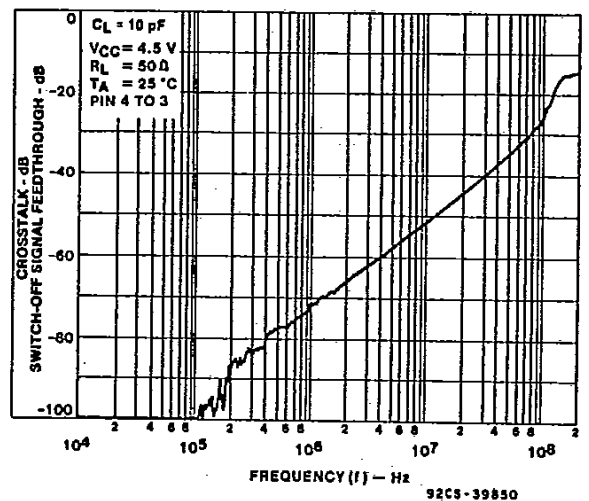Fig. 12 - Switch frequency response, V_{CC} = 4.5 V.

Fig. 13 - Switch-off signal feedthrough and crosstalk vs. frequency, V_{CC} = 4.5 V.