TWELVE (12) LVDT-TO-DIGITAL CONVERTERS
"PROGRAMMABLE" TRACKING CONVERTERS

FEATURES:

- 16-bit resolution
- 0.025% FS accuracy
- Continuous background BIT testing with Excitation and Signal loss detection
- **Self-calibrating. Does not require removal for calibration**
- 360 Hz to 10 kHz operation
- Autoranging input between 2.0 and 28 Vrms
- 12, 8, and 4-channel versions available
- Optional programmable reference excitation
- Transformer isolated
- LATCH feature
- Compensates for ±60° phase shift
- No adjustments or trimming required
- Part Number, S/N, Date Code, and Revision in permanent memory

DESCRIPTION:

This high-density intelligent DSP-based card incorporates up to twelve (12) separate transformer isolated programmable LVDT/RVDT-to-Digital tracking converters with extensive diagnostics, and optional programmable excitation supply. Instead of buying cards that are set for specific inputs, the uniqueness of this design makes it possible to order our standard card that auto-ranges between 2.0 and 28 volts. Operating frequency between 400 Hz and 10 kHz can be specified. Each chanel is programmable for either 2 wire or 3,4 wire inputs. For 2 wire inputs, the output is computed as A/B (where A is the LVDT output and B is the excitation) and is expressed as % FS. For 3 or 4-wire devices, the output is computed as A-B/A+B and is expressed as %FS. This ratiometric technique assures that the output will change only when the LVDT position changes and will ignore excitation voltage variations. The LATCH feature permits the user to read all channels at the same time. Reading will unlatch that channel. The converters utilize a Type II servo loop processing technique that enables tracking, at full accuracy, up to the specified maximum rate. Intermediate transparent latches, on all data and velocity outputs, guarantee that current valid data is always available for any channel, without affecting the tracking performance of the converters. The optional on–board excitation is field programmable. To simplify logistics, Part Number, S/N, Date Code, and Revision are stored in permanent memory locations.

This board incorporates major diagnostics that offer substantial improvements to system reliability because user is alerted to channel malfunction. Three different tests (one on-line and two off-line) can be selected**:**

The D2 Test initiates automatic background BIT testing. Each channel is checked over the programmed Signal range to a measuring accuracy 0.1% FS, and each Signal and Excitation is monitored. Results are available in registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test**,** if enabled, starts an initiated BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.1%FS. External excitation is not required. Results can be read from registers. The testing requires no external programming and can be initiated or terminated via the bus.

The D0 Test is used to check the card and the PCbus interface. All channels are disconnected from the outside world, allowing the user to write any number of input positions to the card and then read the data from the interface. External excitation is not required.

SPECIFICATIONS:

Number of channels:	4, 8, or 12 (see part number)
Resolution:	16-bit
Accuracy:	0.025% FS
Bandwidth:	10% of excitation to 100 Hz max. BW and tracking rate can easily be customized**.**
Input format:	LVDT or RVDT
Input voltage	Autoranging from 2.0 to 28 Vrms. Transformer isolated.
Excitation voltage:	Not required for computation of output but should be connected to allow card to check for excitation loss.
Input Impedance:	40 kΩ min. at 360 Hz
Frequency:	Specify between 360 Hz to 10 kHz, (See Part Number)
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and output up to ±60° (3 or 4-wire units ignore phase shift)
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Power:	+ 5 VDC at 0.35 A ±12 VDC at 0.1 A without Excitation; 1.1 A for 5 VA Excitation Output
Temperature, operating:	0°C to +70°C
Storage temperature:	-45°C to +85°C.
Weight:	20 oz.

EXCITATION:	**Optional** (See part number).
Voltage:	2.0-28 Vrms programmable (resolution 0.1 Vrms) or 115 Vrms fixed. Accuracy ±2%.
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max., no load to full load.
Output power:	5 VA max. at 40° min. inductive.

Principals of LVDT Operation : Typically, the LVDT primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center, the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

Interfacing the LVDT to the Converter

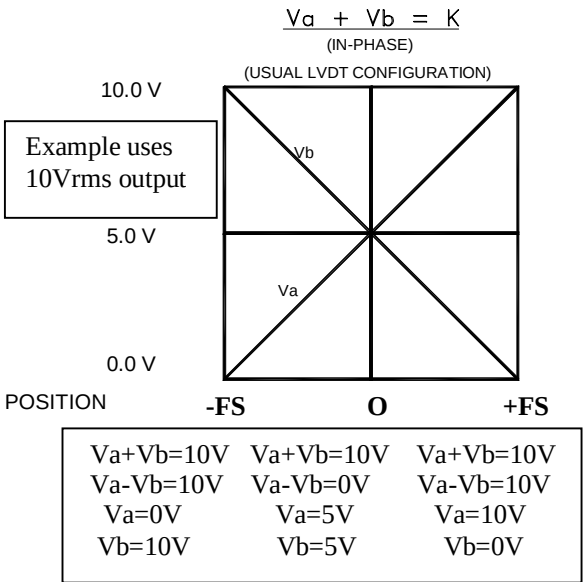
Two common connection methods are:

1. Primary as reference (two-wire system)

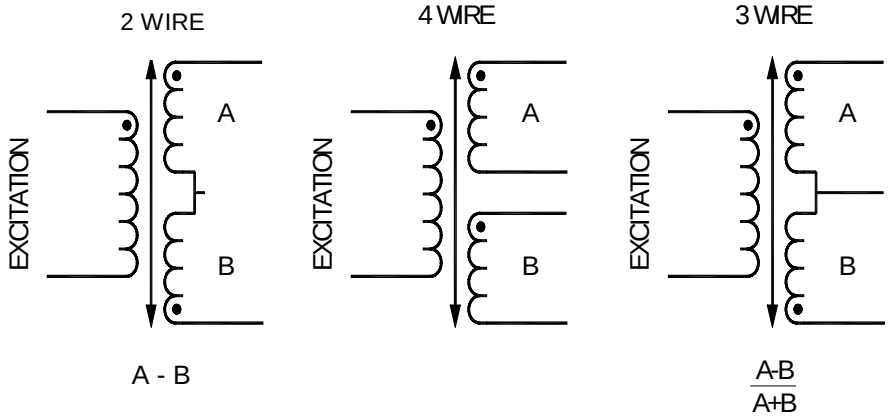
   This method of connection converts the widest range of LVDT sensors and. is the most sensitive to excitation voltage variations, as well as temperature and phase shift effects.

2. Derived reference (three/four-wire LVDT)

   The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement. This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B)/(A+B)



Various LDVT configurations



LVDT Connections:

For 3,4 Wire LVDT's, connect A and B LVDT outputs to Signal A and B inputs. Excitation is not used but should be connected to enable card to sense and report any excitation loss.
For 2 Wire LVDT's, connect A-B output of LVDT to card "A" input and connect external excitation voltage to card "B" input and excitation input.

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:
This card requires 32 consecutive addresses in the I/O address space on a 32 byte boundary. The base address is switch settable in the 000-3E0 hex (0 to 992) address range.

ADDRESS= BASE + OFFSET

BASE	A9	A8	A7	A6	A5	OFFSET	A4, A3, A2, A1, A0	Decimal equiv.
						SW1*		32
						SW2*		64
						SW3*		128
						SW4*		256
						SW5*		512

* "1" = Off "0" = On

NOTE: Base addresses to avoid:

378-37F Parallel Printer Port	3B0-3BF Monochrome Display	3F8-3FF	Asynch Comm	3F0-3F7	Floppy Disk

Page 1 (Offset 1E = 0)

00	Ch.1Lo	read	07	Ch.4 Hi	read	0E	Ch. 8 Lo	read	15	Ch.11 Hi	read	1C	Status, Test Lo	read
01	Ch.1 Hi	read	08	Ch.5 Lo	read	0F	Ch. 8 Hi	read	16	Ch.12 Lo	read	1D	Status, Test Hi	read
02	Ch.2 Lo	read	09	Ch.5 Hi	read	10	Ch. 9 Lo	read	17	Ch.12 Hi	read	1E	Page register = 0	write
03	Ch.2 Hi	read	0A	Ch.6 Lo	read	11	Ch. 9 Hi	read	18	Status, Signal loss Lo	read			
04	Ch.3 Lo	read	0B	Ch.6 Hi	read	12	Ch.10 Lo	read	19	Status, Signal loss Hi	read			
05	Ch.3 Hi	read	0C	Ch.7 Lo	read	13	Ch.10 Hi	read	1A	Status, Exc. Loss Lo	read			
06	Ch.4Lo	read	0D	Ch.7 Hi	read	14	Ch.11 Lo	read	1B	Status, Exc. Loss Hi	read			

Page 2 (Offset 1E = 1)

00	Sig. Ch.1 Lo	write/read	07	Sig. Ch.4 Hi	write/read	0E	Sig. Ch.8 Lo	write/read	15	Sig. Ch.11 Hi	write/read
01	Sig. Ch.1 Hi	write/read	08	Sig. Ch.5 Lo	write/read	0F	Sig. Ch.8 Hi	write/read	16	Sig. Ch.12 Lo	write/read
02	Sig. Ch.2 Lo	write/read	09	Sig. Ch.5 Hi	write/read	10	Sig. Ch.9 Lo	write/read	17	Sig. Ch.12 Hi	write/read
03	Sig. Ch.2 Hi	write/read	0A	Sig. Ch.6 Lo	write/read	11	Sig. Ch.9 Hi	write/read	1E	Page register = 1	write
04	Sig. Ch.3 Lo	write/read	0B	Sig. Ch.6 Hi	write/read	12	Sig. Ch.10 Lo	write/read			
05	Sig. Ch.3 Hi	write/read	0C	Sig. Ch.7 Lo	write/read	13	Sig. Ch.10 Hi	write/read			
06	Sig. Ch.4 Lo	write/read	0D	Sig. Ch.7 Hi	write/read	14	Sig. Ch.11 Lo	write/read			

Page 6 (Offset 1E = 5)

00	(A+B) Ch.1 Lo	read	07	(A+B) Ch.4 Hi	read	0E	(A+B) Ch.8 Lo	read	15	(A+B) Ch.11 Hi	read
01	(A+B) Ch.1 Hi	read	08	(A+B) Ch.5 Lo	read	0F	(A+B) Ch.8 Hi	read	16	(A+B) Ch.12 Lo	read
02	(A+B) Ch.2 Lo	read	09	(A+B) Ch.5 Hi	read	10	(A+B) Ch. 9 Lo	read	17	(A+B) Ch.12 Hi	read
03	(A+B) Ch.2 Hi	read	0A	(A+B) Ch.6 Lo	read	11	(A+B) Ch. 9 Hi	read	1E	Page register = 5	write
04	(A+B) Ch.3 Lo	read	0B	(A+B) Ch.6 Hi	read	12	(A+B) Ch.10 Lo	read			
05	(A+B) Ch.3 Hi	read	0C	(A+B) Ch.7 Lo	read	13	(A+B) Ch.10 Hi	read			
06	(A+B) Ch.4 Lo	read	0D	(A+B) Ch.7 Hi	read	14	(A+B) Ch.11 Lo	read			

Page 7 (Offset 1E = 6)

00	Enable, Test	write/read	07	Test position Hi	read/write	0C	Eo Lo byte	read/write	0F	Active Ch. Hi	read/w
02	Test (D2) verify	write/read	0A	Freq. Lo byte	read/write	0D	Eo Hi byte	read/write	10	2or 3,4 wire input	
06	Test position Lo	read/write	0B	Freq. Hi byte	read/write	0E	Active Ch. Lo	read/write	14	Latch	write
									1E	Page register = 6	write

Page 8 (Offset 1E = 7)

00	Save	write	0F	P/N Hi	read	11	Date code Hi	read	13	Rev. level Hi	read	15	S/N Hi	read
0E	P/N	read	10	Date code Lo	read	12	Rev. level Lo	read	14	S/N Lo	read	1E	Page register = 7	

	Hi byte								Lo byte							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Active channels	X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, signal	X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, excitation	X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
2 or 3,4 wire Input	X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

At **Power-On** or **System Reset**, all parameters are restored to last saved setup.

Enter Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel Register at page 7, 0Eh/0Fh. “1”=active; “0”=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to the Save Register at page 8, 00/01h. This location will automatically clear to 00/01h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.

To restore factory shipped parameters, write AAAAh to the Save Register at page 8, 00/01h, followed by System Reset. Note: After a SAVE or RESTORE, poll page 8, 00h and do not perform any other operation until word is at "0".

Data Format: The output data is A-B/A+B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Signal and Reference

The LVDT primary is energized by either the on-board excitation or from an external excitation. The 4-wire or 3-wire LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs no scaling is required because the inputs are autoranging, however the Signal registers can be used to scale the output code.

Default settings for the Signal Registers at page 2 are FFFFh. This results in a full scale output reading for full travel of the LVDT. A full scale output reading for less than full travel of the LVDT can be programmed by writing to the Signal Registers on page 2. For example, writing 8000h to page 2, 00/01h will result in channel 1 having a full scale output reading for one-half travel of the LVDT.
For 2 wire Inputs, the Signal register can be used to adjust what fraction of the excitation voltage represents "full travel" of the LVDT.

Optional Reference Supply: For frequency, write a 16-bit word (ex: 400 Hz = 1 1001 0000) at Page 7, OAh/OBh. For voltage, write a word (ex: 26.1 Vrms = 1 0000 0101) with LSB = 0.1 Vrms, to address Page 7, OCh/ODh . It is recommended that the user program the required frequency before setting the output voltage.

Selecting 2 or 3,4 Wire operation: Program the proper channel in the appropriate register on page 7,10h. Logic 1 = 2 wire and logic 0 = 3,4 wire.

Read (A+B) output: Read binary number at appropriate register on page 6, and multiply by 0.01 Volt. For 2 wire Inputs, this represents the B voltage.

Latch: All channels may be latched by writing "1" to D1 at Page 7, 14h. Reading channel will disengage latch.

D2 Test Enable: Writing "1" to D2 at page 7, 00h initiates automatic background BIT testing. Each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS, and each Signal and Excitation is monitored. The results are available in Status Registers. The testing is totally transparent to the user,
requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. The card will write 55h to page 7, 02h when D2 is enabled. User can periodically clear to 0000h and then read page 7, 02h again, after 30 seconds, to verify that background BIT testing is activated.

Status, Test: Check the corresponding bit of the Test Status Register at page 1, 1Ch/1Dh for status of BIT testing for each active channel. A "1" = Accuracy OK; "0" = failed. (test cycle takes 45 seconds for accuracy error).

Status, Exc: Check the corresponding bit of the Exc Status Register at page 1, 1AH/1Bh for status of the excitation input for each active channel. A "1" = Exc. ON, "0" = Exc. Loss (Excitation loss is detected after 2 seconds).

Status, Sig: Check the corresponding bit of the Sig Status Register at page 1, 18h/19h for status of the input signals for each active channel. A "1" = Signal ON, "0" = Signal loss (Signal loss is detected after 2 seconds).

D3 Test Enable: Writing "1" to D3 of Test Register at page7, 00h, initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple test voltages that are measured to a test accuracy of 0.1%FS. Test cycle takes about 45 seconds and results can be read from the Status Registers when D3 changes from "1" to "0". External excitation is not required. Testing requires no external programming and can be initiated or terminated (by setting D3 to "0") via the bus.

D0 Test Enable: Checks the card and the PCbus interface. Writing "1" to D0 at page 7, 00h disconnects all channels from the outside world, allowing user to write any number of input positions to the card at page 7 06/07h and then read the data from the PCbus interface (allow 400 ms after writing). External excitation is not required.
NOTE: The DO test will follow the program of channel 1: if channel 1 is programmed for 2 wire, then all channels will be tested in the 2 wire mode. If channel 1 is programmed for 3,4 wire, then all channels will be tested in the 3,4 wire mode.
If the card is set up as a mix of 2 and 3,4 wire channels, then chan 1 must be set as 2 wire (and all channels will be tested with the appropriate channels passing) and then chan 1 set as 3,4 wire (and all channels will be tested with the appropriate channels passing).

Front panel Connector: J1

AMP 748483-5 Mate: AMP 748368-1

Pin	Ch.1	Pin	Ch.2	Pin	Ch.3	Pin	Ch.4	Pin	Ch.5	Pin	Ch.6	Pin	Ch.7	Pin	Ch.8	Pin	Ch.9	Pin	Ch.10
39	Sig. A Lo	18	Sig. A Lo	36	Sig. A Lo	15	Sig. A Lo	33	Sig. A Lo	12	Sig. A Lo	30	Sig. A Lo	9	Sig. A Lo	27	Sig. A Lo	6	Sig. A Lo
78	Sig. A Hi	57	Sig. A Hi	75	Sig. A Hi	54	Sig. A Hi	72	Sig. A Hi	51	Sig. A Hi	69	Sig. A Hi	48	Sig. A Hi	66	Sig. A Hi	45	Sig. A Hi
58	Sig. B Hi	76	Sig. B Hi	55	Sig. B Hi	73	Sig. B Hi	52	Sig. B Hi	70	Sig. B Hi	49	Sig. B Hi	67	Sig. B Hi	46	Sig. B Hi	64	Sig. B Hi
19	Sig. B Lo	37	Sig. B Lo	16	Sig. B Lo	34	Sig. B Lo	13	Sig. B Lo	31	Sig. B Lo	10	Sig. B Lo	28	Sig. B Lo	7	Sig. B Lo	25	Sig. B Lo
38	Exc. Hi	17	Exc. Hi	35	Exc. Hi	14	Exc. Hi	32	Exc. Hi	11	Exc. Hi	29	Exc. Hi	8	Exc. Hi	26	Exc. Hi	5	Exc. Hi
77	Exc. Lo	56	Exc. Lo	74	Exc. Lo	53	Exc. Lo	71	Exc. Lo	50	Exc. Lo	68	Exc. Lo	47	Exc. Lo	65	Exc. Lo	44	Exc. Lo

Pin	Ch.11	Pin	Ch.12	Pin	
24	Sig. A Lo	3	Sig. A Lo	59	Latch +
	Sig. A Hi	42	Sig. A Hi	20	Latch-
43	Sig. B Hi	61	Sig. B Hi	1 & 40	Chassis
4	Sig. B Lo	22	Sig. B Lo	21	Int. Exc. Out Hi
23	Exc. Hi	2	Exc. Hi	60	Int. Exc. Out Lo
62	Exc. Lo	41	Exc. Lo		

Do not connect to any undesignated pins.

CAUTION: The male mating connector can have dangerous voltages on the pins. Be certain that power is turned off before removing the connector.

Code Table

Code	Frequency (Hz)	Notes
01	400	
02	2.8k - 3.2k	
03	2k	
04	2.69k	
05	3k	

PART NUMBER DESIGNATION

77LD1 - XX X X X X - XX

TOTAL NUMBER OF CHANNELS
04 = 4 Channels
08 = 8 Channels
12 = 12 Channels

ENVIRONMENTAL
C = No Conformal Coating
K = Removable Conformal Coating

ISA BUS
1 = 8-Bit ISA Bus
2 = 16-Bit ISA Bus

CODE (See Code Table)

OPTIONS
0 = None
9 = Custom Design (See Separate Spec)

EXCITATION

With On-Board Excitation Supply:
1 = One Common Excitation Input Tied to the Excitation Supply
2 = Individual Excitation Inputs

Without On-Board Excitation Supply
3 = One Common Excitation Input
4 = Individual Excitation Inputs