PCI 9050

August 31, 1996
VERSION 1.0

PCI Bus Target Interface Chip for
Low Cost Adapters

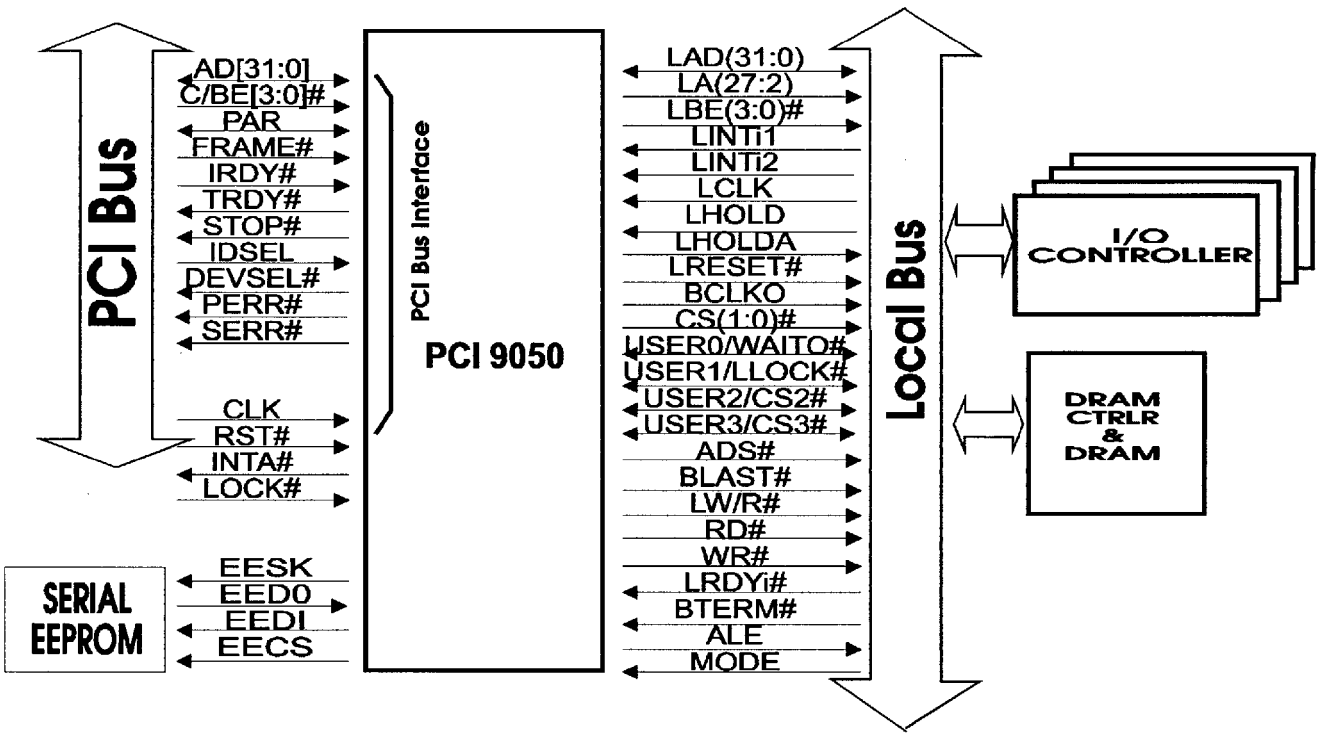
Features

- PCI Specification 2.1 Compliant Target Interface Chip supporting low cost slave adapters. Allows simple conversion of ISA adapters to PCI.
- Up to five local bus address spaces and four chip selects
- Bi-directional FIFO for zero wait-state burst operation
- PCI Bus transfers up to 132 MBytes/sec
- Supports multiplexed and non-multiplexed 32, 16, or 8 bit generic local buses.
- Local bus runs asynchronously to the PCI clock.
- Supports Big/Little Endian byte conversion.
- Low power CMOS in 160Pin Plastic QFP Package

General Description

The PCI 9050 provides a compact high performance PCI bus target (slave) interface for adapter boards. The PCI 9050 was designed to connect a wide variety of local bus designs to the PCI bus and to allow relatively slow local bus designs to achieve 132 Mbytes/sec burst transfers on the PCI bus.

The PCI 9050 can be programmed to connect directly to either the multiplexed or non-multiplexed 8, 16, or 32 bit local bus. The 16 bit mode enables easy conversion of ISA designs to PCI.
The PCI 9050 contains a bi-directional FIFO to speed match the 32 bit wide, 33 MHz PCI bus to a local bus which may be narrower or slower. Up to five local address spaces and up to four chip selects are supported.



PLX Technology, Inc., 390 Potrero Avenue, Sunnyvale, CA 94086 (408) 774-9060 FAX (408) 774-2169

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SECTION 1 - PCI 9050 GENERAL DESCRIPTION

The PCI 9050 is a PCI Specification 2.1 compliant PCI bus target interface chip that connects a PCI host bus to either an 8, 16 or 32 bit local bus which may be either multiplexed or non-multiplexed. The bus width is selected through the configuration registers. The multiplexed/non-multiplexed option is selected through the MODE pin.

Major Features

Direct slave (Target) data transfer mode. The PCI 9050 supports both memory mapped and I/O mapped burst accesses from the PCI bus to the local. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus. The PCI bus is always bursting, but the local bus can be set to either bursting or continuous single cycle.

Interrupt generator. The PCI 9050 can generate a PCI interrupt from two local bus interrupt inputs.

Clock. The PCI 9050 local bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock allowing the local bus to run at an independent rate from the PCI clock. The buffered PCI bus clock(BCLKo) may be connected to the local bus clock(LCLK).

Programmable local bus configurations The PCI 9050 supports 8, 16, or 32 bit local buses which may be either multiplexed or non-multiplexed. The PCI 9050 has four byte enables(LBE[3:0]), 26 address lines(LA[27:2]), and 32/16/8 data lines(LAD[31:0]).

Bus drivers. All control, address, and data signals generated by the PCI 9050 directly drive the PCI bus and the Local bus, without requiring any external drivers.

Serial EEPROM interface. The PCI 9050 contains an optional serial EEPROM interface which can be used to load configuration information. This is useful for loading information which is unique to a particular adapter (e.g. Network ID, Vendor ID, chip selects, etc.).

Four local chip selects The PCI 9050 provides up to four local chip selects. The base address and range of each chip select are independently programmable from the EEPROM or the host.

Five local address spaces The base address and range of each local address space are independently programmable from the EEPROM or the host.

Big/little endian byte swapping The PCI 9050 supports Big and Little Endian byte ordering. The PCI 9050 also supports Big Endian byte lane mode to redirect the current word/byte lane during 16/8 bit local bus operation.

Read/Write strobe delay and Write Cycle Hold The Read and Write (RD# and WR#) signals can be delayed from the beginning of the cycle for legacy interfaces(such as ISA bus).

Local Bus Wait States In addition to the LRDYi# (local ready input) handshake signal for variable wait state generations, the PCI 9050 has an internal wait state(s) generator(R/W address to data, R/W data to data, and R/W data to address).

Programmable Prefetch Counter The local bus prefetch counter can be programmed for 0(no prefetch), 4, 8, 16, or continuous(prefetch counter turned off) prefetch mode. The prefetched data can be used as cached data if a consecutive address were used (must be Lword aligned).

Delayed Read Mode The PCI 9050 supports PCI Specification 2.1 Delayed Read with "PCI Read with Write Flush Mode", "PCI Read No Flush Mode", "PCI Read No Write Mode", and "PCI Write Mode".

PCI Read/Write request time out timer The PCI 9050 has a programmable PCI Target Retry Delay timer, which, when expires generates a RETRY to the PCI bus.

PCI LOCK mechanism The PCI 9050 supports PCI target LOCK sequences. A PCI master can obtain exclusive access to the PCI 9050 device by locking to the PCI 9050.

2. SECTION 2 - BUS OPERATION

2.1 PCI BUS CYCLES

The PCI 9050 is PCI Specification 2.1 Compliant.

2.1.1 PCI Target Command Codes

As a target, the PCI 9050 allows access to the PCI 9050 internal registers and the local bus using the following commands:

Command Type	Code(C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All read or write accesses to the PCI 9050 can be byte, word, or long word accesses. All memory commands are aliased to the basic memory commands. All I/O accesses to the PCI 9050 are decoded to a long word boundary. The byte enables are used to determine which bytes are read from or written to. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.2 LOCAL BUS CYCLES

2.2.1 Local Bus Slave

Not supported No Direct Master capability. The internal registers are not readable/writable from the local side. The internal registers are accessible from the Host CPU on the PCI bus or from the serial EEPROM.

2.2.2 Local Bus Master

The PCI 9050 is the master of the local bus.

2.2.2.1 Ready/Wait State Control

If the READY input is disabled, the external READY input has no effect on wait states for a local access. Wait states between address to data, data to data, and data to address cycles are generated internally by a wait state counter. The wait state counter i initialized with its configuration register value at the start of each data access.

If the READY input is enabled, the READY input has no effect until the wait state counter is 0. The READY input then controls the number of additional wait states.

The BTERM input is not sampled until the wait state counter is 0.

2.2.2.2 Burst Mode and Continuous Burst Mode (BTERM "Burst Terminate" mode)

Burst Mode. If Bursting is enabled and the BTERM input is not enabled, the PCI 9050 bursts as follows: Bursting can start on any boundary and continue up to an address boundary as described below. After the data at the boundary has been transferred, the PCI 9050 generates a new address cycle (ADS#).

32 bit bus: 4 Lwords or up to a quad Lword boundary (LA3,LA2 = 11)
16 bit bus: 4 words or up to a quad word boundary (LA2,LA1 = 11)
8 bit bus: 4 bytes or up to a quad byte boundary (LA1,LA0 = 11)

Continuous Burst Mode (Bterm "Burst Terminate" mode)
BTERM mode enables the PCI 9050 to perform long bursts to devices that can accept longer than 4 Lword bursts. The PCI 9050 generates one address cycle and then continues to burst data. If a device requires a new address cycle after a certain address boundary, it can assert the BTERM# input to cause the PCI 9050 to generate a new address cycle. The BTERM# input is a ready input that acknowledges the current data transfer and requests that a new address cycle be generated (ADS#). The address will be for the next data transfer. If BTERM mode is enabled, the PCI 9050 asserts BLAST# only if its FIFOs become FULL/EMPTY or a transfer is complete.

Partial Lwords Accesses. Lword accesses in which not all byte enables are asserted are broken into single address and data cycles.

Bus Region Descriptor Register Bits		Result
Burst Enable	Bterm Enable	(Number of transfers)
0	0	Single Cycle. (Default)
0	1	Single Cycle.
1	0	Burst Mode: burst 4 Lwords at a time.
1	1	Continuous Burst Mode: burst until BTERM# input is asserted (see above descriptions)

2.2.2.3 Recovery States
In the non-multiplexed mode, the PCI 9050 uses the NXDA (data to address wait states) value in the bus region descriptor register to determine how many recovery states to insert between the last data transfer and the next address cycle. This value can be programmed to between 0 and 3 clock cycles.

In the multiplexed mode, the PCI 9050 inserts a minimum of one recovery state between the last data transfer and the next address cycle. Additional recovery states can be added by programming values greater than 1 into the NXDA bits of the bus region descriptor register.

2.2.2.4 Direct Slave Write Access to 8 and 16 bit bus
For direct slave writes/reads, only the bytes specified by a PCI bus master are written/read. An access to an 8 or 16 bit bus results i the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded to provide local address bits [LA1:LA0].

A Direct PCI access to an 8 bit bus with non-adjacent byte enables in a PCI Lword must not be used. Non-adjacent byte enables cause an incorrect [LA1:LA0] address sequence when bursting to memory. Therefore, for each Lword written to an 8 bit bus, the PCI 9050 does not write data after the first gap. Direct PCI accesses to an 8 bit bus with non-adjacent byte enables are not terminated with a Target Abort.

Therefore, for non-adjacent bytes(illegal byte enables), the PCI master must perform single cycles.

2.2.2.5 Local Bus Little/Big Endian
The PCI bus is a Little Endian bus, where data is longword aligned to the lowermost byte lane. Byte 0 (address 0) appears in AD[07:00], Byte 1 appears in AD[15:08], Byte 2 appears in AD[23:16], and Byte 3 appears in AD[31:24].

The PCI 9050 local bus can be programmed to operate in Big or Little Endian mode. In Big Endian mode, the PCI 9050 transposes the data byte lanes. Data is transferred as follows:

32 bit local bus
Data is longword aligned to the upper most byte lane. Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16], Byte 2 appears on Local Data [15:8] and Byte 3 appears on Local Data [7:0].

16 bit local bus
For a 16 bit local bus, the PCI 9050 can be programmed to use the upper or lower word lane. Byte lanes and burst order are as follows:

upper word lane transfer
1st transfer: Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16]
2nd transfer: Byte 2 appears on Local Data [31:24], Byte 3 appears on Local Data [23:16]

lower word lane transfer
1st transfer: Byte 0 appears on Local Data [15:8], Byte 1 appears on Local Data [7:0]
2nd transfer: Byte 2 appears on Local Data [15:8], Byte 3 appears on Local Data [7:0]

8 bit local bus
For an 8 bit local bus, the PCI 9050 can be programmed to used the upper or lower byte lane. Byte lanes and burst order are as follows:

upper byte lane transfer
1st transfer: Byte 0 appears on Local Data [31:24]
2nd transfer: Byte 1 appears on Local Data [31:24]
3rd transfer: Byte 2 appears on Local Data [31:24]
4th transfer: Byte 3 appears on Local Data [31:24]

lower byte lane transfer
1st transfer: Byte 0 appears on Local Data [7:0]
2nd transfer: Byte 1 appears on Local Data [7:0]
3rd transfer: Byte 2 appears on Local Data [7:0]
4th transfer: Byte 3 appears on Local Data [7:0]

For each of the following transfer types, the PCI 9050 Local bus can be independently programmed to operate in Little Endian or Big Endian mode:

Direct Slave PCI access to Local Address Space 0
Direct Slave PCI access to Local Address Space 1
Direct Slave PCI access to Local Address Space 2
Direct Slave PCI access to Local Address Space 3
Direct Slave PCI access to Expansion ROM Space

2.2.2.6 Local Chip Selects

The PCI 9050 has 4 programmable chip selects. A chip select is asserted when the following are true:

- The value of the local address bus falls within the programmed range of the chip select.
- The chip select is enabled (bit 0 of the Chip Select Base Address Register = 1).
- The local bus is in the address or data phase (chip select is asserted with ADS# and negated at the end of the data phase)

Each chip select has an associated register which determines its range and local base address. Starting from bit 1 of the register and scanning towards bit 27, the first '1' found defines the size. The most significant bits, excluding the first '1' found, define the bas address.

Examples:
To program a chip select with a base of 04567000 and a range of 256 bytes, program 04567081 into the chip select register. This is determined as follows:

- bit 0 <= 1 enables the chip select
- bits 7:1 <= 1000000 define a range of 256 bytes. Bit 7 is the first '1' found while scanning from bit 1 to bit 27, thus removing bits 1 through 7 from the decoding process.
- bits 27:8 <= 0x045670 define the upper 20 bits of the base address

To program a chip select with a base of 00000000 and a range of 256 Mbytes (entire local address space), program 8000001 into the chip select register. This is determined as follows:

- bit 0 <= 1 enables the chip select
- bits 27:1 <= 8000000 define a range of 256 Mbytes. Bit 27 is the first '1' found while scanning from bit 1 to bit 27, thus removing bits 1 through 27 from the decoding process.
- Since there are no more significant bits above bit 27, and the chip select spans the entire local address space, the base address defaults to 0.

Chip selects CS2# and CS3# are multiplexed with user bits USER2 and USER3 respectively. Program bits 6 and 9 in the Miscellaneous Control Register (CNTRL; 50H) to select the function of these pins.

3. SECTION 3 - FUNCTIONAL DESCRIPTION

3.1 PCI 9050 Initialization

During power up, the PCI RST# signal resets all of the PCI 9050 internal registers to their default values. In return, the PCI 9050 outputs the local reset signal (LRESET#) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI 9050 loads the internal registers from the serial EEPROM. Otherwise, the default values are used. The PCI 9050 configuration registers can only be written by the optional serial EEPROM or the PCI host processor. During the serial EEPROM initialization, the PCI 9050 response to PCI target accesses is RETRYs.

3.2 RESET

3.2.1 PCI Bus Input RST#

The PCI bus RST# input causes all PCI bus outputs to float, resets the entire PCI 9050, and asserts the local reset output LRESET#.

3.2.2 Software Reset

A host on the PCI bus can set the software reset bit in the Miscellaneous Control Register (CNTRL; 50h) to reset the PCI 9050 and assert the LRESET# output. The contents of the PCI and local configuration registers will not be reset. When the software reset bit is set, the PCI 9050 responds only to configuration registers accesses, and not to accesses destined for the local bus. The PCI 9050 remains in this reset condition until the PCI host clears the software reset bit.

3.2.3 Local Bus Output LRESET#

LRESET# is asserted when PCI bus RST# input is asserted(4ns to 10ns delay) or bit 30 (the software reset bit) in the Miscellaneous Control Register (CNTRL; 50h) is set to a 1.

3.3 EEPROM

After reset, the PCI 9050 attempts to read the EEPROM to determine its presence. An active low start bit indicates that the EEPROM is present. Refer to the manufacturer's data sheet for the particular EEPROM being used. If the first word in the EEPROM is not FFFF, then the PCI 9050 assumes that the device is not blank, and continues reading.

The bits are organized such that the most significant bit of each 32-bit word is stored first in EEPROM. (The first bit in the EEPROM is bit 15 of the Device ID). The 25 32-bit words are stored sequentially in the EEPROM (Example: National NM93CS46 or compatible.) **Note: 2K bit devices such as 93CS56 are not compatible.**

The EEPROM can be read or programmed by a host on the PCI bus. Bits 24 through 29 of the Miscellaneous Control Register (CNTRL: 50h) control the PCI 9050 pins which enable the reading or writing of EEPROM bits. Refer to the manufacturer's data sheet for the particular EEPROM being used.

To reload the Serial EEPROM: Write '1' to bit #29 of register (CNTRL; 50h) to reload the serial EEPROM data into the PCI9050 internal registers.

To Read/Write to the serial EEPROM: 1. Enable the EEPROM CS# by writing '1' to Bit #25 of register (CNTRL; 50h). 2. Generate the Serial EEPROM clock by writing '0' and '1'. The data will be read or written during the zero-to-one transition.(refer to bit #24). 3. Send the command code to the Serial EEPROM. 4. If the Serial EEPROM is present, you will get a '0' value as a start bit after command code. 5. Read or write the data. 6. Write '0' to bit #25 to end the Serial EEPROM access(the Serial EEPROM CS# pin will go low).

The EEPROM load sequence chart on the next page uses the following abbreviations:

MSW = Most Significant Word(bits 31 - 16)
LSW = Least Significant Word(bits 15 - 0)

3.3.1 EEPROM LOAD SEQUENCE

Note: The EEPROM Value shown is the register value for PCI9050 DEMO Board.

EEPROM Offset	Register Offset	EEPROM Value	Register Description
0	PCI 02	9050	Device ID.
2	PCI 00	10B5	Vendor ID.
4	PCI 0A	0680	Class Code.
6	PCI 08	000x	Class code (Revision is not loadable).
8	PCI 2E	9050	Subsystem ID.
A	PCI 2C	10B5	Subsystem Vendor ID.
C	PCI 3E	xxxx	(Maximum Latency and Minimum Grant is not loadable).
E	PCI 3C	01xx	Interrupt Pin (Interrupt Line Routing is not loadable).
10	LOCAL 02	0FFE	MSW of Range for PCI to Local Address Space 0 (1Mbytes).
12	LOCAL 00	0000	LSW of Range for PCI to Local Address Space 0 (1Mbytes).
14	LOCAL 06	0FFE	MSW of Range for PCI to Local Address Space 1.
16	LOCAL 04	0000	LSW of Range for PCI to Local Address Space 1.
18	LOCAL 0A	0FFF	MSW of Range for PCI to Local Address Space 2.
1A	LOCAL 08	0000	LSW of Range for PCI to Local Address Space 2.
1C	LOCAL 0E	0FFC	MSW of Range for PCI to Local Address Space 3.
1E	LOCAL 0C	0000	LSW of Range for PCI to Local Address Space 3.
20	LOCAL 12	0000	MSW of Range for PCI to Local Expansion ROM (64 Kbytes).
22	LOCAL 10	0000	LSW of Range for PCI to Local Expansion ROM (64 Kbytes).
24	LOCAL 16	0000	MSW of Local Base Address (Re-Map) for PCI to Local Address Space 0.
26	LOCAL 14	0001	LSW of Local Base Address (Re-Map) for PCI to Local Address Space 0.
28	LOCAL 1A	0002	MSW of Local Base Address (Re-Map) for PCI to Local Address Space 1.
2A	LOCAL 18	0001	LSW of Local Base Address (Re-Map) for PCI to Local Address Space 1.
2C	LOCAL 1E	0004	MSW of Local Base Address (Re-Map) for PCI to Local Address Space 2.
2E	LOCAL 1C	0001	LSW of Local Base Address (Re-Map) for PCI to Local Address Space 2.
30	LOCAL 22	0008	MSW of Local Base Address (Re-Map) for PCI to Local Address Space 3.
32	LOCAL 20	0001	LSW of Local Base Address (Re-Map) for PCI to Local Address Space 3.
34	LOCAL 26	0010	MSW of Local Base Address (Re-Map) for PCI to Local Expansion ROM.
36	LOCAL 24	0000	LSW of Local Base Address (Re-Map) for PCI to Local Expansion ROM.
38	LOCAL 2A	0080	MSW of Bus Region Descriptors for Local Address Space 0.
3A	LOCAL 28	0026	LSW of Bus Region Descriptors for Local Address Space 0.
3C	LOCAL 2E	0080	MSW of Bus Region Descriptors for Local Address Space 1.
3E	LOCAL 2C	003F	LSW of Bus Region Descriptors for Local Address Space 1.
40	LOCAL 32	0040	MSW of Bus Region Descriptors for Local Address Space 2.
42	LOCAL 30	0037	LSW of Bus Region Descriptors for Local Address Space 2.
44	LOCAL 36	5421	MSW of Bus Region Descriptors for Local Address Space 3.
46	LOCAL 34	38E9	LSW of Bus Region Descriptors for Local Address Space 3.
48	LOCAL 3A	0000	MSW of Bus Region Descriptors for Expansion ROM Space.
4A	LOCAL 38	0000	LSW of Bus Region Descriptors for Expansion ROM Space.
4C	LOCAL 3E	0004	MSW of Chip Select(CS) 0 Base and Range Register.
4E	LOCAL 3C	0001	LSW of Chip Select(CS) 0 Base and Range Register.
50	LOCAL 42	000A	MSW of Chip Select(CS) 1 Base and Range Register.
52	LOCAL 40	0001	LSW of Chip Select(CS) 1 Base and Range Register.
54	LOCAL 46	0000	MSW of Chip Select(CS) 2 Base and Range Register.
56	LOCAL 44	0000	LSW of Chip Select(CS) 2 Base and Range Register.
58	LOCAL 4A	0004	MSW of Chip Select(CS) 3 Base and Range Register.
5A	LOCAL 48	8001	LSW of Chip Select(CS) 3 Base and Range Register.
5C	LOCAL 4E	0000	MSW of Interrupt Control / Status Register.
5E	LOCAL 4C	0000	LSW of Interrupt Control / Status Register.
60	LOCAL 52	0005	MSW of EEPROM Control and Misc. Control Register.
62	LOCAL 50	4291	LSW of EEPROM Control and Misc. Control Register.

3.4 Internal Register Access

The PCI 9050 chip provides several internal registers allowing for maximum flexibility in bus interface design and performance. The register types are:

- **PCI Registers** (accessible from PCI bus and EEPROM)
- **Local Configuration Registers** (accessible from PCI and EEPROM)

Note: The Local Configuration Base Address Register access can be limited to memory mapped or I/O mapped or both access can be disabled via bit #[13:12] of the register at (CNTRL; 50h).

3.4.1 Internal Registers

Device and vendor ID
There are two sets of device and vendor IDs. The Device and Vendor ID are located at offset 0 of the PCI Configuration Registers, while the Subsystem Vendor ID and Subsystem Device ID are at offset 2Ch of the PCI configuration Registers. The Device and Vendor ID identify the particular device, and manufacturer of the device, respectively. The Subsystem Vendor ID and Subsystem ID provide a way to distinguish between vendors of the PCI interface chip and the manufacturer of the add-in board which is utilizing the PCI chip.

Status Register
The Status register contains information of PCI bus-related events.

Command Register
This register controls a device's ability to respond to PCI accesses. It controls whether the device responds to I/O space or memory space accesses.

Class Code Register
This register identifies the general function of the device. Refer to the PCI Specification for further details.

Revision ID Register
The value read from this register represents the current silicon revision of the PCI 9050.

Header Type
This register defines the format of the device's configuration header and whether the device is single-function or multi-function.

Cache Line Size
This register defines the system cache line size in units of 32-bit words.

PCI Base Address Register for Memory Accesses to Local Configuration Registers
This register is used by the system BIOS to assign a segment of the PCI address space for memory accesses to the PCI 9050 Local Configuration Registers. The PCI address range which is occupied by these configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, and reads back FFFFFF70, thus determining that 128 bytes of memory space is required. The host then writes the base address to bits 31 through 7.

PCI Base Address Register for I/O Accesses to Local Configuration Registers
This register is used by the system BIOS to assign a segment of the PCI address space for I/O accesses to the PCI 9050 Local Configuration Registers. The PCI address range which is occupied by these configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, and reads back FFFFFF71, thus determining that 128 bytes of I/O space is required. The host then writes the base address to bits 31 through 7.

PCI Base Address Register for Accesses to Local Address Space 0 (Also true for Space 1, 2, and 3)
This register is used by the system BIOS to assign a segment of the PCI address space for accesses to Local Address Space 0. The PCI address range which is occupied by this space is determined by the Local Address Space 0 Range Register. During initialization, the host writes FFFFFFFF to this register, and reads back a value determined by the range. The host then writes the base address to the upper bits of this register.

PCI Expansion ROM Base Address Register
This register is used by the system BIOS to assign a segment of the PCI address space for accesses to the Expansion ROM. The PCI address range which is occupied by this space is determined by Expansion ROM Range Register. During initialization, the host writes FFFFFFFF to this register, and reads back a value determined by the range. The host then writes the base address to the upper bits of this register.

PCI Interrupt Line Register
This register identifies where the device's interrupt line is connected on the system's interrupt controller(s).

PCI Interrupt Pin Register
This register specifies which interrupt request pin (if any) is used.

3.4.2 PCI Bus Access to Internal Registers

The PCI 9050 PCI configuration registers are be accessed from the PCI bus via a configuration type 0 cycle.

The PCI 9050 local configuration registers are accessed via a memory cycle with the PCI bus address matching the base address specified in the PCI Base Address Register for Memory Accesses to Local Configuration Registers (PCIBAR0; 10h) or an I/O cycle with the PCI bus address matching the base address specified in the PCI Base Address Register for I/O Accesses to Local Configuration Registers (PCIBAR1; 14h).

All PCI read or write accesses to the PCI 9050 registers can be byte, word, or long word accesses. Memory accesses to the PCI 9050 registers can be burst or non-burst. The PCI 9050 responds with a PCI Disconnect for all I/O accesses to the PCI 9050 registers.

3.5 Direct Data Transfer Modes

The PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI 9050 control the decoding and re-mapping of these accesses to the local address space. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

3.5.1 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI 9050 supports both memory mapped burst transfer accesses and I/O mapped single transfer accesses to the local bus from the PCI bus. PCI Base Address registers are provided to determine the adapter's location in PCI memory and I/O space. In addition, local mapping registers are provided to allow address translation from the PCI address space to the local address space.

The PCI 9050 disconnects after one transfer for all Direct Slave I/O accesses. For single cycle Direct Slave reads, the PCI 9050 reads a single local bus Lword. For Direct Slave memory accesses, burst read pre-fetching can be enabled or disabled through the Local Address Space Bus Region Descriptor Registers. If read prefetching is disabled, the PCI 9050 disconnects after one read transfer. If prefetching is enabled, the read prefetch size can be programmed through the Local Address Space Bus Region Descriptor Registers.

The PCI 9050 can be programmed though the Miscellaneous Control Register (CNTRL; 50h) to perform delayed reads as specified in the PCI Specification rev 2.1.

3.5.1.1 PCI to Local Address Mapping

Five local address spaces (local spaces 0-3 and expansion ROM) are accessible from the PCI bus. Each space is defined by a set of four registers: PCI Base Address, Local Range, Local Base Address (Re-map), and the Local Bus Region Descriptor which defines the local bus characteristics.

Byte Enables (LBE[3:0]#, Pin 46,47, 48, and 49) are encoded based on configured bus width as follows:

32 bit bus: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle.
BE3# Byte Enable 3 - LD[31:24]
BE2# Byte Enable 2 - LD[23-16]
BE1# Byte Enable 1 - LD[15-8]
BE0# Byte Enable 0 - LD[7-0]

16 bit bus: For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provide BHE#, LA1, and BLE# respectively.
BE3# Byte High Enable (BHE#) - LD[15:8]
BE2# not used
BE1# Address bit 1 (LA1)
BE0# Byte Low Enable (BLE#) - LD[7-0]

8 bit bus: For an 8 bit bus BE1# and BE0# are encoded to provide LA1 and LA0 respectively.
BE3# not used
BE2# not used
BE1# Address bit 1 (LA1)
BE0# Address bit 0 (LA0)

Each PCI to Local Address space is defined as part of the reset initialization as follows:

Local Bus Initialization Software:
Range: Specifies which PCI address bits are to be used to decode a PCI access to Local bus space. Each of the bits corresponds to an address bit with Bit 31 corresponding to Address bit 31. A value of 1 should be written to all bits that are included in the decoding and a 0 to those that are ignored..

Re-map PCI Address into a Local Address: The bits in this register re-map (replace) the PCI address bits used in decoding into the Local Address bits.

Local Bus Region Descriptor: Specifies the local bus characteristics such as bus width, bursting, prefetching, and number of wait states..

PCI Initialization Software:
PCI bus initialization software on the host determines how much address space is required by writing a value of all ones (1) to a PCI Base Address register and then reading the value back. The PCI 9050 returns 0s in don't care address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register.

Example: A 1 MB local address space 02300000h through 023FFFFFh is accessible from the PCI bus at PCI addresses 78900000h through 789FFFFFh.

1. Local initialization software sets the Range and Local Base address registers as follows:
   Range- FFF00000h (1 MB, decode the upper 12 PCI address bits)
   Local Base Address(re-map)- 023XXXXXh (Local Base Address for PCI to Local accesses)

2. PCI Initialization software writes all 1s to the PCI Base Address and then reads it back. The PCI 9050 returns a value FFF00000h. The PCI software then writes to the PCI Base Address register.
   PCI Base Address- 789XXXXXh (PCI Base Address for access to Local Address space)

For PCI accesses to the local bus, the PCI 9050 has a 16 Lword (64 byte) write FIFO and a 8 Lword (32 byte) read FIFO. The FIFO enables the local bus to operate independently of the PCI bus. The PCI 9050 can be programmed to either return a RETRY response or to throttle TRDY for PCI bus transactions that attempt to write to the PCI 9050 local bus when the write FIFO is full.

For PCI read transactions from the PCI 9050 local bus, the PCI 9050 holds off TRDY while gathering the local bus Lword to be returned. For read accesses mapped to the PCI memory space, the PCI 9050 prefetches up to 4 Lwords from the local bus. Unused read data is flushed from the FIFO. For read accesses mapped to the PCI I/O space, the PCI 9050 does not prefetch read data. It breaks each read of the burst cycle into a single address/data cycle on the local bus.

The period of time that the PCI 9050 holds off TRDY is programmed in the Miscellaneous Control Register (CNTRL: 50h). The PCI 9050 issues a RETRY to the PCI bus master when the programmed time period expires. This happens when the PCI 9050 can not gain control of the local bus and return TRDY within the programmed time period.

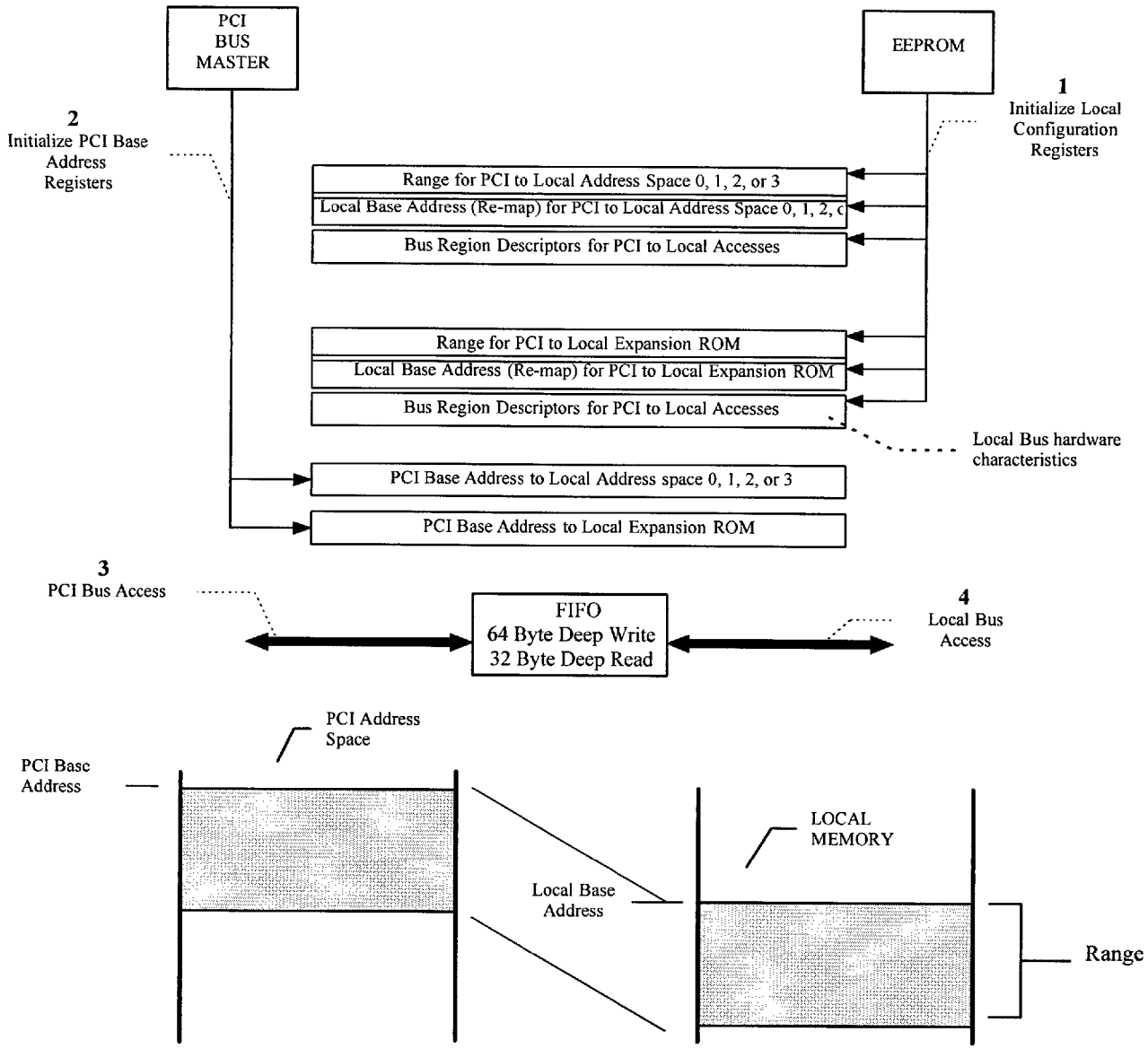


Figure 1. PCI Master Direct Access of Local Bus

3.5.1.2 Direct Slave Lock.

The PCI 9050 supports direct PCI to local bus exclusive accesses (locked atomic operations). A PCI locked operation to local bus results in the entire address space 0-3 and expansion ROM space being locked until released by the PCI bus master. The PCI 9050 asserts LLOCKo# during the first clock of an atomic operation (address cycle) and negates it a minimum of one clock following the last bus access for the atomic operation. LLOCKo# is negated after the PCI 9050 detects PCI FRAME# and PCI LOCK# negated at the same time. Refer to the timing diagrams included in this specification. Locked operations are enabled through the Miscellaneous Control Register (CNTRL: 50h).

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. For example, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the local bus to other masters until the locked operation is complete.

3.5.1.3 Arbitration

The PCI 9050 takes control of the local bus when a new transfer request is detected from the PCI bus. Another device can gain control of the local bus by asserting LHOLD. If the PCI 9050 has no cycles to run, it will assert LHOLDA, thus transferring control to the external master. If the PCI 9050 needs the local bus before the external master has finished, LHOLDA will be negated (preempt condition). The arbiter then waits for LHOLD to be negated before taking control of the bus again.

3.6 PCI Interrupts (INTA#)

The two local interrupt inputs LINTI1 and LINTI2 as well as the software interrupt (CNTRL register bit 30), can cause a PCI Interrupt (INTA#) to be generated. INTA# or individual sources of an interrupt can be enabled or disabled through the PCI 9050 Interrupt Control/Status Register. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt

The PCI 9050 PCI bus interrupt is an asynchronous level output. An interrupt can be cleared by disabling a source's interrupt enable bit or clearing the cause of an interrupt.

3.7 PCI SERR# (PCI NMI)

The PCI 9050 generates a SERR# pulse if parity checking is enabled in the PCI Command Register and an address parity error is detected. The SERR# output is enabled through the PCI Command Register.

4. SECTION 4 - REGISTERS

4.1 Register Address Mapping

PCI CONFIGURATION REGISTERS

PCI CFG register address	**To ensure software compatibility with future enhancements, all unused bits should be written with a zero.** 31 24 23 16 15 8 7 0				PCI Writable	EEPROM Writable
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	N
08h	Class Code			Revision ID	N	Y(31:8)
0Ch	BIST	Header Type	Latency Timer	Cache Line Size	Y(7:0)	N
10h	PCI Base Address 0 for Memory Mapped Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O Mapped Configuration Registers				Y	N
18h	PCI Base Address 2 for Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Local Address Space 1				Y	N
20h	PCI Base Address 4 for Local Address Space 2				Y	N
24h	PCI Base Address 5 for Local Address Space 3				Y	N
28h	Cardbus CIS Pointer (Not Supported)				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Base Address for Local Expansion ROM				Y	N
34h	Reserved				N	N
38h	Reserved				N	N
3Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y(7:0)	Y(15:8)

LOCAL CONFIGURATION REGISTERS

PCI (Offset from Local Base address)	**To ensure software compatibility with future enhancements, all unused bits should be written with a zero.** 31 0	PCI and EEPROM Writable
00h	Local Address Space 0 Range	Y
04h	Local Address Space 1Range	Y
08h	Local Address Space 2 Range	Y
0Ch	Local Address Space 3 Range	Y
10h	Local Expansion ROM Range	Y
14h	Local Address Space 0 Local Base Address (Re-map)	Y
18h	Local Address Space 1 Local Base Address (Re-map)	Y
1Ch	Local Address Space 2 Local Base Address (Re-map)	Y
20h	Local Address Space 3 Local Base Address (Re-map)	Y
24h	Expansion ROM Local Base Address (Re-map)	Y
28h	Local Address Space 0 Bus Region Descriptors	Y
2Ch	Local Address Space 1 Bus Region Descriptors	Y
30h	Local Address Space 2 Bus Region Descriptors	Y
34h	Local Address Space 3 Bus Region Descriptors	Y
38h	Expansion ROM Bus Region Descriptors	Y
3Ch	Chip Select 0 Base Address	Y
40h	Chip Select 1 Base Address	Y
44h	Chip Select 2 Base Address	Y
48h	Chip Select 3 Base Address	Y
4Ch	Interrupt Control / Status	Y
50h	EEPROM Control, PCI Slave Response, User I/O Control, Init Control	Y

4.2 PCI Configuration Registers

All registers may be written to or read from in byte, word, or long word accesses.

4.2.1 (PCIIDR; 00h) PCI Configuration ID Register

Table 1: PCI Configuration ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX if no EEPROM is present.	Yes	EEPROM	10B5h
31:16	Device ID - Identifies the particular device. Defaults to the PLX part number for PCI interface chip if no EEPROM is present.	Yes	EEPROM	9050h

4.2.2 (PCICR; 04h) PCI Command Register

Table 2: PCI Command Register Description

Field	Description	Read	Write	Value after Reset
0	I/O Space. A value of 1 allows the device to respond to I/O space accesses. A value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. A value of 1 allows the device to respond to memory space accesses. A value of 0 disables the device from responding to memory space accesses.	Yes	Yes	0
2	Master Enable. A value of 1 allows the device to behave as a bus master. A value of 0 disables the device from generating bus master accesses.	Yes	No	0
3	Special Cycle. This bit is not supported.	Yes	No	0
4	Memory Write/Invalidate. This bit is not supported.	Yes	No	0
5	VGA Palette Snoop. This bit is not supported.	Yes	No	0
6	Parity Error Response. A value of 0 indicates that a parity error is ignored and operation continues. A value of 1 indicates that parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether or not the device does address/data stepping. A 0 value indicates the device never does stepping. A value of 1 indicates that the device always does stepping. This value is hardwired to 0.	Yes	No	0
8	SERR# Enable. A value of 1 enables the SERR# driver. A value of 0 disables the driver	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. A value of 1 indicates that fast back-to-back transfers can occur to any agent on the bus. A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15:10	Reserved.	Yes	No	0

4.2.3 (PCISR; 06h) PCI Status Register

Table 3: PCI Status Register Description

Field	Description	Read	Write	Value after Reset
6:0	Reserved	Yes	No	0
7	Fast Back-to-Back Capable. When this bit is set to a 1, it indicates the adapter can accept fast back-to-back transactions. A 0 indicates the adapter cannot.	Yes	No	1h
8	Master Data Parity Error Detected. Not supported.	Yes	No	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. A value of 01 is medium.	Yes	No	01
11	Target Abort. When this bit is set to a 1, this bit indicates the PCI 9050 has signaled a target abort. Writing a 1 to this bit clears the bit.	Yes	Yes	0
12	Received Target Abort. When set to a 1, this bit indicates the PCI 9050 has received a target abort signal. Not supported	Yes	No	0
13	Received Master Abort. When set to a 1, this bit indicates the PCI 9050 has received a master abort signal. Not supported	Yes	No	0
14	Signaled System Error. When set to a 1, this bit indicates the PCI 9050 has reported a system error on the SERR# signal. Writing a 1 to this bit clears the error status bit.	Yes	Yes	0
15	Detected Parity Error. When set to a 1, this bit indicates the PCI 9050 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). One of two conditions cause this bit to be set: 1) the PCI 9050 detected a parity error during a PCI address phase; 2) the PCI 9050 detected a data parity error when it was the target of a write. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0

4.2.4 (PCIREV; 08h) PCI Revision ID Register

Table 4: PCI Revision ID Register Description

Field	Description	Read	Write	Value after Reset
7:0	Revision ID. The silicon revision of the PCI 9050.	Yes	No	Current Revision

4.2.5 (PCICCR; 09-0Bh) PCI Class Code Register

Table 5: PCI Class Code Register Description

Field	Description	Read	Write	Value after Reset
7:0	Specific register level programming interface (00h). No interface defined.	Yes	EEPROM	00
15:8	Sub-class Encoding (80h). Other bridge device.	Yes	EEPROM	80h
23:16	Base Class Encoding other Bridge Device	Yes	EEPROM	06h

4.2.6 (PCICLSR; 0Ch) PCI Cache Line Size Register

Table 6: PCI Cache Line Size Register Description

Field	Description	Read	Write	Value after Reset
7:0	System cache line size in units of 32-bit words. This register can be written and read, but the value has no effect on the operation of the chip.	Yes	Yes	0

4.2.7 (PCILTR; 0Dh) PCI Latency Timer Register

Table 7: PCI Latency Timer Register Description

Field	Description	Read	Write	Value after Reset
7:0	Latency Timer. Not supported	Yes	No	0

4.2.8 (PCIHTR; 0Eh) PCI Header Type Register

Table 8: PCI Header Type Register Description

Field	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies the layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	No	0
7	Header Type. A 1 indicates multiple functions, a 0 indicates a single function.	Yes	No	0

4.2.9 (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST) Register

Table 9: PCI Built-In Self Test (BIST) Register Description

Field	Description	Read	Write	Value after Reset
7:0	A value of 0 means the device has passed its test. Not supported	Yes	No	0

4.2.10 (PCIBAR0; 10h) PCI Base Address Register for Memory Accesses to Local Configuration Registers

Table 10: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. Note: Hardwired to 0.	Yes	No	0
2:1	Location of register: 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 MByte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved Note: Hardwired to 0.	Yes	No	0
3	Prefetchable. A value of 1 indicates there are no side effects on reads. Note: Hardwired to 0.	Yes	No	0
6:4	Memory Base Address. Memory base address for access to local configuration registers (Default 128 bytes) Note: Hardwired to 0.	Yes	No	0
31:7	Memory Base Address. Memory base address for access to local configuration registers	Yes	Yes	0

NOTE: PCIBAR0 can be enabled or disabled using bits 12 and 13 in the CNTRL register.

4.2.11 (PCIBAR1; 14h) PCI Base Address Register for I/O Accesses to Local Configuration Registers

Table 11: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. Note: Hardwired to 1	Yes	No	1h
1	Reserved	Yes	No	0
6:2	I/O Base Address. Base Address for I/O access to local configuration registers. (Default 128 bytes) Note: Hardwired to 0.	Yes	No	0
31:7	I/O Base Address. Base Address for I/O access to local configuration registers.	Yes	Yes	0

NOTE: PCIBAR1 can be enabled or disabled using bits 12 and 13 in the CNTRL register.

4.2.12 (PCIBAR2; 18h) PCI Base Address Register for Memory Access to Local Addr Space 0

Table 12: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS0RR register).	Yes	No	0
2:1	Location of register (If Memory Space): 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 Mbyte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved (Specified in LAS0RR register). If I/O Space, bit 1 is always 0, and bit 2 is included in the base address	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (If Memory Space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS0RR register, and only provides status to the system. This bit has no effect on the operation of the PCI 9050. Prefetching features of this address space are controlled by the associated Bus Region Descriptor Register (LAS0BRD). (Specified in LAS0RR register). If I/O Space, bit 3 is included in the base address	Yes	Mem: No I/O: Yes	0
31:4	Base Address for accesses to the local address space.	Yes	Yes	0

NOTE: PCIBAR2 can be enabled or disabled by setting or clearing bit 0 in the LAS0BA register.

4.2.13 (PCIBAR3; 1Ch) PCI Base Address Register for Memory Access to Local Addr Space 1

Table 13: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS1RR register).	Yes	No	0
2:1	Location of register (If Memory Space): 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 Mbyte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved (Specified in LAS1RR register). If I/O Space, bit 1 is always 0, and bit 2 is included in the base address	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (If Memory Space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS1RR register, and only provides status to the system. This bit has no effect on the operation of the PCI 9050. Prefetching features of this address space are controlled by the associated Bus Region Descriptor Register (LAS1BRD). (Specified in LAS1RR register). If I/O Space, bit 3 is included in the base address	Yes	Mem: No I/O: Yes	0
31:4	Base Address for accesses to the local address space.	Yes	Yes	0

NOTE: PCIBAR3 can be enabled or disabled by setting or clearing bit 0 in the LAS1BA register.

4.2.14 (PCIBAR4; 20h) PCI Base Address Register for Memory Access to Local Addr Space 2

Table 14: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS2RR register).	Yes	No	0
2:1	Location of register (If Memory space).: 00 - Locate anywhere in 32 bit memoryaddress space 01 - Locate below 1 MByte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved (Specified in LAS2RR register). If I/O Space, bit 1 is always 0, and bit 2 is included in the base address	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (If Memory Space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS2RR register, and only provides status to the system. This bit has no effect on the operation of the PCI 9050. Prefetching features of this address space are controlled by the associated Bus Region Descriptor Register (LAS2BRD). (Specified in LAS2RR register). If I/O Space, bit 3 is included in the base address	Yes	Mem: No I/O: Yes	0
31:4	Base Address for accesses to the local address space.	Yes	Yes	0

NOTE: PCIBAR4 can be enabled or disabled by setting or clearing bit 0 in the LAS2BA register.

4.2.15 (PCIBAR5; 24h) PCI Base Address Register for Memory Access to Local Addr Space 3

Table 15: PCI Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Specified in LAS3RR register).	Yes	No	0
2:1	Location of register (If Memory Space): 00 - Locate anywhere in 32 bit memory address space 01 - Locate below 1 MByte memory address space 10 - Locate anywhere in 64 bit memory address space 11 - Reserved (Specified in LAS3RR register). If I/O Space, bit 1 is always 0, and bit 2 is included in the base address	Yes	Mem: No I/O: bit 1 no, bit 2 yes	0
3	Prefetchable (If Memory Space). A value of 1 indicates there are no side effects on reads. This bit reflects the value of bit 3 in the LAS3RR register, and only provides status to the system. This bit has no effect on the operation of the PCI 9050. Prefetching features of this address space are controlled by the associated Bus Region Descriptor Register (LAS3BRD). (Specified in LAS3RR register). If I/O Space, bit 3 is included in the base address	Yes	Mem: No I/O: Yes	0
31:4	Base Address for accesses to the local address space.	Yes	Yes	0

NOTE: PCIBAR5 can be enabled or disabled by setting or clearing bit 0 in the LAS3BA register.

4.2.16 (PCICIS; 28h) PCI Cardbus CIS Pointer Register

Table 16: PCI Cardbus CIS Pointer Register Description

Field	Description	Read	Write	Value after Reset
31:0	Cardbus Information Structure Pointer for PCMCIA. Not Supported	Yes	No	0

4.2.17 (PCISVID; 2Ch) PCI Subsystem Vendor ID

Table 17: PCI Subsystem Vendor ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID. (Unique add-in board vendor ID)	Yes	EEPROM	0

4.2.18 (PCISID; 2Eh) PCI Subsystem ID

Table 18: PCI Subsystem ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Subsystem ID. (Unique add-in board device ID)	Yes	EEPROM	0

4.2.19 (PCIERBAR; 30h) PCI Expansion ROM Base Address Register

Table 19: PCI Expansion ROM Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Address Decode Enable. A value of 1 indicates the device accepts accesses to the expansion ROM address. A value of 0 indicates the device does not accept accesses to expansion ROM space.	Yes	Yes	0
10:1	Reserved	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits)	Yes	Yes	0

4.2.20 (PCIILR; 3Ch) PCI Interrupt Line Register

Table 20: PCI Interrupt Line Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Value indicates which input of the system interrupt controller(s) the device's interrupt line is connected to.	Yes	Yes	0

4.2.21 (PCIIPR; 3Dh) PCI Interrupt Pin Register

Table 21: PCI Interrupt Pin Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Pin register. Indicates which interrupt pin the device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	EEPROM	1h

4.2.22 (PCIMGR; 3Eh) PCI Min_Gnt Register

Table 22: PCI Min_Gnt Register Description

Field	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Used to specify how long a burst period the device needs assuming a clock rate of 33 MHz. Value is multiple of 1/4µs increments. Not supported.	Yes	No	0

4.2.23 (PCIMLR; 3Fh) PCI Max_Lat Register

Table 23: PCI Max_Lat Register Description

Field	Description	Read	Write	Value after Reset
7:0	Max_Lat. Used to specify how often the device needs to gain access to the PCI bus. Value is multiple of 1/4µs increments. Not supported.	Yes	No	0

4.3 Local Configuration Registers

4.3.1 (LAS0RR; 00h) Local Address Space 0 Range Register

Table 24: Local Address Space 0 Range Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 0 maps into PCI memory space. A value of 1 indicates address space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: 2/1 Meaning 0 0 locate anywhere in 32 bit PCI address space 0 1 locate below 1 Meg in PCI address space 1 0 locate anywhere in 64 bit PCI address space 1 1 reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits 3 through 27 to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates that reads are prefetchable (Bit has no effect on the operation of the PCI 9050, but is for system status) If mapped into I/O space, bit is included with bits 2 through 27 to indicate decoding range.	Yes	Yes	0
27:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 0. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 18h). Default is 1 Mbyte.	Yes	Yes	FF0000
31:28	Unused. (PCI address bits 31-28 are always included in decoding)	Yes	No	0

4.3.2 (LAS1RR; 04h) Local Address Space 1 Range Register

Table 25: Local Address Space 1 Range Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 1 maps into PCI memory space. A value of 1 indicates address space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: 2/1 Meaning 0 0 locate anywhere in 32 bit PCI address space 0 1 locate below 1 Meg in PCI address space 1 0 locate anywhere in 64 bit PCI address space 1 1 reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits 3 through 27 to indicate decoding range.		Yes	0
3	If mapped into memory space, a 1 indicates that reads are prefetchable. If mapped into I/O space, bit is included with bits 2 through 27 to indicate decoding range.	Yes	Yes	0
27:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 1. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 1Ch).	Yes	Yes	0
31:28	Unused. (PCI address bits 31-28 are always included in decoding)	Yes	No	0

4.3.3 (LAS2RR; 08h) Local Address Space 2 Range Register

Table 26: Local Address Space 2 Range Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 2 maps into PCI memory space. A value of 1 indicates address space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: 2/1 Meaning 0 0 locate anywhere in 32 bit PCI address space 0 1 locate below 1 Meg in PCI address space 1 0 locate anywhere in 64 bit PCI address space 1 1 reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits 3 through 27 to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates that reads are prefetchable . If mapped into I/O space, bit is included with bits 2 through 27 to indicate decoding range.	Yes	Yes	0
27:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 2. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 20h).	Yes	Yes	0
31:28	Unused. (PCI address bits 31-28 are always included in decoding)	Yes	No	0

4.3.4 (LAS3RR; 0Ch) Local Address Space 3 Range Register

Table 27: Local Address Space 3 Range Register Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 3 maps into PCI memory space. A value of 1 indicates address space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: 2/1 Meaning 0 0 locate anywhere in 32 bit PCI address space 0 1 locate below 1 Meg in PCI address space 1 0 locate anywhere in 64 bit PCI address space 1 1 reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits 3 through 27 to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates that reads are prefetchable . If mapped into I/O space, bit is included with bits 2 through 27 to indicate decoding range.	Yes	Yes	0
27:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 3. Each of the bits corresponds to an address bit. Bit 27 corresponds to Address bit 27. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 24h).	Yes	Yes	0
31:28	Unused. (PCI address bits 31-28 are always included in decoding)	Yes	No	0

4.3.5 (EROMRR; 10h) Expansion ROM Range Register

Table 28: Expansion ROM Range Register Description

Field	Description	Read	Write	Value after Reset
10:0	Not used	Yes	No	0
27:11	Specifies which PCI address bits will be used to decode a PCI to local bus expansion ROM. Each of the bits corresponds to an Address bit. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 30h). Default is 64 Kbytes.	Yes	Yes	11111111111100000
31:28	Unused (PCI address bits 31-28 are always included in decoding)	Yes	No	0

4.3.6 (LAS0BA; 14h) Local Address Space 0 Local Base Address (Re-Map) Register

Table 29: Local Address Space 0 Local Base Address (Re-Map) Register Description

Field	Description	Read	Write	Value after Reset
0	Space 0 Enable. A 1 value enables Decode of PCI addresses for Direct Slave access to local space 0. A value of 0 disables Decode.	Yes	Yes	1
1	Not Used	Yes	Yes	0
3:2	If local space 0 is mapped into memory space, bits are not used. If mapped into I/O space, bits are included with bits 4 through 27 for re-mapping.	Yes	Yes	0
27:4	Re-map of PCI Address to Local Address Space 0 into a Local Address Space. The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits 31-28 do not exist in PCI 9050)	Yes	No	0

4.3.7 (LAS1BA; 18h) Local Address Space 1 Local Base Address (Re-Map) Register

Table 30: Local Address Space 1 Local Base Address (Re-Map) Register Description

Field	Description	Read	Write	Value after Reset
0	Space 1 Enable. A 1 value enables Decode of PCI addresses for Direct Slave access to local space 1. A value of 0 disables Decode.	Yes	Yes	0
1	Not Used	Yes	Yes	0
3:2	If local space 1 is mapped into memory space, bits are not used. If mapped into I/O space, bits are included with bits 4 through 27 for re-mapping.	Yes	Yes	0
27:4	Re-map of PCI Address to Local Address Space 1 into a Local Address Space. The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits 31-28 do not exist in PCI 9050)	Yes	No	0

4.3.8 (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Re-Map) Register

Table 31: Local Address Space 2 Local Base Address (Re-Map) Register Description

Field	Description	Read	Write	Value after Reset
0	Space 2 Enable. A 1 value enables Decode of PCI addresses for Direct Slave access to local space 2. A value of 0 disables Decode.	Yes	Yes	0
1	Not Used	Yes	Yes	0
3:2	If local space 2 is mapped into memory space, bits are not used. If mapped into I/O space, bits are included with bits 4 through 27 for re-mapping.	Yes	Yes	0
27:4	Re-map of PCI Address to Local Address Space 2 into a Local Address Space. The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits 31-28 do not exist in PCI 9050)	Yes	No	0

4.3.9 (LAS3BA; 20h) Local Address Space 3 Local Base Address (Re-Map) Register

Table 32: Local Address Space 3 Local Base Address (Re-Map) Register Description

Field	Description	Read	Write	Value after Reset
0	Space 3 Enable. A 1 value enables Decode of PCI addresses for Direct Slave access to local space 3. A value of 0 disables Decode.	Yes	Yes	0
1	Not Used	Yes	Yes	0
3:2	If local space 3 is mapped into memory space, bits are not used. If mapped into I/O space, bits are included with bits 4 through 27 for re-mapping.	Yes	Yes	0
27:4	Re-map of PCI Address to Local Address Space 3 into a Local Address Space. The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0
31:28	Unused. (Local address bits 31-28 do not exist in PCI 9050)	Yes	No	0

4.3.10 (EROMBA; 24h) Expansion ROM Local Base Address (Re-map) Register

Table 33: Expansion ROM Local Base Address (Re-map) Register Description

Field	Description	Read	Write	Value after Reset
10:0	Not Used	Yes	No	0
27:11	Re-map of PCI Expansion ROM space into a Local address space. The bits in this register re-map (replace) the PCI address bits used in decode as the Local address bits. Default base = 1 Mbyte (above default Local Address Space 0).	Yes	Yes	00000001000000000
31:28	Unused. (Local address bits 31-28 do not exist in PCI 9050)	Yes	No	0

4.3.11 (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor Register

Table 34: Local Address Space 0 Bus Region Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Burst Enable. 1 = Bursting Enabled. 0 = Disabled. Bursting will only occur if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. 1 = READY input enabled. 0 = Disabled.	Yes	Yes	0
2	Bterm Input Enable. 1 = BTERM input enabled. 0 = Disabled, Burst length limited to 4 long words.	Yes	Yes	0
4:3	Prefetch Count. Number of long words to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Don't prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 long words if bit 5 is set. 10 = Prefetch 8 long words if bit 5 is set. 11 = Prefetch 16 long words if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable; When set to a 1, the PCI 9050 will prefetch up to the number of Lwords specified in the prefetch count. When set to a 0, the count will be ignored and prefetching will continue until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Addr wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit, 11 = Reserved	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian, 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A 1 value specifies that in Big Endian mode byte lanes 31:16 be used for a 16-bit local bus, and byte lane 31:24 for an 8-bit local bus. A value of 0 specifies that in Big Endian mode byte lanes 15:0 be used for a 16-bit local bus, and byte lane 7:0 for an 8-bit local bus.	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be <= NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be <= NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR negation until the end of the cycle.(0-3).	Yes	Yes	0

4.3.12 (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor Register

Table 35: Local Address Space 1 Bus Region Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Burst Enable. 1 = Bursting Enabled. 0 = Disabled. Bursting will only occur if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. 1 = READY input enabled. 0 = Disabled.	Yes	Yes	0
2	Bterm Input Enable. 1 = BTERM input enabled. 0 = Disabled, Burst length limited to 4 long words.	Yes	Yes	0
4:3	Prefetch Count. Number of long words to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Don't prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 long words if bit 5 is set. 10 = Prefetch 8 long words if bit 5 is set. 11 = Prefetch 16 long words if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable; When set to a 1, the PCI 9050 will prefetch up to the number of Lwords specified in the prefetch count. When set to a 0, the count will be ignored and prefetching will continue until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Addr wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit, 11 = Reserved	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian, 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A 1 value specifies that in Big Endian mode byte lanes 31:16 be used for a 16-bit local bus, and byte lane 31:24 for an 8-bit local bus. A value of 0 specifies that in Big Endian mode byte lanes 15:0 be used for a 16-bit local bus, and byte lane 7:0 for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be <= NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be <= NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR negation until the end of the cycle.(0-3).	Yes	Yes	0

4.3.13 (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor Register

Table 36: Local Address Space 2 Bus Region Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Burst Enable. 1 = Bursting Enabled. 0 = Disabled. Bursting will only occur if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. 1 = READY input enabled. 0 = Disabled.	Yes	Yes	0
2	Bterm Input Enable. 1 = BTERM input enabled. 0 = Disabled, Burst length limited to 4 long words.	Yes	Yes	0
4:3	Prefetch Count. Number of long words to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Don't prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 long words if bit 5 is set. 10 = Prefetch 8 long words if bit 5 is set. 11 = Prefetch 16 long words if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable; When set to a 1, the PCI 9050 will prefetch up to the number of Lwords specified in the prefetch count. When set to a 0, the count will be ignored and prefetching will continue until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Addr wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit, 11 = Reserved	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian, 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A 1 value specifies that in Big Endian mode byte lanes 31:16 be used for a 16-bit local bus, and byte lane 31:24 for an 8-bit local bus. A value of 0 specifies that in Big Endian mode byte lanes 15:0 be used for a 16-bit local bus, and byte lane 7:0 for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be <= NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be <= NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR negation until the end of the cycle.(0-3).	Yes	Yes	0

4.3.14 (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor Register

Table 37: Local Address Space 3 Bus Region Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Burst Enable. 1 = Bursting Enabled. 0 = Disabled. Bursting will only occur if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. 1 = READY input enabled. 0 = Disabled.	Yes	Yes	0
2	Bterm Input Enable. 1 = BTERM input enabled. 0 = Disabled, Burst length limited to 4 long words.	Yes	Yes	0
4:3	Prefetch Count. Number of long words to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Don't prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 long words if bit 5 is set. 10 = Prefetch 8 long words if bit 5 is set. 11 = Prefetch 16 long words if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable; When set to a 1, the PCI 9050 will prefetch up to the number of Lwords specified in the prefetch count. When set to a 0, the count will be ignored and prefetching will continue until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Addr wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit, 11 = Reserved	Yes	Yes	10
24	Byte Ordering. 1 = Big Endian, 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A 1 value specifies that in Big Endian mode byte lanes 31:16 be used for a 16-bit local bus, and byte lane 31:24 for an 8-bit local bus. A value of 0 specifies that in Big Endian mode byte lanes 15:0 be used for a 16-bit local bus, and byte lane 7:0 for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be <= NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be <= NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR negation until the end of the cycle.(0-3).	Yes	Yes	0

4.3.15 (EROMBRD; 38h) Expansion ROM Bus Region Descriptor Register

Table 38: Expansion ROM Bus Region Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Burst Enable. 1 = Bursting Enabled. 0 = Disabled. Bursting will only occur if the Prefetch Count is not equal to 00.	Yes	Yes	0
1	Ready Input Enable. 1 = READY input enabled. 0 = Disabled.	Yes	Yes	0
2	Bterm Input Enable. 1 = BTERM input enabled. 0 = Disabled, Burst length limited to 4 long words.	Yes	Yes	0
4:3	Prefetch Count. Number of long words to prefetch during memory read cycle. Only used if bit 5 is high (prefetch count enabled). 00 = Don't prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 long words if bit 5 is set. 10 = Prefetch 8 long words if bit 5 is set. 11 = Prefetch 16 long words if bit 5 is set.	Yes	Yes	0
5	Prefetch Count Enable; When set to a 1, the PCI 9050 will prefetch up to the number of Lwords specified in the prefetch count. When set to a 0, the count will be ignored and prefetching will continue until terminated by the PCI bus.	Yes	Yes	0
10:6	NRAD Wait States. Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0
12:11	NRDD Wait States. Number of Read Data-to-Data wait states (0-3).	Yes	Yes	0
14:13	NXDA Wait States. Number of Read/Write Data-to-Addr wait states (0-3).	Yes	Yes	0
19:15	NWAD Wait States. Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0
21:20	NWDD Wait States. Number of Write Data-to-Data wait states (0-3).	Yes	Yes	0
23:22	Bus Width: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit, 11 = Reserved	Yes	Yes	0
24	Byte Ordering. 1 = Big Endian, 0 = Little Endian	Yes	Yes	0
25	Big Endian Byte Lane Mode. A 1 value specifies that in Big Endian mode byte lanes 31:16 be used for a 16-bit local bus, and byte lane 31:24 for an 8-bit local bus. A value of 0 specifies that in Big Endian mode byte lanes 15:0 be used for a 16-bit local bus, and byte lane 7:0 for an 8-bit local bus	Yes	Yes	0
27:26	Read Strobe Delay. Number of clocks from beginning of cycle until RD strobe is asserted (0-3). This value must be <= NRAD for RD to be asserted.	Yes	Yes	0
29:28	Write Strobe Delay. Number of clocks from beginning of cycle until WR strobe is asserted (0-3). This value must be <= NWAD for WR to be asserted.	Yes	Yes	0
31:30	Write Cycle Hold. Number of clocks from WR negation until the end of the cycle.(0-3).	Yes	Yes	0

4.3.16 (CS0BASE; 3Ch) Chip Select 0 Base Address Register

Table 39: Chip Select 0 Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Chip Select 0 Enable. 1 = Enabled, 0 = Disabled	Yes	Yes	0
27:1	Local Base Address of Chip Select 0. Write zeroes in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning towards bit 27, the first '1' found defines the size. The remaining most significant bits, excluding the first '1' found define the base address.	Yes	Yes	0
31:28	Unused	Yes	No	0

4.3.17 (CS1BASE; 40h) Chip Select 1 Base Address Register

Table 40: Chip Select 1 Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Chip Select 1 Enable. 1 = Enabled, 0 = Disabled	Yes	Yes	0
27:1	Local Base Address of Chip Select 1. Write zeroes in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning towards bit 27, the first '1' found defines the size. The remaining most significant bits, excluding the first '1' found define the base address.	Yes	Yes	0
31:28	Unused	Yes	No	0

4.3.18 (CS2BASE; 44h) Chip Select 2 Base Address Register

Talbe 41: Chip Select 2 Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Chip Select 2 Enable. 1 = Enabled, 0 = Disabled	Yes	Yes	0
27:1	Local Base Address of Chip Select 2. Write zeroes in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning towards bit 27, the first '1' found defines the size. The remaining most significant bits, excluding the first '1' found define the base address.	Yes	Yes	0
31:28	Unused	Yes	No	0

4.3.19 (CS3BASE; 48h) Chip Select 3 Base Address Register

Table 42: Chip Select 3 Base Address Register Description

Field	Description	Read	Write	Value after Reset
0	Chip Select 3 Enable. 1 = Enabled, 0 = Disabled	Yes	Yes	0
27:1	Local Base Address of Chip Select 3. Write zeroes in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning towards bit 27, the first '1' found defines the size. The remaining most significant bits, excluding the first '1' found define the base address.	Yes	Yes	0
31:28	Unused	Yes	No	0

4.3.20 (INTCSR; 4Ch) Interrupt Control/Status Register

Talbe 43: Interrupt Control/Status Register Description

Field	Description	Read	Write	Value after Reset
0	Local interrupt 1 enable. 1 = Enabled. 0 = Disabled.	Yes	Yes	0
1	Local interrupt 1 polarity. 1 = Active high. 0 = Active low.	Yes	Yes	0
2	Local interrupt 1 status. 1 = Interrupt active. 0 = Interrupt not active	Yes	No	0
3	Local interrupt 2 enable. 1 = Enabled. 0 = Disabled.	Yes	Yes	0
4	Local interrupt 2 polarity. 1 = Active high. 0 = Active low.	Yes	Yes	0
5	Local interrupt 2 status. 1 = Interrupt active. 0 = Interrupt not active	Yes	No	0
6	PCI interrupt enable. A value of 1 will enable PCI interrupt.	Yes	Yes	0
7	Software Interrupt. 1 = Generate interrupt.	Yes	Yes	0
31:8	Not used.	Yes	No	0

4.3.21(CNTRL; 50h) User I/O, PCI Target Response, EEPROM, Initialization Control Register

Table 44: User I/O, PCI Target Response, EEPROM, Initialization Control Register Description

Field		Read	Write	Value after Reset
0	User I/O 0 or WAITO Pin Select. This bit selects the function of the USERIO0/WAITO pin. 1 = pin is WAITO; 0 = pin is USER I/O 0.	Yes	Yes	0
1	User I/O 0 direction. 0 = Input, 1 = Output. The pin is always an output if the WAITO function is selected.	Yes	Yes	0
2	User I/O 0 data. If programmed as an output, writing a 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
3	User I/O 1 or LLOCK Pin Select. This bit selects the function of the USERIO1/LLOCK pin. 1 = pin is LLOCK; 0 = pin is USER I/O 1.	Yes	Yes	0
4	User I/O 1 direction. 0 = Input, 1 = Output. The pin is always an output if the LLOCK function is selected.	Yes	Yes	0
5	User I/O 1 data. If programmed as an output, writing a 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
6	User I/O 2 or CS2 Pin Select. This bit selects the function of the USERIO2/CS2 pin. 1 = pin is CS2; 0 = pin is USER I/O 2.	Yes	Yes	0
7	User I/O 2 direction. 0 = Input, 1 = Output. The pin is always an output if the CS2 function is selected.	Yes	Yes	0
8	User I/O 2 data. If programmed as an output, writing a 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
9	User I/O 3 or CS3 Pin Select. This bit selects the function of the USERIO3/CS3 pin. 1 = pin is CS3; 0 = pin is USER I/O 3.	Yes	Yes	0
10	User I/O 3 direction. 0 = Input, 1 = Output. The pin is always an output if the CS3 function is selected.	Yes	Yes	0
11	User I/O 3 data. If programmed as an output, writing a 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
13:12	Local Configuration Base Address Register (BAR) Enables. 00 = BAR0 (Memory) and BAR1 (I/O) enabled. 01 = BAR0 (Memory) only. 10 = BAR1 (I/O) only. 11 = BAR0 (Memory) and BAR1 (I/O) enabled.	Yes	Yes	00
14	PCI Read Mode. 1 = disconnect immediately for a read. Then prefetch the data into the direct slave read FIFO. Return data when PCI read cycle is retried (PCI 2.1 compatible). 0 = negate TRDY until read data is available.	Yes	Yes	0
15	PCI Read with Write Flush Mode. 1 = flush a pending read cycle if a write cycle is detected. 0 = Don't effect pending reads when a write cycle occurs (PCI 2.1 compatible)	Yes	Yes	0
16	PCI Read No Flush Mode. 1 = don't flush the read FIFO if the PCI read cycle completes (cached read mode) 0 = Flush the read FIFO if a PCI read cycle completes	Yes	Yes	0
17	PCI Read No Write Mode. 1 = force retry on writes if read pending. 0 = allow write to occur while read is pending.	Yes	Yes	0
18	PCI Write Mode. 1 = disconnect if write FIFO becomes full. 0 = negate TRDY until space is available in the direct slave write FIFO.	Yes	Yes	0

22:19	PCI Target Retry Delay Clocks. The number of PCI clocks (multiplied by 8) after the beginning of a direct slave cycle until a retry is issued. Only valid for read cycles if bit 14 is low. Only valid for write cycles if bit 17 is low.	Yes	Yes	0
23	Direct Slave Lock Enable. 1 = enable PCI direct slave locked sequences. 0 = disable direct slave locked sequences.	Yes	Yes	0
24	EEPROM clock for Local or PCI bus reads or writes to EEPROM. Toggling this bit generates an EEPROM clock. Refer to the manufacturer's data sheet for the particular EEPROM being used.	Yes	Yes	0
25	EEPROM chip select. For Local or PCI bus reads or writes to EEPROM, setting this bit to a 1 provides the EEPROM chip select.	Yes	Yes	0
26	Write bit to EEPROM. For writes, this output bit is the input to the EEPROM. It is clocked into the EEPROM by the EEPROM clock.	Yes	Yes	0
27	Read EEPROM data bit. For reads, this input bit is the output of the EEPROM. It is clocked out of the EEPROM by the EEPROM clock.	Yes	No	--
28	EEPROM valid. A 1 in this bit indicates that a valid EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When this bit is 0, writing a 1 causes the PCI 9050 to reload the PCI configuration registers from EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. A value of 1 written to this bit will reset the PCI 9050 and issue a reset to the local bus. The contents of the PCI and Local configuration registers will not be reset.	Yes	Yes	0
31	Mask Revision	Yes	No	0

5. SECTION 5 - PIN DESCRIPTION

5.1 Pin Summary

The following tables describe the PCI 9050 pins:

Power and Ground Pin Description
EEPROM interface Pin Description
PCI System Bus Interface Pin Description
Local Bus Support Pin Descriptions
Local Bus Data Transfer Pin Descriptions

Unspecified pins are no connects.

The following abbreviations are used for pin types:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Tri-state Pin
OC - Open Collector Pin
TP - Totem Pole Pin
STS - Sustained Tri-state Pin, driven high for 1 CLK before float

All local bus inputs (Pin Type I) are internally connected to Vcc through a 10k ohm pull-up resistor.

Table 1 Power and Ground Pin Description (23 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	99	Test Pin. Pull high for test, low for normal operation. When TEST is pulled high, all outputs except RD# (pin 126) are placed in tri-state. RD# provides a NAND-TREE output when TEST is pulled high.
SPARE	Spare	2		45,67	Unused
VDD	Power	10	I	1,10,27,41,50,66,81,103,121,146	Five volt power supply pins. Liberal .01 uF to .1 uF decoupling capacitors should be placed near the PCI 9050.
VSS	Ground	10	I	9,26,40,51,65,80,104,120,147,160	Ground pins.

Table 2 EEPROM Interface Pin Description (4 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	EEPROM Chip Select	1	O TP 6 mA	142	EEPROM Chip Select
EEDO	EEPROM Data OUT	1	I	143	EEPROM Read data
EEDI	EEPROM Data In	1	O TP 6MA	145	EEPROM Write data
EESK	EEPROM Serial Data Clock	1	O TP 6 mA	144	EEPROM Clock

Table 3 PCI System Bus Interface Pin Description (49 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS 6mA	150,151,152, 153,154,155, 156,157,2,3, 4,5,6,7,8,11, 23,24,25,28, 29,30,31,32, 34,35,36,37, 38,39,42,43	These are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The PCI 9050 supports both read and write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	158,12,22,33	These are multiplexed on the same PCI pins. During the address phase of a transaction C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. Refer to PCI spec for further detail if needed.
CLK	Clock	1	I	149	This provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33MHz.
DEVSEL#	Device Select	1	O STS 6mA	16	When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	Cycle Frame	1	I	13	This is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase.
IDSEL	Initialization Device Select	1	I	159	This is used as a chip select during configuration read and write transactions.
INTA#	Interrupt A	1	O OC 6mA	44	This is used to request an interrupt.
IRDY#	Initiator Ready	1	I	14	This indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
LOCK#	Lock	1	I	18	Lock indicates an atomic operation that may require multiple transactions to complete.

PAR	Parity	1	I/O TS 6mA	21	This is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.
PERR#	Parity Error	1	O STS 6mA	19	This is only the reporting of data parity errors during all PCI transactions except a Special Cycle.
RST#	Reset	1	I	148	This is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	Systems Error	1	O OC 6mA	20	This is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	O STS 6mA	17	This indicates the current target is requesting the master to stop the current transaction.
TRDY#	Target Ready	1	O STS 6mA	15	This indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.

Table 4 Local Bus Support Pin Descriptions (14 Pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
MODE	Bus Mode	1	I	68	Selects the bus operation mode of the PCI 9050: 1 = multiplexed bus, 0 = non-multiplexed
LINTI1	Local Interrupt 1 In	1	I	137	When asserted causes a PCI interrupt. Polarity is determined by INTCSR configuration register.
LINTI2	Local Interrupt 2 In	1	I	136	When asserted causes a PCI interrupt. Polarity is determined by INTCSR configuration register.
LCLK	Local Bus Clock	1	I	135	Local clock up to 33 MHz, and may be asynchronous to the PCI clock.
LHOLD	Hold Request	1	I	134	A local bus master asserts LHOLD to request use of the local bus.
LHOLDA	Hold Acknowledge	1	O TP 6mA	133	The PCI 9050 asserts LHOLDA to grant control of the local bus to a local bus master. When the PCI 9050 needs the local bus, it can signal a preempt by negating LHOLDA
LRESET#	Local Reset Out	1	O TP 6 MA	132	This pin is the Local bus reset output. It is asserted when the PCI 9050 chip is reset, and is used to reset devices on the local bus.
BCLKO	BCLK Out	1	O TP 6MA	63	This is a buffered version of the PCI clock for optional use by the local bus.

CS[1:0]#	Chip selects	2	O TS 6mA	131,130	These are general purpose chip selects. The base and range of each may be programmed in the configuration registers
USER0/WAITO#	User I/O 0 or WAIT Out	1	I/O TS 6 mA	138	This pin can be programmed to be either a configurable User I/O pin, or the local bus WAIT out pin. WAITO# is asserted when wait states are being caused by the internal wait state generator. It can be thought of as an output providing ready out status.
USER1/LLOCK#	User I/O 1 or LLOCK Out	1	I/O TS 6 mA	139	This pin can be programmed to be either a configurable User I/O pin, or the local bus LLOCK out pin. Lock indicates an atomic operation that may require multiple transactions to complete and can be used by the local bus to lock resources.
USER2/CS2#	User I/O 2 or CS2 Out	1	I/O TS 6 mA	140	This pin can be programmed to be either a configurable User I/O pin, or as the Chip Select 2 pin.
USER3/CS3#	User I/O 3 or CS3 Out	1	I/O TS 6 mA	141	This pin can be programmed to be either a configurable User I/O pin, or as the Chip Select 3 pin.

Table 5 Local Bus Data Transfer Pins Description (Mode Independent) (7 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	O TS 24 mA	123	Address strobe indicates valid address and the start of a new bus access. ADS# is asserted for the first clock of a bus access.
ALE	Address Latch Enable	1	O TS 6mA	64	ALE is asserted during the address phase and negated before the data phase.
LW/R	Write/Read	1	O TS 6 mA	127	LW/R is asserted high for writes and low for reads.
BLAST#	Burst Last	1	O TS 6 mA	124	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
RD#	Read Strobe	1	O TS 24mA	126	General purpose read strobe. The timing is controlled by the current Bus Region Descriptor Register.
WR #	Write Strobe	1	O TS 24mA	125	General purpose write strobe. The timing is controlled by the current Bus Region Descriptor Register.
LRDYI#	Local Ready In	1	I	128	Local ready input indicates that read data is on the local bus, or that write data has been accepted. LRDYI# is used in conjunction with the programmable wait state generator.

Table 6 Local Bus Data Transfer Pins Description (Non-multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If BTERM# is disabled through the PCI 9050 configuration registers, the PCI 9050 will burst up to 4 Lwords, depending upon the bus width and type. If enabled, the PCI 9050 will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122,119,118, 117,116,115, 114,113,112, 111,110,109, 108,107,106, 105,102,101, 100,98,97,969 5,94,93,92	Address bus carries the upper 26 bits of the 28-bit physical address bus. During bursts [LA27:2] increment to indicate successive data cycles.
LAD[31:00]	Data Bus	32	I/O TS 6 mA	52,53,54,55, 56,57,58,59, 60,61,62,69,70 ,71,72,73, 74,75,76,77, 78,79,82,83, 84,85,86,87, 88,89,90,91	Data bus carries 32,16, or 8 bit data quantities depending on bus width configuration. 8-bit LD[7:0] 16-bit LD[15:0] 32-bit LD[31:0]

LBE[3:0]#	Byte Enables	4	O TS 24 mA	46,47,48,49	The byte enables are encoded based on configured bus width as follows: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LAD[31:24] BE2# Byte Enable 2 - LAD[23-16] BE1# Byte Enable 1 - LAD[15-8] BE0# Byte Enable 0 - LAD[7-0] For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provide BHE#, A1, and BLE# respectively. BE3# Byte High Enable (BHE#) - LAD[15:8] BE2# not used BE1# Address bit 1 (A1) BE0# Byte Low Enable (BLE#) - LAD[7-0] For an 8 bit bus BE1# and BE0# are encoded to provide A1and A0 respectively. BE3# not used BE2# not used BE1# Address bit 1 (A1) BE0# Address bit 0 (A0)

Table 7 Local Bus Data Transfer Pins Description (Multiplexed Mode) (63 pins)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I	129	If BTERM# is disabled through the PCI 9050 configuration registers, the PCI 9050 will burst up to 4 Lwords. If enabled, the PCI 9050 will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the wait state generator.
LA[27:2]	Address Bus	26	O TS 6 mA	122,119,118, 117,116,115, 114,113,112, 111,110,109, 108,107,106, 105,102,101, 100,98,97,96 95,94,93,92	Address bus carries the upper 26 bits of the 28-bit physical address bus. During bursts [LA27:2] increment to indicate successive data cycles.

LAD[31:00]	Address/Data Bus	32	I/O TS 6 mA	52,53,54,55, 56,57,58,59, 60,61,62,69, 70,71,72,73, 74,75,76,77, 78,79,82,83, 84,85,86,87, 88,89,90,91	During the address phase the bus carries the upper 26 bits of the 28-bit physical address bus. During the data phase the bus carries 32,16, or 8 bit data quantities depending on bus width configuration. 8-bit LAD[7:0] 16-bit LAD[15:0] 32-bit LAD[31:0]
LBE[3:0]#	Byte Enables	4	I/O TS 24 mA	46,47,48,49	The byte enables are encoded based on configured bus width as follows: For a 32 bit bus, the four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LAD[31:24] BE2# Byte Enable 2 - LAD[23-16] BE1# Byte Enable 1 - LAD[15-8] BE0# Byte Enable 0 - LAD[7-0] For a 16 bit bus, BE3#, BE1#, and BE0# are encoded to provide BHE#, A1, and BLE# respectively. BE3# Byte High Enable (BHE#) - LAD[15:8] BE2# not used BE1# Address bit 1 (A1) BE0# Byte Low Enable (BLE#) - LAD[7-0] For an 8 bit bus BE1# and BE0# are encoded to provide A1and A0 respectively. BE3# not used BE2# not used BE1# Address bit 1 (A1) BE0# Address bit 0 (A0)

6. SECTION 6 - ELECTRICAL AND TIMING SPECIFICATIONS

Absolute Maximum Ratings

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS -0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS -0.5V VDD + 0.5V

Operating Ranges

Ambient Temp.	Junction Temp.	Supply Voltage (VDD)	Input Voltage (VIN)
0 °C to +70 °C	115 °C Maximum	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -4.0 mA	2.4		V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Tables		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
IOZ	Tri-state Output Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
ICC	Power Supply Current	VDD=5.25V, PCLK=LCLK=33Mhz			130	mA

AC Electrical Characteristics (Local Outputs) Measured Over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, VCC = 5.0± 5%	T_{VALID} (MIN) NSEC (HOLD)	T_{VALID} NSEC Typical min/max	T_{VALID} (MAX) NSEC (WORST CASE)
LHOLDA	3	-	9
ADS#	3	8	10
BLAST#	5	9	16
LBE[3:0]#	4	10	15
LW/R#	4	7	12
LD[31:0]	5	11	16
LA[27:2]	5	10	14
LRESET#	5*	14	17*
RD#	7	16	27
ALE	4	8/23	12
WR#	4	8	13
BCLKo	2	7	8
USER0/WAIT0#	4*	5 PCLK /8	12*
USER1/LLOCK#	4*	5 PCLK /8	12*
USER2/CS2#	5*	5 PCLK /11	17*
USER3/CS3#	5*	5 PCLK /11	17*
CS[1:0]#	4	11	17

Note: The values with an asterisk(*) following them are referenced from the PCI side.

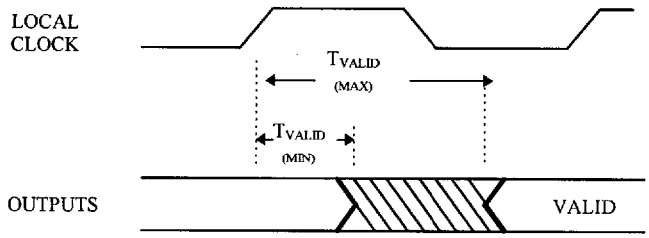


Figure 2. PCI 9050 Local Output Delay

Local Bus Input Set-up and Hold Times:

- hold time = 2 ns min
- setup time = 8 ns max

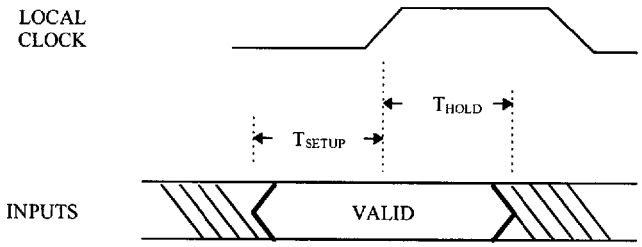


Figure 3. PCI 9050 Local Input Setup and Hold Waveform

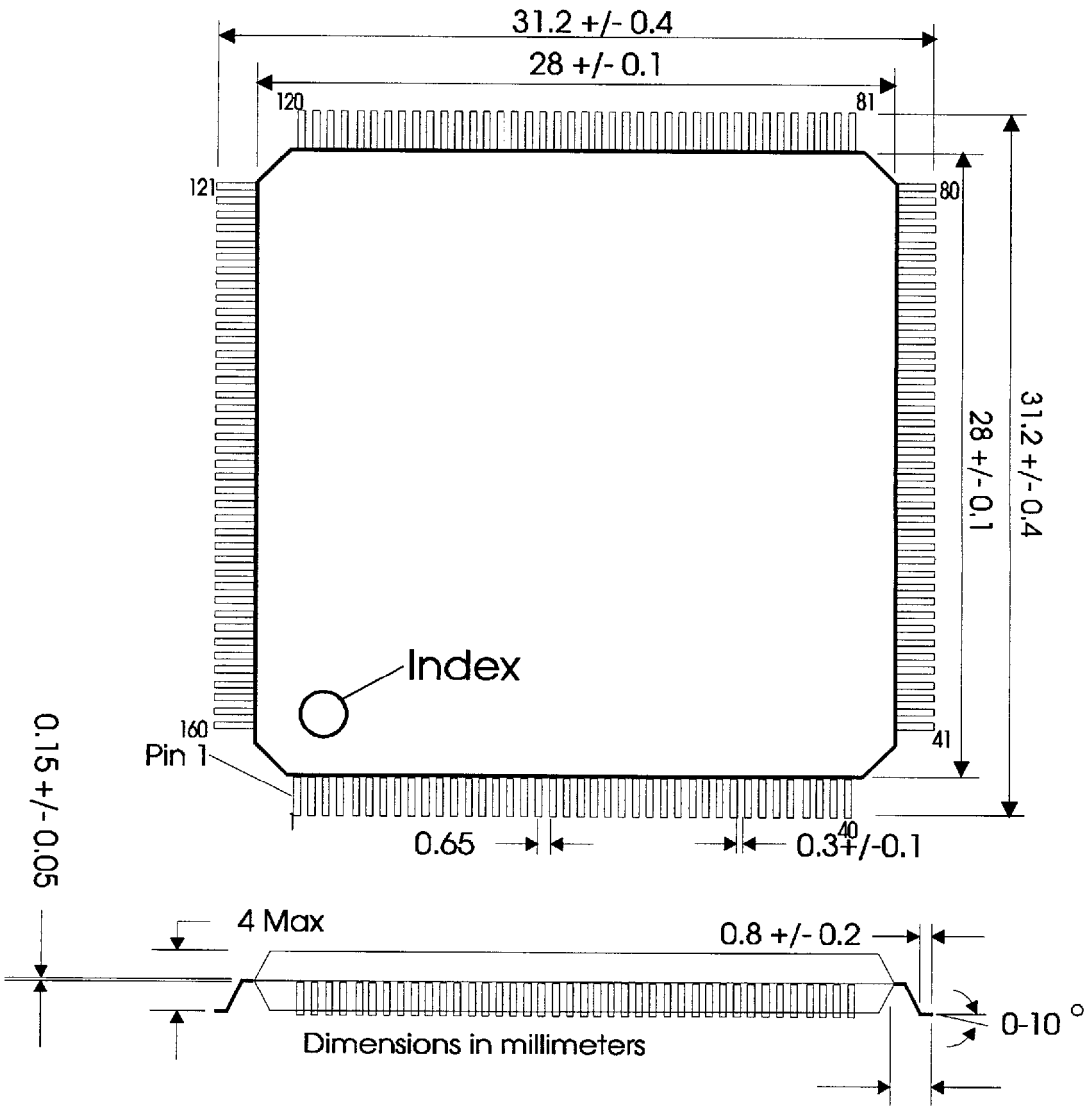
Clock Frequencies:

	Min	Max
Local Clock Input Frequency	0	40 MHz
PCI Clock Input Frequency	0	33 MHz

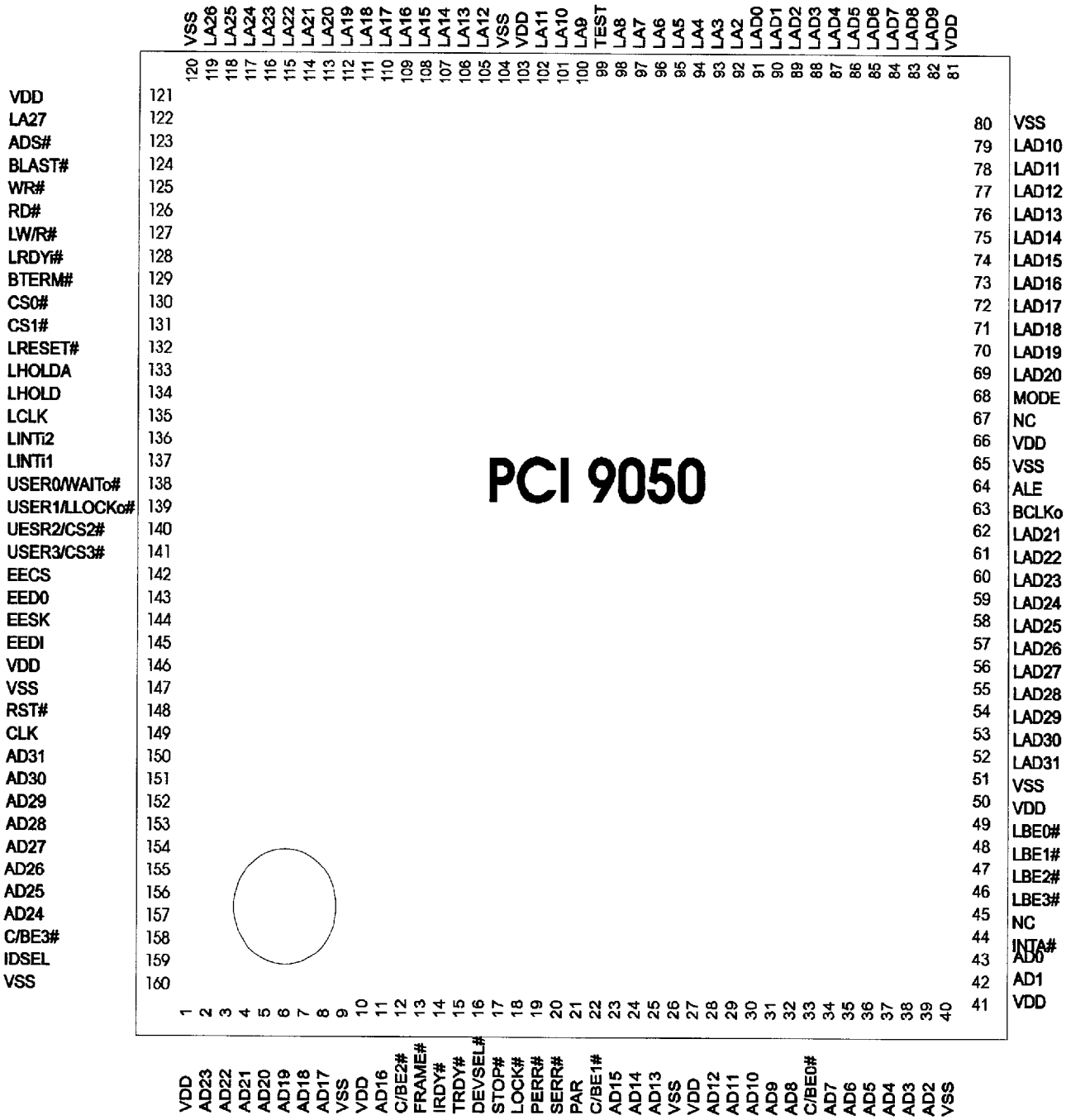
7. SECTION 7 - PACKAGE MECHANICAL DIMENSIONS

7.1 PACKAGE MECHANICAL DIMENSIONS

For 160 pin PQFP



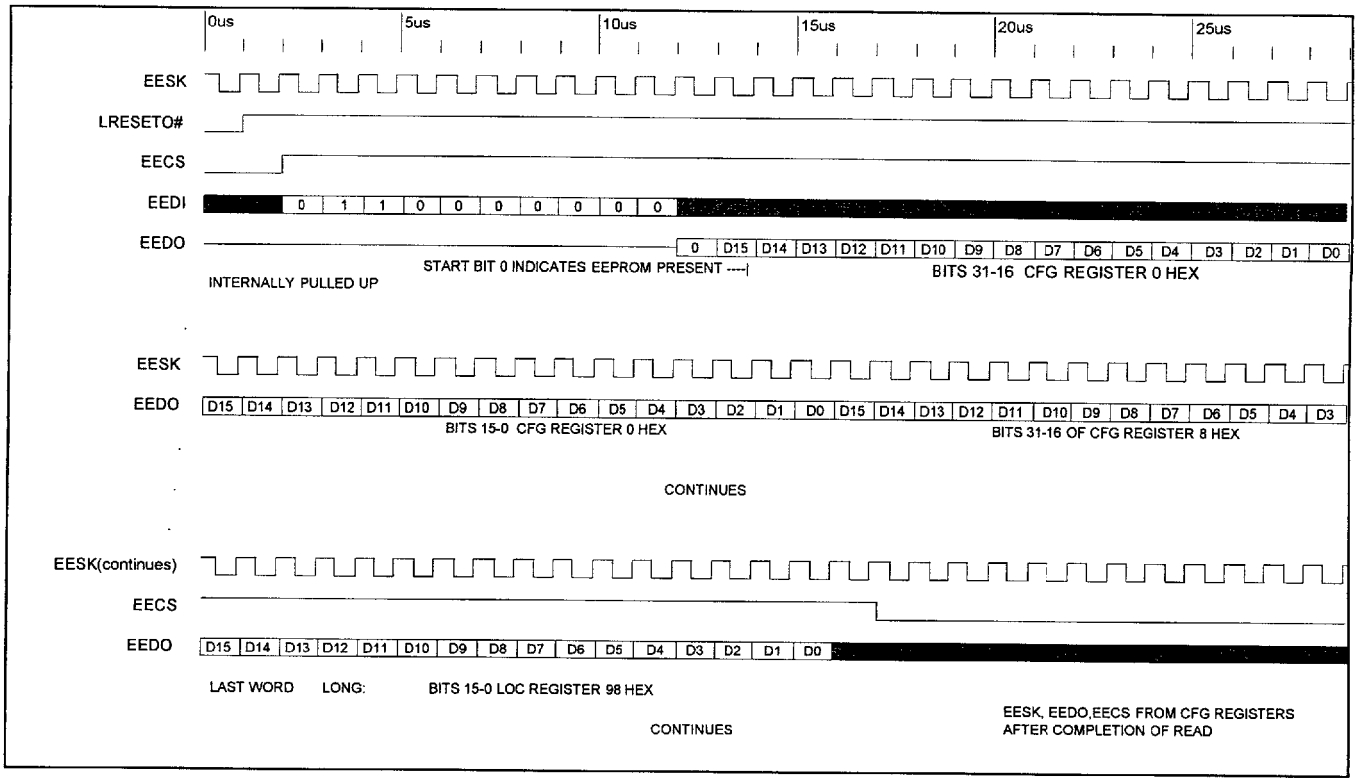
7.2 PCI 9050 PIN OUT



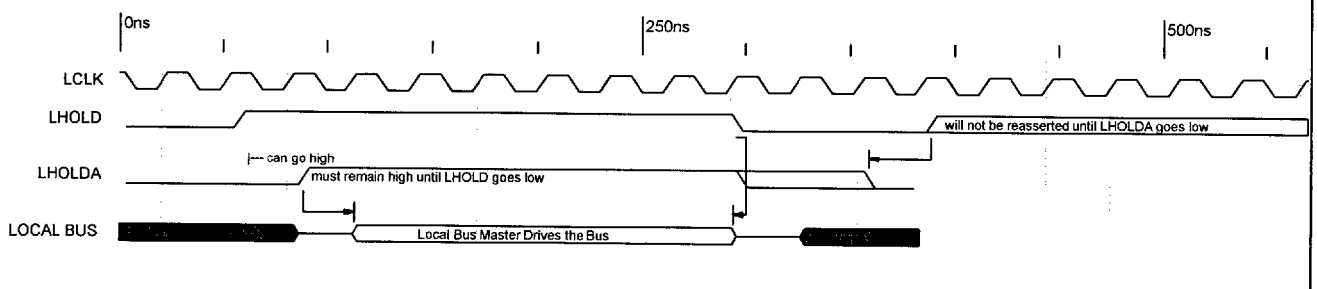
SECTION 8- TIMING DIAGRAMS

List of Timing Diagrams

Timing Diagram 1. Initialization from Serial EEPROM

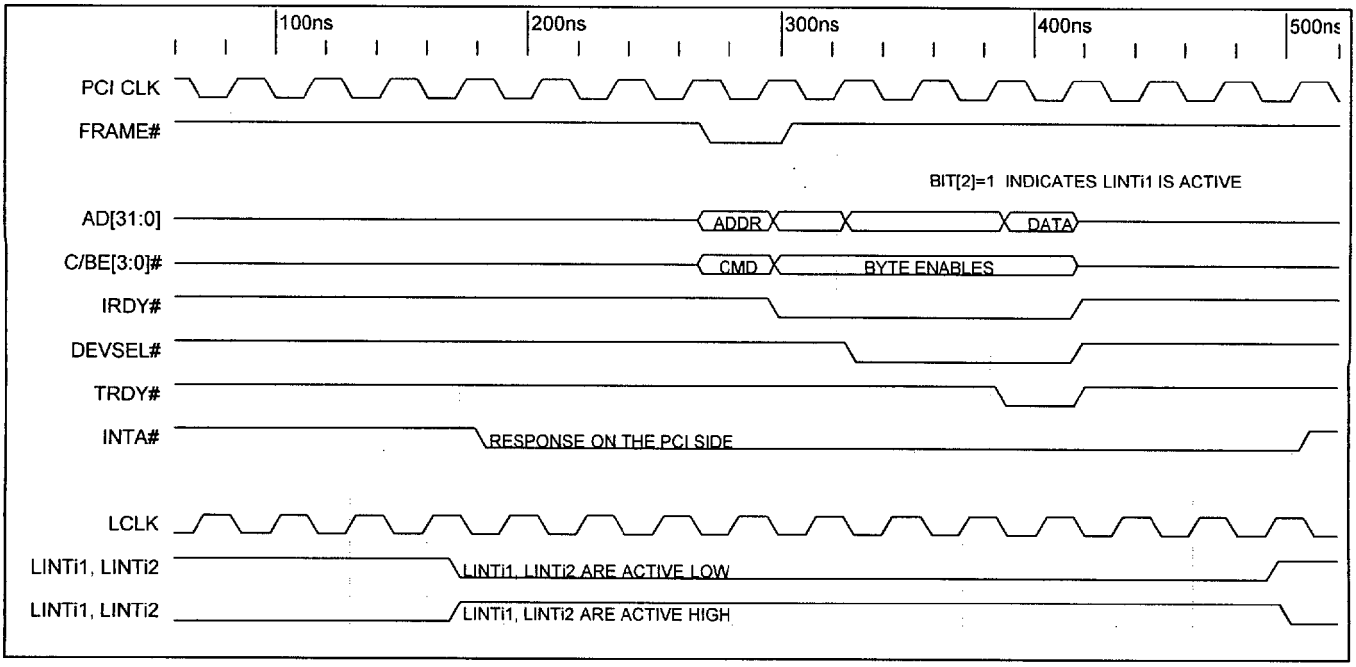


Timing Diagram 2. PCI9050 Local bus Arbitration

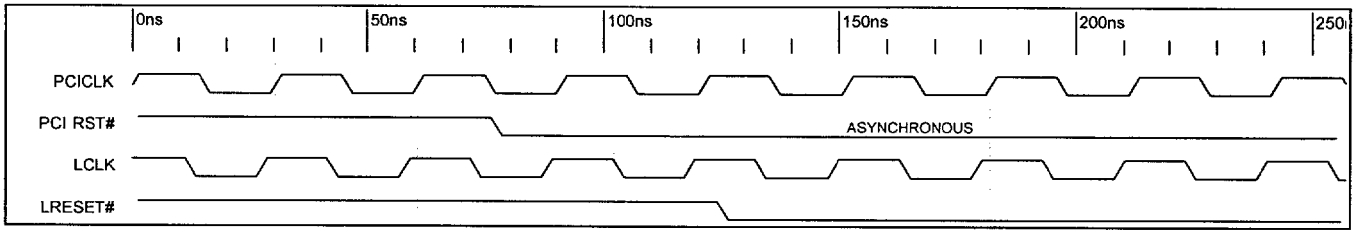


PCI9050 always gives up bus between different Direct Slave access.

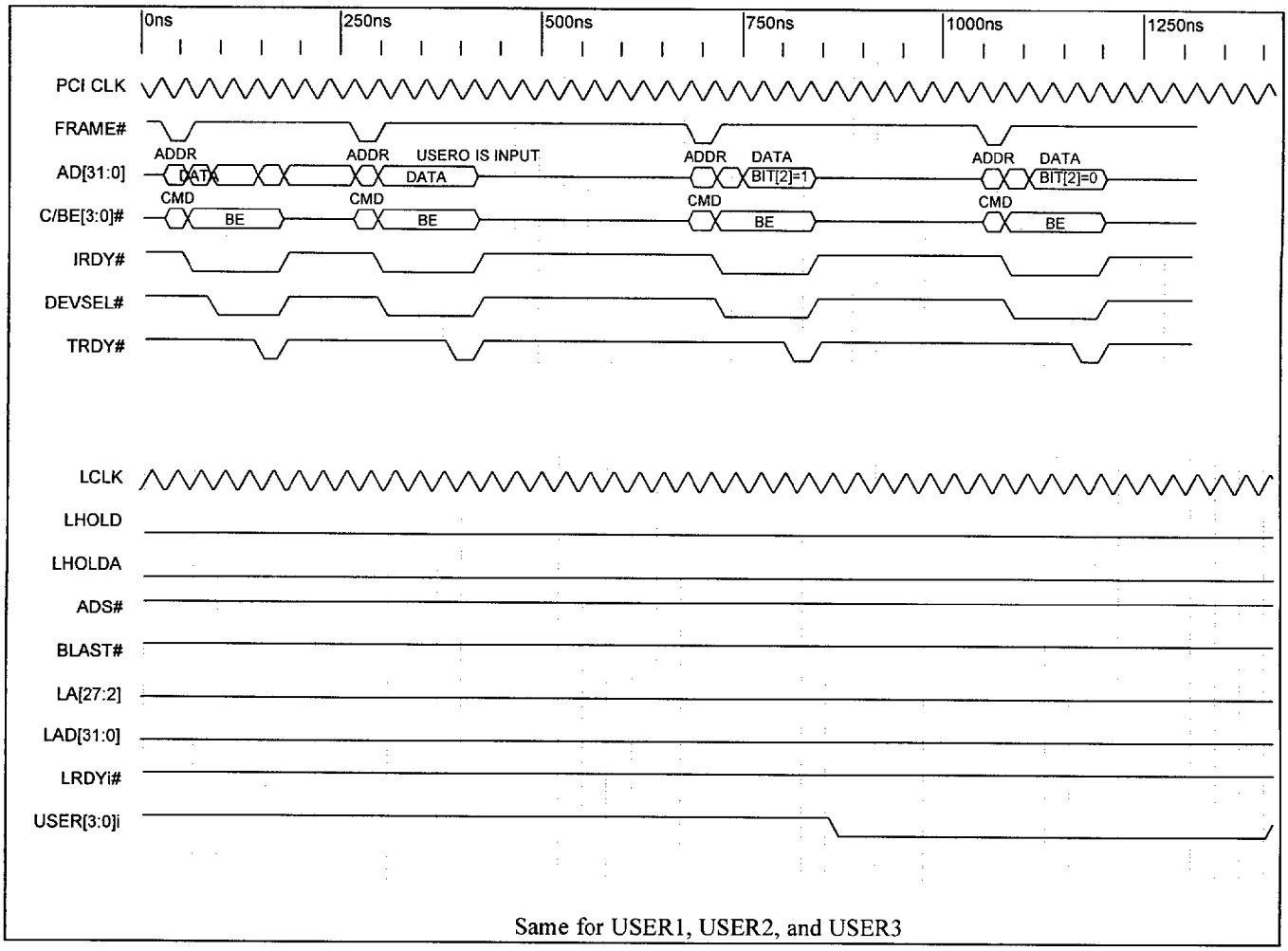
Timing Diagram 3. Local LINTi1# Input Asserting PCI Output INTA#



Timing Diagram 4. PCI RST# Asserting Local Output LRESET#

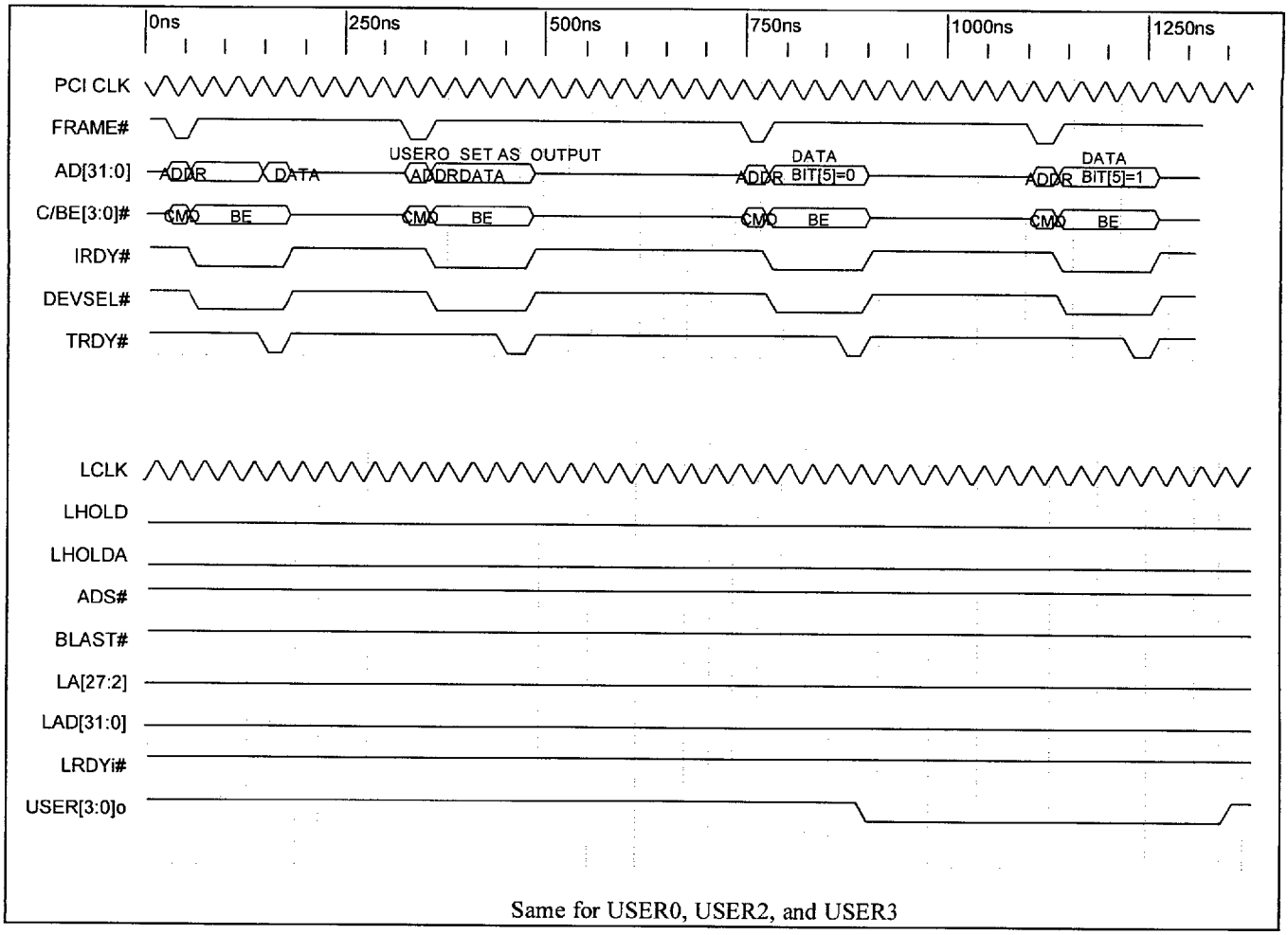


Timing Diagram 5. USER I/O Pin 0 is an Input



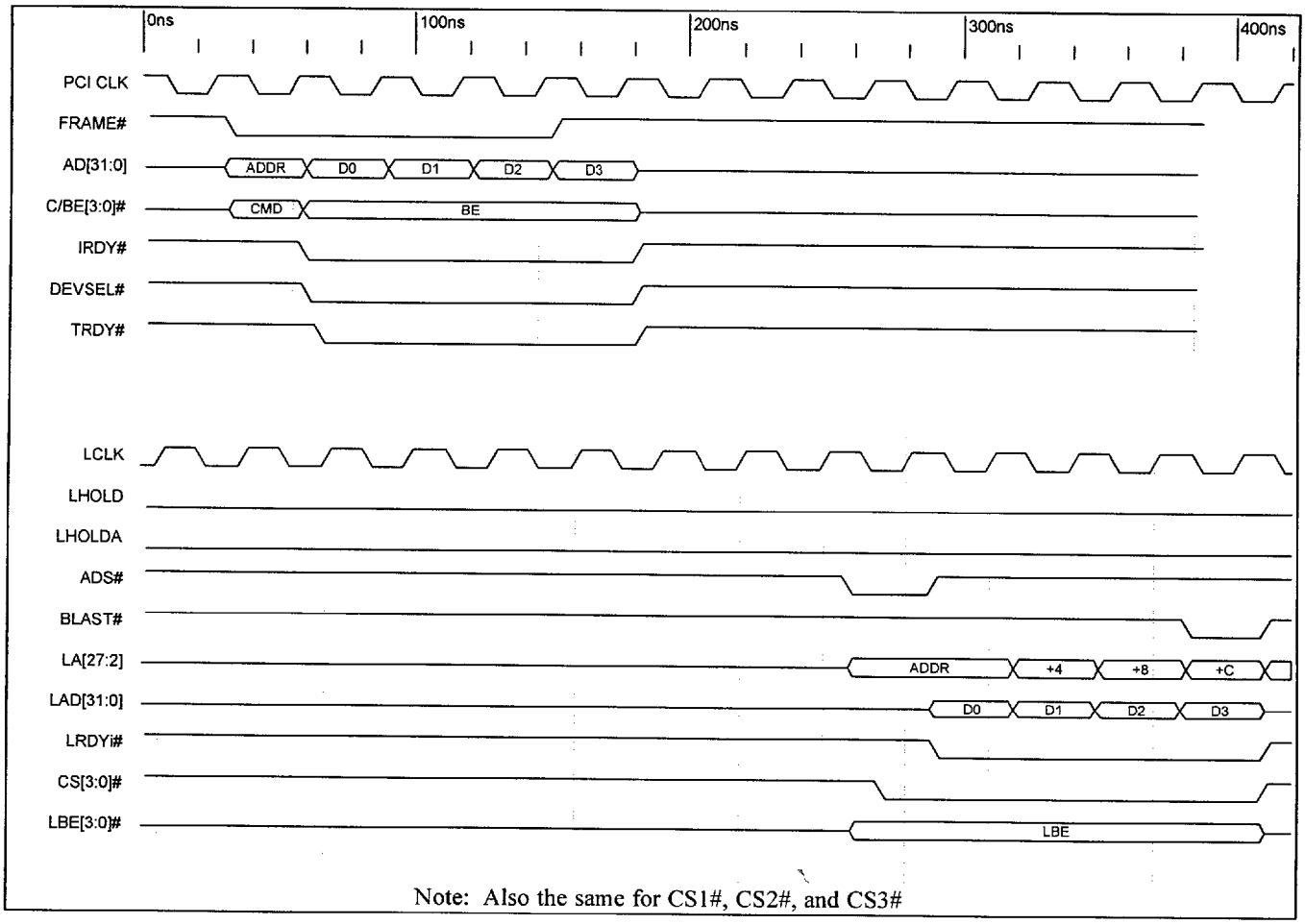
Same for USER1, USER2, and USER3

Timing Diagram 6. USER I/O Pin 1 is an Output



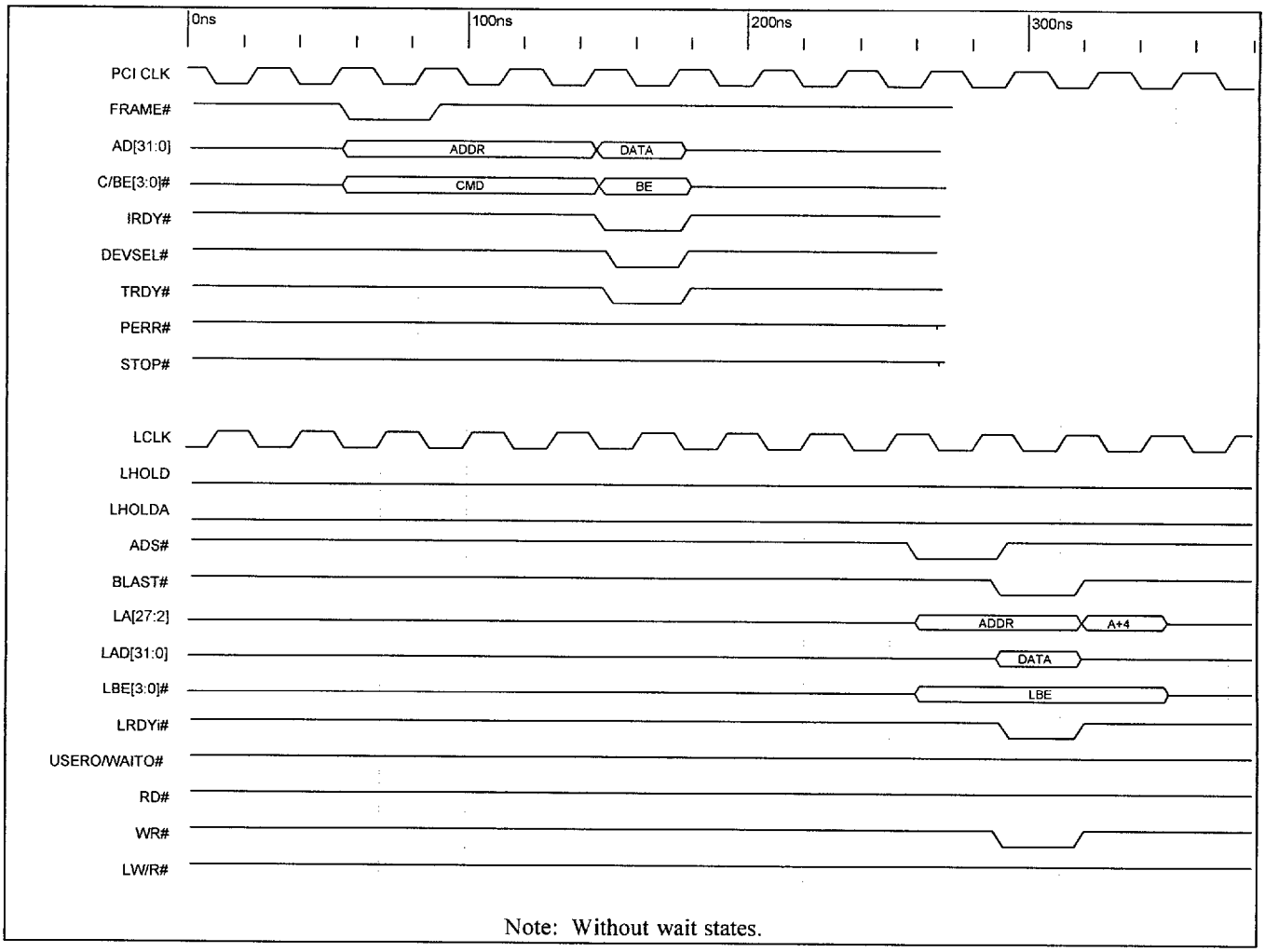
Same for USER0, USER2, and USER3

Timing Diagram 7. Chip Select 0 (CS0#)



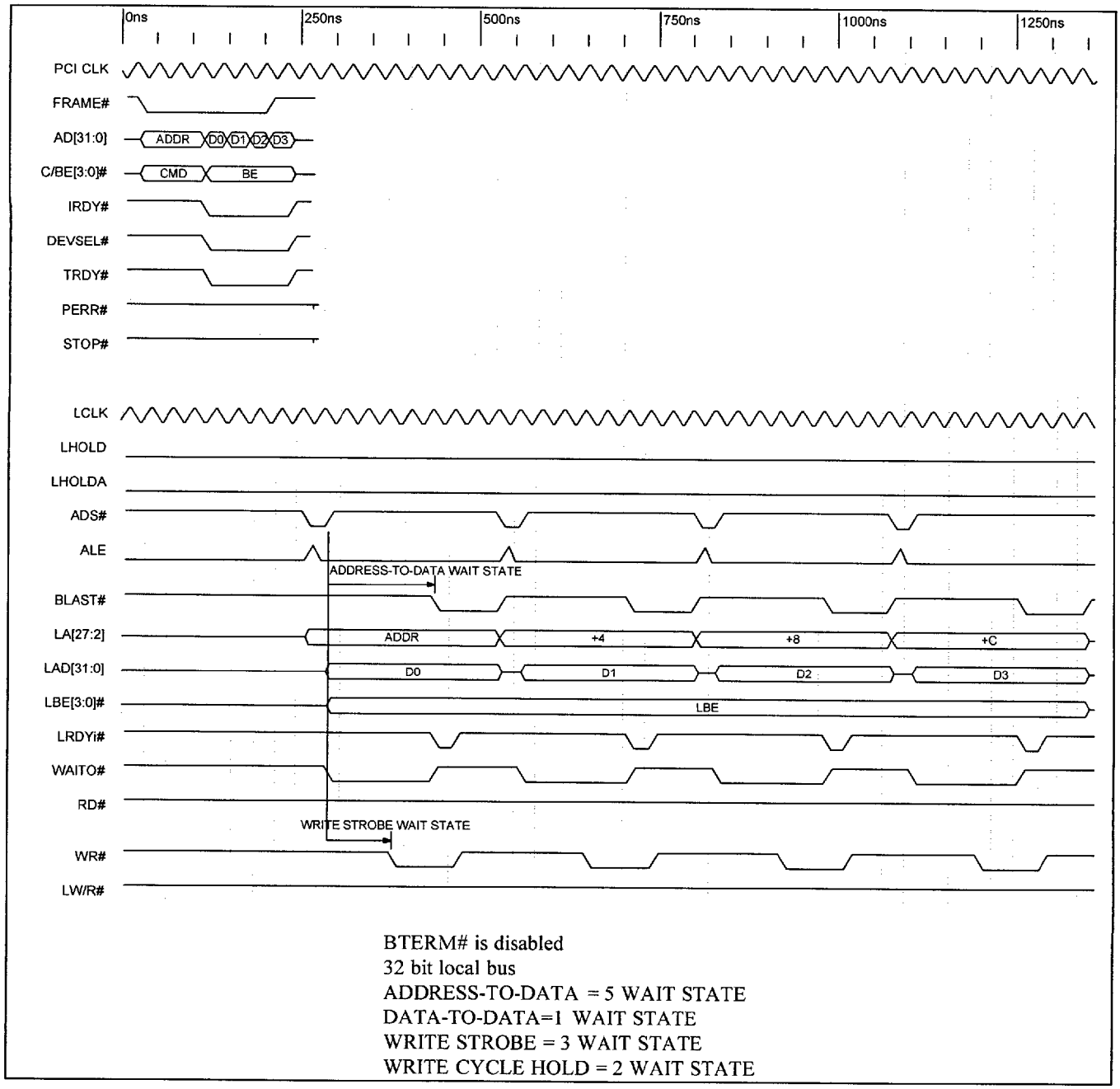
Note: Also the same for CS1#, CS2#, and CS3#

Timing Diagram 8. Direct Slave Single Write(32 Bit Local Bus)



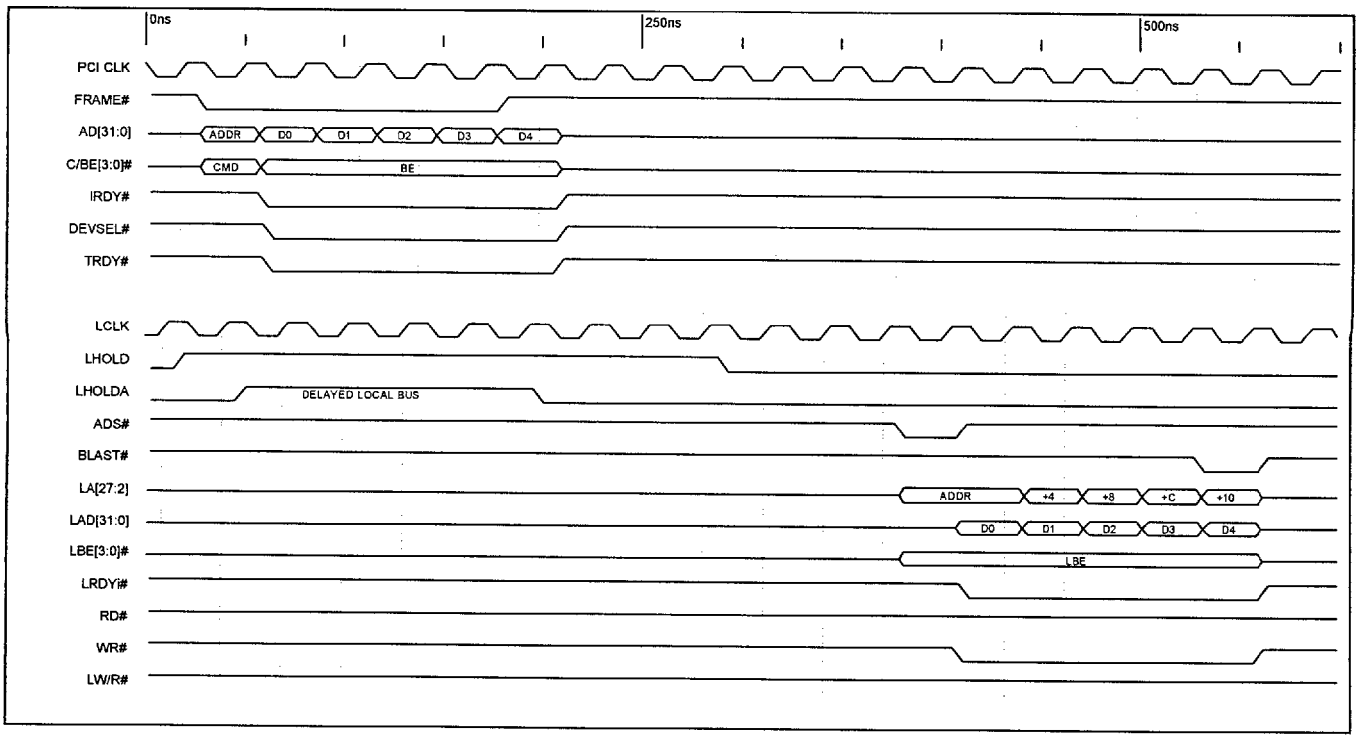
Note: Without wait states.

Timing Diagram 9. Direct Slave NON-Burst Write With Wait States(32 Bit Local Bus)

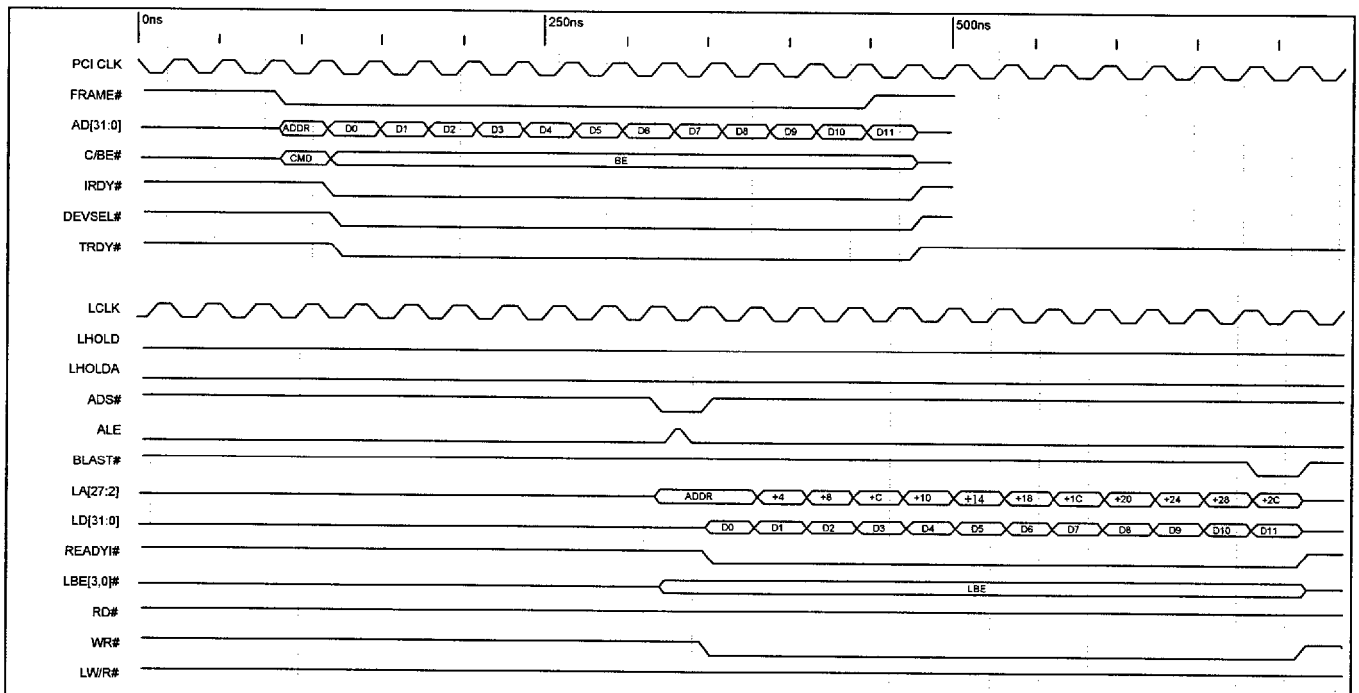


BTERM# is disabled
32 bit local bus
ADDRESS-TO-DATA = 5 WAIT STATE
DATA-TO-DATA=1 WAIT STATE
WRITE STROBE = 3 WAIT STATE
WRITE CYCLE HOLD = 2 WAIT STATE

Timing Diagram 10. Direct Slave Burst Write With Delayed Local Bus(32 Bit Local Bus)

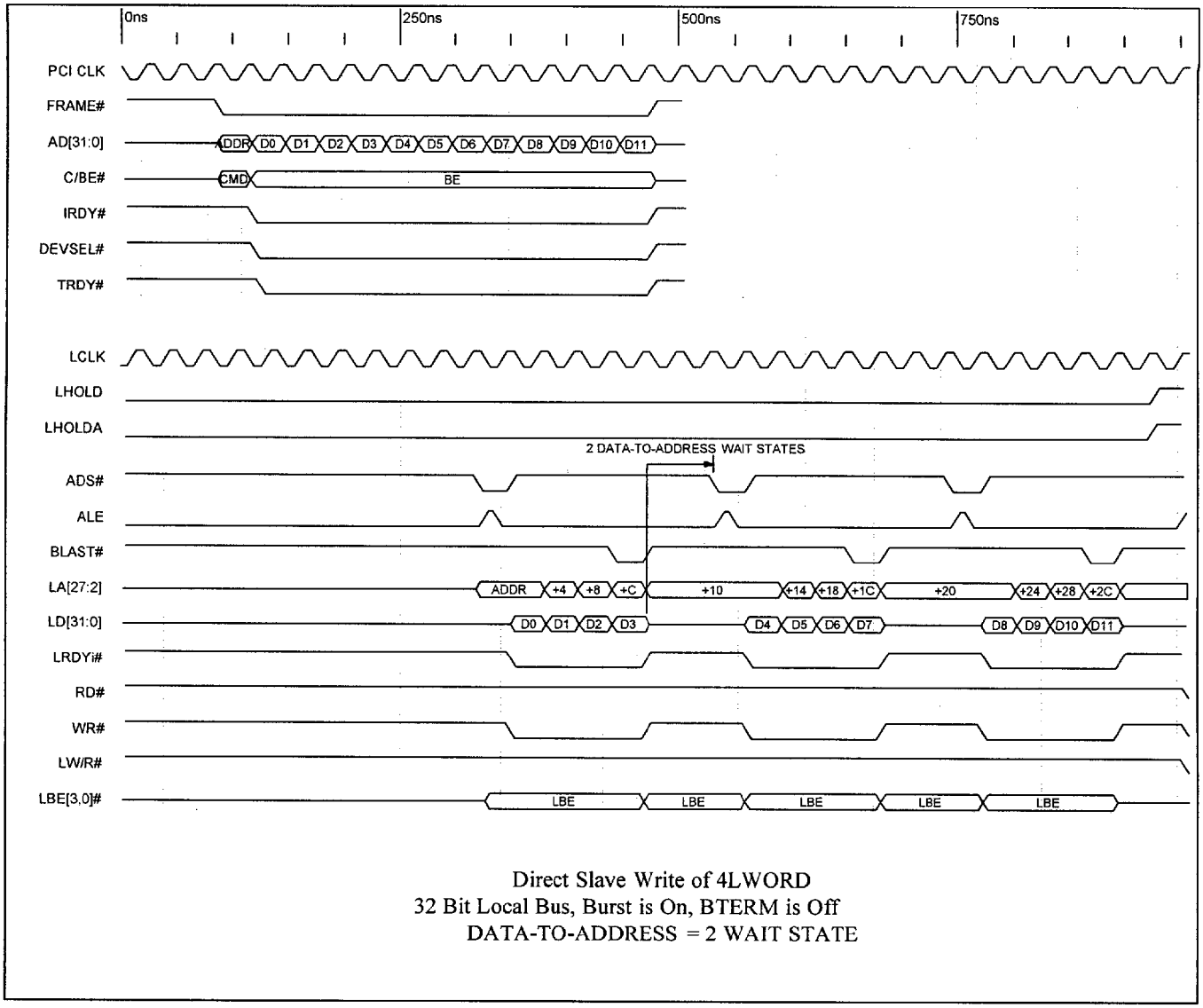


Timing Diagram 11. Direct Slave Burst Write With BTERM On(32 Bit Local Bus)



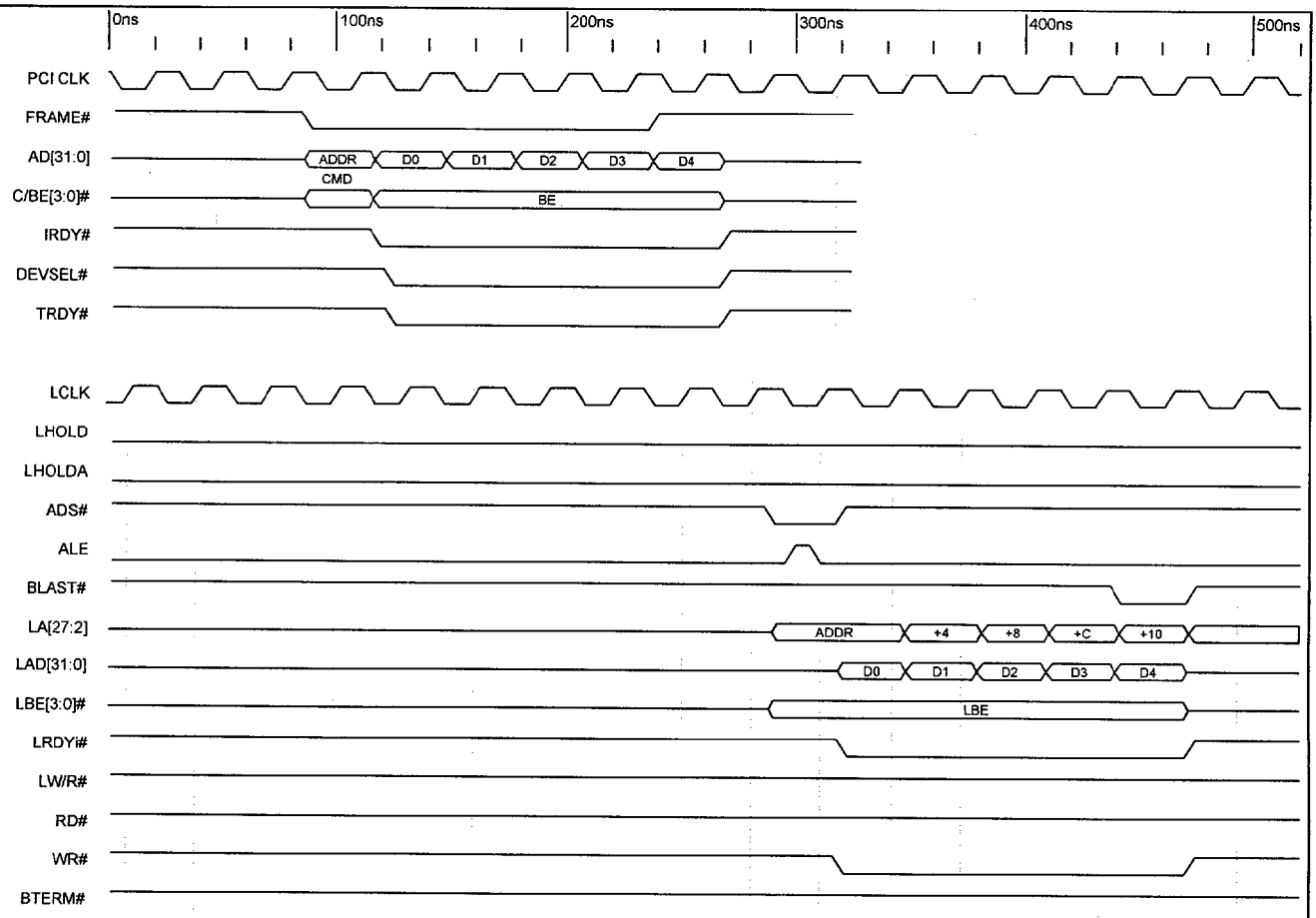
Burst is On, BTERM is On
This is for Space 2 but it is the same for Space 0, 1, 3, and Expansion ROM

Timing Diagram 12. Direct Slave Burst Write With BTERM Off and With Wait States(32 Bit Local Bus)



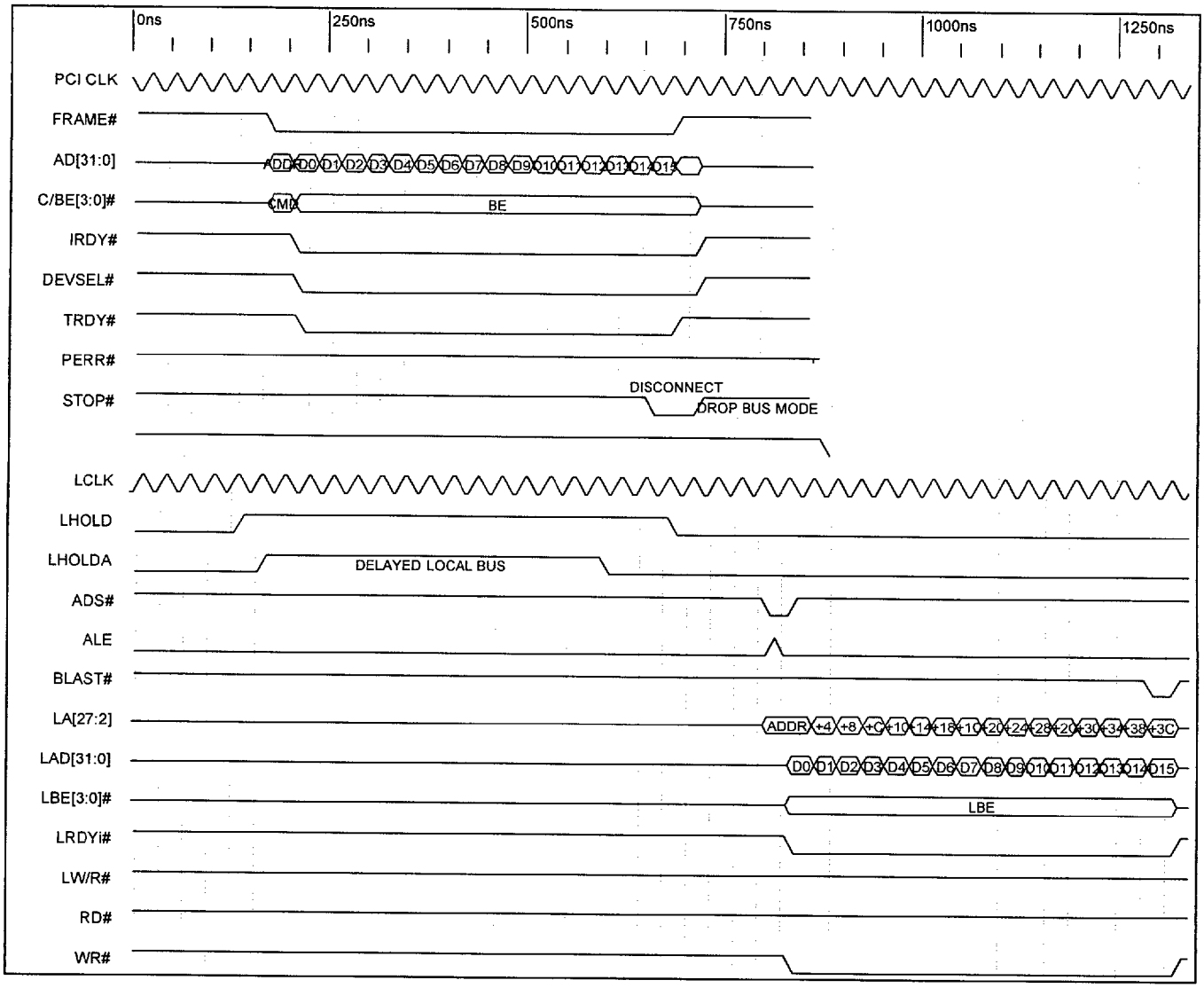
Direct Slave Write of 4LWORD
32 Bit Local Bus, Burst is On, BTERM is Off
DATA-TO-ADDRESS = 2 WAIT STATE

Timing Diagram 13. Direct Slave Burst Write With BTERM# Enabled(32 Bit Local Bus)

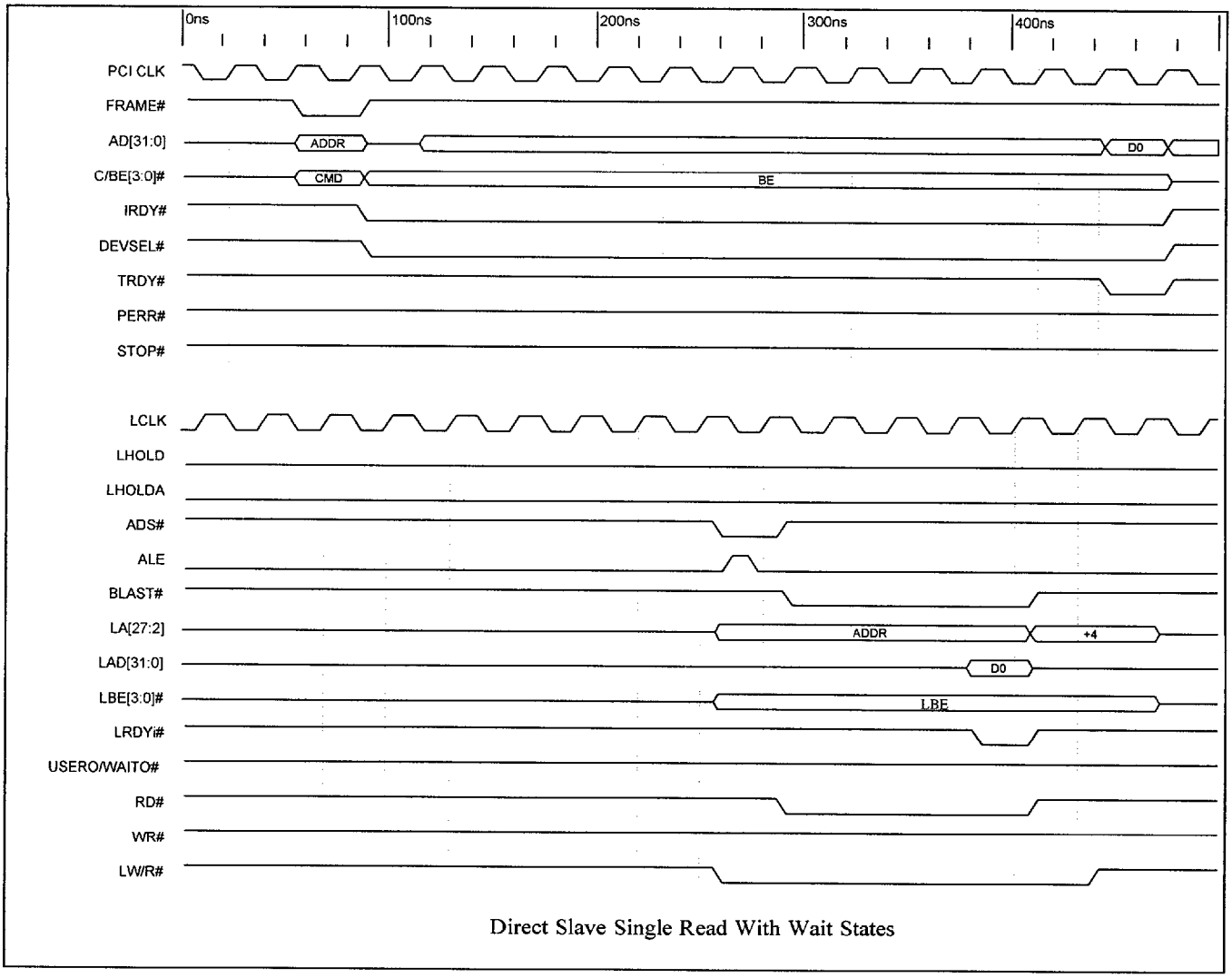


Burst Write of 5 LWORDS
BTERM# is Enabled
32 Bit Local Bus

Timing Diagram 14. Direct Slave Write 2.1 Spec(32 Bit Local Bus)

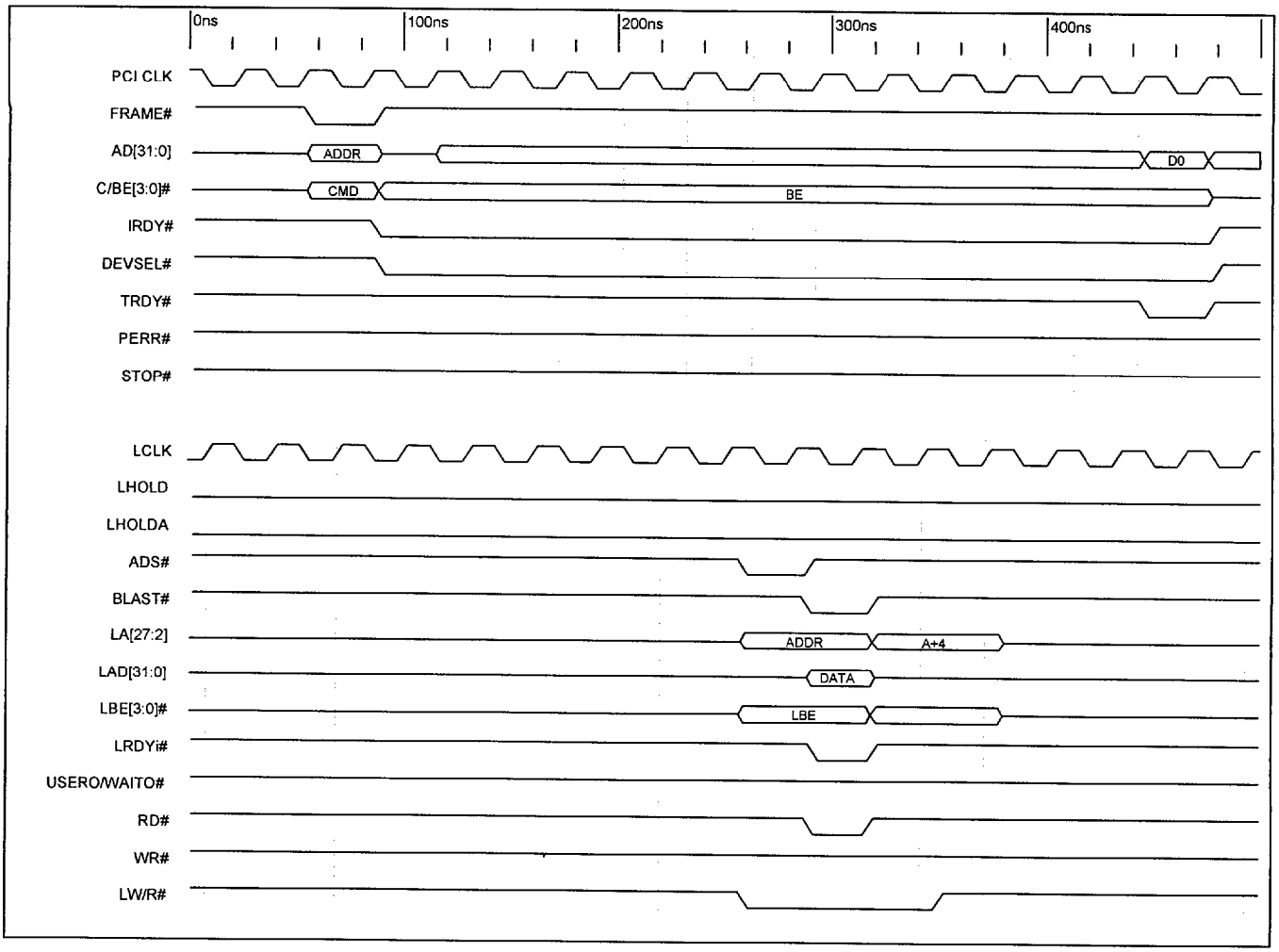


Timing Diagram 15. Direct Slave Single Read With Wait States (32 Bit Local Bus)

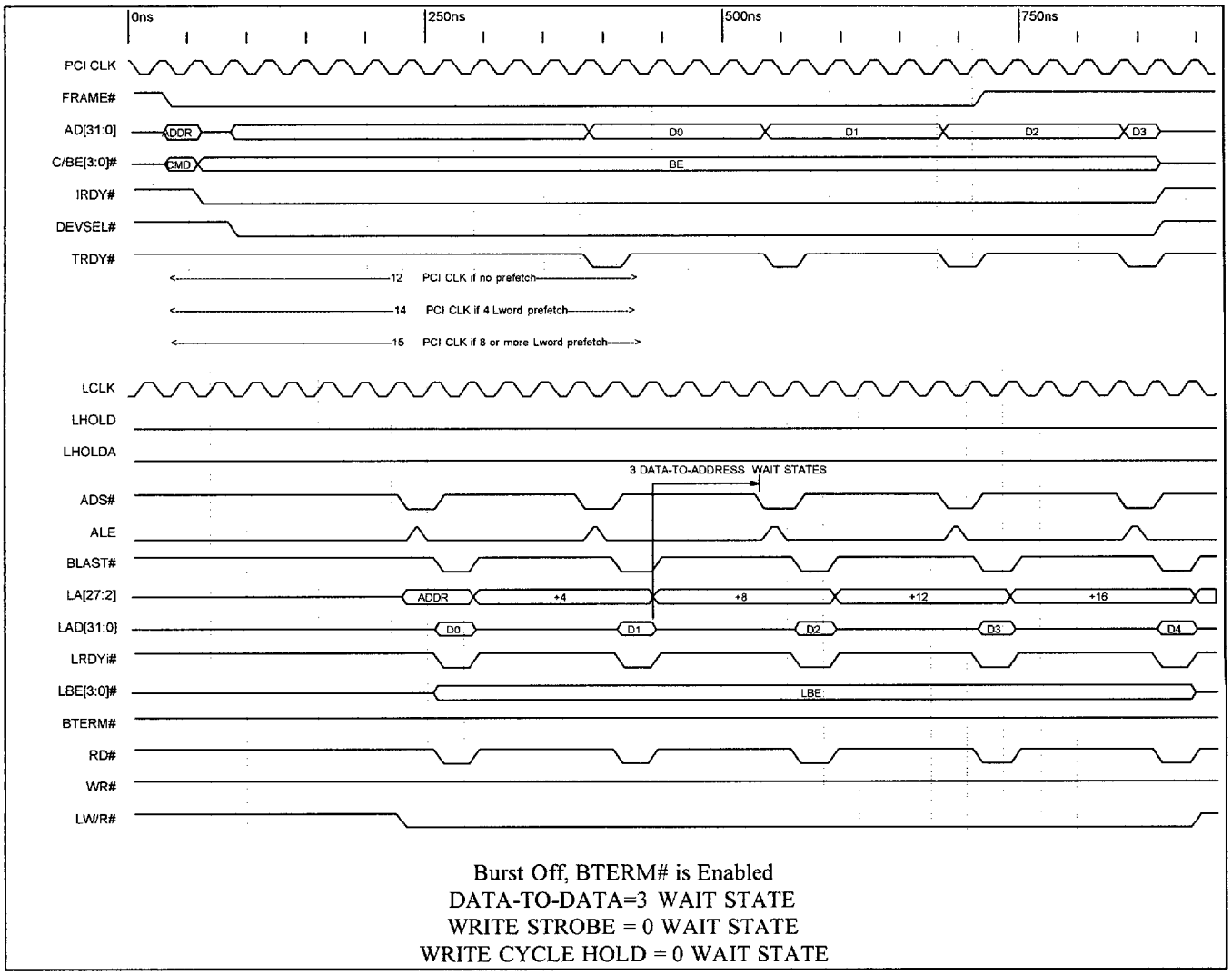


Direct Slave Single Read With Wait States

Timing Diagram 16. Direct Slave Single Read Without Wait States (32 Bit Local Bus)

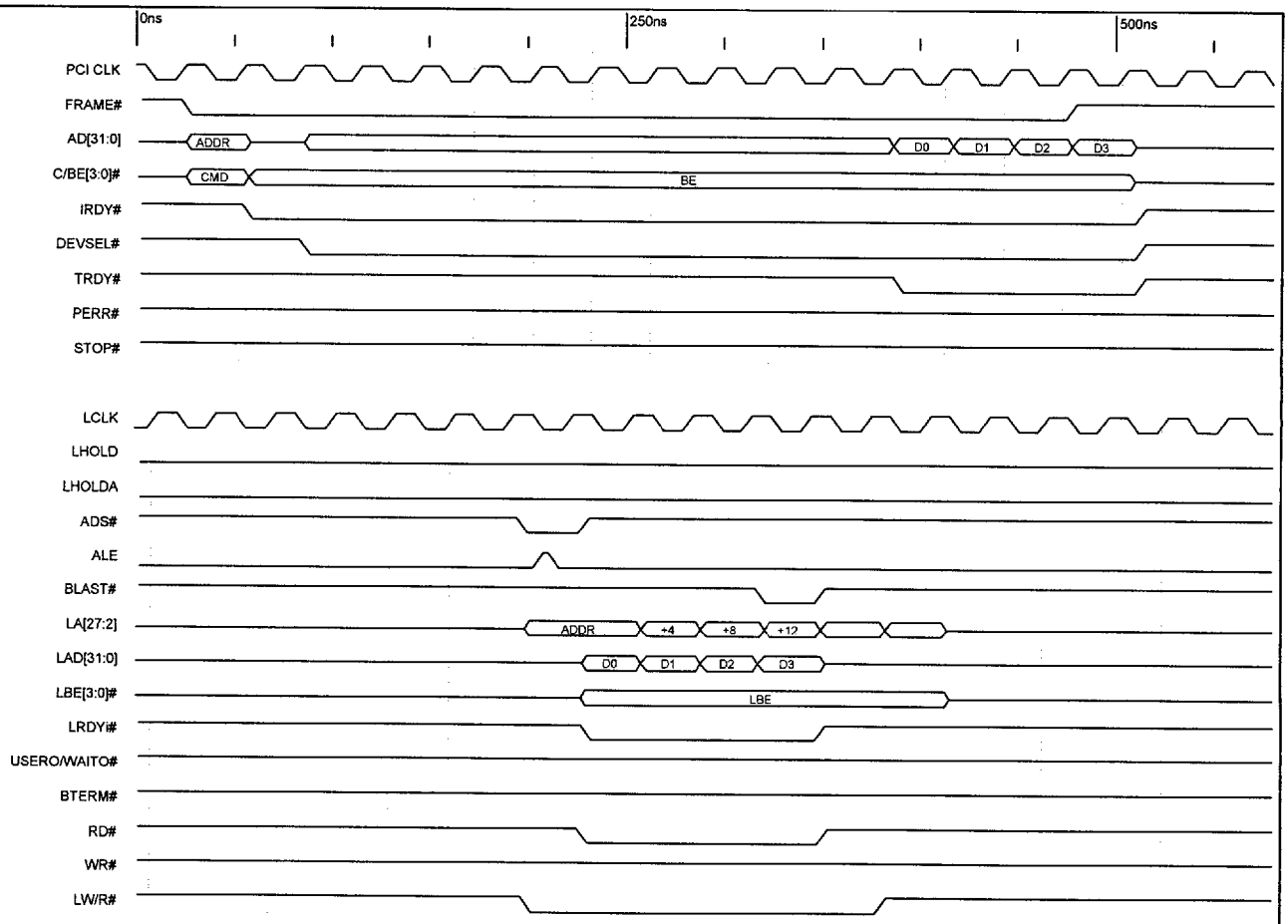


Timing Diagram 17. Direct Slave NON-Burst Read With BTERM# Enabled (32 Bit Local Bus)



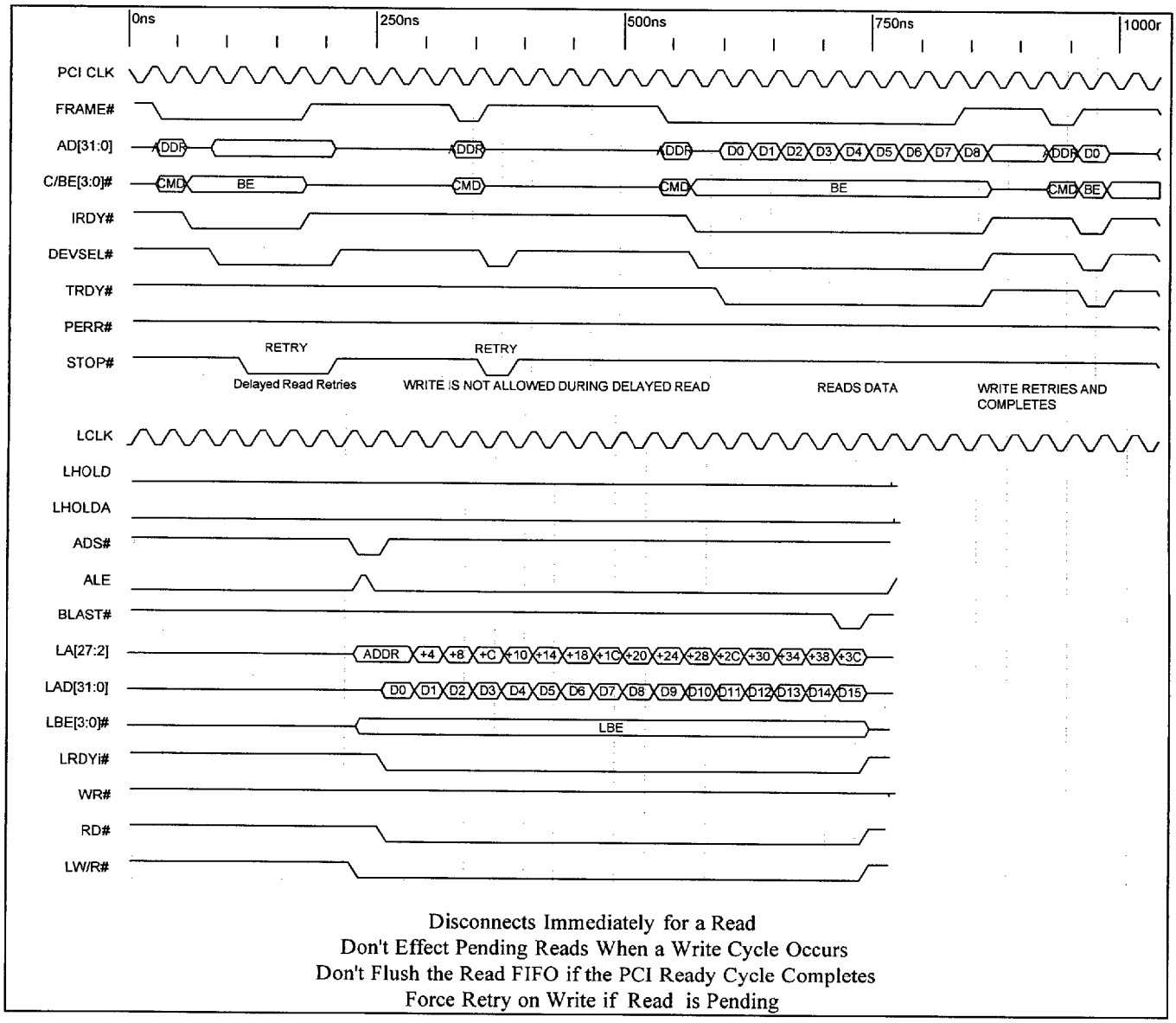
Burst Off, BTERM# is Enabled
DATA-TO-DATA=3 WAIT STATE
WRITE STROBE = 0 WAIT STATE
WRITE CYCLE HOLD = 0 WAIT STATE

Timing Diagram 18. Direct Slave Burst Read With Prefetch of 4LWORD (32 Bit Local Bus)

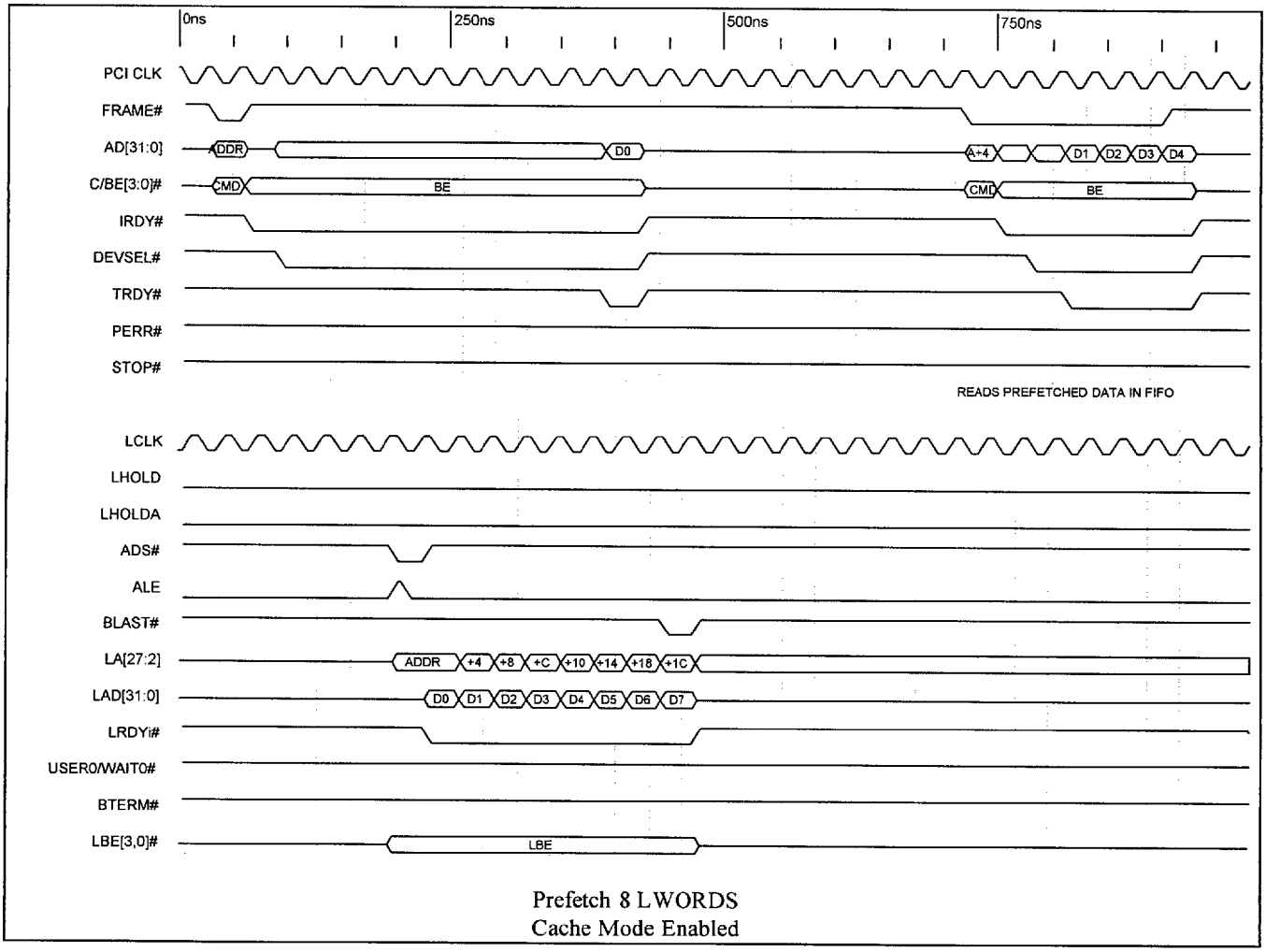


Burst is On, Prefetch 4LWORDS
ADDRESS-TO-DATA=0 WAIT STATE
DATA-TO-DATA= 0 WAIT STATE
READ STROBE=0 WAIT STATE

Timing Diagram 19. Direct Slave Read 2.1 Spec (32 Bit Local Bus)

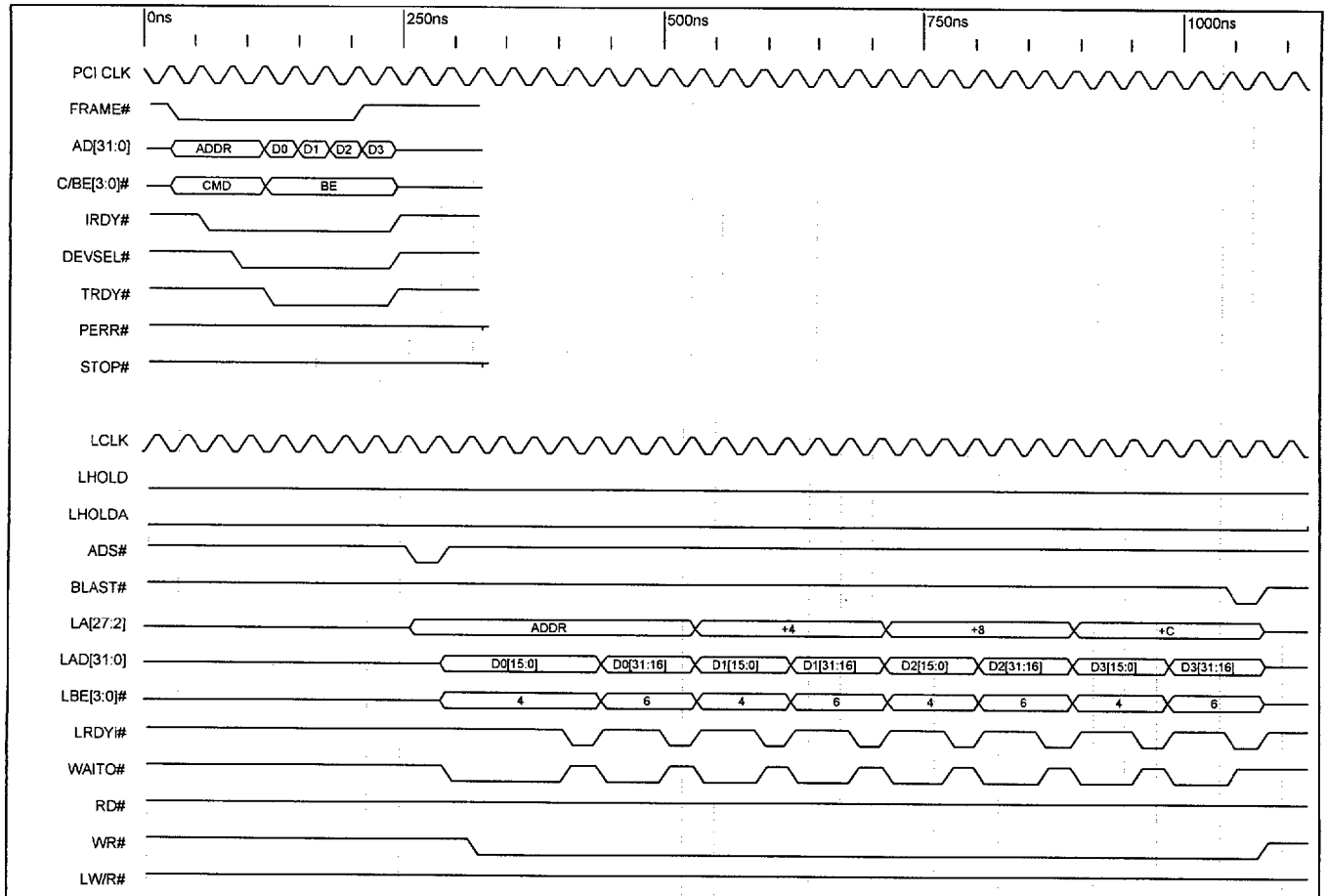


Timing Diagram 20. Direct Slave Read With Cache Mode Enabled (32 Bit Local Bus)



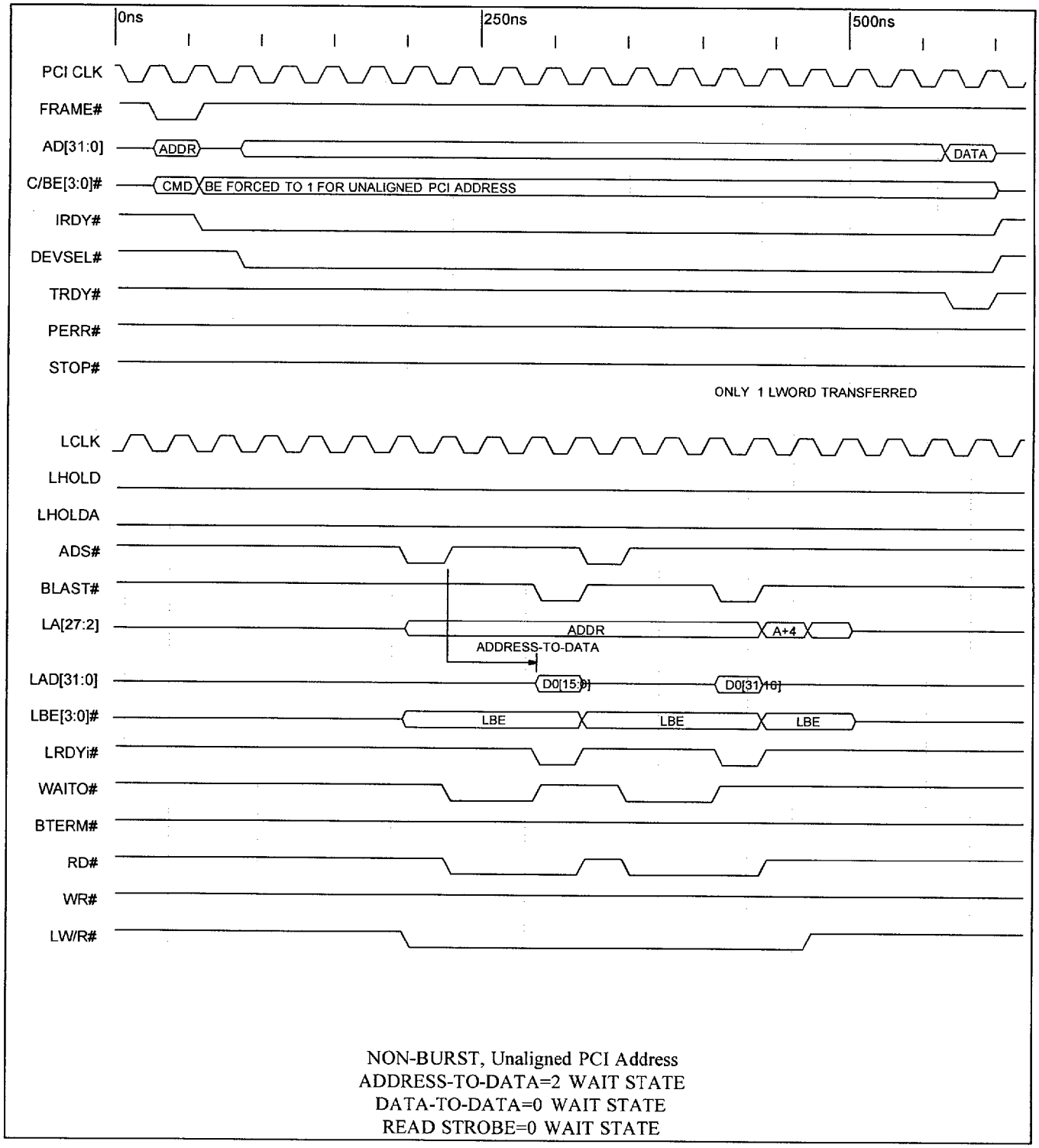
Prefetch 8 LWORDS
Cache Mode Enabled

Timing Diagram 21. Direct Slave Burst Write (16 Bit Local Bus)



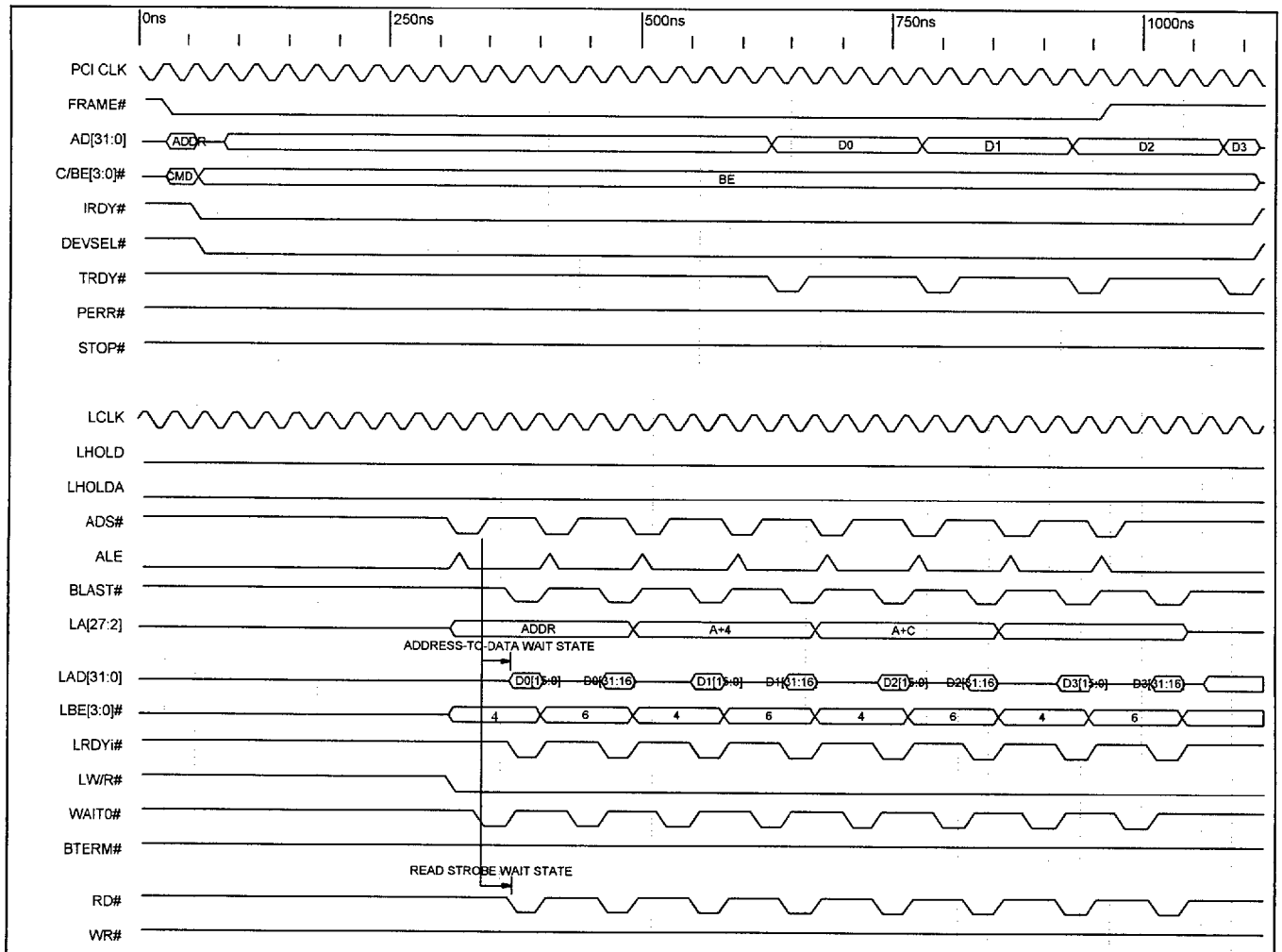
Burst is On
ADDRESS-TO-DATA=4 WAIT STATE
DATA-TO-DATA=2 WAIT STATE
WRITE STROBE=1 WAIT STATE
WRITE CYCLE HOLD=0 WAIT STATE

Timing Diagram 22. Direct Slave NON-Burst Read With Unaligned PCI Address (16 Bit Local Bus)



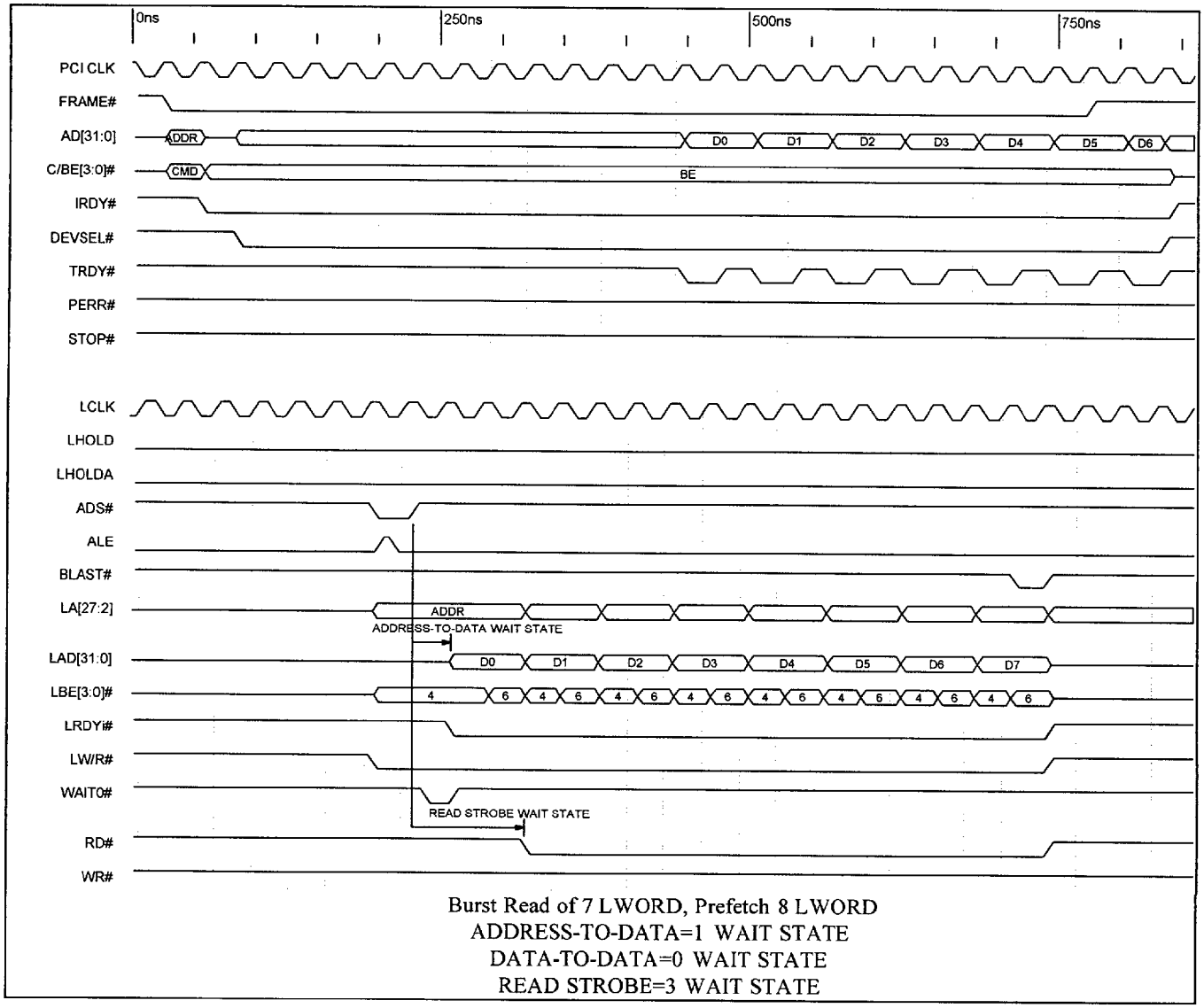
NON-BURST, Unaligned PCI Address
ADDRESS-TO-DATA=2 WAIT STATE
DATA-TO-DATA=0 WAIT STATE
READ STROBE=0 WAIT STATE

Timing Diagram 23. Direct Slave NON-Burst Read With Prefetch (16 Bit Local Bus)



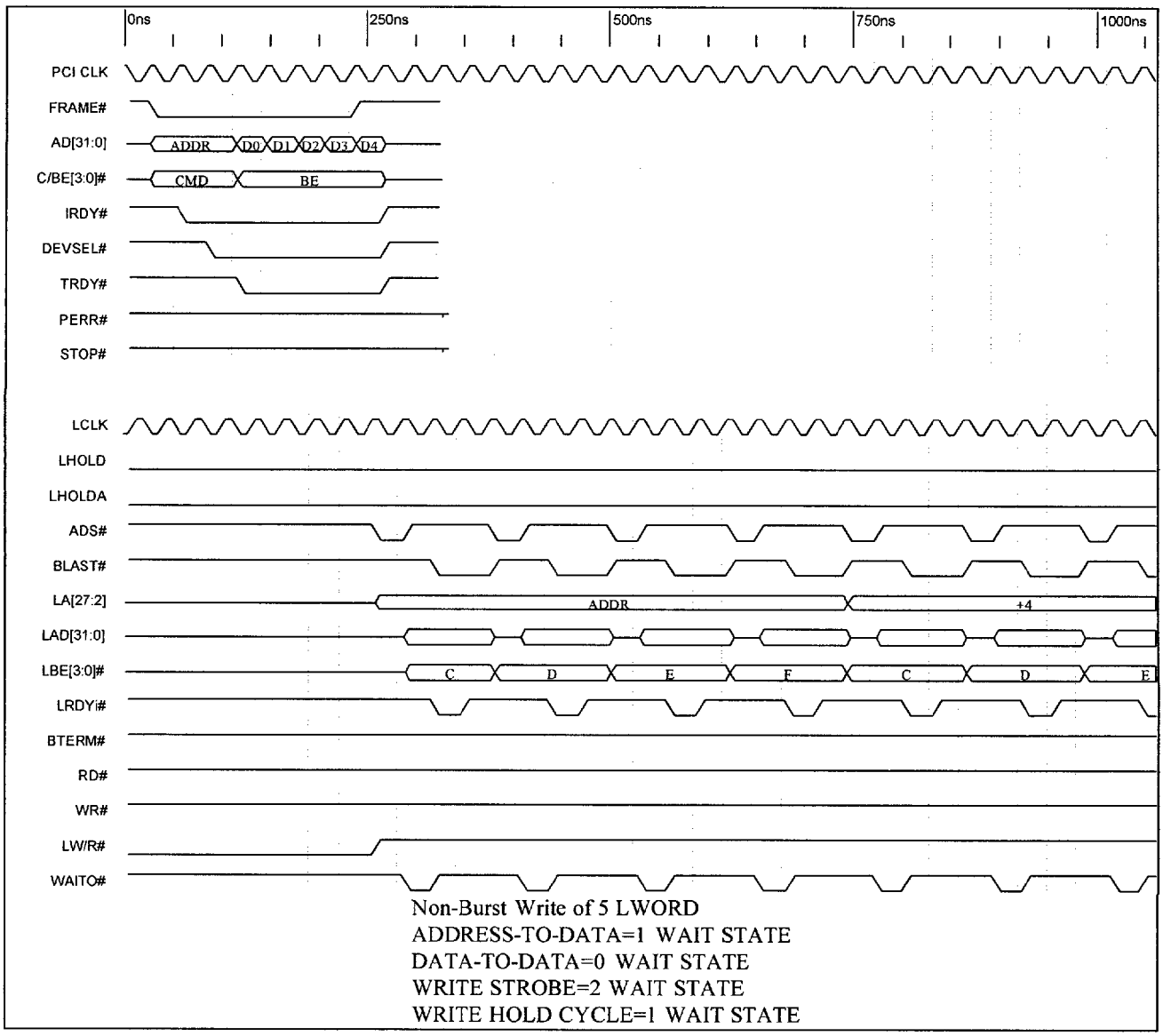
Non-Burst Read of 4LWORD
ADDRESS-TO-DATA=1 WAIT STATE
DATA-TO-DATA=1 WAIT STATE
READ STROBE= 1 WAIT STATE

Timing Diagram 24. Direct Slave Burst Read With Prefetch (16 Bit Local Bus)

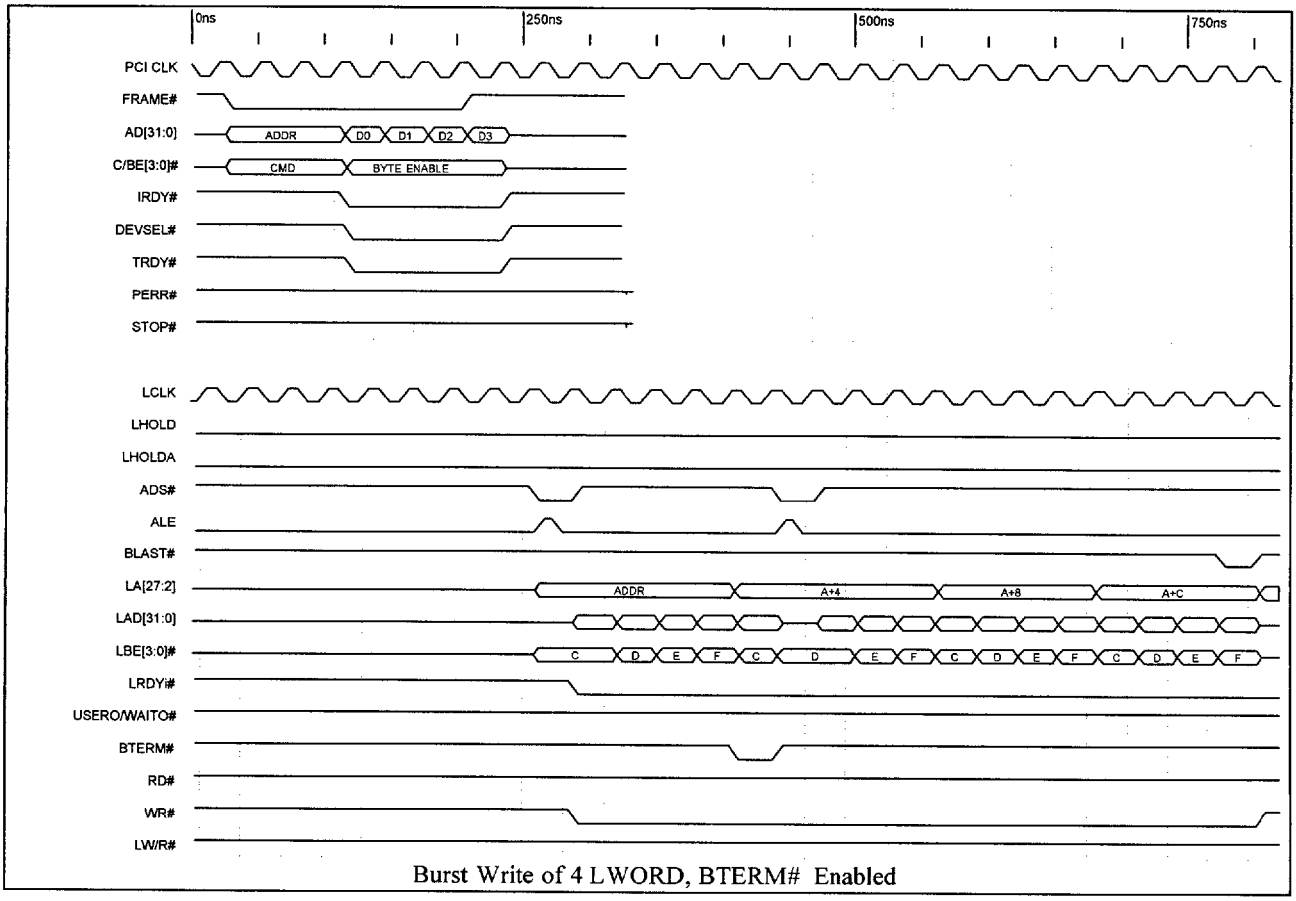


Burst Read of 7 LWORD, Prefetch 8 LWORD
ADDRESS-TO-DATA=1 WAIT STATE
DATA-TO-DATA=0 WAIT STATE
READ STROBE=3 WAIT STATE

Timing Diagram 25. Direct Slave NON-Burst Write (8 Bit Local Bus)

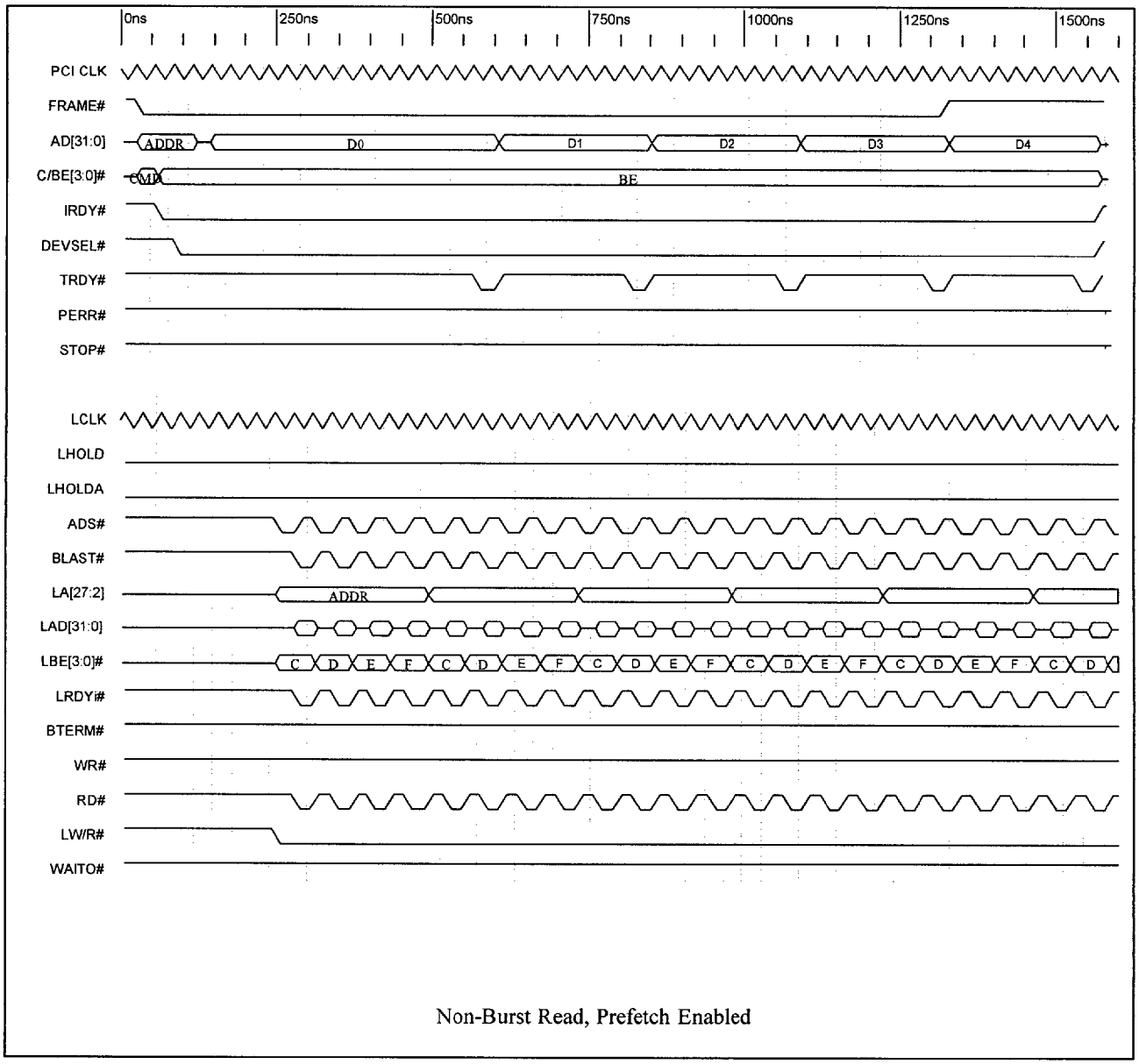


Timing Diagram 26. Direct Slave Burst Write With BTERM# Enabled (8 Bit Local Bus)



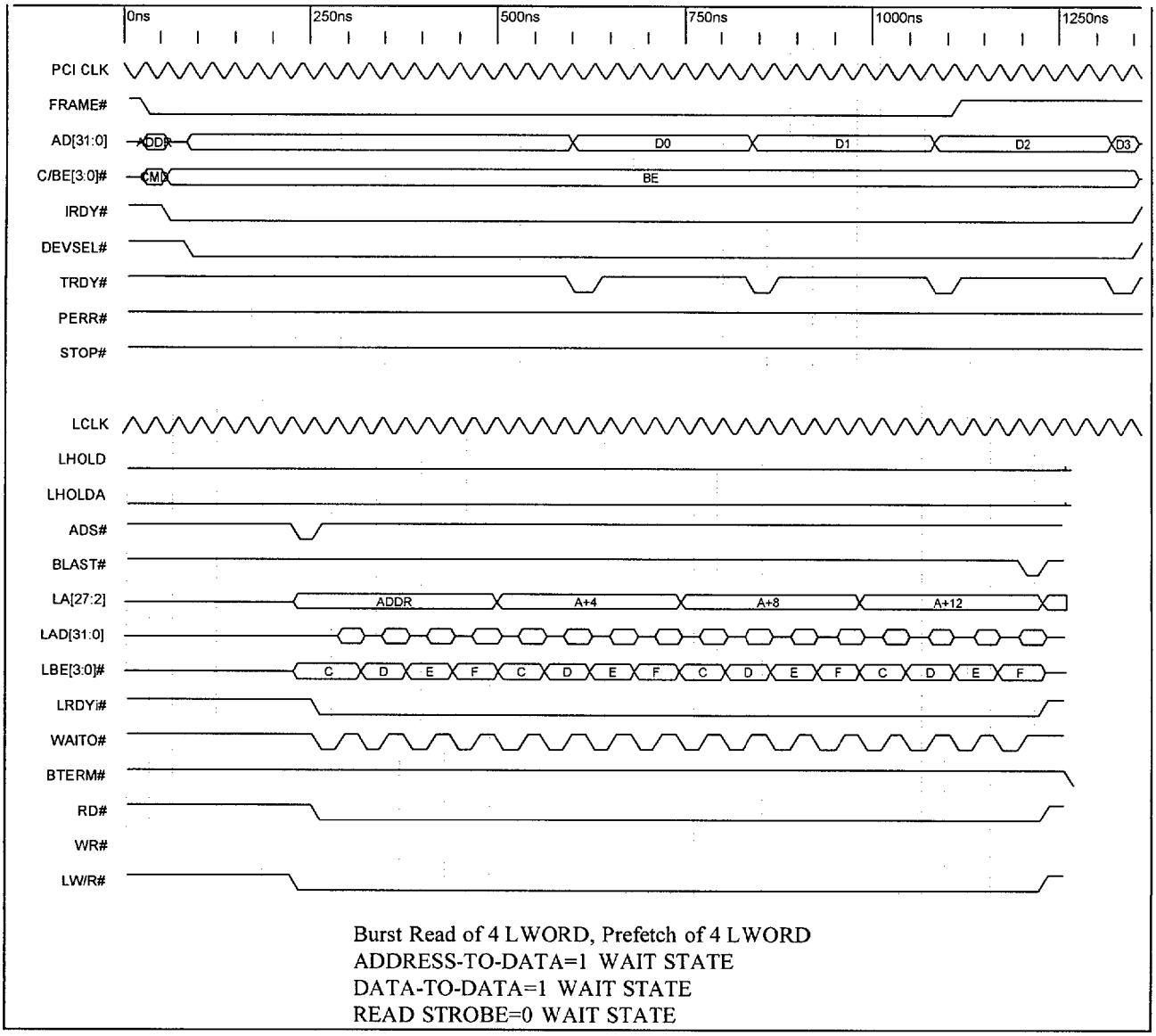
Burst Write of 4 LWORD, BTERM# Enabled

Timing Diagram 27. Direct Slave Non-Burst Read With Prefetch (8 Bit Local Bus)



Non-Burst Read, Prefetch Enabled

Timing Diagram 28. Direct Slave Burst Read With Prefetch



Burst Read of 4 LWORD, Prefetch of 4 LWORD
ADDRESS-TO-DATA=1 WAIT STATE
DATA-TO-DATA=1 WAIT STATE
READ STROBE=0 WAIT STATE