CIRRUS LOGIC®

CL-MD9624AT/EC2

Data Book

FEATURES

- **Lowest chip count to support data/fax/voice**
- **Data Modem Modes**
  - CCITT: V.22 bis and V.22
  - Bell®: 212A and 103
  - Speeds: 2400, 1200 and 300 bps
  - Industry-standard 'AT' command set
- **Fax Modem Send and Receive Modes**
  - CCITT: V.29, V.27 ter and V.21 ch2
  - Speeds: 9600, 7200, 4800, 2400 and 300 bps
  - Supports Group 3 fax
  - Data/Fax EIA/TIA-578 Class 1 'AT' command set
- **Voice Mode**
  - Embedded Voice Mode 'AT' command set
  - Auto-recognition (fax/voice) Answer Mode
- **V.42/MNP Protocols (CL-MD9624EC2 only)**
  - Error correction: V.42 and MNP 2-4
  - Data compression: V.42 bis and MNP 5
- **Selectable TIES/Hayes® Escape Sequence**
- **Two built-in DTE (data terminal) interfaces**
  - Parallel 16C550A/16C450 register-compatible
    - Enhances Microsoft® Windows™ compatibility
    - Built-in COM 1-4 address decoding
    - Direct connection to PC ISA Bus
  - Serial RS-232 (V.24)
- **Low power requirement**
  - Automatic sleep (power-down) and wake-up
  - Operates from a single +5V power supply
  - Typical power requirements:
    - Operating power: 330 mW
    - Sleep Mode: 8 mW
    - Stop Mode: < 1 mW

(cont.)

Intelligent Data/Fax/Voice Modem Device Sets

OVERVIEW

The Cirrus Logic CL-MD9624AT is a complete, intelligent, multi-mode modem combining data, fax and voice capability in only two devices, the CL-MD1024 and CL-MD1624.

The CL-MD9624EC2 is a two-device set (CL-MD1224 and CL-MD1624) that includes all the features of the CL-MD9624AT and adds V.42/MNP 2-4 error correction and V.42 bis/MNP 5 data compression during Data Mode.

Both device sets offer the most complete, highly integrated solutions on the market today. These device sets operate up to 9600 bps as a fax modem and up to 2400 bps as a data modem. Each device set provides a complete solution *not requiring any additional firmware development.*

An extended data and fax 'AT' command set interpreter is embedded in the device sets, allowing system designers to develop a Hayes-compatible modem with a minimum of effort.

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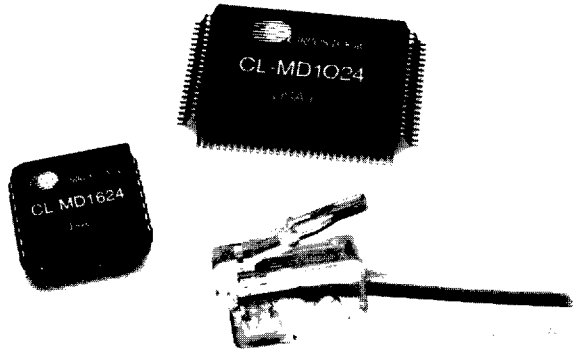

The CL-MD9624AT Device Set

CIRRUS LOGIC

FEATURES (cont.)

- **No external microprocessor required**
- **Accommodates additional data buffering**
- **Fax and voice application software available**
- **DTMF and tone generation/detection**
- **Analog, local, and remote digital loopback tests**
- **Automatic adaptive and fixed compromise equalizers**
- **Non-volatile RAM (NVRAM) interface**
- **Eye pattern interface**
- **Direct connection to a speaker**
- **Expansion Bus**
- **PCMCIA-compatible packages available**
- **Small package dimensions**
  - DSµP (CL-MD1024 and CL-MD1224): 100-pin PQFP and 100-pin VQFP
  - SAFE (CL-MD1624): 28-pin PLCC and 44-pin VQFP

APPLICATIONS

- Notebook computers
- Laptop computers
- Integral modems
- Box modems
- Pocket modems
- PCMCIA cards

OVERVIEW (cont.)

The CL-MD9624AT/EC2 implements the EIA/TIA-578 Class 1 fax 'AT' command set standard that allows any DTE to communicate with Group 3 fax machines. A Voice Mode 'AT' command set is also provided to allow a host computer and a CL-MD9624AT/EC2 modem to emulate a telephone answering machine.

The Sigma-Delta Analog Front End (SAFE™) device — the CL-MD1624 — incorporates a unique and proprietary Sigma-Delta design. SAFE provides a higher D/A and A/D conversion accuracy than traditional switched-capacitor-based analog front ends. Its higher accuracy improves performance at low signal levels and reduces sensitivity to board layout.

Both device sets accommodate external data buffering to allow operation in multitasking or background modes where host interrupts may be temporarily disabled. The 'AT device set buffers fax and voice; the 'EC2 device set buffers data, fax, and voice.

Device Set Memory Requirements

	Chipset	SRAM	NVRAM	EPROM
Basic Modem	'9624AT	none	optional	none
Buffered Modem	'9624AT	8K x 8	optional	none
Error-correcting Modem	'9624EC2	32K x 8	optional	none

ADVANTAGES

Unique Features	*Benefits*
• ***Lowest chip count to support data/fax/voice***	Reduces overall system chip count.
• ***Voice Mode***	System can emulate an answering machine.
• ***16C550A register-compatible UART***	Supports enhanced communication software for improved data throughput.
• ***Small package sizes***	Minimizes board area (e.g., PCMCIA cards).
• ***Sleep and Stop Mode***	Substantially reduces power consumption by over 99 percent.
• ***Accommodates external data buffering***	Reduces Background Mode data loss when host interrupts are temporarily disabled.
• ***Direct connection to PC ISA Bus***	Eliminates the need for bus drivers and address decoding logic.
• ***Requires single +5V power supply***	Simplifies board design.

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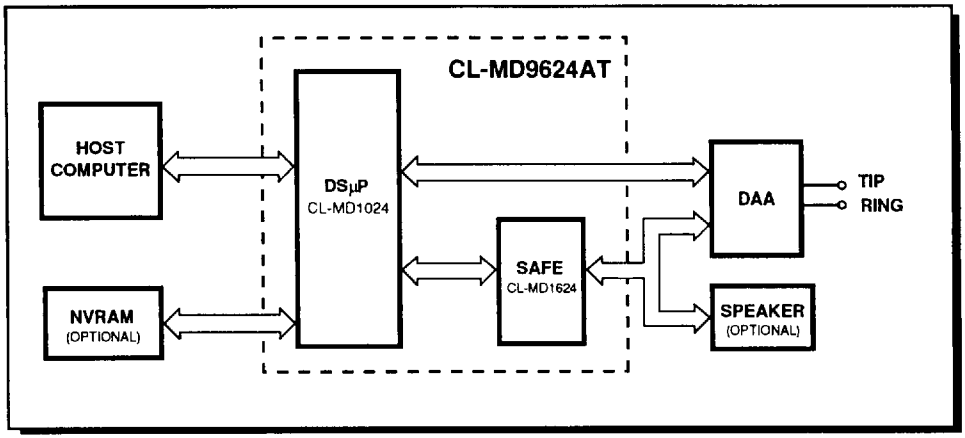

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Figure 1–1. CL-MD9624AT Functional Block Diagram

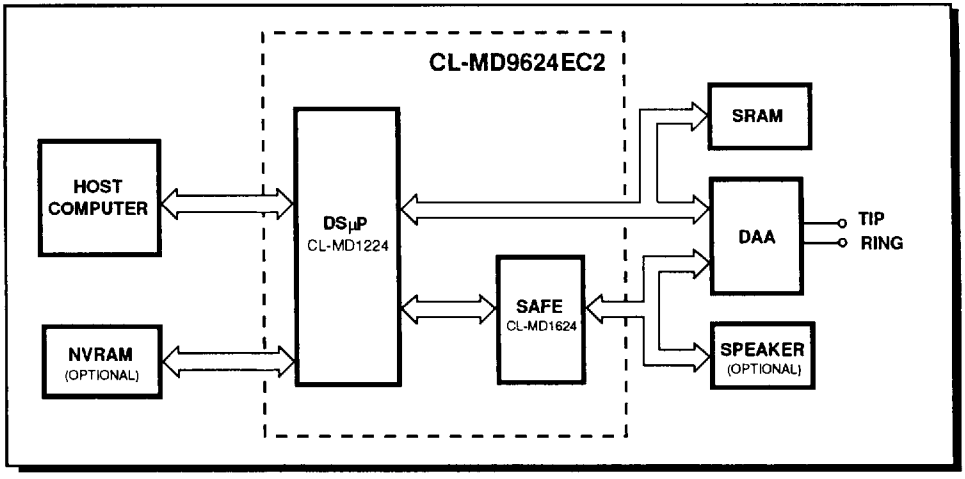

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Figure 1–2. CL-MD9624EC2 Functional Block Diagram

1. DEVICE SET DESCRIPTION

The CL-MD9624AT and CL-MD9624EC2 are two-device sets consisting of a Digital Signal Microprocessor (DSμP) and a Sigma-Delta Analog Front End (SAFE). The 'AT' suffix refers to an 'AT' command set smart modem. The 'EC2' suffix refers to a two-device error correction and data compression 'AT' command set Smart Mode modem.

1.1 Digital Signal Microprocessor (DSμP)

The Digital Signal Microprocessor (DSμP) performs the functions of both a microprocessor and a digital signal processor (DSP). The DSμP implements all of the 'AT' commands, manages data transmission and reception, controls the Sigma-Delta Analog Front End (SAFE), and interfaces to the DTE.

The CL-MD9624AT DSμP contains all the necessary code to support Group 3 Fax Mode, Data Mode (without error correction or data compression) and Voice Mode. The CL-MD9624EC2 DSμP contains all the necessary code to support all the features of the CL-MD9624AT plus Data Mode error correction and data compression.

1.2 Sigma-Delta Analog Front End (SAFE)

The Sigma-Delta Analog Front End (SAFE), incorporates unique and proprietary Sigma-Delta digital-to-analog and analog-to-digital functions, as well as all other analog circuitry for the device set. The SAFE Sigma-Delta implementation for the analog-to-digital conversion process results in higher receiver accuracy that improves performance at low receive signal levels. Another advantage to using Sigma-Delta conversion is that a significant amount of signal processing is performed digitally instead of by analog techniques. For the SAFE, this means the analog front-end functions are more stable and less sensitive to board layout than prior analog front-end technologies.

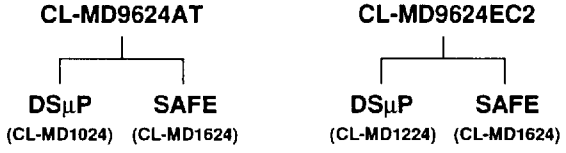


Figure 1–3. Device Set Composition

2. SYSTEM DESCRIPTION

The CL-MD9624AT/EC2 provides the complete modem functions for Group 3 fax, data and voice modes of operation. Modem system block diagrams using the CL-MD9624AT and CL-MD9624EC2 are shown in Figure 2–1 and Figure 2–2, respectively. The data rates and modulation schemes for both device sets are presented in Table 2–1. The data terminal equipment (DTE) communicates with the modem through 'AT' commands. Each mode of operation has its own unique command set.

2.1 Data Mode

In Data Mode, the CL-MD9624AT/EC2 implements all of the data rates and modulation schemes in CCITT standards V.22 bis, V.22, Bell 212A and Bell 103. The device set operates up to 2400 bps as a Data Mode modem.

The CL-MD9624AT implements a basic Data Mode 'AT' command set that is compatible with any communication application software that supports the Hayes 'AT' command set. The CL-MD9624EC2 includes all the features of the CL-MD9624AT and adds V.42/MNP 2-4 error correction and V.42/MNP 5 data compression during Data Mode.

2.2 Fax Mode

In Fax Mode, the CL-MD9624AT/EC2 implements all of the data rates and modulation schemes in CCITT standards V.29, V.27 ter and V.21 ch 2. The device set operates up to 9600 bps (transmit and receive) as a Fax Mode modem.

Table 2–1. Communication Modes and Data Rates

Application	Mode	Data Rate (bps)	Modulation	Baud Rate (symbols/sec.)	Carrier Frequency (Hz) (originate/answer)	Constellation Points
Fax	V.29	9600	QAM	2400	1700	16
		7200	QAM	2400	1700	8
		4800	QAM	2400	1700	4
	V.27 ter	4800	DPSK	1600	1800	8
		2400	DPSK	1200	1800	4
	V.21	300	FSK	300	1650 M 1850 S	1
Data	V.22 bis	2400	QAM	600	1200/2400	16
	V.22	1200	DPSK	600	1200/2400	4
	Bell 212A	1200	DPSK	600	1200/2400	4
	Bell 103	300	FSK	300	1270 M/2225 M 1070 S/2025 S	1

NOTES: M = Mark FSK = Frequency Shift Keying DPSK = Differential Phase Shift Keying
S = Space QAM = Quadrature Amplitude Modulation

The modem implements a Fax Mode 'AT' command set that is compatible with any communication application software that supports EIA/TIA-578 Data/Fax Class 1 standard. This feature allows a DTE and a CL-MD9624AT/EC2-based modem to communicate with Group 3 fax machines.

2.3 Voice Mode

The CL-MD9624AT/EC2 provides a Voice Mode that allows a DTE to record and play back voice messages. Voice Mode is accessed by an extended 'AT' command set.

2.4 V.42/MNP 2-4 and V.42 bis/MNP 5 Modes

The CL-MD9624EC2 provides all the functionality for error correction (V.42 and MNP 2-4) and data compression (V.42 bis and MNP 5). Error correction ensures error-free data transfer. Data compression substantially increases the modem data throughput over the basic data rate.

Depending on the data stream, Microcom Networking Protocol® Class 5 (MNP 5) may provide up to 2-to-1 compression. Alternately, CCITT V.42 bis may provide up to 4-to-1 compression. A description of the 'AT' commands and S-Registers that support error correction and data compression are provided in Table 4–4 on page 14.

2.5 Power Modes

The CL-MD9624AT/EC2 provides both a Sleep and Stop Mode to reduce power consumption when the modem is not being used. Stop Mode effectively turns the modem power off except for the circuitry required to maintain the host interface signals at the appropriate high-impedance state. To enter Stop Mode, the host asserts the DSμP Stop Pin. When the Stop Pin is deasserted, the modem exits Stop Mode, performs an internal reset and enters Power-on Mode. After the modem internal reset, the DTE must reconfigure the modem. Power-on Mode is differentiated into Operational Mode and Sleep (or Power-down) Mode. In Operational Mode, the modem device set is fully powered and is either communicating with the host and/or another modem or is performing some internal processing. In Sleep Mode, power to most of the internal circuitry of the DSμP and SAFE is turned off.

Sleep Mode is controlled by S-Register S30. When enabled, the DSμP will enter Sleep or Power-down Mode whenever the modem has been inactive for a user-programmable time delay. The modem is considered to be in an inactive state when:

1) No internal processing is being performed;
2) There is no activity between the host and the modem within a specified time period;
3) The modem is off-line.

The modem exits Sleep Mode whenever the host reads or writes to the modem, or a ring signal is detected.

Parallel host interface power requirements for each power mode are presented in Table 2–2.

Table 2–2. Chipset Power Requirements

Mode	Typical @ 25° C		Maximum @ 0° C	
	Current	Power	Current	Power
Operational	66 mA	330 mW	89 mA	445 mW
Sleep (power-down)	1.6 mA	8 mW	3.3 mA	16.5 mW
Stop (power-off)	< 0.2 mA	< 1 mW	0.9 mA	4.5 mW

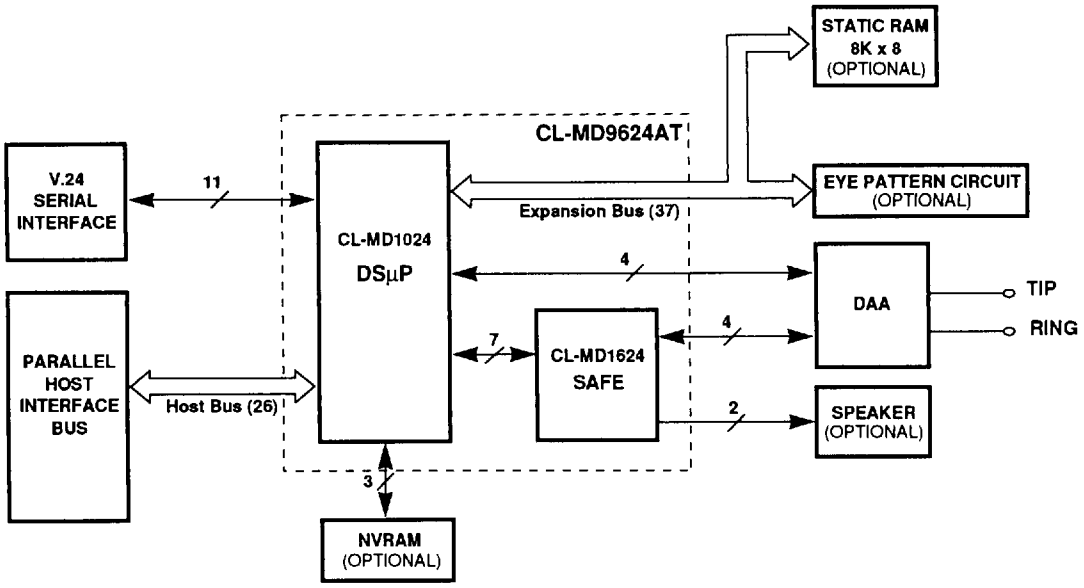


Figure 2–1. Modem System Block Diagram (CL-MD9624AT)

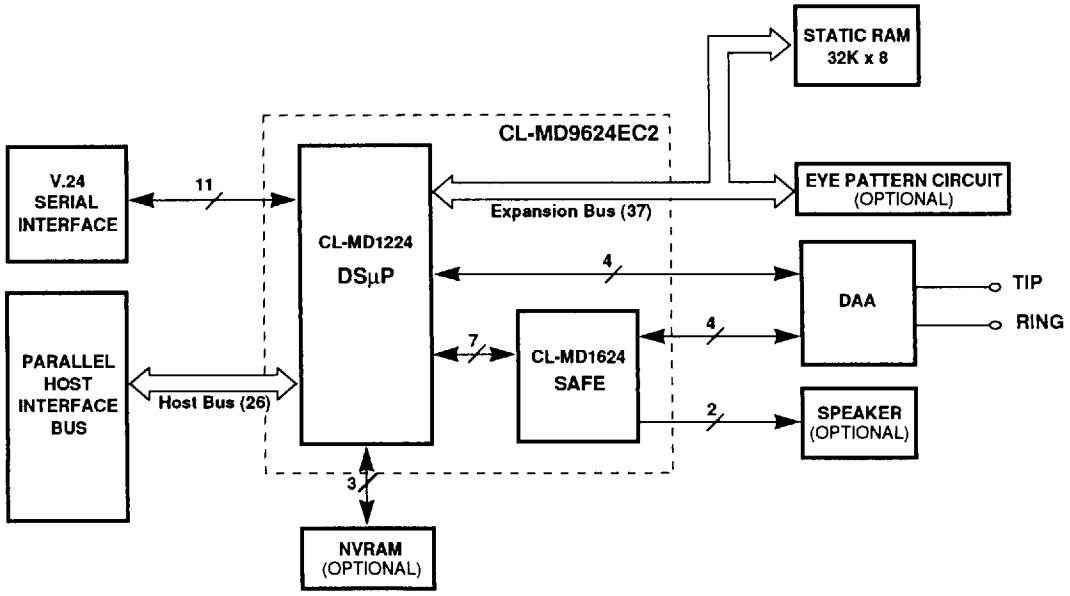


Figure 2–2. Modem System Block Diagram (CL-MD9624EC2)

2.6 Transmit Levels

The transmit level is -10 dBm +/- 1 dB at tip and ring.

2.7 Transmit Tone Levels

The modem generates DTMF, answer, call, and guard tones. The specification for each tone is provided in Tables 2–3 and 2–4. DTMF tones are transmitted at -6 dBm for Tone1 and -4 dBm for Tone2.

2.8 Receive Level

The receiver can accommodate a receive signal from -9 dBm to -43 dBm. Data carrier detect (DCD) turns on at -43 dBm and above, and turns off at -48 dBm and below.

2.9 Receiver Tracking

The receiver can compensate for up to +/- 7 Hz of carrier-frequency offset.

2.10 Equalizers

Automatic adaptive and compromise equalizers are provided to compensate for line distortions.

2.11 Test Modes

Local and remote digital, and analog loop tests are provided for testing modem-to-modem and modem-to-DTE communication integrity. These tests are accessed through the 'AT&Tn' command.

2.12 Call Progress

The modem monitors and reports to the DTE the detection of call-progress tones during call origination. Call-progress tones include: dial tone, busy tone, ring back, and answer tone.

Table 2–3. DTMF Tone Pairs

DIAL DIGIT	TONE1 (Hz)	TONE2 (Hz)
0	941	1336
1	697	1209
2	697	1336
3	697	1447
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1447
*	941	1209
#	941	1447
A	697	1633
B	770	1633
C	852	1633
D	941	1633

Table 2–4. Transmit Tones

TONE	VALUE	APPLICATION
Calling tone	1100 Hz	Fax originator
Answer tone	2100 Hz 2225 Hz	Data/Fax (CCITT) Data (Bell Mode)
Guard tone	1800 Hz 500 Hz	Data (Answer Mode)

3. HARDWARE INTERFACES

The CL-MD9624AT/EC2 supports hardware interfaces for the host, DAA, LEDs, eye pattern, and Expansion Bus.

3.1 Host Interface

The CL-MD9624AT/EC2 can be selected to support either a parallel or a serial host interface. The interface type is selected by tying the DSμP HOSTSEL Pin to V_{CC} or ground. The serial interface is compatible with a RS-232 interface. The serial interface also provides LED drivers for commonly used status information such as auto-answer enable (AA) and modem off-hook (OH).

The parallel interface emulates the electrical and register functions of a 16C550A and 16C450 UART. Upon modem reset, the UART interface defaults to a 16C450. The DTE can then configure the UART to function as a 16C550A. Table 3–1 shows the UART Register bit assignments.

The parallel UART interface can be selected to internally decode the addresses for COM 1-4. For applications not utilizing COM 1-4, the standard method of selecting the modem with external address decoding is also provided. The type of address decoding is selected by either asserting or deasserting the signal at the DSμP ADRDEC Hardware Pin.

Additionally, the parallel UART provides an internal Tri-state Bus interface that eliminates the need for external bus drivers between the Host Bus and the modem UART. These features eliminate the need for a 74HCT245 and a 74HCT30 device, and facilitates system designs with lower chip counts, power requirements, and costs.

3.2 Expansion Bus Interface

An Expansion Bus is provided for accessing external memory and/or circuitry. The Expansion Bus is used to add enhancements to the modem and add eye-pattern circuitry. An eye pattern is used to display the received signal point data for diagnostic purposes.

An optional 55-ns SRAM may be connected to the Expansion Bus for the CL-MD9624AT, but is required for the CL-MD9624EC2. The SRAM is used to buffer data during voice, fax, and V.42/MNP modes of operation.

3.3 NVRAM Interface

A serial interface is provided for an optional nonvolatile RAM (NVRAM). A NVRAM may be used for storing modem configurations and telephone numbers.

3.4 DAA Interface

A DAA interface is provided for controlling the telephone line on-hook relays, detecting a ring signal, and transmitting and receiving the analog signal.

3.5 Speaker Interface

The SAFE internally implements both the volume control and amplifier necessary to drive an external speaker. The output of the internal amplifier can be connected directly to a speaker or to the input of the host speaker amplifier. The internal amplifier is capable of driving a minimum load of 8 ohms. The speaker volume is controlled by the 'ATLn' command.

Table 3–1. Parallel Host Interface UART Register Bit Assignments

REGISTER ADDRESS	REGISTER NAME	BIT NUMBER							
		7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register (SCR)							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCDD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	Error in RCVR FIFO (See 'Note')	Transmitter Empty (TEMT)	Transmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break (SBRK)	Stick Parity (SPAR)	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	FIFO Control Register [write only] (FCR)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA Mode Select (DMA)	XMIT FIFO Reset (XFIFOR)	RCVR FIFO Reset (RFIFOR)	FIFO Enable (FIFOE)
2	Interrupt Identity Register [Read only] (IIR)	FIFOs Enabled (See 'Note')	FIFOs Enabled (See 'Note')	0	0	Interrupt ID Bit 2 (See 'Note')	Interrupt ID Bit 1	Interrupt ID Bit 0	A '0' if Interrupt Pending
1 DLAB=0	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (MSIE)	Receiver Line Status Interrupt Enable (RLSIE)	Transmitter Holding Reg. Empty Int. Enable (THREIE)	Received Data Available Int. Enable (RDAIE)
0 DLAB=0	Transmit Holding Register [Write only] (THR)	Transmit Holding Register (THR) [Write only]							
0 DLAB=0	Receiver Buffer Register [Read only] (RBR)	Receiver Buffer Register (RBR) [Read only]							
1 DLAB=1	Divisor Latch (MS) (DLM)	Divisor Latch (MS)							
0 DLAB=1	Divisor Latch (LS) (DLL)	Divisor Latch (LS)							

NOTE: These bits are always a '0' in 16C450 Mode.

4. 'AT' COMMAND SET

4.1 'AT' Command Description

The CL-MD9624AT/EC2 'AT' command set and S-Registers are divided into four categories: Group 3 fax, data, V.42/MNP and voice. Tables 4–1 through 4–5 provide summaries of all the commands, and Table 4–6 provides a summary of all the S-Registers.

All command lines sent to the modem, except for 'A/', must be preceded by an 'AT' and terminated by the contents of S-Register S3 (typically a carriage return <CR>). An 'AT' prompts the modem to receive a command line from the DTE. A <CR> informs the modem that the entire command string has been transmitted and that it should start processing all the commands within the command line. A command line may include one or more 'AT' commands that may or may not be separated by a space. Fax 'AT' commands must have a semicolon (;) after the command if there are multiple commands on a line. To repeat the last command type 'A/'.

Four examples are as follows:

```
ATS1?<CR>
A/
AT &C1 &D2 +FCLASS=? <CR>
AT &C1 &D2 +FCLASS=?; S0=1 <CR>
```

The modem provides status information to the DTE in the form of response codes. The supported response codes are provided in Tables 4–7 through 4–9.

4.2 'AT' Escape Sequence

The CL-MD9624AT/EC2 provides two industry-standard escape sequences. The supported escape sequences are the Time Independent Escape Sequence (TIES) and the Hayes Escape Sequence.

Currently, most modems implement the Hayes Escape Sequence; however, because a license from Hayes may be needed, the CL-MD9624AT/EC2 provides an alternate escape sequence (TIES).

TIES is an escape sequence designed to work with existing communication software written for the Hayes Escape Sequence.

The escape sequence type defaults to the TIES Escape Sequence unless the DSμP ESCAPE Pin is connected to ground. When connected to ground, the Hayes Escape Sequence is selected.

TIES/Hayes® Escape Sequences

The Cirrus Logic CL-MD9624AT and CL-MD9624EC2 Modem Device Sets are manufactured so the Time Independent Escape Sequence (TIES) is the default setting. By activating the DSμP ESCAPE Pin, you may change the default from TIES to the Hayes Escape Sequence. It is Hayes' position that you must either have, or obtain a valid licence from Hayes Micro Computer of Norcross, Georgia before activating the ESCAPE Pin and producing modem systems that utilize the Hayes Escape Sequence.

Cirrus Logic accepts no responsibility and does not indemnify nor in any way provide protection for patent or possible patent violations to its customers or users of its products.

Table 4–1. Basic Data Modem 'AT' Commands

Command		Default	Function
A/	**	none	Repeat last command
A		none	Answer command
Bn	*	1	Select CCITT or Bell
Cn		1	Carrier Control Option
D		none	Dial command
En	*	1	Command Mode echo
Fn		1	On-line echo
Hn		0	Switch hook control
In		0	Identification/checksum
Kn		none	Buffer control
Ln	*	2	Speaker volume control
Mn	*	1	Speaker control
Nn	*	1	Select data rate handshake
On		0	Go on line
P	*	none	Select pulse dialing
Qn	*	0	Result code display control
Sn		none	Select an S-Register
Sn=x		none	Write to an S-Register
Sn?		none	Read from an S-Register
?		none	Read last accessed S-Register
T	*	none	Select DTMF dialing
Vn	*	1	Result code form
Xn	*	4	Result code type/call progress
Yn	*	0	Long space disconnect
Zn		0	Reset modem/recall stored profile
&Cn	*	1	DCD option
&Dn	*	2	DTR option
&F		none	Load factory defaults
&Gn	*	0	Guard tone option
&Jn	*	0	Auxiliary relay control
&Mn	*	0	Communication Mode option
&Pn	*	0	Dial pulse ratio
&Qn	*	0	Communication Mode option
&Sn	*	0	DSR option
&Tn		0	Self-test commands
&Vn		0	View active configuration and stored profiles
&Wn		0	Store active profile
&Yn	*	0	Select stored profile on power up
&Zn=x		none	Store telephone number
%En	*	1	Auto-retrain control

Table 4–2. Data/Fax Class 1 'AT' Commands

Command	Function
+FCLASS?	Mode query
+FCLASS=n	Mode selection
+FCLASS=?	Supported modes
+FRH=<mod>	Receive HDLC data
+FRM=<mod>	Receive data
+FRS=<time>	Wait for Silence
+FTH=<mod>	Transmit HDLC data
+FTM=<mod>	Transmit data
+FTS=<time>	Stop transmission and pause

Table 4–3. Voice Mode 'AT' Commands

Command	Default	Function
#VBP	none	Generate Beep Tone
#VCL=n	0	Voice Mode Selection
#VIP=n	0	Initialize Parameter
#VLN=n	0	Relay/Speaker Control
#VPL=n	127	Play Level
#VPY	none	Play Mode
#VRD	none	Record Mode
#VRL=n	127	Recording Level
#VSM=n	CL1	Sampling Mode
#VSR=n	9600	Sampling Rate

Table 4–4. V.42, MNP 'AT' Commands

Command		Default	Function
%An	*	13	Set auto-reliable fallback character
%Cn	*	1	MNP 5 data compression control
\An	*	3	MNP block size
\Bn	*	none	Transmit break
\Cn	*	0	Set auto-reliable buffer
\Gn	*	0	Set modem port flow control
\Jn	*	0	Bps rate adjust control
\Kn	*	5	Set break control
\Nn	*	3	Set Operating Mode
\O		none	Originate reliable link
\Qn	*	3	Set serial port flow control
\Tn	*	0	Set inactivity timer
\U		none	Accept auto-reliable link
\Vn	*	2	Modify result code form
\Xn	*	0	Set XON/XOFF passthrough
\Y		none	Switch to Reliable Mode
\Z		none	Switch to Normal Mode
-Jn	*	1	Set V.42 detect phase
"Hn	*	3	V.42 bis compression control
"On		16	V.42 bis string length

* Value Saved in NVRAM
** Command not preceded by an 'AT'

Table 4–5. Dial Modifiers

Command	Function
0 to 9	Dialing digits
A,B,C, D, *, #	Tone dial characters
P	Pulse dial
R	Reverse Originate Mode
S=n	Dial NVRAM telephone number
T	Tone dial
W	Wait for dial tone
,	Pause
!	Flash hook
@	Wait for quiet answer
;	Return to idle state
- ( )	Ignored by modem

Table 4–6. S-Registers Summary

Register		Default	Function
S0	*	0	No. of Rings to auto-answer on
S1		0	Ring count
S2	*	43	Escape character
S3		13	Carriage return character
S4		10	Line feed character
S5		8	Backspace character
S6	*	2	Wait before blind dialing
S7	*	30	Wait for carrier/dial tone
S8	*	2	Pause time for dial modifier
S9	*	6	Carrier detect recovery time
S10	*	14	Lost carrier hang up delay
S11	*	70	DTMF dialing speed
S12	*	50	Guard Time
S13		none	Reserved
S14	*	none	Bit-mapped options
S15		none	Reserved
S16	*	none	Modem test options
S17		none	Reserved
S18	*	0	Modem test timer
S19		none	Reserved
S20		none	Reserved
S21	*	none	Bit-mapped options
S22	*	none	Bit-mapped options
S23	*	none	Bit-mapped options
S24		none	Reserved
S25	*	5	Detect DTR change
S26	*	1	RTS to CTS delay interval
S27	*	none	Bit-mapped options
S28	*	none	Reserved
S29	*	none	Reserved
S30	*	10	Sleep Mode timer

* Value Saved in NVRAM

Table 4–7. Basic Response Codes (\V0)

Numeric Code	Verbose Code
0	OK
1	CONNECT
2	RING
3	NO CARRIER
4	ERROR
5	CONNECT 1200
6	NO DIAL TONE
7	BUSY
8	NO ANSWER
10	CONNECT 2400
+F4	+FCERROR

Table 4–8. Modified Response Codes (\V1)

Numeric Code	Verbose Code
22	CONNECT 300/REL
24	CONNECT 1200/REL
25	CONNECT 2400/REL

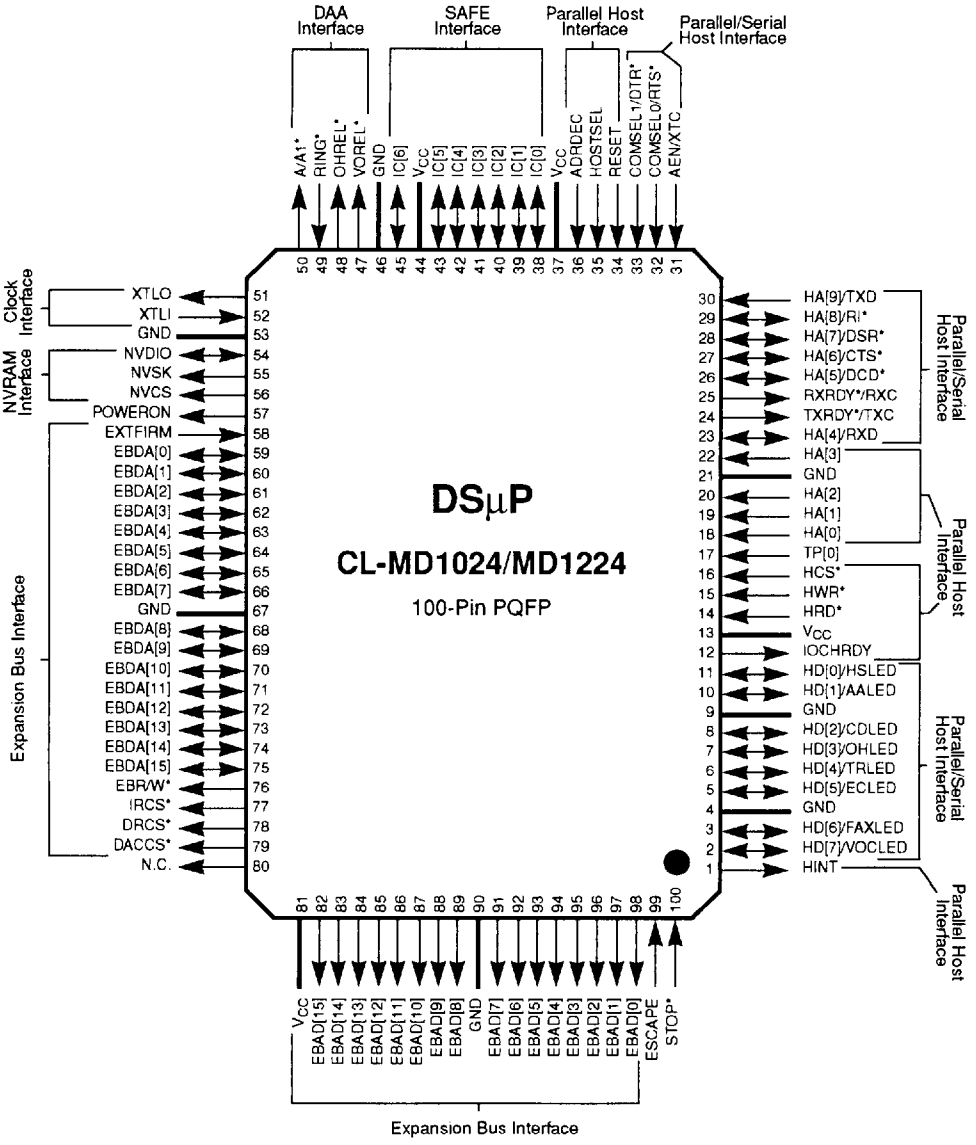
Table 4–9. V.42 Extended Response Codes (\V2)

Numeric Code	Verbose Code
32	CONNECT 300/REL-MNP
34	CONNECT 1200/REL-MNP
35	CONNECT 2400/REL-MNP
42	CONNECT 300/REL-MNP 5
44	CONNECT 1200/REL-MNP 5
45	CONNECT 2400/REL-MNP 5
52	CONNECT 300/REL-LAPM
54	CONNECT 1200/REL-LAPM
55	CONNECT 2400/REL-LAPM
62	CONNECT 300/REL-LAPM V.42 BIS
64	CONNECT 1200/REL-LAPM V.42 BIS
65	CONNECT 2400/REL-LAPM V.42 BIS

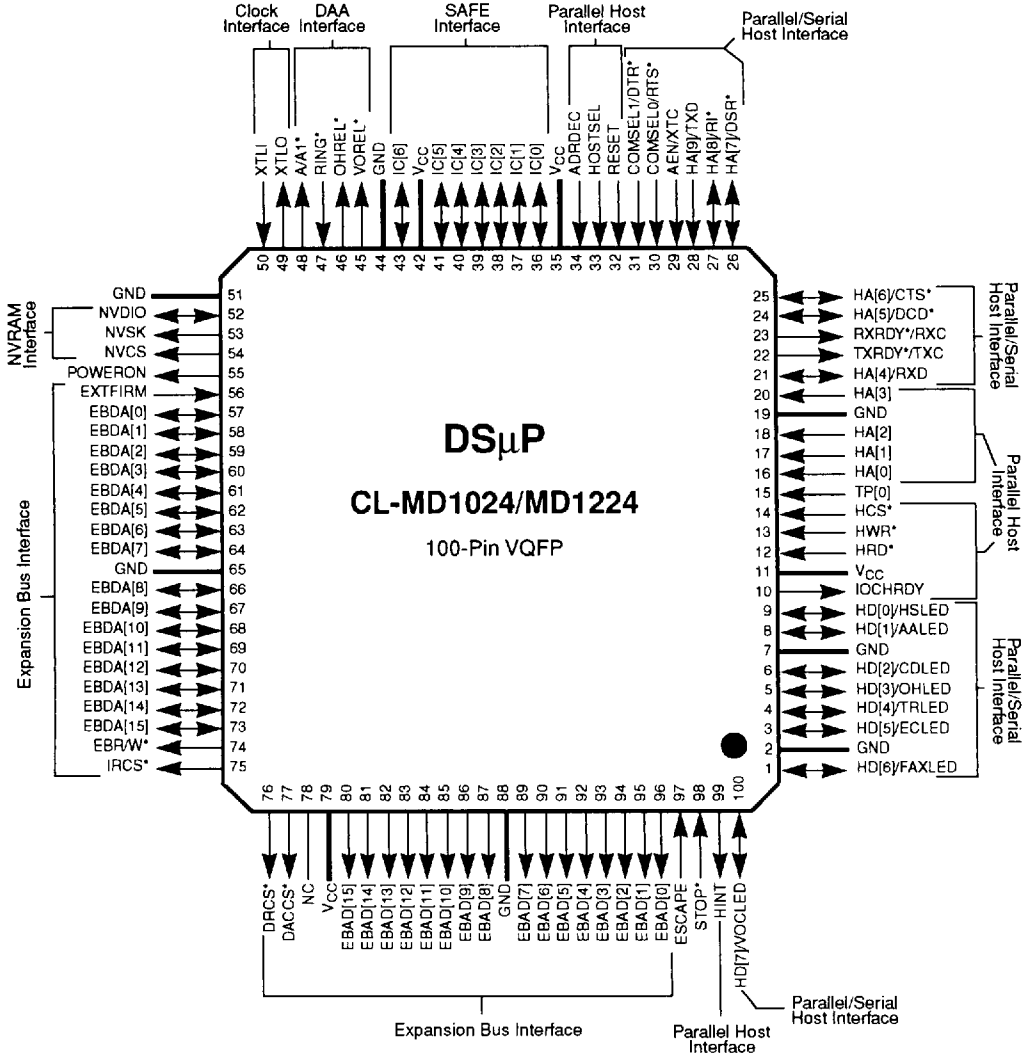
5. HARDWARE SIGNALS

5.1 DSμP Pin Diagram

5.1.1 DSμP PQFP Pin Diagram

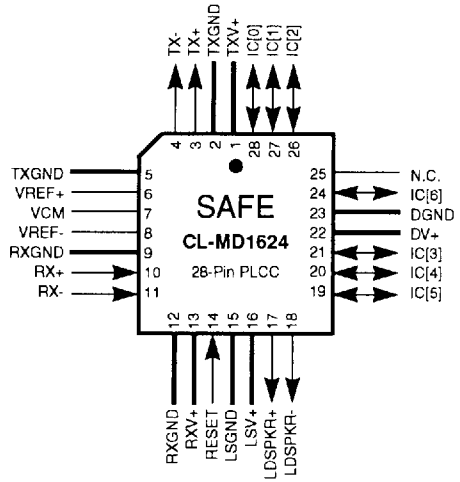


5.1.2 DSµP VQFP Pin Diagram

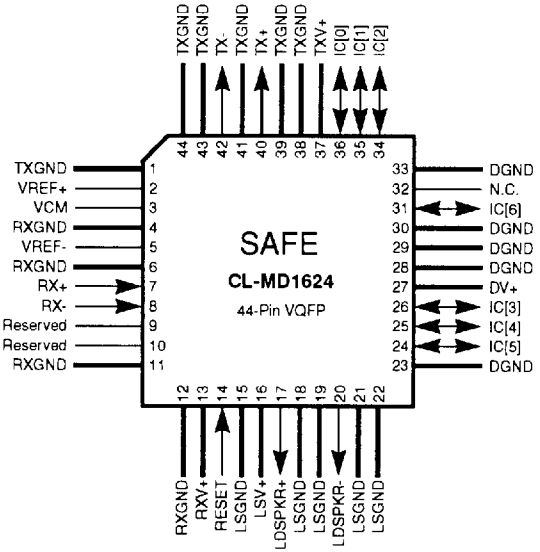


5.2 SAFE Pin Diagram

5.2.1 SAFE PLCC Pin Diagram



5.2.2 SAFE VQFP Pin Diagram



NOTE: N.C. denotes no connect.

5.3 DSµP Pin Descriptions

This section describes the DSµP hardware pins. The following conventions are used in the pin assignment tables: (*) denotes an active-low signal; all other pin names are active-high. I = Input, I/O = Input/Output, O = Output, GND = Ground, AGND = Analog Ground, PWR = Power Supply.

5.3.1 DSµP General Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
ADRDEC	36	34	I	**HOST ADDRESS DECODE SELECTION**: When HOSTSEL is high, then the signal at ADRDEC determines the host address decoding type. ADRDEC has no functionality when HOSTSEL is low. When ADRDEC is high, then the DSµP will internally decode COM Ports 1-4. The extra address lines needed to decode the COM ports are provided within the parallel/serial host interface pins. When ADRDEC is low, only the parallel host interface pins are used to decode the host address. ***CAUTION**: ADRDEC must be grounded when HOSTSEL is low (i.e., for serial host interface).*
ESCAPE	99	97	I	**ESCAPE SEQUENCE SELECTION**: This pin selects the modem escape sequence. A high input or floating (no-connect) signal causes the modem to use the Time Independent Escape Sequence (TIES). A low input signal causes the modem to use the Hayes Escape Sequence. Refer to Section 4.2 on page 13 for more detailed information. **NOTE:** A license may be required to use the Hayes Escape Sequence.
EXTFIRM	58	56	I	**EXECUTE EXTERNAL FIRMWARE ONLY**: This input signal is used to select whether the DSµP executes the internal firmware or only the external firmware. A high input signal causes the DSµP to execute only the external firmware. A low signal causes the DSµP to execute the internal code. **NOTE:** The internal code accesses any external code space as needed.
N.C.	80	78		**NO CONNECT**: This pin is reserved for future enhancements to the device sets and should be left unconnected.
HOSTSEL	35	33	I	**PARALLEL/SERIAL HOST INTERFACE SELECTION**: HOSTSEL high selects the parallel host interface. HOSTSEL low select the serial host interface. When HOSTSEL is low, then ADRDEC must be tied low.
POWERON	57	55	O	**POWER ON STATE INDICATOR**: A high output signal indicates the modem device set is fully powered (i.e., Operational Mode). A low output signal indicates the modem device set is in Sleep or Stop Mode.

5.3.1 DSμP General Pin Descriptions *(cont.)*

Symbol	PQFP	VQFP	Type	Description
RESET	34	32	I	**DSμP RESET**: This pin is used to generate a modem reset. A modem reset is accomplished by pulsing the signal at the RESET Pin from a low to high to low. The RESET Input Pin must be high for at least 1 μs. The modem requires 200 ms, after the high-to-low transition, to initialize all modem functions before receiving any 'AT' commands.
STOP*	100	98	I	**STOP MODE**: A high input signal powers up the device set. A low input signal places the modem in Stop Mode that effectively turns off all device set power usage except for some internal control logic. When Stop Mode is not needed, this input pin should be pulled up to V_{CC}.
XTLI XTLO	52 51	50 49	I O	**DSμP CRYSTAL INPUT AND OUTPUT**: These two pins provide a feed-back circuit for generating the device set system clock.

5.3.2 Non-Volatile RAM (NVRAM) Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
NVCS	56	54	O	**NON-VOLATILE RAM CHIP SELECT**: This output pin provides the NVRAM chip select for reading and writing to the NVRAM. This signal should be connected to the NVRAM CS Pin.
NVDIO	54	52	I	**NON-VOLATILE RAM SERIAL DATA INPUT/OUTPUT**: This pin receives the serial data stream from the NVRAM DO Pin and provides the serial data stream into the NVRAM DI Pin.
NVSK	55	53	O	**NON-VOLATILE RAM SHIFT CLOCK**: This output pin provides the clock for the NVRAM serial data stream. This pin should be connected to the NVRAM SK Pin.

5.3.3 DSμP Parallel Host Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
HA[3]	22	20	I	**HOST ADDRESS LINES[3]**: When both HOSTSEL and ADRDEC are high, this pin is used as Host Address Line 3. (In Serial Mode, tie HA[3] to ground.)
HA[0:2]	18-20	16-18	I	**HOST ADDRESS LINES[0-2]**: These three address lines are used to select the UART Interface Registers. (In Serial Mode, tie HA[0] to V_{CC} and tie HA[1:2] to ground.)

5.3.3 DSμP Parallel Host Interface Pin Descriptions *(cont.)*

Symbol	PQFP	VQFP	Type	Description
HCS*	16	14	I	**HOST CHIP SELECT (UART)**: When HOSTSEL is high and ADRDEC is low, a low input signal at this pin allows the host computer to read or write to the UART Interface Registers. (In Serial Mode, tie HCS* to ground.)
HINT	1	99	O	**HOST INTERRUPT**: When enabled, this signal goes high whenever certain bits change within the UART Registers. There are four possible interrupt sources that may be enabled or disabled using the UART IER Register: receiver data available, Transmitter Holding Register empty, receiver line status, and modem line status. The UART interface automatically drops the HINT Signal level whenever the host performs the appropriate action for the interrupt source.
HRD*	14	12	I	**HOST READ**: When HRD* and HCS* are low, the host can read the data, control and status information from the selected UART Registers. (In Serial Mode, tie HRD* to ground when the DSμP LED drivers [Pins 2, 3, 5, 6, 7, 8, 10, and 11] are used; otherwise, tie HRD* to V_{CC}.)
HWR*	15	13	I	**HOST WRITE**: When HWR* and HCS* are low, the host can write control information or data to the selected UART Registers. (In Serial Mode, tie HWR* to V_{CC}.)
IOCHRDY	12	10	O	**IOCHRDY**: This pin provides a wait-stated output for data, control and status information reads and writes to the modem UART.

5.3.4 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions

The function of these pins depends on the signal at HOSTSEL. The serial RS-232 definition applies to the pin *only* when HOSTSEL is low. The parallel address line description applies to the pin *only* when HOSTSEL and ADRDEC are both high. The parallel data line description applies to the pin *only* when HOSTSEL is high.

Symbol	PQFP	VQFP	Type	Description
AEN/XTC	31	29	I	**PARALLEL ADDRESS ENABLE/SERIAL EXTERNAL TRANSMIT CLOCK**: In Parallel Mode, this pin is used for host address enable. In Serial Synchronous Mode, the DTE may supply the external transmit clock for TXD. This clock must exhibit the same characteristics as TXC.

5.3.4 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions *(cont.)*

Symbol	PQFP	VQFP	Type	Description
COMSEL0/RTS*	32	30	I	**PARALLEL COM PORT SELECTION LINE 0/SERIAL REQUEST TO SEND**: In Parallel Mode with ADRDEC high, the states of COMSEL0 and COMSEL1 are used to select a COM port. In Serial Mode, when low, this signal informs the modem that the DTE is ready to send data on TXD.
COMSEL1/DTR*	33	31	I	**PARALLEL COM PORT SELECTION LINE 1/SERIAL DATA TERMINAL READY**: In Parallel Mode, the states of COMSEL0 and COMSEL1 are used to select a COM port. In Serial Mode, when low, this signal informs the modem that the DTE is ready to establish a communication link.
HA[4]/RXD	23	21	I/O	**PARALLEL ADDRESS LINE 4/SERIAL RECEIVE DATA**: In Parallel Mode with ADRDEC high, this pin is used for Host Address Line 4. In Serial Mode, this is the serial data output to the DTE.
HA[5]/DCD*	26	24	I/O	**PARALLEL ADDRESS LINE 5/SERIAL DATA CARRIER DETECT**: In Parallel Mode with ADRDEC high, this pin is used for Host Address Line 5. In Serial Mode when low, this signal informs the DTE that the modem has detected the remote modem data carrier.
HA[6]/CTS*	27	25	I/O	**PARALLEL ADDRESS LINE 6/SERIAL CLEAR TO SEND**: In Parallel Mode with ADRDEC high, this pin is used for Host Address Line 6. In Serial Mode when low, this signal informs the DTE that the modem is ready to receive data on TXD.
HA[7]/DSR*	28	26	I/O	**PARALLEL ADDRESS LINE 7/SERIAL DATA SET READY**: In Parallel Mode with ADRDEC high, this pin is used for Host Address Line 7. In Serial Mode when low, this signal informs the DTE that the modem is ready to establish a communication link.
HA[8]/RI*	29	27	I/O	**PARALLEL ADDRESS LINE 8/SERIAL RING INDICATOR**: In Parallel Mode with ADRDEC high, this pin is used for Host Address Line 8. In Serial Mode, when low, this signal informs the DTE that the modem has received a valid ring signal.
HA[9]/TXD	30	28	I	**PARALLEL ADDRESS LINE 9/SERIAL TRANSMIT DATA**: In Parallel Mode with ADRDEC high, this pin is used for the Host Address Line 9. In Serial Mode, this signal is the serial data input from the DTE.

HA[0:9]	*COM Port*	*COMSEL1*	*COMSEL0*
3F8-3FF	1	0	0
2F8-2FF	2	0	1
3E8-3EF	3	1	0
2E8-2EF	4	1	1

5.3.4 DSμP Parallel/Serial (RS-232) Host Interface Pin Descriptions *(cont.)*

Symbol	PQFP	VQFP	Type	Description
HD[0]/HSLED	11	9	I/O	**PARALLEL DATA BUS LINE 0/SERIAL HIGH SPEED LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 0. In Serial Mode, when high, this signal indicates the modem is set up for Data Mode 2400 bps or Fax Mode 9600 bps.
HD[1]/AALED	10	8	I/O	**PARALLEL DATA BUS LINE 1/SERIAL AUTO ANSWER — RING DETECT LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 1. In Serial Mode, when high, this signal indicates the modem is set up for Auto-answer Mode. This signal will flash on and off whenever a ring signal is detected.
HD[2]/CDLED	8	6	I/O	**PARALLEL DATA BUS LINE 2/SERIAL CARRIER DETECT — TEST MODE LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 2. In Serial Mode, when high, this signal indicates the modem is receiving valid data carrier (refer to the '&Cn' command).
HD[3]/OHLED	7	5	I/O	**PARALLEL DATA BUS LINE 3/SERIAL OFF HOOK LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 3. In Serial Mode, when high, this signal indicates the modem is off hook.
HD[4]/TRLED	6	4	I/O	**PARALLEL DATA BUS LINE 4/SERIAL TERMINAL READY LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 4. In Serial Mode, when high, this signal indicates the state of DTR (refer to the '&Dn' command).
HD[5]/ECLED	5	3	I/O	**PARALLEL DATA BUS LINE 5/SERIAL ERROR CORRECTION — DATA COMPRESSION LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 5. In Serial Mode when high, this signal indicates the modem is in Error Correction/Data Compression Mode. In Serial Mode, this signal will flash on and off whenever the modem is in a Test Mode (&Tn).
HD[6]/FAXLED	3	1	I/O	**PARALLEL DATA BUS LINE 6/SERIAL FAX MODE LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 6. In Serial Mode when high, this signal indicates the modem is in Fax Modem Mode. When low, this signal indicates the modem is in Data Modem Mode or Voice Mode.
HD[7]/VOCLED	2	100	I/O	**PARALLEL DATA BUS LINE 7/SERIAL VOICE MODE LED:** In Parallel Mode, this pin is used for the Host Data Bus Line 7. In Serial Mode when high, this signal indicates the modem is in Voice Mode. When low, this signal indicates the modem is in Data Modem or Fax Modem Mode.

5.3.5 DSμP Expansion Bus Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
RXRDY*/RXC	25	23	O	**PARALLEL DMA RECEIVER READ/SERIAL RECEIVE CLOCK**: In Parallel Mode, this pin is the 16C550A DMA Receiver Ready Signal. In Serial Synchronous Mode, RXC is the output clock for RXD.
TXRDY*/TXC	24	22	O	**PARALLEL DMA TRANSMITTER READY/SERIAL TRANSMIT CLOCK**: In Parallel Mode, this is the 16C550A DMA Transmitter Ready Signal. In Serial Synchronous Mode, TXC is the output clock for TXD.
DACCS*	79	77	O	**DAC CHIP SELECT**: This output pin is the chip select for an eye-pattern circuit. The DSμP sends the values for the received signal point data to the Expansion Bus for diagnostic purposes.
DRCS*	78	76	O	**DATA RAM CHIP SELECT**: This output pin provides the chip select for external RAM.
EBAD[0:15]	82-89, 91-98	80-87, 89-96	O	**EXPANSION BUS ADDRESS LINES**: These pins provide the addresses necessary for accessing external memory.
EBDA[0:15]	59-66, 68-75	57-64, 66-73	I/O	**EXPANSION BUS DATA LINES**: This bus provides bidirectional data access between the DSμP and external memory.
EBR/W*	76	74	O	**EXPANSION BUS DATA RAM READ/WRITE* LINE**: This pin selects whether the DSμP is reading or writing to the external RAM. This signal works in conjunction with the DRCS* Pin.
IRCS*	77	75	O	**INSTRUCTION ROM CHIP SELECT**: This output pin provides the chip select for external ROM.

5.3.6 DSμP Power Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
GND	4, 9, 21, 46, 53, 67, 90	2, 7 19, 44, 51, 65, 88	GND	**DIGITAL GROUND**.
V_{CC}	13, 37, 44, 81	11, 35, 42, 79	PWR	**+5V POWER SUPPLY**: The DSμP requires only +5 volts to perform all the digital processing.

5.3.7 DSμP DAA Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
A/A1*	50	48	O	**KEY TELEPHONE HOLD INDICATOR**: This output signal indicates to a multi-phone system the modem has telephone-line control. This output can sink up to 10 mA for a normally-open relay. ***CAUTION:*** *The A/A1 function should never be used on an RJ-11 telephone jack, since most homes provide a second telephone signal on RJ-11 Pins 2 and 5.*
OHREL*	48	46	O	**OFF-HOOK RELAY CONTROL**: This pin is used to control a relay connected to the telephone line. This output can sink up to 10 mA for a normally-open relay.
RING*	49	47	I	**RING SIGNAL**: The ring signal from the DAA is fed into this input pin for ring detection.
VOREL*	47	45	O	**VOICE RELAY CONTROL**: This pin is used to control a relay for recording a voice message. This output can sink up to 10 mA.

5.3.8 DSμP SAFE Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
IC[0:6]	38-43, 45	36-41, 43	I/O	**MODEM INTERCONNECTIONS**: These pins provide the control/data/clock signals between the DSμP and the SAFE. No external components should be connected to these signals.

5.3.9 DSμP Cirrus Logic Manufacturing Test Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
TP[0]	17	15	I	**MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing testing. This pin should be pulled up to V_{CC} for all applications.

5.4 SAFE Pin Descriptions

5.4.1 SAFE General Pin Descriptions

Symbol	PLCC	VQFP	Type	Description
LDSPKR+ LDSPKR-	17 18	17 20	O O	**LOUDSPEAKER OUTPUT**: These pins provide a differential output signal for driving an external loudspeaker. These pins can be connected directly to a ≥ 8-ohm speaker or a speaker-amplifier.
Reserved	—	9, 10	I	**RESERVED**: These pins are reserved for future enhancements. These pins should be grounded unless otherwise noted.
N.C.	25	32	—	**NO CONNECT**: This pin should be left floating.
RESET	14	14	I	**SAFE RESET**: This pin is used to generate a SAFE reset. A reset is accomplished by pulsing the signal at the RESET Pin from a low to high to low. The RESET Input Pin must be high for at least 10 µs. The SAFE requires 200 ms, after the high-to-low transition, before communicating with the DSµP.

5.4.2 SAFE Power Supply Pin Descriptions

Symbol	PLCC	VQFP	Type	Description
DGND	23	23, 28, 29, 30, 33	GND	**DIGITAL GROUND REFERENCE.**
DV+	22	27	PWR	**DIGITAL SUPPLY** (5 volts +/- 5%).
LSGND	15	15, 18, 19, 21, 22	AGND	**LOUDSPEAKER ANALOG GROUND REFERENCE.**
LSV+	16	16	PWR	**LOUDSPEAKER SUPPLY VOLTAGE** (5 volts +/- 5%).
RXGND	9,12	4, 6, 11, 12	AGND	**RECEIVER ANALOG GROUND REFERENCE.**
RXV+	13	13	PWR	**RECEIVER ANALOG SUPPLY VOLTAGE** (5 volts +/- 5%).
TXGND	2, 5	1, 38, 39, 41, 43, 44	AGND	**TRANSMITTER ANALOG GROUND REFERENCE.**
TXV+	1	37	PWR	**TRANSMITTER ANALOG SUPPLY VOLTAGE** (5 volts +/- 5%).
VCM	7	3	I	**VOLTAGE COMMON MODE**: The SAFE provides an internal 2.5V reference for the differential analog circuitry. This pin allows the reference to be bypassed using an external 1.0-µF capacitor.

5.4.2 SAFE Power Supply Pin Descriptions *(cont.)*

Symbol	PLCC	VQFP	Type	Description
VREF+ VREF-	6 8	2 5	I I	**VOLTAGE REFERENCE BUFFER**: The SAFE incorporates an internal differential voltage reference. These pins allow the internal differential reference to be bypassed using an external 1.0-µF capacitor.

5.4.3 SAFE DSµP Interface Pin Descriptions

Symbol	PLCC	VQFP	Type	Description
IC[0:6]	19-21 24, 26-28	24-26 31, 34-36	I/O	**MODEM INTERCONNECTIONS**: These pins provide the control/data/clock signals between the DSµP and the SAFE. No external component should be connected to these signals.

5.4.4 SAFE DAA Interface Pin Descriptions

Symbol	PLCC	VQFP	Type	Description
RX+ RX-	10 11	7 8	I I	**RECEIVE ANALOG DATA**: These input pins receive the analog-differential signals from the DAA.
TX+ TX-	3 4	40 42	O O	**TRANSMIT ANALOG DATA**: These pins provide the analog-transmitter-differential output signals to the DAA.

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Supply voltage (V_{CC}) ..... +6.0 Volts
Input voltages, with respect to ground: ..... -0.3 Volts to V_{CC} +0.5 Volts
Operating temperature (T_A): ..... 0° C to 70° C
Storage temperature: ..... -65° C to 150° C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

Supply voltage (V_{CC}) ..... 5V ± 5%
Operating free air ambient temperature ..... 0° C < T_A < 70° C
Crystal frequency ..... 11.0592 MHz

6.3 DC Electrical Characteristics — CL-MD1024 and CL-MD1224

(@ V_{CC} = 5V ± 5%, T_A = 0° C to 70° C)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–	V_{CC}	V	(See Notes below)
V_{OL}	Output Low Voltage		–	0.4	V	I_{OL} = 2.4 mA; (See Notes)
V_{OH}	Output High Voltage	2.4	–		V	I_{OH} = -400 µA
I_{IL}	Input Leakage Current	-10	–	10	µA	$0 < V_{IN} < V_{CC}$
I_{LL}	Data Bus 3-State Leakage Current	-10	–	10	µA	$0 < V_{OUT} < V_{CC}$
I_{OC}	Open-Drain Output Leakage Current	-10	–	10	µA	$0 < V_{OUT} < V_{CC}$
I_{CC}	Power Supply Current	–	40	50	mA	Operational Mode CLK = 11.0592 MHz
C_{IN}	Input Capacitance	–	–	10	pF	
C_{OUT}	Output Capacitance	–	–	10	pF	

NOTES: V_{OL} for open-drain signals is 0.5V @ 16 mA sinking. V_{IH} is 2.7 V minimum on RESET*.

6.4 AC/DC Electrical Characteristics — CL-MD1624

(@ V_{CC} = 5V ± 5%, T_A = 0° C to 70° C)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
P_D	Power Dissipation	–	130	195	mW	Operational Mode
P_{Down}	Power Dissipation (Power-down Mode)	–	–	500	µW	Loud Speaker Driver Off
I_A	Analog Current (TV+, RV+)	–	24	–	mW	Loud Speaker Driver Off
I_D	Digital Current (DV+)	–	2	–	mA	
I_{IDS}	Loud Speaker Current (LDSPKR+, LDSPKR-)	–	–	125	mA	
R_X	Loud Speaker Impedance	8	–	–	Ohms	

6.5 Index of Timing Information

Table 6–1. Parallel Host Interface Timing (ADRDEC Pin Low) — Write Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	HA[2:0] set-up time to HCS* low	0	–	ns
t_2	HCS* low to HWR* low set-up time	10	–	ns
t_3	HD[7:0] valid from HWR* low	–	10	ns
t_4	HWR* low to IOCHRDY low	–	30	ns
t_5	HWR* low to IOCHRDY tri-stated	–	250	ns
t_6	HWR* hold time after IOCHRDY high	0	–	ns
t_7	HD[7:0] hold time after HWR* high	0	–	ns
t_8	HCS* hold time after HWR* high	0	–	ns
t_9	HA[2:0] hold time after HWR* high	0	–	ns

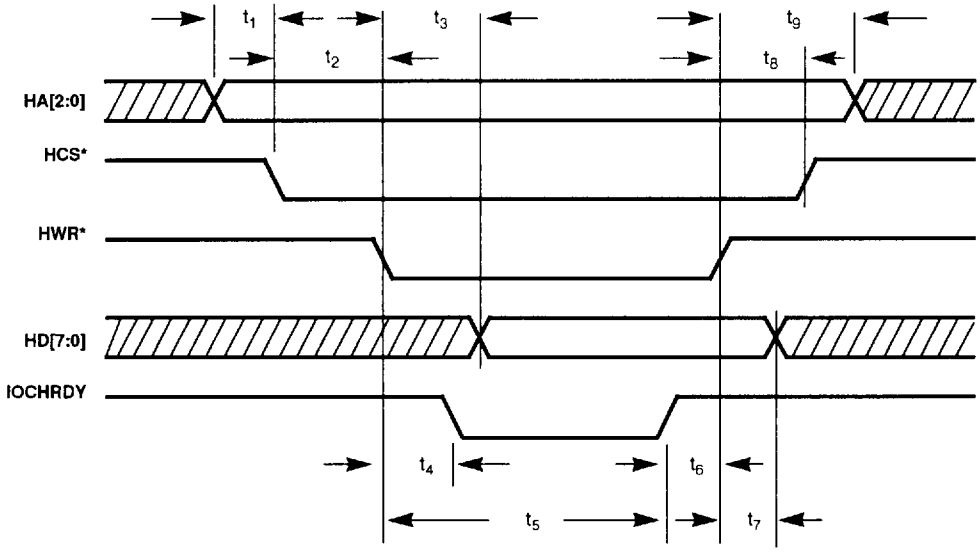


Figure 6–1. Parallel Host Interface Timing Diagram (ADRDEC Pin Low) — Write Cycle

Table 6–2. Parallel Host Interface Timing (ADRDEC Pin High) — Write Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	HA[9:0], AEN set-up time to HWR* low	10	–	ns
t_2	HD[7:0] valid from HWR* low	–	10	ns
t_3	HWR* low to IOCHRDY low	–	30	ns
t_4	HWR* low to IOCHRDY tri-stated	–	250	ns
t_5	HWR* hold time after IOCHRDY high	0	–	ns
t_6	HD[7:0] hold time after HWR* high	0	–	ns
t_7	HA[9:0], AEN hold time after HWR* high	0	–	ns

NOTE: HCS* must be tied high when ADRDEC is tied high.

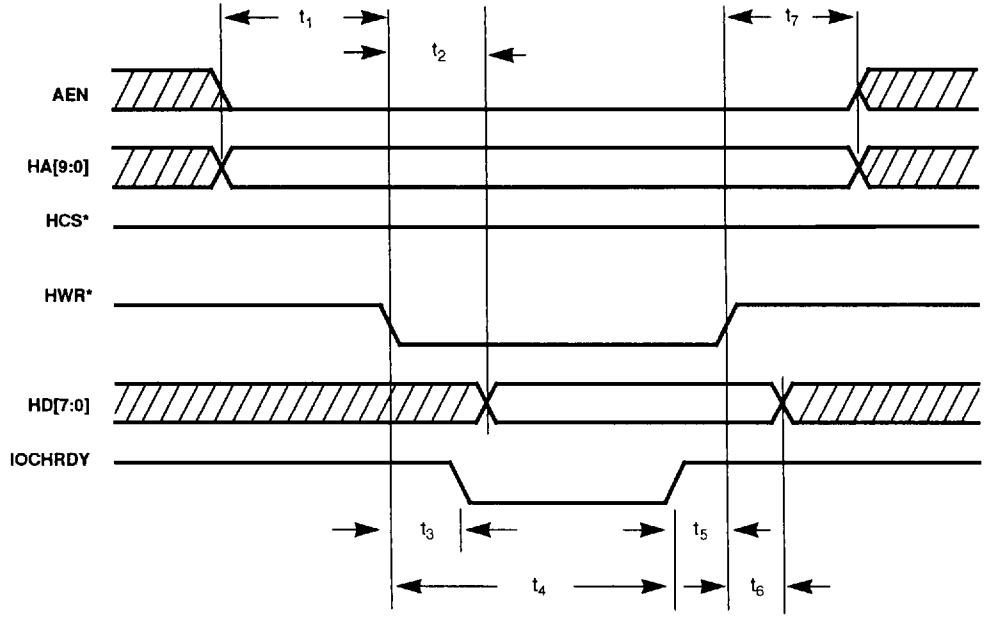


Figure 6–2. Parallel Host Interface Timing Diagram (ADRDEC Pin High) — Write Cycle

Table 6–3. Parallel Host Interface Timing (ADRDEC Pin Low) — Read Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	HA[2:0] set-up time to HCS* low	0	–	ns
t_2	HCS* set-up time to HRD* low	10	–	ns
t_3	HD[7:0] valid after HRD* low	–	250	ns
t_4	HRD* low to IOCHRDY low	–	30	ns
t_5	HRD* low to IOCHRDY tri-state	–	250	ns
t_6	HRD* hold time after IOCHRDY high	0	–	ns
t_7	HRD* high to HD[7:0] tri-state	–	30	ns
t_8	HCS* hold time after HRD* high	0	–	ns
t_9	HA[2:0] hold time after HRD* high	0	–	ns

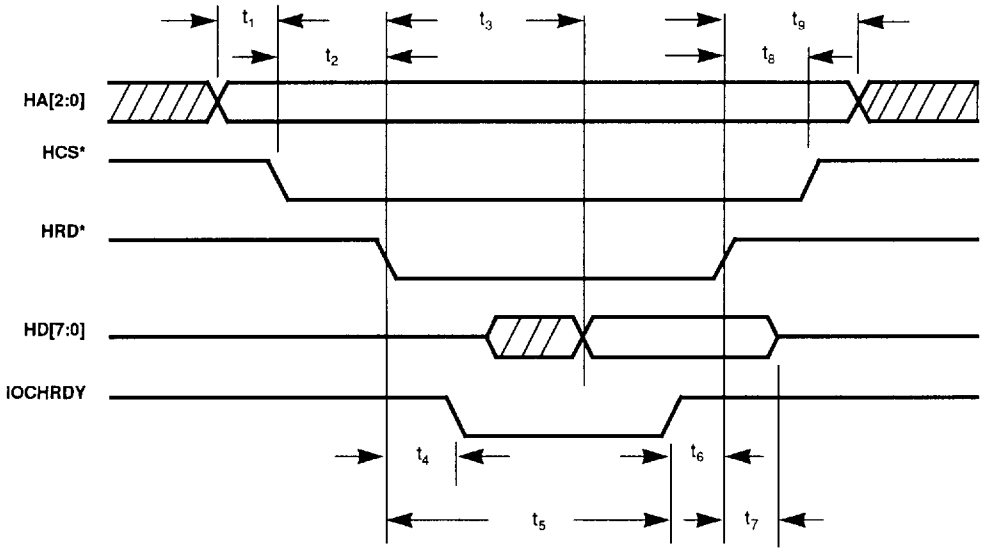


Figure 6–3. Parallel Host Interface Timing (ADRDEC Pin Low) — Read Cycle

Table 6–4. Parallel Host Interface Timing (ADRDEC Pin High) — Read Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	HA[9:0], AEN set-up time to HRD* low	10	–	ns
t_2	HD[7:0] valid after HRD* low	–	250	ns
t_3	HRD* low to IOCHRDY low	–	30	ns
t_4	HRD* low to IOCHRDY tri-state	–	250	ns
t_5	HRD* hold time after IOCHRDY high	0	–	ns
t_6	HRD* high to HD[7:0] tri-state	–	30	ns
t_7	HA[9:0], AEN hold time after HRD* high	0	–	ns

NOTE: HCS* must be tied high when ADRDEC is tied high.

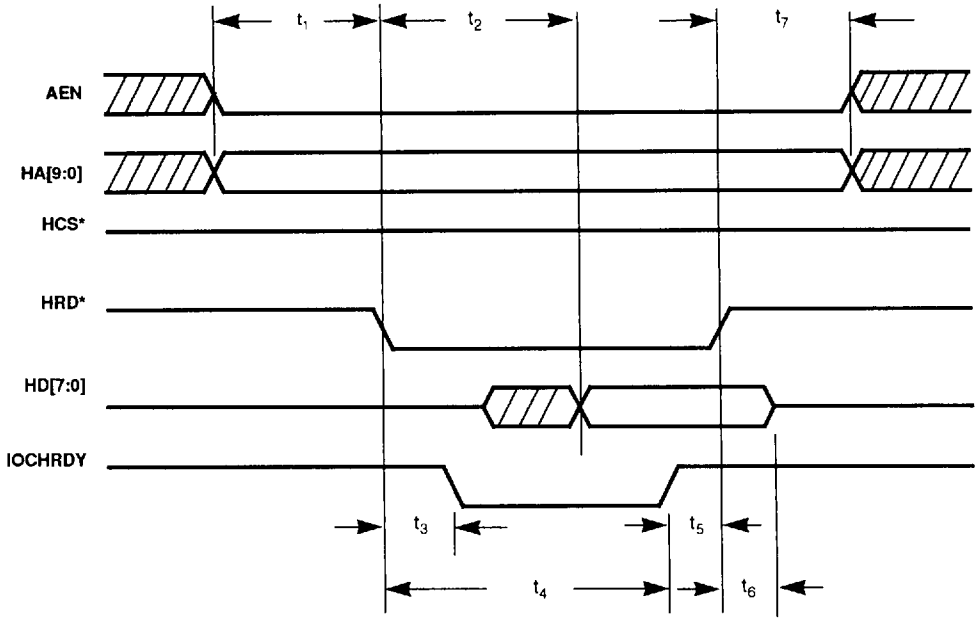


Figure 6–4. Parallel Host Interface Timing Diagram (ADRDEC Pin High) — Read Cycle

Table 6–5. Expansion Bus Timing — Write Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	DRCS*, DACCS* active duration	85	–	ns
t_2	EBAD[15:0], DRCS*, DACCS* set-up time before EBR/W* low	–	10	ns
t_3	EBAD[15:0] hold time after DRCS*, DACCS* high	0	–	ns
t_4	EBDA[15:0] valid from EBR/W* low	–	8	ns
t_5	EBR/W* active duration	38	–	ns
t_6	DRCS*, DACCS* high after EBR/W* high	0	–	ns
t_7	EBDA[15:0] hold time after EBR/W*	2	–	ns

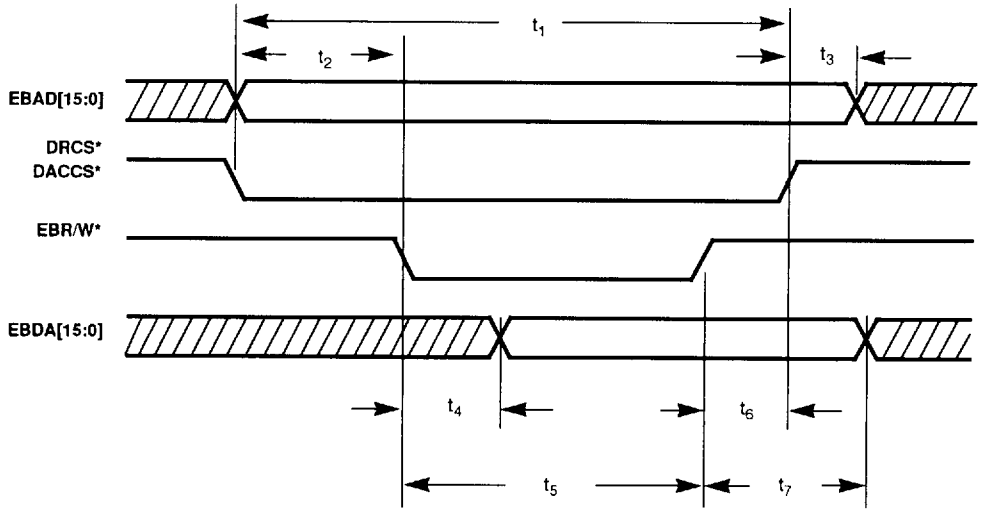


Figure 6–5. Expansion Bus Timing — Write Cycle

Table 6–6. Expansion Bus Timing — Read Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	DRCS*, DACCS*, IRCS* active duration	85	–	ns
t_2	EBAD[15:0] hold time after DRCS*, DACCS*, IRCS* high	0	–	ns
t_3	EBDA[15:0] set-up time before DRCS*, DACCS*, IRCS* high	30	–	ns
t_4	EBDA[15:0] hold time after DRCS* DACCS*, IRCS* high	0	–	ns

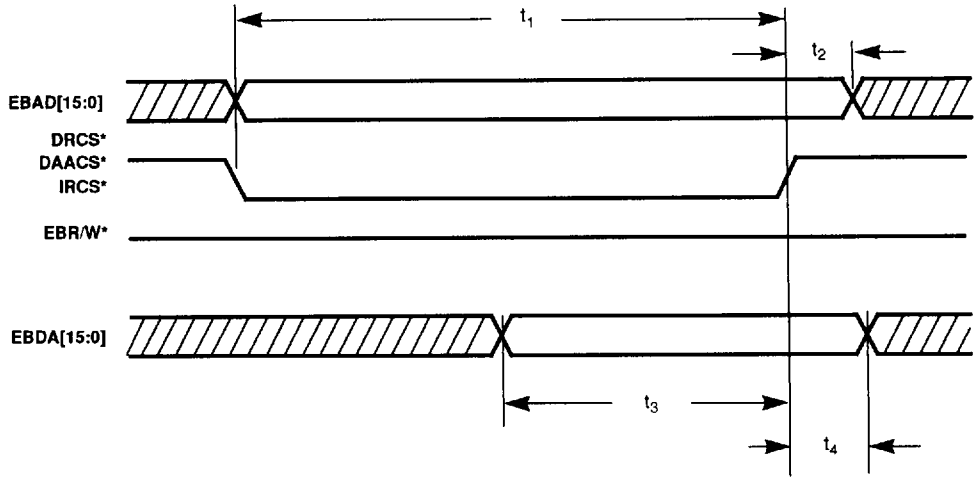
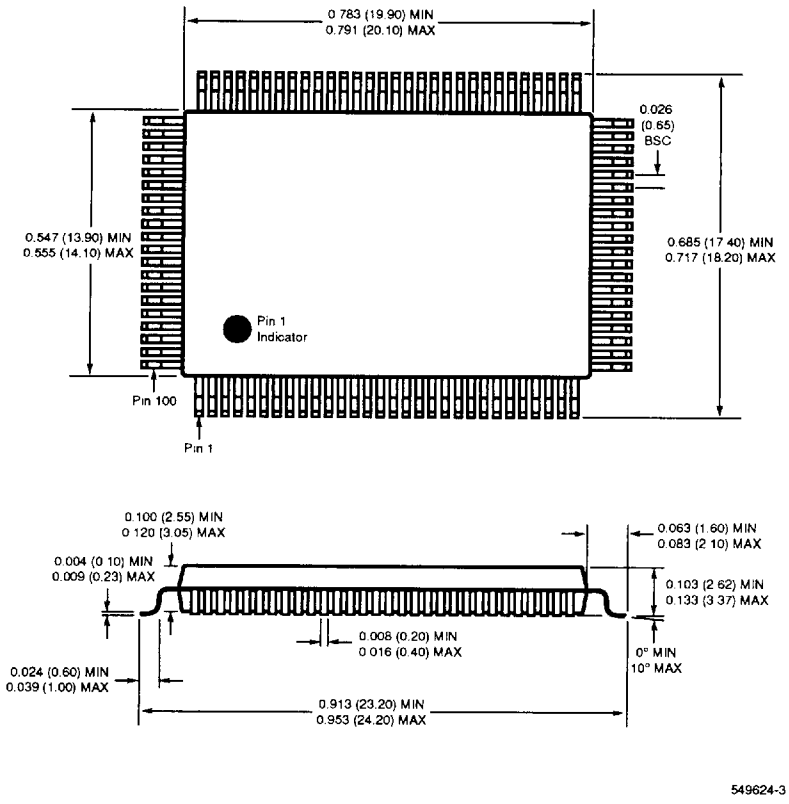


Figure 6–6. Expansion Bus Timing — Read Cycle

7. SAMPLE PACKAGE INFORMATION

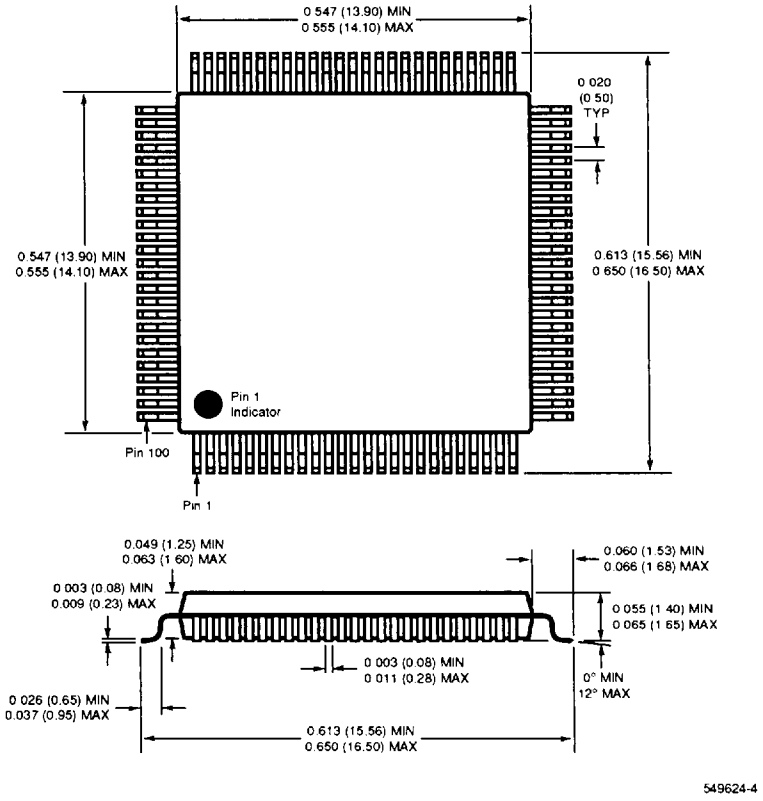
7.1 100-Pin PQFP Package Dimensions



549624-3

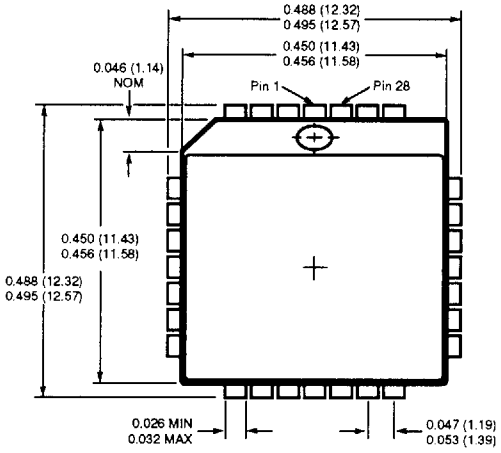
NOTE: All dimensions are in inches and parenthetically in millimeters.

7.2 100-Pin VQFP Package Dimensions

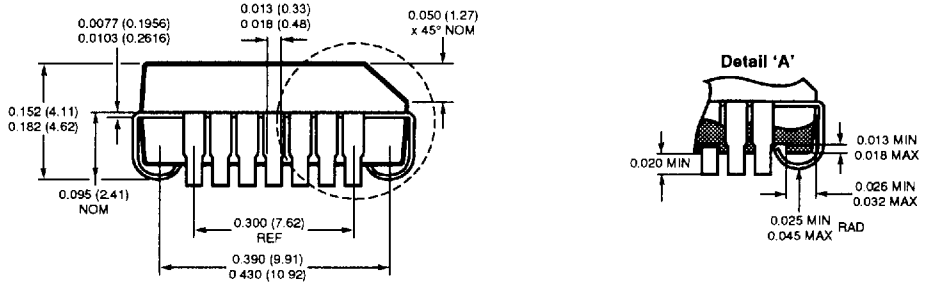


NOTE: All dimensions are in inches and parenthetically in millimeters.

7.3 28-Pin PLCC Package Dimensions



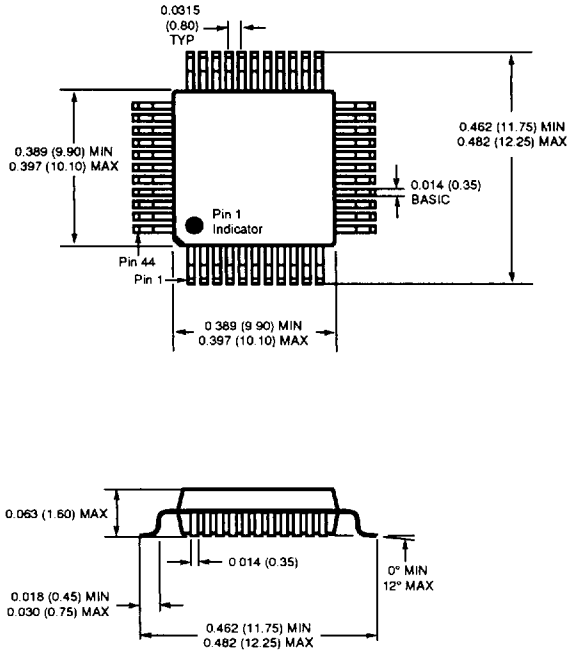
549624-5a



549624-5b

NOTE: All dimensions are in inches and parenthetically in millimeters.

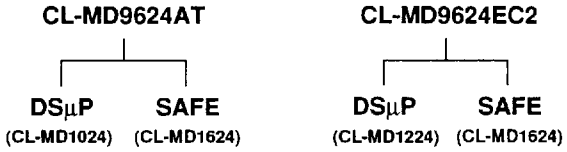
7.4 44-Pin VQFP Package Dimensions



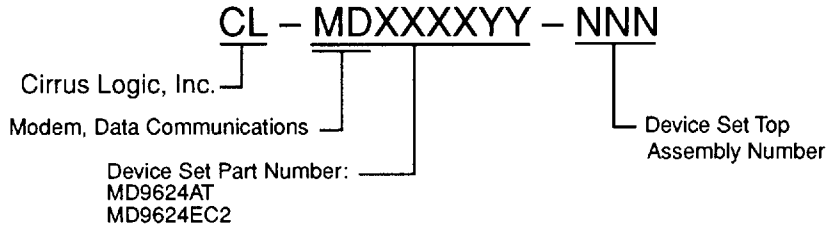
NOTE: All dimensions are in inches and parenthetically in millimeters.

8. ORDERING INFORMATION

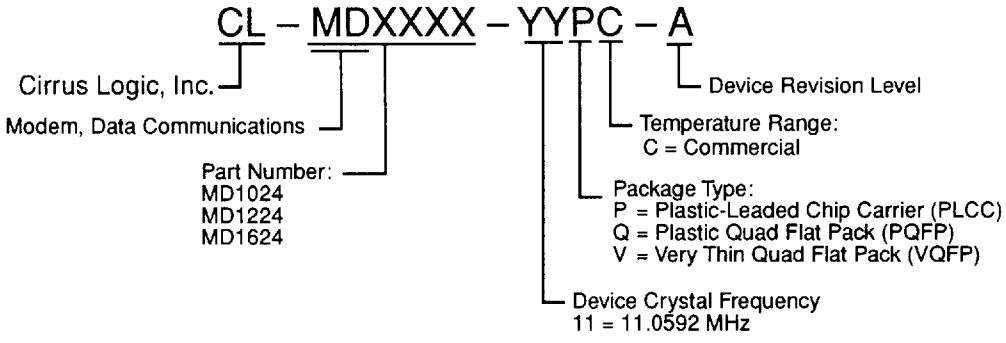
Device Set Composition



Device Set Information



Device Information



9. SCHEMATICS

This section provides several modem design examples. The key segments for a typical modem are divided into separate figures or circuits. These individual circuits may then be combined to form a modem for a specific application. For example:

An internal modem with local record/playback (with V.42/MNP):	Figures 9–1, 9–2b, 9–3, and 9–5
An internal modem without local record (without V.42/MNP):	Figures 9–1, 9–2a, and 9–5
A box modem with local record/playback (with V.42/MNP):	Figures 9–6, 9–2b, 9–3, and 9–5
A box modem with local record/playback (without V.42/MNP):	Figures 9–6, 9–2b, and 9–5

A list of the circuits provided is as follows:

Figure 9–1. Parallel host interface and DSµP-SAFE interface

Figure 9–2a. DAA design for data/fax/voice without local record function (local playback through speaker)

Figure 9–2b. DAA design for data/fax/voice with local phone powered by modem (allows local record/playback)

Figure 9–3. SRAM interface for CL-MD9624EC2 (V.42/MNP) and optional external buffers for CL-MD9624AT designs

Figure 9–4. A/A1 circuit — not recommended for U.S. home market

Figure 9–5a. Direct-connect speaker circuit

Figure 9–5b. Amplified speaker circuit

Figure 9–6. Serial host interface (RS-232); refer to Figure 9–1 for DSµP-SAFE interface

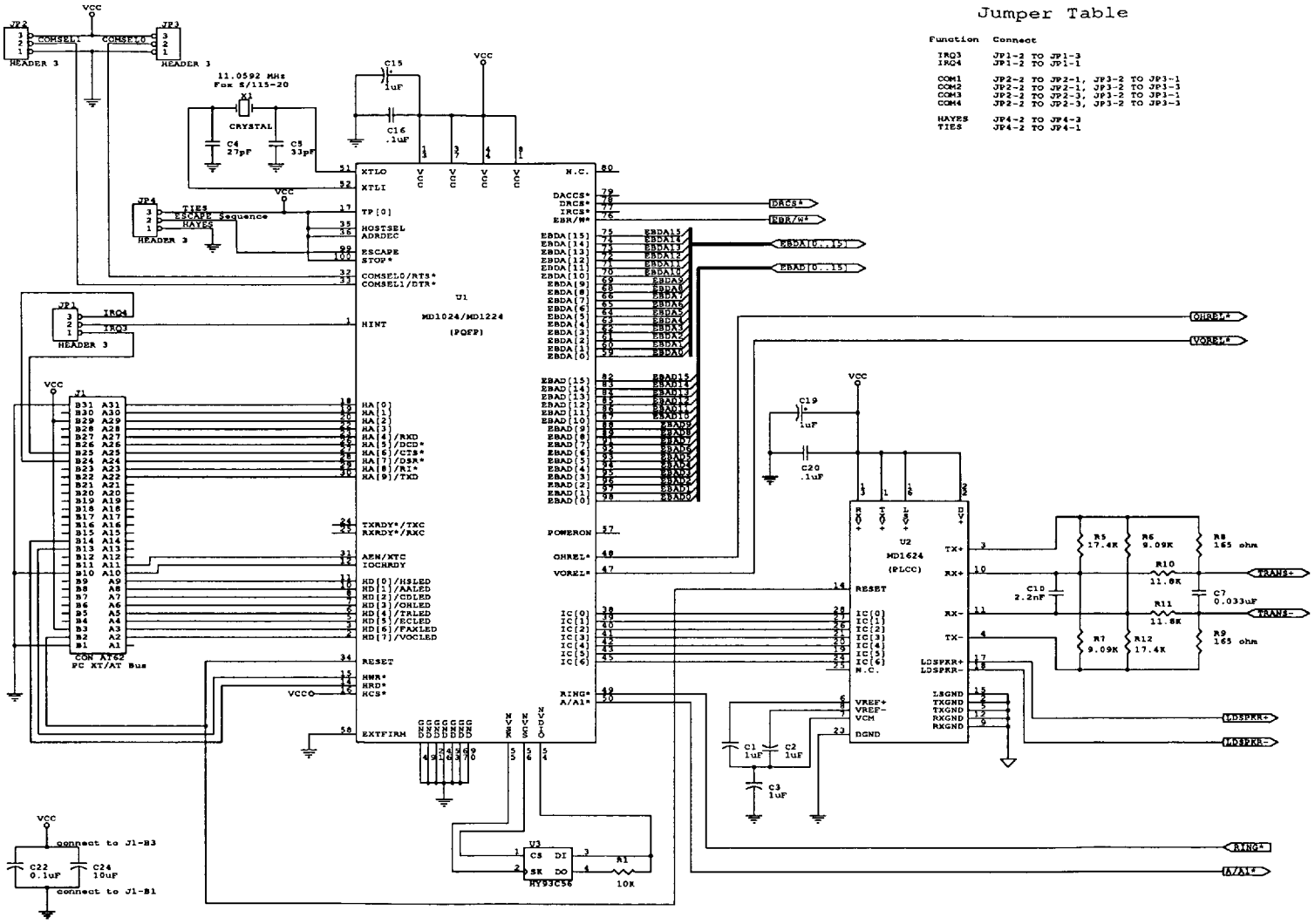


Figure 9-1. CL-MD9624AT/EC Internal Modem Schematic (bus interface)

(3/10/93)

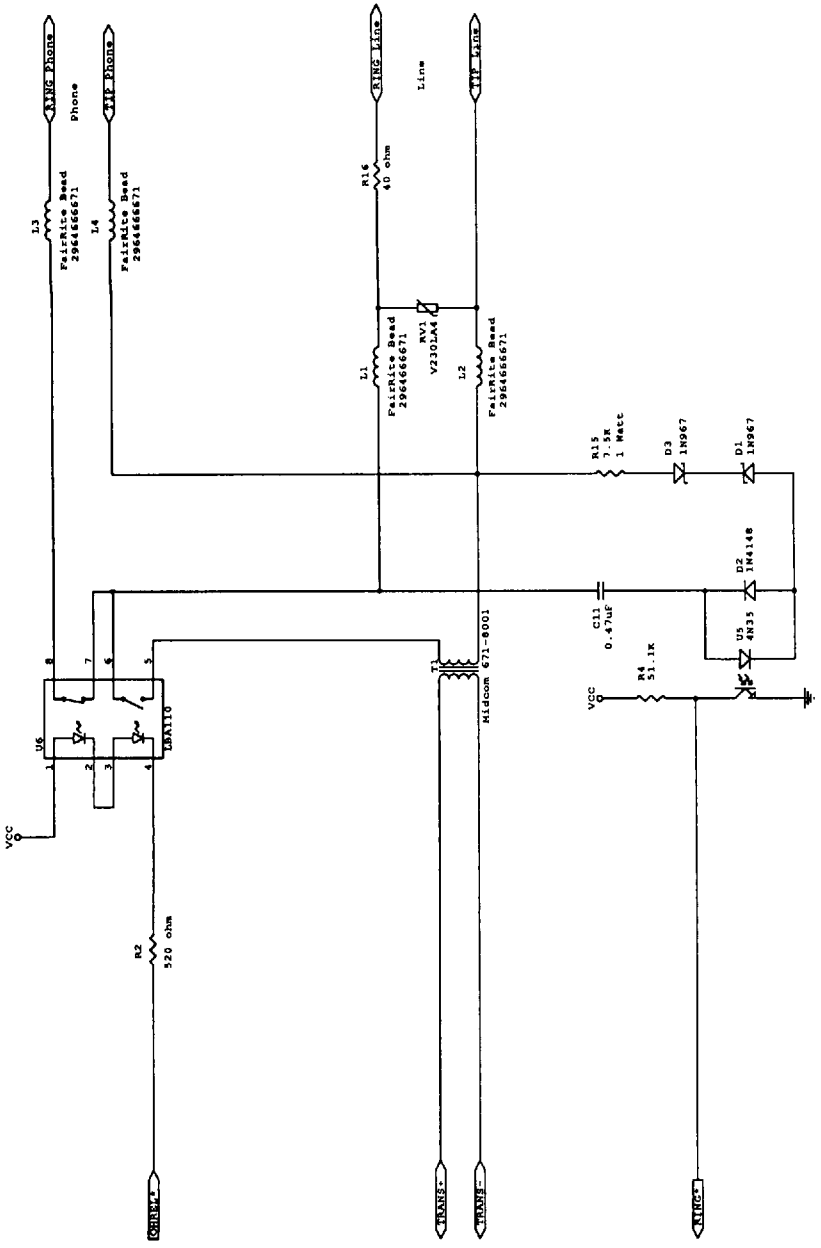


Figure 9-2a. CL-MD9624AT/EC DAA Design without local Voice Recording

(2/25/93)

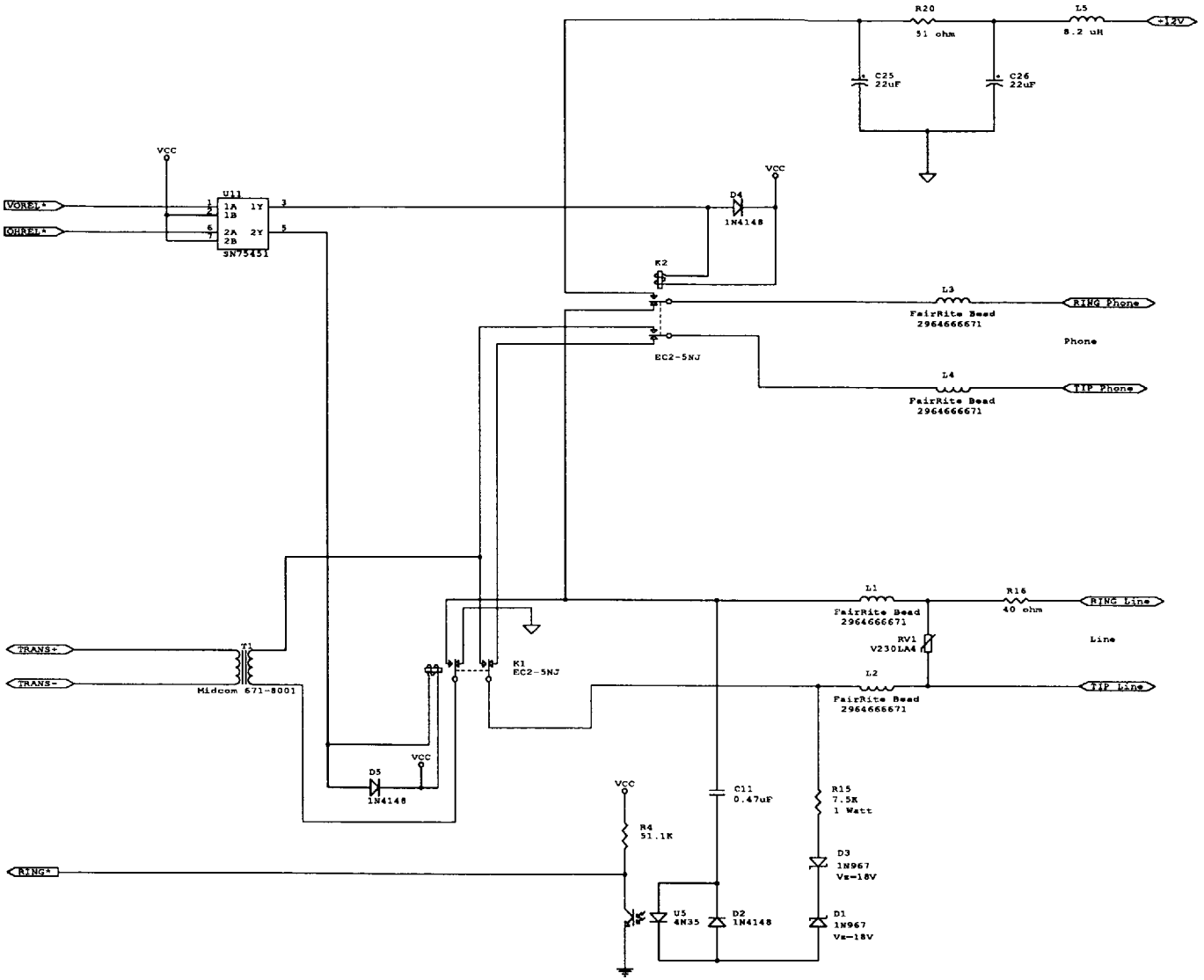


Figure 9-2b. CL-MD9624AT/EC DAA Design with local Voice Recording

(2/25/93)

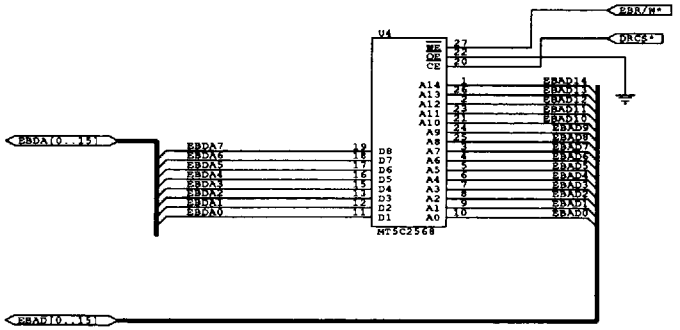


Figure 9-3. SRAM Circuit (CL-MD9624EC only)

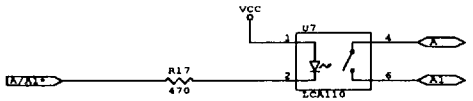


Figure 9-4. A/A1 Circuit

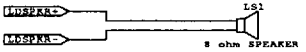


Figure 9-5a. Direct Connect to Speaker Circuit

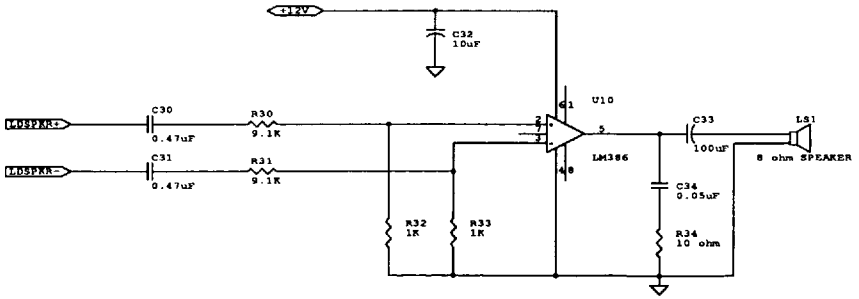


Figure 9-5b. Amplified Speaker Circuit

(2/25/93)

45

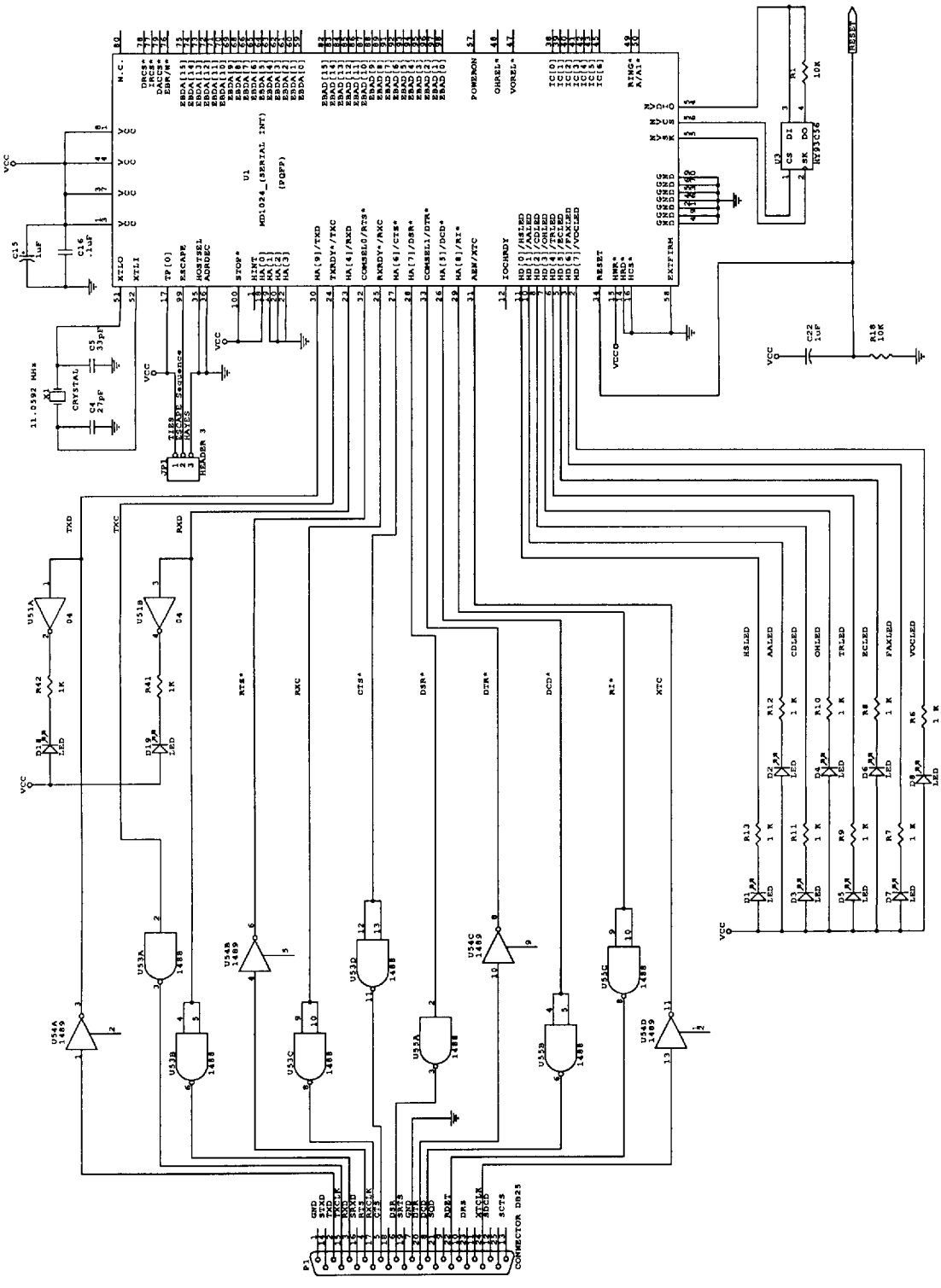


Figure 9-6. CL-MD9624AT/EC Serial Host Interface Schematic