REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-03-15

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, FUTUREBUS ARBITRATION CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-95543
A	67268	

SHEET 1 OF 34

DESC FORM 193
JUL 94

5962-E109-95

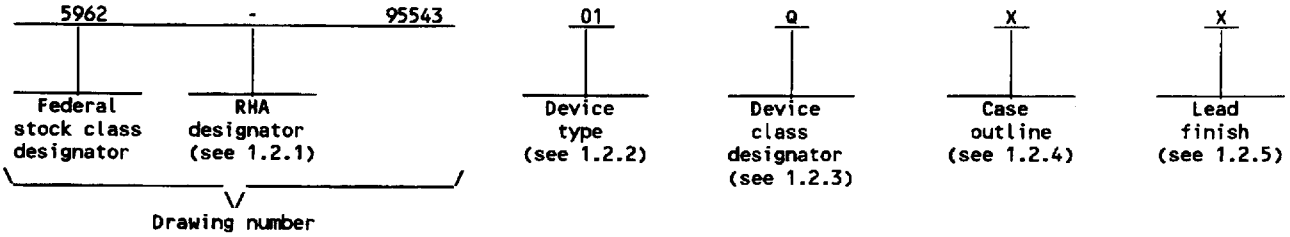
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0009877 752

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	DS3875	futurebus arbitration controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	see figure 1	68	flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	6.5 V
Control input voltage	5.5 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D) 2/	3.9 W
Lead temperature (soldering,10 seconds)	+260°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	3.4°C/W
Thermal resistance, junction-to-ambient (Θ_{JA})	38°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing Logic tests (MIL-STD-883, test method 5012)	3/ XX percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate at 11.5 mW/C above 25°C.
3/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 100 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = 5 V ±10% 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical 1 input voltage	V_{IH}		1, 2, 3	01	2.8		V
Logical 0 input voltage	V_{IL}		1, 2, 3	01		0.75	V
Logical 0 output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 8 mA	1, 2, 3	01		0.7	V
Logical 1 output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -4 mA	1, 2, 3	01	2.4		V
Input leakage diode current	I_I	V_{CC} = 5.5 V V_{IN} = V_{DD} or V_{SS}	1, 2, 3	01	-3	3	µA
Static supply current	I_{CC}	V_{CC} = 5.5 V input at standby	1, 2, 3	01		30	mA
Dynamic supply current	I_{DD}	V_{CC} = 5.5 V	1, 2, 3	01		100	mA
Functional test		V_{CC} = 4.5 V, 5.5 V See 4.4.1b	7, 8				
$\overline{BRQ}$ asserted to Bgrant asserted	t_1	V_{CC} = 4.5 V See figure 4	9, 10, 11	01		36	ns
Aqi negated to AcOo, Aclo	t_2		9, 10, 11	01		30	ns
Aqi negated to Apo asserted	t_3		9, 10, 11	01		31	ns
$\overline{MGRQ}$ or $\overline{BRQ}$ asserted to Apo asserted	t_4		9, 10, 11	01		38	ns
$\overline{ENDT}$ asserted to Apo asserted (dummy cycle)	t_5		9, 10, 11	01		46	ns
$\overline{BRQ}$ asserted to Apo asserted (consecutive bus request)	t_6		9, 10, 11	01		34	ns

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = 5 V ±10% 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{Halt}}$ negated to Apo asserted	t_7	V_{CC} = 4.5 V See figure 4	9, 10, 11	01		28	ns
Max CN_$\overline{\text{LE}}$ negated to ARO negated	t_{100}		9, 10, 11	01		4+ (0-25)	ns
CN_$\overline{\text{LE}}$ width	t_{101}		9, 10, 11	01	18	28	ns
CN port setup time	t_{102}		9, 10, 11	01	23		ns
Iba-$\overline{\text{CMPT}}$ asserted to Aro negated. (determined by programmable value IBA mode)	t_{104}		9, 10, 11	01	20+ (0-25)		ns
$\overline{\text{CMPT}}$ asserted to Aro negated. (determined by programmable value)	t_{105}		9, 10, 11	01	20+ (0-25)		ns
ACOO asserted to Aro negated. (determined by programmable value slow mode)	t_{106}		9, 10, 11	01	18+ (0-25)		ns
APO asserted to CN_$\overline{\text{LE}}$ asserted. CTRL3 (0), "go" bit is set	t_{107}		9, 10, 11	01		32	ns
APO asserted to CMPT asserted	t_{108}		9, 10, 11	01		24	ns
APO asserted to IBA_CMPT asserted	t_{109}		9, 10, 11	01		22	ns
APO asserted to ACOO asserted slow mode	t_{110}		9, 10, 11	01		32	ns
ARI negated to AB_RE asserted	t_{200}		9, 10, 11	01		62	ns

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = 5 V ±10% 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
IBA_$\overline{S}$ asserted to BGRNT asserted IBA mode	t_{202}	V_{CC} = 4.5 V See figure 4	9, 10, 11	01		40	ns
$\overline{WIN}$_$\overline{GT}$ asserted to Aqo asserted after TA expired	t_{203}		9, 10, 11	01		35	ns
AQI asserted to AQO asserted	t_{204}		9, 10, 11	01		24	ns
ARI negated to AQO asserted	t_{205}		9, 10, 11	01		30+TA	ns
IBA_$\overline{S}$ asserted to AQO asserted	t_{207}		9, 10, 11	01		35	ns
AC10 asserted to APO negated	t_{300}		9, 10, 11	01		29	ns
AS_$\overline{Cancel}$ negated to APO negated	t_{301}		9, 10, 11	01		27	ns
APO negated to AB_RE negated	t_{310}		9, 10, 11	01		10	ns
AQO asserted to AC10 asserted	t_{320}		9, 10, 11	01		13	ns
AC1I asserted to APO negated	t_{321}		9, 10, 11	01	5	21	ns
AS_$\overline{Cancel}$ asserted to APO negated	t_{322}		9, 10, 11	01	5	21	ns
AC1I asserted to APO negated	t_{330}		9, 10, 11	01		24	ns

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = 5 V ±10% 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{MGRQ}$ or $\overline{BRQ}$ negated to AC00, AC10 asserted	t_{340}	V_{CC} = 4.5 V See figure 4	9, 10, 11	01		40	ns
AQO asserted to AC00 negated	t_{341}		9, 10, 11	01		4	ns
AQO asserted to ERIT asserted	t_{342}		9, 10, 11	01		23	ns
API negated to CMPT negated	t_{400}		9, 10, 11	01		34	ns
AC1I asserted to ARO asserted	t_{401}		9, 10, 11	01		26	ns
AS_$\overline{Cancel}$ asserted to AC10 asserted	t_{403}		9, 10, 11	01	7	24	ns
ARI asserted to ARO asserted	t_{405}		9, 10, 11	01		25	ns
$\overline{ENDT}$ asserted to ARO asserted	t_{407}		9, 10, 11	01		32	ns
ARO asserted to BGRNT asserted	t_{500}		9, 10, 11	01		12	ns
$\overline{BGRNT}$, $\overline{MGTX}$, $\overline{UNLK}$ or any interrupt asserted to AQO negated	t_{501}		9, 10, 11	01	3		ns
ARO asserted to FSTR negated	t_{502}		9, 10, 11	01		10	ns
ARO asserted to IBA_CMPT negated	t_{503}		9, 10, 11	01		10	ns
ARO asserted to $\overline{MGTX}$, $\overline{UNLK}$ or any interrupt asserted	t_{504}		9, 10, 11	01		10	ns

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{CC} = 5\ V \pm 10\%$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RST}$ Pulse width	t_{601}	V_{CC} = 4.5 V See figure 4	9, 10, 11	01	50		ns
Output reset time	t_{602}		9, 10, 11	01		54	ns
$\overline{RST}$ negated to ARO asserted	t_{603}		9, 10, 11	01		25	ns
$\overline{RINT}$ pulse width	t_{604}		9, 10, 11	01	50		ns
Output initialization reset time	t_{605}		9, 10, 11	01		45	ns
$\overline{CS}$ pulse width	t_{701}		9, 10, 11	01	35		ns
$\overline{CS}$ recovery time	t_{702}		9, 10, 11	01	15		ns
$\overline{CS}$ asserted to $\overline{DSACK}$ asserted	t_{703}		9, 10, 11	01		23	ns
ADD (3:0) setup time	t_{704}		9, 10, 11	01	5		ns
ADD (3:0) hold time	t_{705}		9, 10, 11	01	9		ns
$\overline{CS}$ negated to $\overline{DSACK}$ negated	t_{706}		9, 10, 11	01	5		ns
R_$\overline{W}$ set up	t_{707}		9, 10, 11	01	0		ns
Data (7:0) setup time with respect to $\overline{DSACK}$	t_{710}		9, 10, 11	01	28		ns
Data (7:0) hold time with respect to $\overline{DSACK}$	t_{711}		9, 10, 11	01	0		ns

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = 5 V ±10% 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SEL hold time	t_{712}	V_{CC} = 4.5 V See figure 4	9, 10, 11	01	5		ns
Data (7:0) setup time with respect to CS negated	t_{724}		9, 10, 11	01	15		ns
Data (7:0) hold time with respect to CS negated	t_{725}		9, 10, 11	01	5		ns
Data (7:0) access time with respect to CS asserted	t_{729}		9, 10, 11	01		33	ns
AB_$\overline{RE}$ negated to CN (7:0) TRI-STATE	t_{612}		9, 10, 11	01	0		ns
$\overline{CS}$ asserted to interrupt negated	t_{621}		9, 10, 11	01		43	ns
$\overline{ALL1}$ asserted with respect to WIN_GT	t_{641}		9, 10, 11	01		5	ns
$\overline{PER}$ asserted with respect to WIN_GT	t_{642}		9, 10, 11	01		5	ns
$\overline{MGRQ}$ negated to MGTX negated	t_{651}		9, 10, 11	01		23	ns
$\overline{ENDT}$ asserted to BGRNT negated	t_{662}		9, 10, 11	01		25	ns
$\overline{LKD}$ negated to $\overline{UNLK}$ negated	t_{671}		9, 10, 11	01		25	ns

1/ All testing to be performed, shall be at worst-case tests conditions, unless otherwise specified.

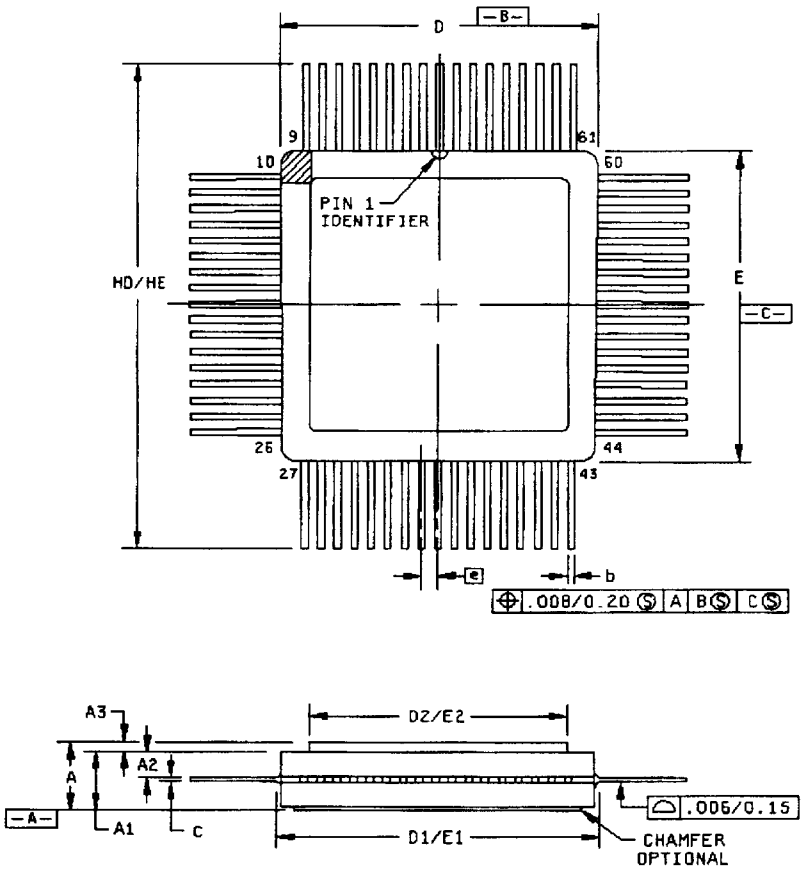


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95543
		REVISION LEVEL	SHEET 11

Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	3.30	4.06	.130	.160
A1		3.05		.120
A2		1.17		.046
A3	0.64		.025	
b	0.46	0.56	.018	.022
D/E	21.90	22.40	.862	.882
e	1.32	1.22	.048	.052
D1/E1	22.86 BSC		.900 BSC	
D2/E2	18.29	18.65	.720	.734
HD/HE	37.97	38.23	1.495	1.505

NOTES:
1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurements. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Lead number 1 is identified by a tab located on the lead.
3. Lead numbers are shown for reference only and do not appear on package.

FIGURE 1. Case outline.- continued

Device types	01		
Case outlines	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CN2	35	DATA4
2	CN1	36	V_{DD3}
3	CN0	37	DATA5
4	$\overline{CN_P}$	38	DATA6
5	$\overline{WIN}\_\overline{GT}$	39	$\overline{DATA7}$
6	$\overline{ALL}1$	40	$\overline{DSACK}$
7	PER	41	R_W
8	AC11	42	CS
9	AC10	43	SEL
10	AC01	44	ADD0
11	AC00	45	ADD1
12	API	46	ADD2
13	APO	47	$\overline{ADD3}$
14	AQI	48	$\overline{RST}$
15	AQO	49	RINT
16	ARI	50	$\overline{GND1}$
17	ARO	51	$\overline{PFINT}$
18	V_{DD1}	52	$\overline{UNLK}$
19	$\overline{HALT}$	53	$\overline{LKD}$
20	CLK	54	ENDT_
21	GND4	55	$\overline{IBA\_S}$
22	C1	56	IBA_CMPT
23	V_{DD4}	57	$\overline{AS\_CANCEL}$
24	$\overline{MGINT}$	58	$\overline{FSTR}$
25	$\overline{ERINT}$	59	$\overline{AB\_RE}$
26	$\overline{MGTX}$	60	$\overline{CN\_LE}$
27	$\overline{MGRQ}$	61	CMPT
28	$\overline{BGRNT}$	62	CN7
29	BRQ	63	CN6
30	DATA0	64	CN5
31	DATA1	65	GND2
32	DATA2	66	CN4
33	DATA3	67	V_{DD2}
34	GND3	68	CN3

FIGURE 2. Terminal connections

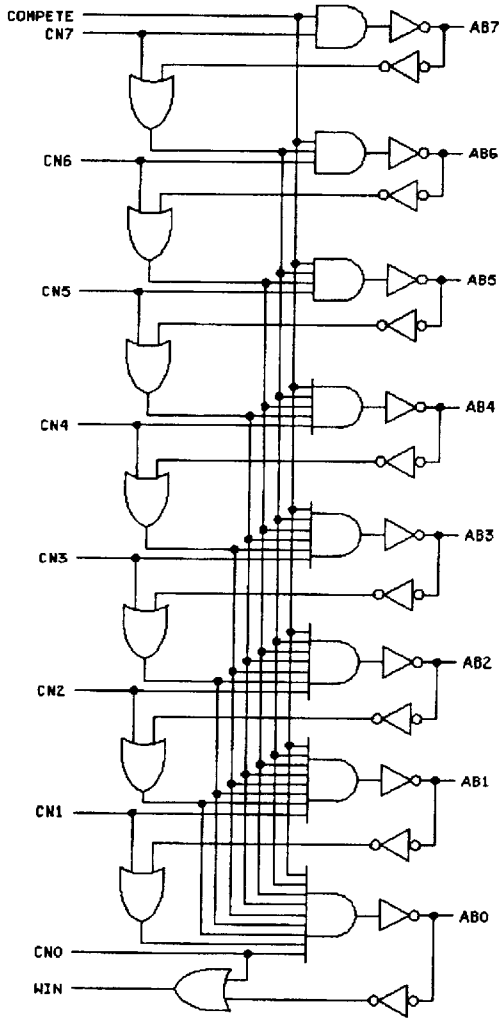
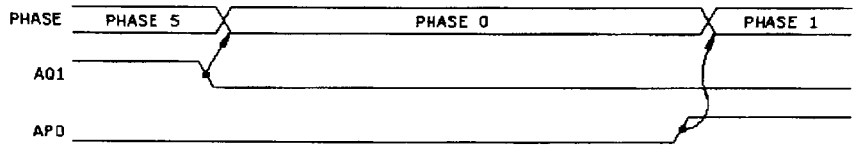
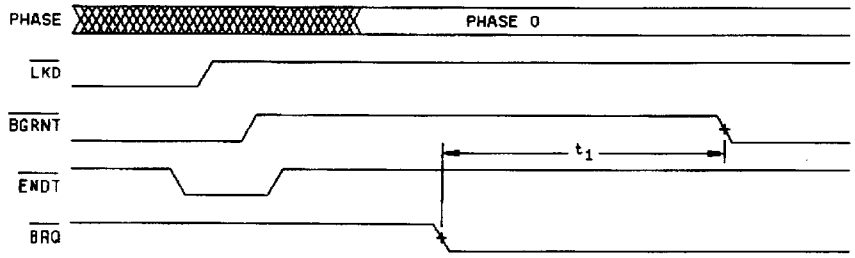


FIGURE 3. Logic diagram.

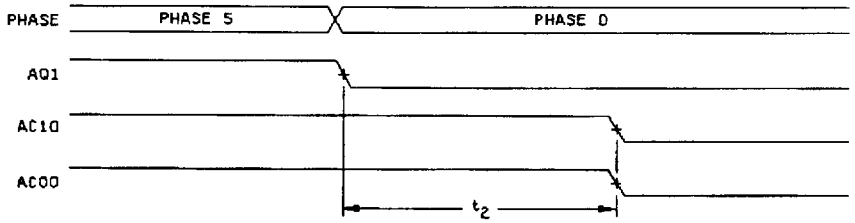
A. TRANSITIONING INTO AND OUT OF PHASE 0



B. PARKING (ASSUME IBA_PK)



C. NEGATING AC10 AND AC00 WHEN ENTERING PHASE 0



D. ANOTHER MODULE INITIATING COMPETITION

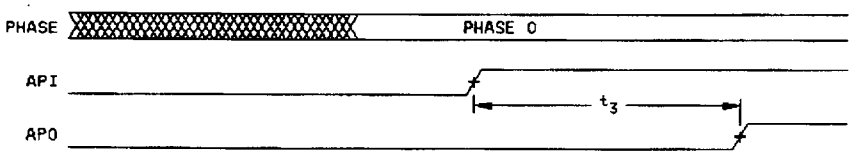
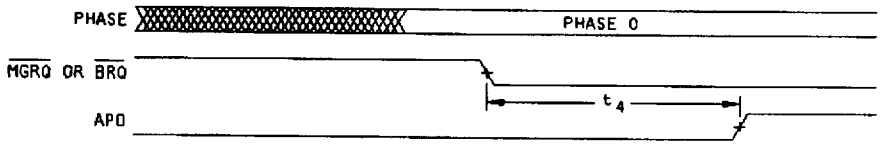
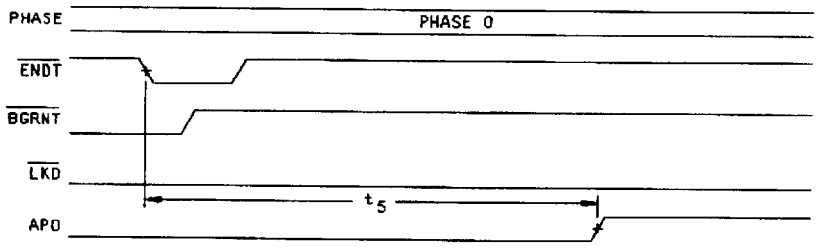


FIGURE 4. Waveforms.

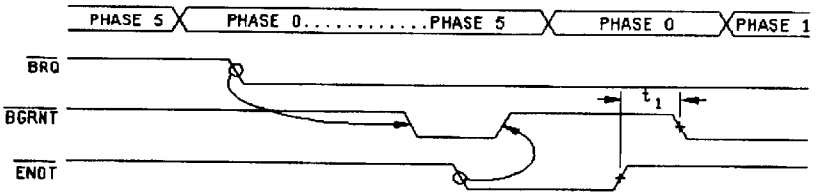
E. MESSAGE REQUEST OR BUS REQUEST INITIATING COMPETITION



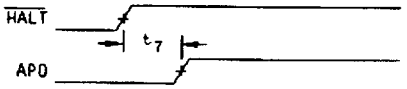
F. DUMMY CYCLE TO GENERATE UNLOCK (I UNLK) DURING PHASE 5



G. CONSECUTIVE BUS REQUESTS: PARKING



H. HALT RELEASE



I. CONSECUTIVE BUS REQUESTS: NON-PARKING

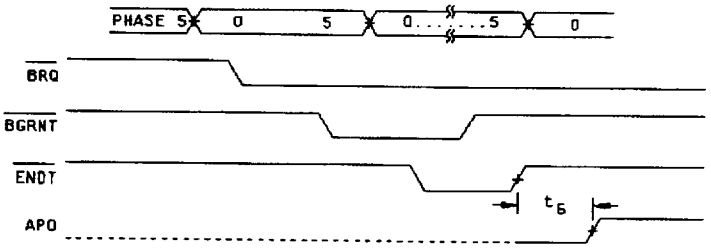


FIGURE 4. Waveforms. - continued

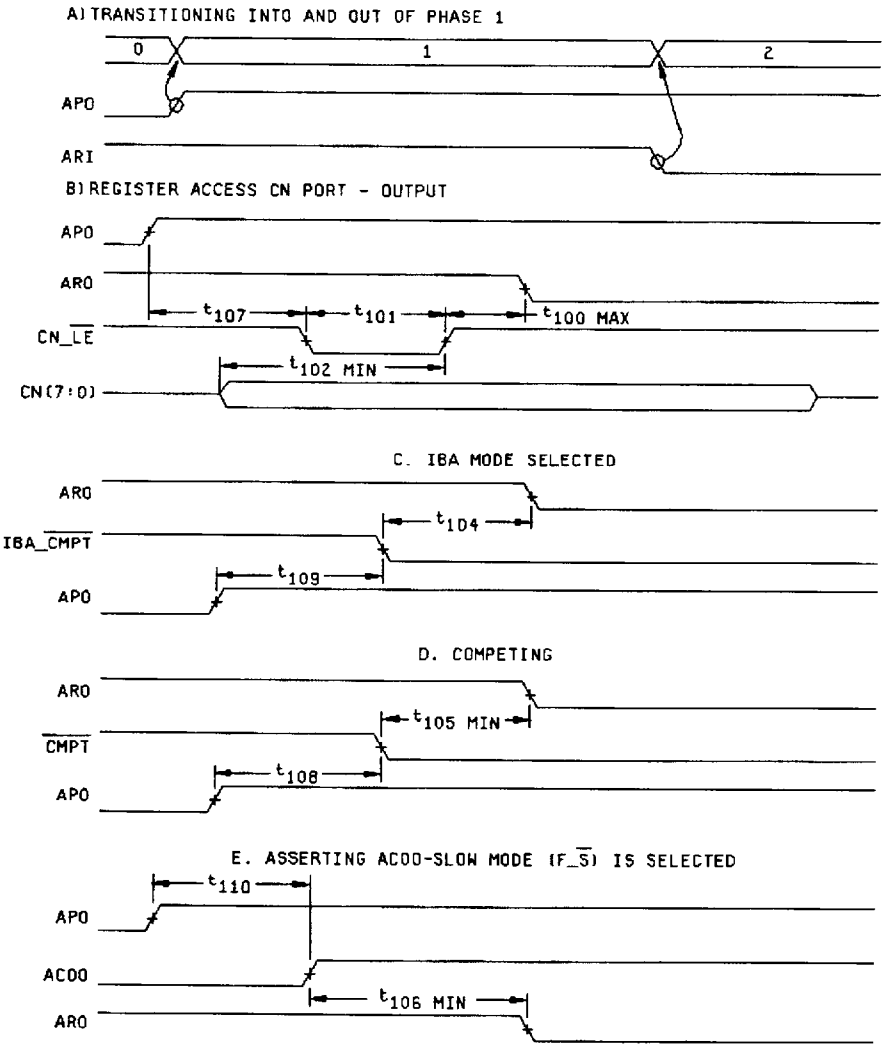
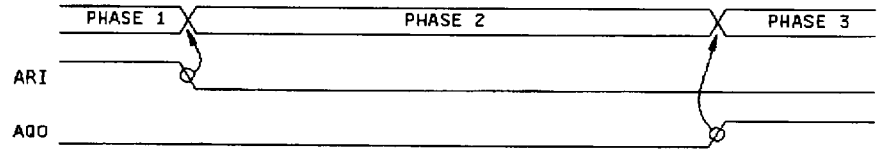
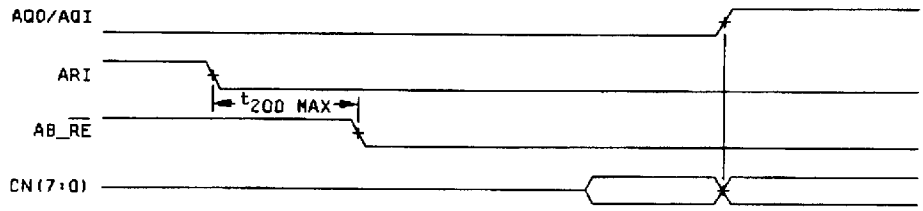


FIGURE 4. Waveforms. - continued

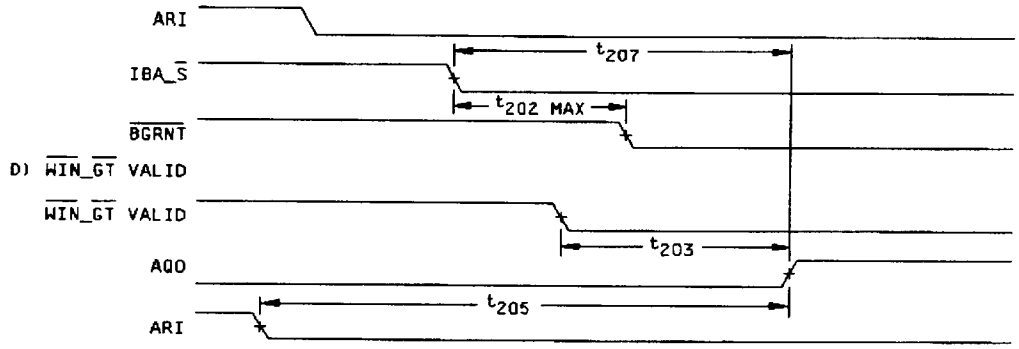
A. TRANSITIONING INTO AND OUT OF PHASE 2



B. REGISTER ACCESS ON PORT-INPUT



C. IBA MODE SELECTED-WINNER OF COMPETITION



E. BYSTANDER

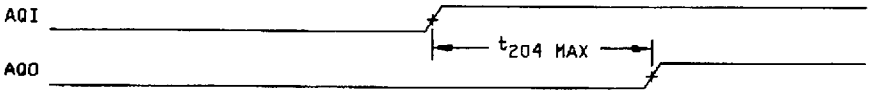


FIGURE 4. Waveforms. - continued

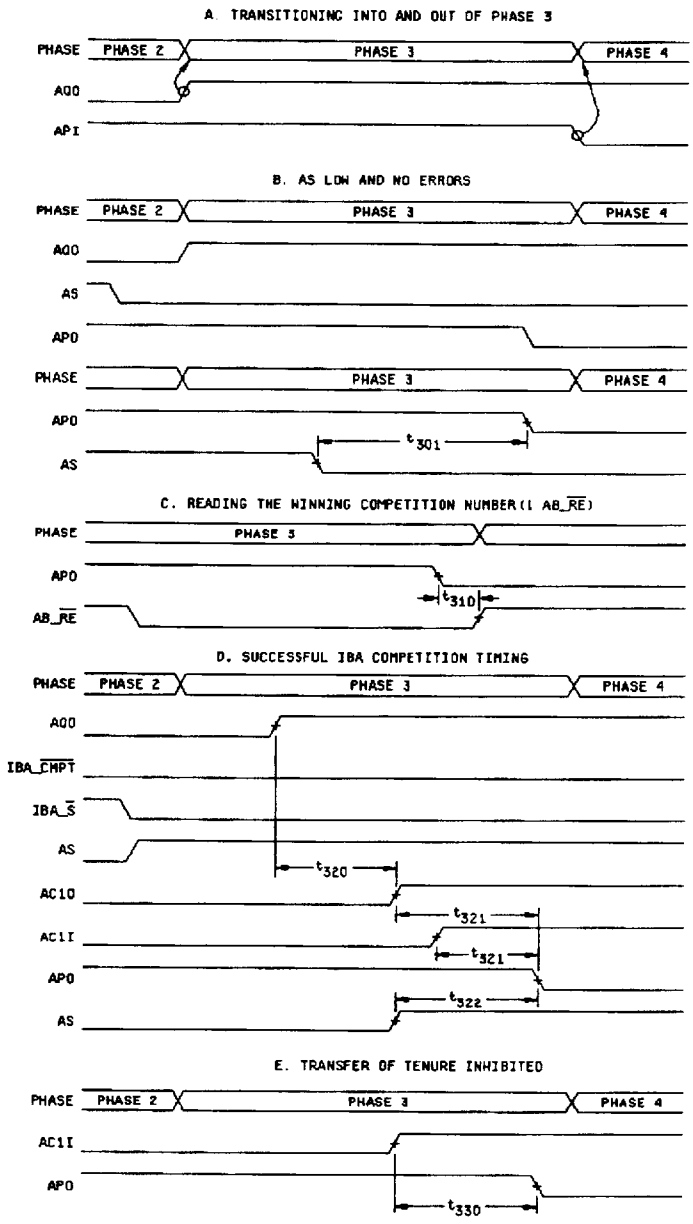


FIGURE 4. Waveforms. - continued

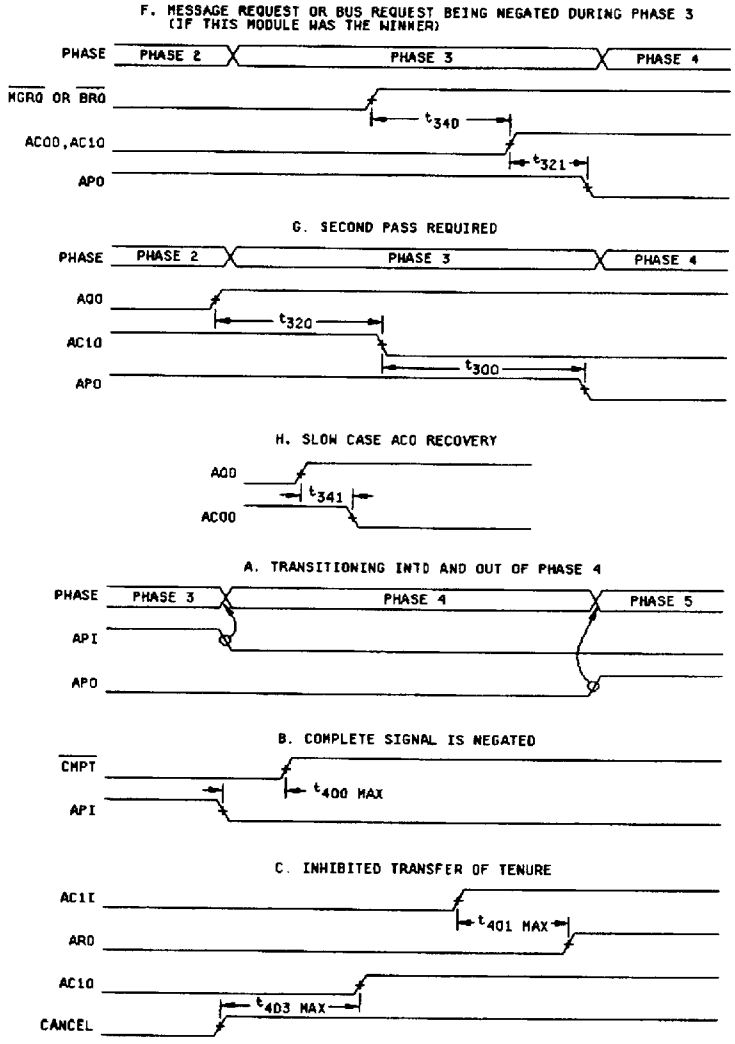


FIGURE 4. Waveforms. - continued

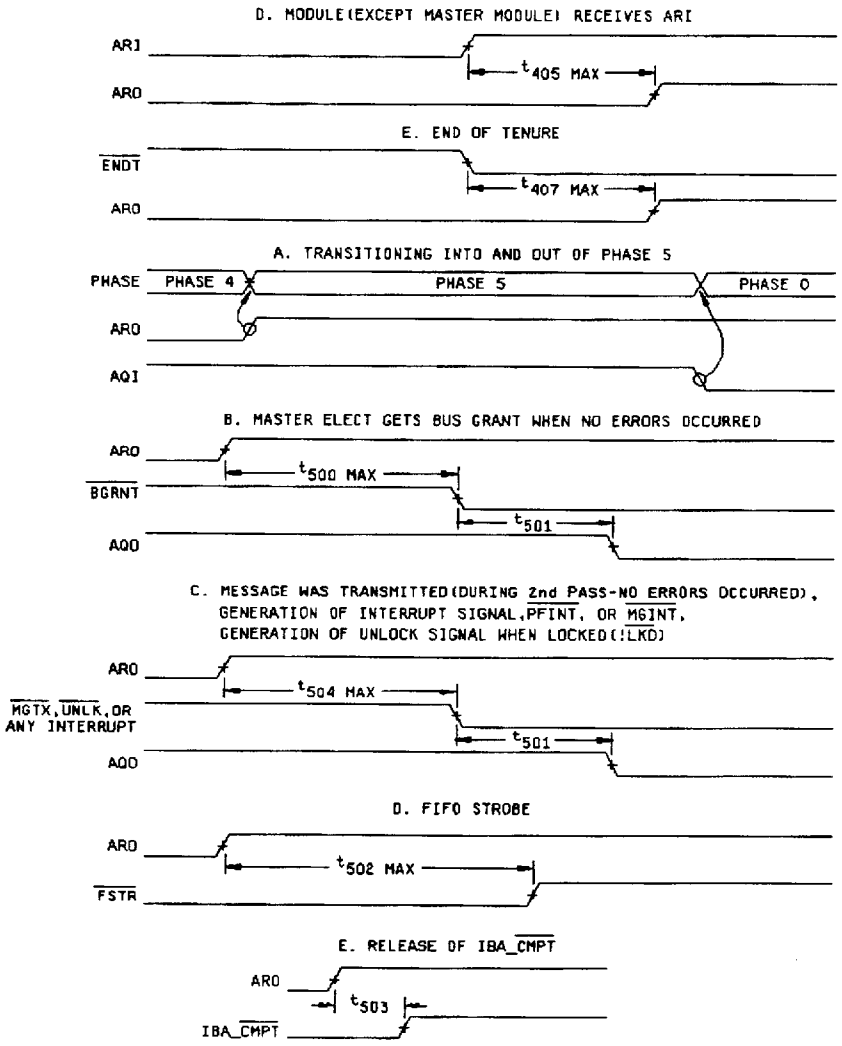


FIGURE 4. Waveforms. - continued

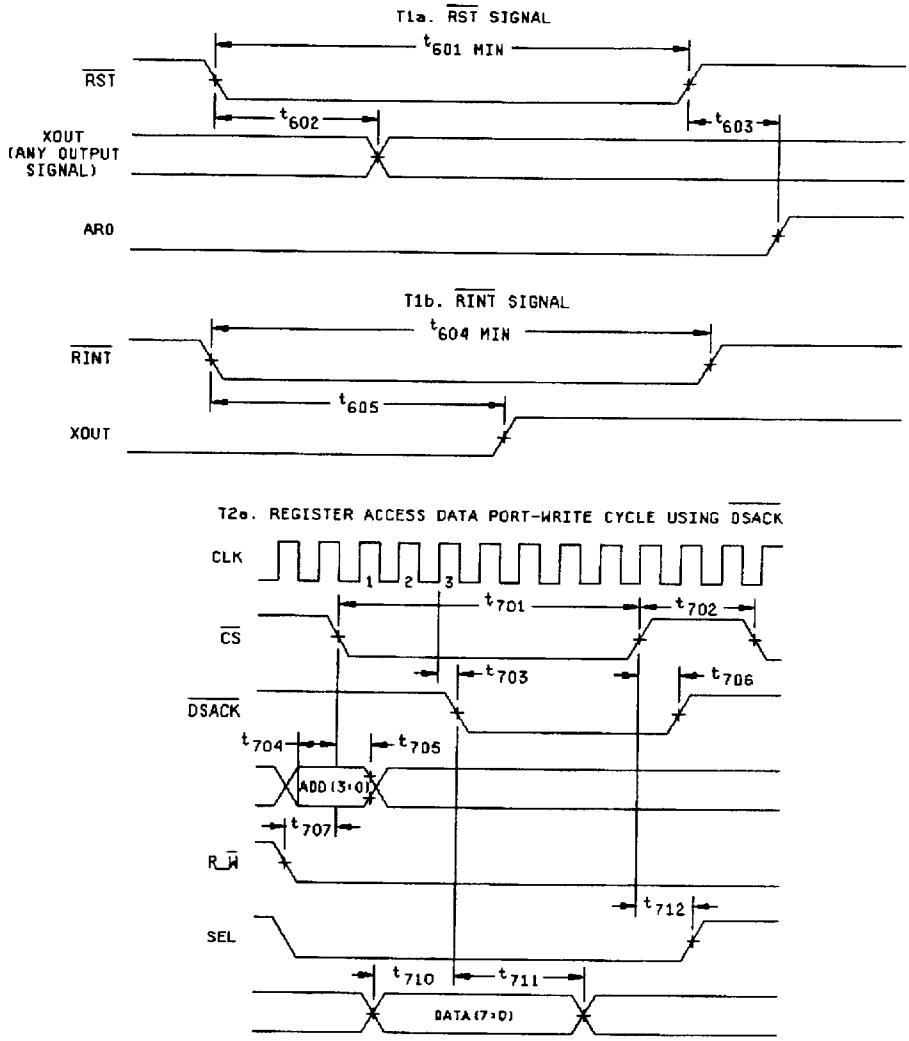
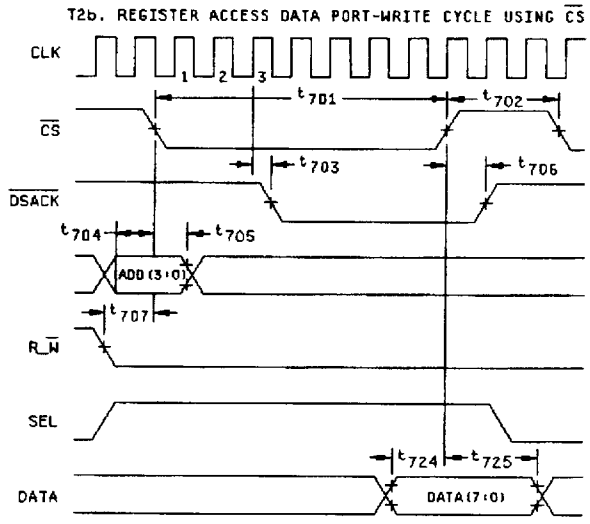


FIGURE 4. Waveforms. - continued

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95543
		REVISION LEVEL	SHEET 22



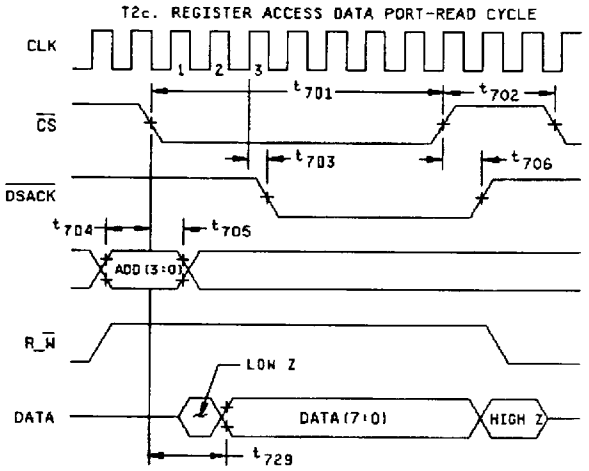
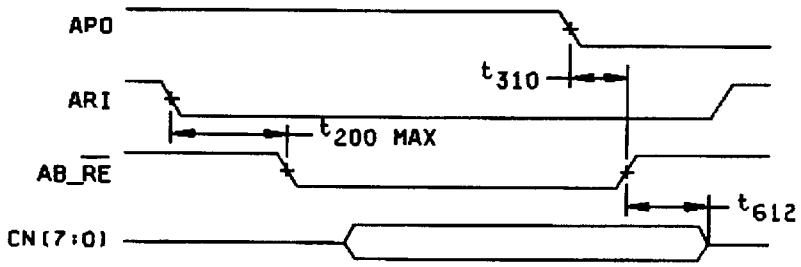
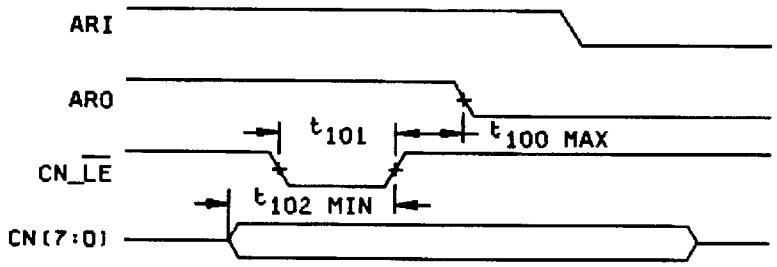


FIGURE 4. Waveforms. - continued

T3. REGISTER ACCESS CN PORT-INPUT



T4. REGISTER ACCESS CN PORT-OUTPUT



T5. CLEARING INTERRUPTS

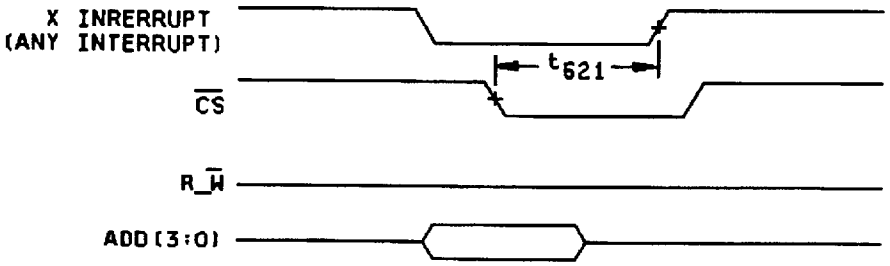
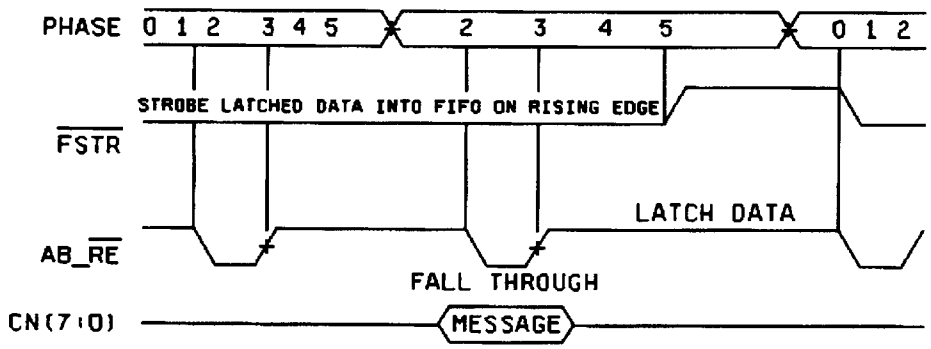
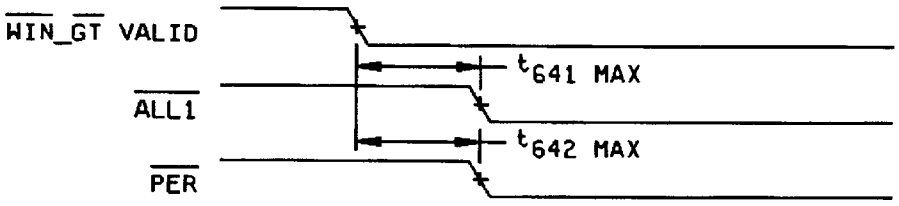


FIGURE 4. Waveforms. - continued

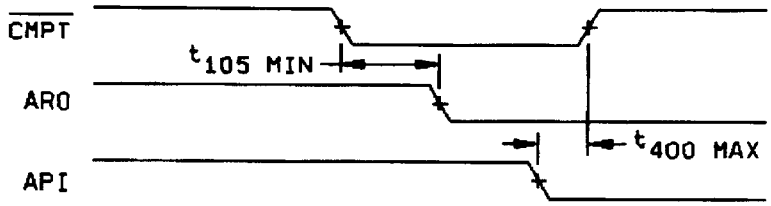
T6. FIFO STROBE



T7. $\overline{\text{WIN\_GT}}$ VALID



T8. COMPLETE SIGNAL



T9. MESSAGE SIGNALS

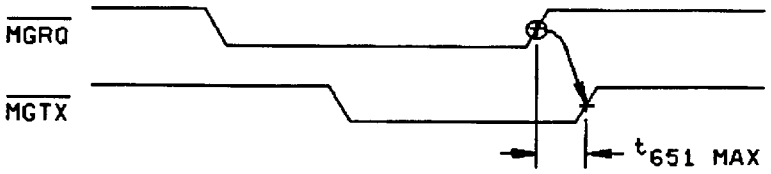
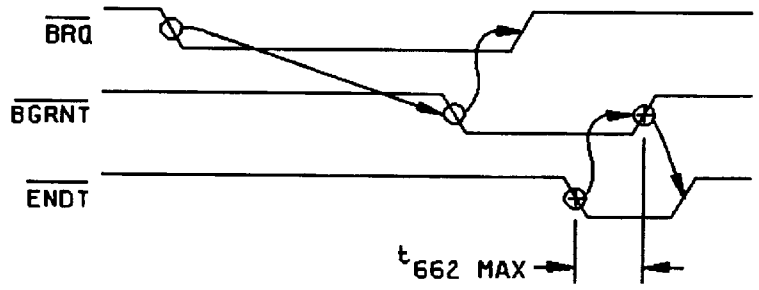


FIGURE 4. Waveforms. - continued

T10. BUSREQUEST,BUSGRANT AND END OF TENURE HANDSHAKE



T11. LKD AND UNLK HANDSHAKE SIGNALS

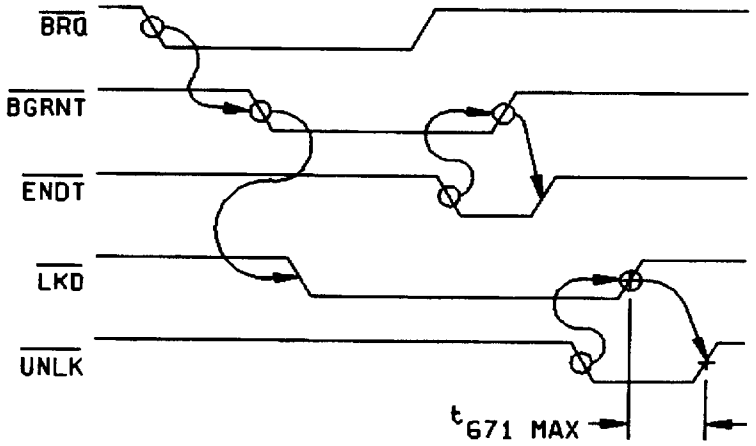


FIGURE 4. Waveforms. - continued

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 1/ 10, 11	1, 2, 3, 7, 8, 1/ 9, 10, 11	1,2,3,7,8 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1,2,3,7,8,9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5765, or telephone (513) 296-8525.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows.

PIN DEFINITIONS.

PINS	# OF PINS	TYPE	DESCRIPTION
SIGNAL TO/FROM THE HANDSHAKE TRANSCEIVER			
APO	1	O	Arbitration handshake signal from the controller.
AQO	1	O	Arbitration handshake signal from the controller.
ARO	1	O	Arbitration handshake signal from the controller.
AC0O	1	O	Arbitration condition signal from the controller.
AC1O	1	O	Arbitration condition signal from the controller.
API	1	I	Arbitration handshake signal from Futurebus +. This signal is the filtered and inverted version of the Futurebus + backplane signal AP*.
AQI	1	I	Arbitration handshake signal from Futurebus +. This signal is the filtered and inverted version of the Futurebus + backplane signal AQ*.
ARI	1	I	Arbitration handshake signal from Futurebus +. This signal is the filtered and inverted version of the Futurebus + backplane signal AR*.
AC0I	1	I	Arbitration condition signal from Futurebus +.
AC1I	1	I	Arbitration condition signal from Futurebus +.

PIN	# OF PINS	TYPE	DESCRIPTION
SIGNAL TO/FROM THE ARBITRATION TRANSCEIVER (Note: These pins are mapped to/from the Futurebus+ Arbitration Transceiver).			
CN(7:0)	8	I/O	The bus to carry competition number to/from the arbitration transceiver.
CN_p	1	O	Parity bit of the competition number.
$\overline{CMPT}$	1	O	Enables the Arbitration number onto Futurebus+.
AB_$\overline{RE}$	1	O	Direction control for the competition number bus to/from the transceiver.
CN_$\overline{LE}$	1	O	Latch enable for latching the Arbitration number from the controller into the transceiver.
$\overline{PER}$	1	I	**PARITY ERROR:** Indicates that a parity error was detected on the winner's arbitration number.
$\overline{WIN}$_$\overline{GT}$	1	I	Win signal when competing/greater than signal when not competing (used to preempt).
$\overline{ALL1}$	1	I	Indicates that all the arbitration number lines on the bus are asserted (used for messages).

PIN DEFINITIONS - continued

PIN	# OF PINS	TYPE	DESCRIPTION
SIGNALS TO/FROM THE PARALLEL PROTOCOL CONTROLLER			
$\overline{BRQ}$	1	I	**BUS REQUEST:** Indicates to the controller to acquire the bus for the module's use.
$\overline{BGRNT}$	1	O	**BUS GRANT:** Signal asserted by the controller after the detection of a bus request. The module can start using the bus.
$\overline{RINT}$	1	I	Will put the arbitration controller on phase 0 and release all the bus lines except AR*. A selective reset is performed. The rising edge will release controller from phase 0. This reset is to be used for bus initialization.
$\overline{RST}$	1	I	Reset signal from the host. An internal reset is performed. All bus signals are released. The rising edge will put the controller in phase 0 (same as power-up reset).
$\overline{HALT}$	1	I	Will halt the arbitration controller in phase 0. This signal is for use during live insertion.
$\overline{ENDT}$	1	I	**END OF TENURE:** Indicates the true end of bus tenure of the current master. This line may be asserted only after all the parallel protocol lines are released. (Generated via external logic from BRQ* released).

PIN DEFINITIONS - continued

PIN	# OF PINS	TYPE	DESCRIPTION
SIGNALS TO/FROM THE HOST (CPU Plus External Interfcae Logic)			
DATA(7:0)	8	I/O	Data bus for the host to access the register bank of the controller.
ADD(3:0)	4	I	Address bits for the register bank of the controller.
$\overline{CS}$	1	I	**CHIP SELECT:** The host can read or write to/from the controller.
R $\overline{W}$	1	I	Read/write signal from the host.
$\overline{DSACK}$	1	O	Data acknowledge pin for host read/write.
SEL	1	I	**SELECT:** Determines how the controller latches in data. A "1" on the pin uses the rising edge of CS*. A "0" on the pin uses the falling edge of DSACK*.
$\overline{MGRQ}$	1	I	**MESSAGE REQUEST:** Indicates to the controller to send an arbitration message.
$\overline{MGTX}$	1	O	**MESSAGE TRANSMIT:** Indicates the successful transmission of an arbitration message.
$\overline{ERINT}$	1	O	**ERROR INTERRUPT:** Indicates that an error occurred during the arbitration cycle.
$\overline{MGINT}$	1	O	**MESSAGE INTERRUPT:** Indicates the reception of an arbitration message.
$\overline{PFINT}$	1	O	**POWER FAIL INTERRUPT:** Indicates that a powerful message was received.

PIN DEFINITIONS - continued

PIN	# OF PINS	TYPE	DESCRIPTION
EXTERNAL LOGIC			
IBA___$\overline{\text{CMPT}}$	1	O	Signal to indicate that the Parallel Protocol controller may assert its bit on the ADDRESS/DATA bus if it is participating in an Idle Bus Arbitration.
IBA___$\overline{\text{S}}$	1	I	This signal indicates that IBA was successful. If this module was a competitor in the IBA competition (!BRQ*), then this module is the winner and now the bus master. If this module was the master, but did not compete in the IBA competition and IBA was successful, then the M bit (Status register) is negated.
AS___CANCEL	1	I	Indicates the start of the disconnection phase of the current master or cancel the current arbitration cycle.
$\overline{\text{LKD}}$	1	I	**LOCKED:** Signal to indicate that resources have been locked in the current tenure and hence generate either a dummy cycle if current master or UNLK* otherwise. (Decoded from Futurebus+ Command port output from Data Path Unit).
$\overline{\text{UNLK}}$	1	O	**UNLOCK:** Transfer of tenure indication to the parallel protocol controller for unlocking its resources. Generated only if the LKD* signal is asserted. (To external logic).
$\overline{\text{FSTR}}$	1	O	**FIFO STROBE:** Signal generated to load an external FIFO for received arbitration messages.
CLK	1	I	Clock input to the internal PLL.
C1	1	I	External capacitor input for PLL---0.1 μF.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.