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PRELIMINARY **VIC068A**

CYPRESS SEMICONDUCTOR

VMEbus Interface Controller

Features

- Complete VMEbus interface controller and arbiter
  - 58 internal registers provide configuration control and status of VMEbus and local operations
  - Drives arbitration, interrupt, address modifier utility, strobe, address lines A07through A01 and data lines D07 through D00 directly, and provides signals for control logic to drive remaining address and data lines
  - Direct connection to 68xxx family and mappable to non-68xxx processors
- Complete master/slave capability
  - Supports read, write, write posting, and block transfers
  - Accommodates VMEbus timing requirements with internal digital delay line (½-clock granularity)
  - Programmable metastability delay
  - Programmable data acquisition delays
  - Provides timeout timers for local bus and VMEbus transactions.
- Interleaved block transfers over VMEbus
  - Acts as DMA master on local bus
  - Programmable burst count, transfer length, and interleaved period interval
  - Supports local module-based DMA.
- Arbitration support
  - Supports single-level, priority and round robin arbitration
  - Supports fair request option as requester.
- Interrupt support
  - Complete support for the VMEbus interrupts: interrupter and interrupt handler
  - Seven local interrupt lines
  - 8-level interrupt priority encode
  - Total of 29 interrupts mapped through the VIC068A.
- Miscellaneous features
  - Refresh option for local DRAM
  - Four broadcast location monitors
  - Four module-specific location monitors
  - Eight interprocessor communications registers
  - PGA or QFP packages
  - Compatible with IEEE Specification 1014, Rev. C
  - Supports RMC operations

Functional Description

The VMEbus interface controller (VIC068A) is a single chip designed to minimize the cost and board area requirements and to maximize performance of the VMEbus interface of a VMEbus master/slave module. This can be implemented on either a 8-bit, 16-bit, or 32-bit VMEbus system. The VIC068A was designed using high-performancestandard cells on an advanced 1 micron CMOS process. The VIC068A performs all VMEbus system controller functions plus many others, which simplify the development of a VMEbus interface. The VIC068A utilizes patented on-chip output buffers. These CMOS high-drive buffers provide direct connection to the address and data lines. In addition to these signals, the VIC068A connects directly to the arbitration, interrupt, address modifier, utility and strobe lines. Signals are provided which control data direction and latch functions needed for a 32-bit implementation.

The VIC068A was developed through the efforts of a consortium of board vendors, under the auspices of the VMEbus International Trade Association (VITA). The VIC068A thus insures compatibility between boards designed by different manufacturers.

BUS

Pin Configurations

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Pin Grid Array (PGA)
Bottom View

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
VSS	$\overline{IPL2}$	$\overline{IACKO}$	$\overline{IRQ2}$	$\overline{IRQ5}$	$\overline{ASIZ1}$	$\overline{ASIZ0}$	$\overline{SLSEL1}$	WORD	$\overline{FIACK}$	A02	A04	VDD	VSS	$\overline{IRQ4}$	1
LD6	$\overline{BLT}$	$\overline{IPL1}$	VDD	$\overline{IRQ1}$	$\overline{IRQ4}$	$\overline{IRQ6}$	$\overline{ICFSEL}$	$\overline{MWB}$	A01	A03	A05	A07	$\overline{IRQ3}$	$\overline{IRQ7}$	2
LD2	LD5	$\overline{DEDLK}$	$\overline{IPL0}$	LAEN	$\overline{IRQ3}$	$\overline{IRQ7}$	VSS	$\overline{SLSEL0}$	VSS	A06	$\overline{IRQ1}$	$\overline{IRQ2}$	$\overline{IRQ6}$	$\overline{ACFAIL}$	3
LD1	LD3	LD7	LOCATOR PIN									$\overline{IRQ5}$	VDD	$\overline{IACKOUT}$	4
LA7	LD0	LD4										$\overline{SYSFAIL}$	$\overline{SYSRESET}$	$\overline{DTACK}$	5
LA3	LA5	LA6										$\overline{IACKIN}$	$\overline{IACK}$	AM0	6
LA2	LA4	VSS										VSS	$\overline{AS}$	AM1	7
LA1	LA0	VCC7										VSS	AM2	AM3	8
$\overline{CS}$	$\overline{DSACK1}$	$\overline{DS}$										VDD	$\overline{LWORD}$	AM4	9
$\overline{PAS}$	$\overline{LBERR}$	$\overline{RESET}$										$\overline{BERR}$	$\overline{WRITE}$	AM5	10
$\overline{DSACK0}$	R/$\overline{W}$	FC1										$\overline{BR2}$	$\overline{DS1}$	$\overline{DS0}$	11
$\overline{HALT}$	$\overline{RMC}$	$\overline{LBR}$										$\overline{BBSY}$	$\overline{BR1}$	$\overline{BR0}$	12
FC2	SIZ0	$\overline{SCON}$	CLK64M	LADI	VSS	VDD	VSS8	VCC5	D00	$\overline{BG1OUT}$	$\overline{BG2IN}$	$\overline{BG0IN}$	$\overline{BR3}$	VSS	13
SIZ1	$\overline{IRESET}$	LADO	$\overline{LEDI}$	$\overline{DDIR}$	$\overline{LWDENIN}$	$\overline{DENO}$	D06	D03	D01	VSS7	$\overline{BG0OUT}$	$\overline{BG3IN}$	$\overline{BG1IN}$	$\overline{BCLR}$	14
$\overline{LBG}$	$\overline{ABEN}$	VDD	LEDO	$\overline{UWDENIN}$	$\overline{SWDEN}$	$\overline{ISOBE}$	D07	D05	D04	D02	$\overline{BG3OUT}$	$\overline{BG2OUT}$	SYSCLK	VSS	15

Pin Configurations (continued)

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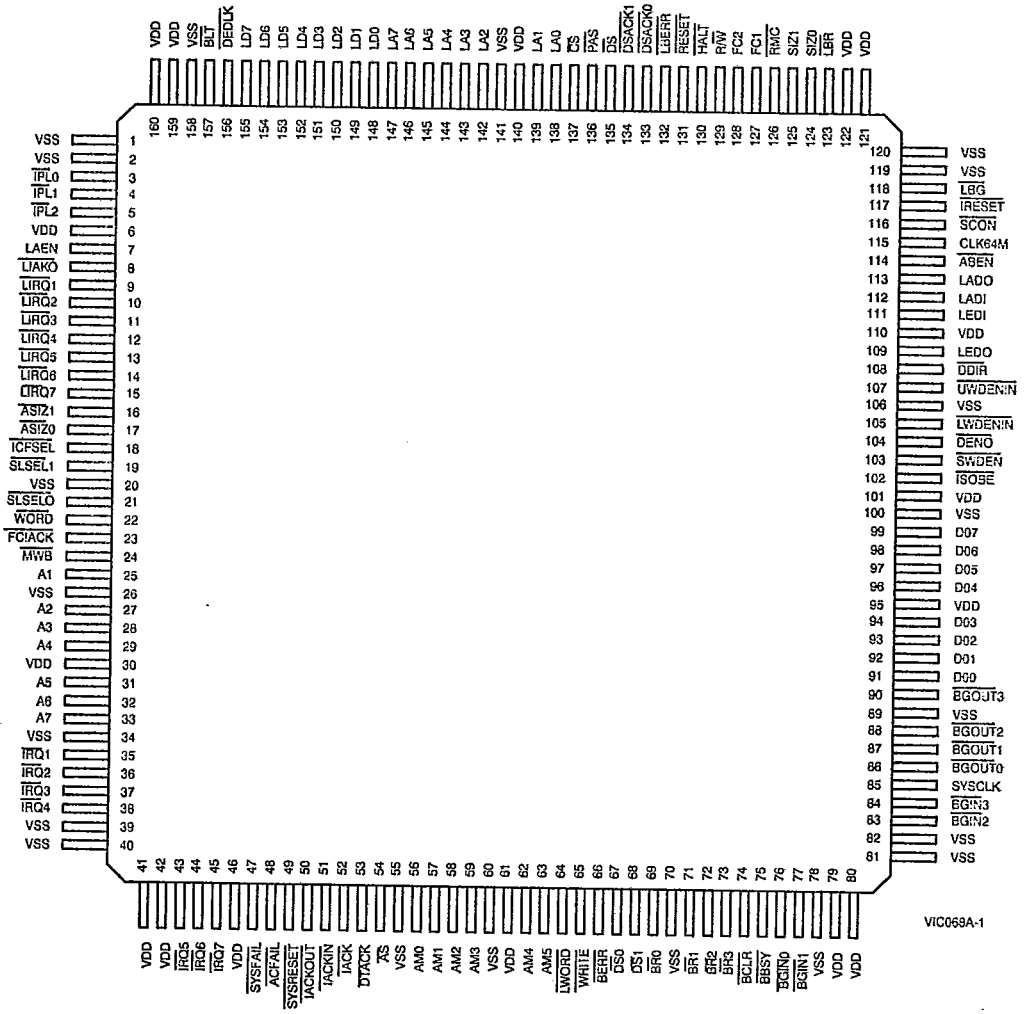
Quad Flat Pack (QFP)
Top View



VIC069A-1

BUS

VIC068A on 68030 Board

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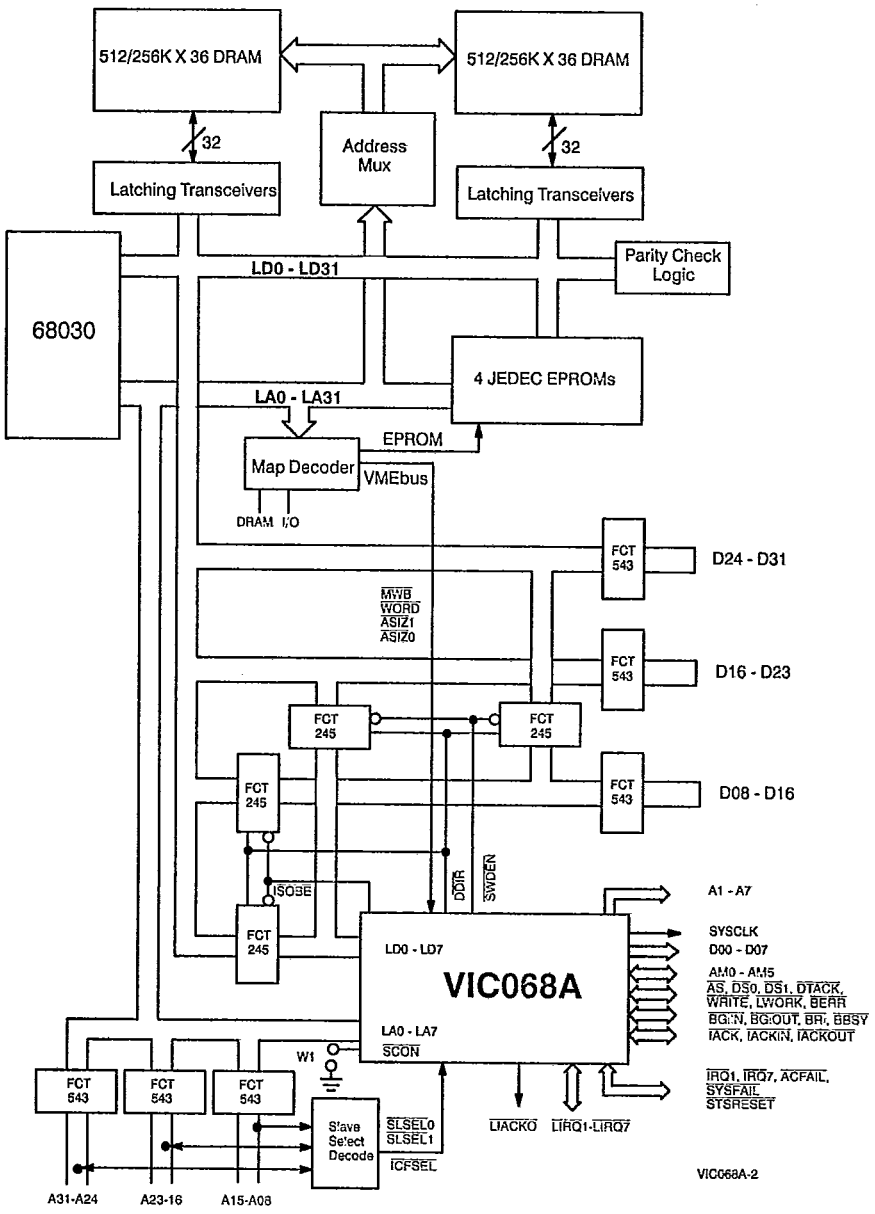

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Signal Descriptions

VMEbus Signals

The following signals are VMEbus specified signals that are driven and received directly by the VIC068A. For complete definitions and description of these signals refer to the VMEbus specification (IEEE 1014).

$\overline{\text{SYSRESET}}$

Input: Yes
Output: Yes, open collector
Drive: 64 mA

The VMEbus system reset signal. A LOW level on this signal resets the internal logic of the VIC068A and asserts the signals $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$. These signals remain asserted for a minimum of 200 ms. If the VIC068A is configured as VMEbus system controller, a LOW level on $\overline{\text{IRESET}}$ asserts $\overline{\text{SYSRESET}}$ for a minimum of 200 ms.

$\overline{\text{ACFAIL}}$

Input: Yes
Output: No
Drive: None

The VMEbus AC fail signal. This signal should be driven by the VMEbus power monitor (if installed). The VIC068A can be enabled to provide a local interrupt on the assertion of this signal.

$\overline{\text{SYSFAIL}}$

Input: Yes
Output: Yes, open collector
Drive: 64 mA

As an output the $\overline{\text{SYSFAIL}}$ signal is asserted when $\overline{\text{HALT}}$ has been detected asserted for more than 4,ms (by a source other then the VIC068A).

This signal is asserted by the VIC068A after a global reset. It may be masked by clearing ICR6[6] or by setting ICR7[7]. The VIC068A can also be enabled to provide a local interrupt on the assertion of this signal.

SYSCLK

Input: No
Output: Yes, 3-state
Drive: 64 mA

The VMEbus system clock signal. This signal is driven by the VIC068A when configured as system controller ($\overline{\text{SCON}}$ asserted). The frequency driven is 1/4th the frequency delivered to the VIC068A CLK64M signal. To deliver the required 16 MHz on this signal, the VIC068A must run at 64 MHz. The VIC068A does not use this signal internally for any purpose.

$\overline{\text{BR3}}$ – $\overline{\text{BR0}}$

Input: Yes
Output: Yes, open collector
Drive: 64 mA

The VMEbus Bus Request signals.

$\overline{\text{BG3IN}}$ – $\overline{\text{BG0IN}}$

Input: Yes
Output: No
Drive: None

The VMEbus daisy-chained Bus-Grant-In signals.

$\overline{\text{BG3OUT}}$ – $\overline{\text{BG0OUT}}$

Input: No
Output: Yes
Drive: 8 mA

The VMEbus daisy-chained Bus-Grant-Out signals.

$\overline{\text{BBSY}}$

Input: Yes
Output: Yes, rescinding
Drive: 64 mA

The VMEbus Bus-Busy signal.

$\overline{\text{BCLR}}$

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus Bus-Clear signal.

D7 – D0

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus low-order data lines.

A7 – A1

Input: Yes
Output: Yes, 3-state
Drive 64 mA

The VMEbus low-order address lines.

$\overline{\text{AS}}$

Input: Yes
Output Yes, rescinding
Drive: 64 mA

The VMEbus Address Strobe signal.

$\overline{\text{DS1}}$ – $\overline{\text{DS0}}$

Input: Yes
Output: Yes, rescinding
Drive: 64 mA

The VMEbus Data Strobe signals.

$\overline{\text{DTACK}}$

Input: Yes
Output: Yes, rescinding
Drive: 64 mA

The VMEbus Data-Transfer-Acknowledge signal.

BUS

$\overline{\text{BERR}}$

Input: Yes
Output: Yes, rescinding
Drive: 64 mA

The VMEbus Bus-Error signal.

$\overline{\text{WRITE}}$

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus Data-Direction signal.

$\overline{\text{LWORD}}$

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus Long-word signal.

AM5 – AM0

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus Address-Modifier signals.

$\overline{\text{IACK}}$

Input: Yes
Output: Yes, 3-state
Drive: 64 mA

The VMEbus Interrupt Acknowledge signal.

$\overline{\text{IACKIN}}$

Input: Yes
Output: No
Drive: None

The VMEbus daisy-chained Interrupt-Acknowledge-In signal.

$\overline{\text{IACKOUT}}$

Input: No
Output: Yes
Drive: 8 mA

The VMEbus daisy-chained Interrupt-Acknowledge-Out signal.

$\overline{\text{IRQ7}}$ – $\overline{\text{IRQ0}}$

Input: Yes
Output: Yes, open collector
Drive: 64 mA

The VMEbus Interrupt request signals.

Local Signals

These signals define the local bus structure of the VIC068A. They are modeled after Motorola 68K signals.

LD7 – LD0

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Input: Yes
Output: Yes, 3-state
Drive: 8 mA

The Local Data 7–0 signals. These signals are typically connected to the local processor data lines D(7:0) through an isolation buffer. VIC068A register accesses are also made through these data signals.

LA7 – LA0

Input: Yes
Output: Yes, 3-state
Drive: 8 mA

The Local Address 7–0 signals. These signals are typically connected to the local processor address lines. VIC068A registers are also addressed through these signals. When acting as the local bus master, the VIC068A drives these lines with the $\overline{\text{LAEN}}$ signal to supply the local address.

$\overline{\text{CS}}$

Input: Yes
Output: No
Drive: None

The VIC068A chip select signal. This signal should be asserted whenever access to the VIC068A internal registers is required.

$\overline{\text{PAS}}$

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The physical/processor address strobe. This signal is used to qualify an incoming address when performing VMEbus master operations or register operations. This signal is driven when becoming the local bus master and performing slave transfers, DRAM refresh, slave block transfers and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is configured by the Local Bus Timing Register.

$\overline{\text{DS}}$

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local data strobe. This signal is used to qualify incoming data when performing VMEbus master operations or register operations. This signal is driven when becoming the local bus master and performing slave transfers, DRAM refresh, slave block transfers, and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is directed by the Local Bus Timing Register.

$\overline{\text{DSACK1}}$, $\overline{\text{DSACK0}}$

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local data-size-acknowledge signals. One or both of these signals should be asserted to the VIC068A whenever the VIC068A is local bus master to acknowledge the successful completion of each cycle of a slave transfer, slave block transfer, or block transfers with local DMA. The VIC068A asserts one or both of these signals to

acknowledge the successful completion of a VMEbus master operation (after receiving the VMEbus $\overline{DTACK}$ signal). The following should be noted about the DSACK1/0 signals:

- The VIC068A only asserts a 16 bit $\overline{DSACKi}$ code when the $\overline{WORD}$ signal is asserted indicating access to a D16 VMEbus resource is complete.
- The VIC068A treats the assertion of any $\overline{DSACK1/0}$ signal as a 32-bit acknowledge for slave accesses.
- The VIC068A does not directly support 16 or 8-bit local port sizes.
- The VIC068A always asserts both DSACKs for register accesses. as well as for interrupt acknowledge cycles.

$\overline{LBERR}$

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local bus-error signal. This signal should be asserted to the VIC068A whenever the VIC068A is local bus master to acknowledge the unsuccessful completion of a cycle of a slave transfer, slave block transfer, and block transfers with local DMA in which case the VIC068A asserts the VMEbus $\overline{BERR}$ signal. The VIC068A asserts this signal to acknowledge the unsuccessful completion of a VMEbus master operation (after receiving the VMEbus $\overline{BERR}$ signal).

$\overline{RESET}$

Input: No
Output: Yes, Open-collector
Drive: 8 mA

The local reset indication signal. This signal is asserted whenever the VIC068A is in a reset condition. an internal, global, or system reset causes the VIC068A to assert $\overline{RESET}$ for a minimum of 200 ms. If the reset condition continues for longer then 200 ms, $\overline{RESET}$ begins additional 200 ms timeouts until all reset conditions are cleared.

$\overline{HALT}$

Input: Yes
Output: Yes, Open collector
Drive: 8 mA

The "halted" condition indication signal. This signal, along with $\overline{RESET}$, is asserted during reset conditions. An internal, global, and system reset causes the VIC068A to assert $\overline{HALT}$ for a minimum of 200 ms. If the reset condition continues for longer then 200 ms, $\overline{HALT}$ begins an additional 200 ms timeouts until all reset conditions are cleared. Assertion of $\overline{HALT}$ for greater than 4 ms by anything other then the VIC068A causes the VIC068A to assert $\overline{SYSFAIL}$.

$\overline{HALT}$ may be configured to assert during dead-lock conditions along with $\overline{LBERR}$ to initiate a retry sequence for Motorola 68K processors.

R/$\overline{W}$

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local data direction signal. This signal is driven while VIC068A is a local bus master to indicate local data direction. As an input, R/$\overline{W}$ indicates data direction for VMEbus master cycles. In this case, $\overline{WRITE}$ reflects the value of R/$\overline{W}$. An asserted condition indicates a write operation.

FC2, FC1

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Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local function code signals. These signals identify the type of local cycle in progress. As inputs, they should reflect the type of operations in terms of User/Supervisory Code/Data. They may be connected directly to the Motorola FC2/1 outputs for 68000-30 processors. For the 68040, the FC2/1 inputs may be connected to the TM2/1 outputs respectively. Additional qualification may be required for 68040 applications since the 68040 uses previously reserved/unused function codes.

FC2	FC1	Description
0	0	User Data
0	1	User Program
1	0	Supervisory Data
1	1	Supervisory Program

As outputs, the VIC068A drives these signals whenever local bus master to indicate the type of local cycle the VIC068A is performing.

FC2	FC1	Description
0	0	Slave Block Transfer
0	1	Local DMA
1	0	Slave Access
1	1	DRAM Refresh

SIZ1, SIZ0

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

The local data size signals. As inputs, these signals should identify the width of the VMEbus data to be transferred. The SIZi signals should not be used to indicate the physical port size of the slave device (D16, or D32). This is done with the $\overline{WORD}$ signal. As outputs, they are driven by the VIC068A as local bus master to identify the width of the incoming data.

SIZ1	SIZ0	Data Width
0	0	Long Word
0	1	Byte
1	0	Word
1	1	3-Byte

$\overline{LBR}$

Input: No
Output: Yes
Drive: 8 mA

The local bus request signal. This signal is asserted whenever the VIC068A desires mastership of the local bus. This signal remains asserted for the entire bus tenure.

Local bus mastership is requested when each of the following operations is desired:

- Standard slave accesses

- Slave block transactions
- Block transfers with local DMA
- DRAM refresh

$\overline{LBG}$

Input: Yes
Output: No
Drive: None

The local bus grant signal. The signal should be asserted in response the assertion of the $\overline{LBR}$ signal. The VIC068A does not incorporate a local bus grant acknowledge protocol so, the $\overline{LBG}$ signal should remain asserted for the duration of $\overline{LBR}$.

$\overline{MWB}$

Input: Yes
Output: No
Drive: None

The "Module-Wants-Bus" signal. This signal should be asserted by local resources to begin a VMEbus transaction. When qualified by the $\overline{PAS}$ signal, the VIC068A asserts the VMEbus $\overline{BRI}$ signal. This signal is usually asserted by local-to-VMEbus address decoders.

$\overline{FCIACK}$

Input: Yes
Output: No
Drive: None

The local interrupt acknowledge signal. This signal should be asserted (qualified by $\overline{PAS}$) to acknowledge all VIC068A-generated local interrupts.

$\overline{SLSEL1}$, $\overline{SLSEL0}$

Input: Yes
Output: No
Drive: None

The slave select signals. These signals indicate the VIC068A has been selected to perform a VMEbus slave operation. When qualified by $\overline{AS}$ and valid AM codes, the VIC068A requests the local bus to perform the slave cycle. These signals are usually asserted by VMEbus-to-local address decoders.

The SLSEL1/0 signals may be used independently of each other to provide unique slave characteristics as defined by the Slave Select Control registers.

$\overline{ICFSEL}$

Input: Yes
Output: No
Drive: None

The Interprocessor Communication Facility (ICF) Select signal. This signal is used to indicate that the ICF functions of the VIC068A have been selected. These include the ICF registers and the ICF switch interrupts. This signal is qualified with $\overline{AS}$ and A16 AM codes (A16/Supervisory for global switches).

$\overline{ASIZ1}$, $\overline{ASIZ0}$ T-52-33-55

Input: Yes
Output: No
Drive: None

The VMEbus address size signals. These signals should be driven to indicate the VMEbus address size of master VMEbus transfers. The address size information is issued on the VMEbus AM codes. The assertion of $\overline{ASIZ0}$ indicates an A16 transaction. The assertion of $\overline{ASIZ1}$ indicates an A32 transaction. Asserting neither indicates an A24 transaction. User-defined address spaces may be accessed by asserting both $\overline{ASIZ1/0}$ signals. In this case, the AM codes are issued according to the programming of the Address Modifier Source Register.

$\overline{ASIZ1}$	$\overline{ASIZ0}$	Address Size
0	0	User defined
0	1	A32
1	0	A16
1	1	A24

The $\overline{ASIZ1/0}$ signals are also used for cycle acknowledge signals for module-based DMA transfers. During a module-based DMA transfer, the $\overline{ASIZ0}$ signal is used as a data-transfer-acknowledge signal (analogous to $\overline{DTACK}$). The $\overline{ASIZ1}$ signal is used as a bus-error signal (analogous to $\overline{BERR}$).

$\overline{WORD}$

Input: Yes
Output: No
Drive: None

The VMEbus data-width control signal. This signal, when asserted, indicates the requested VMEbus transaction should be treated as a D16 data path. When negated, the VMEbus data path is assumed to be D32. This signal should be used to configure VMEbus data-width for master cycles only. Data-width for slave cycles is configured in the Slave Select Control Registers.

This signal is also used to configure the data-width for block transfers with local DMA. When this signal is asserted during the block transfer initiation cycle, the block transfer is assumed to be a D16 block transfer.

This signal may be changed dynamically for individual transfers, or strapped LOW at power-up for permanent D16 operation. If $\overline{WORD}$ is strapped LOW at power-up, the VIC068A is configured as a D16 slave independent of the slave configuration in the Slave Select Control Registers.

$\overline{WORD}$ should not be used to indicate data size (i.e., byte, word, or long-word) only local data port size (i.e., D16 or D32).

$\overline{BLT}$

Input: Yes
Output: Yes, open-collector
Drive: 8 mA

The Block transfer with local DMA indication signal. This signal is used to indicate that a block transfer with local DMA is in progress. This signal remains asserted for the entire block transfer including interleave periods with the exception of local page boundary crossings. $\overline{BLT}$ toggles during local boundary crossings to increment the external LA(+:8) counters.

If the $\overline{BLT}$ signal is asserted simultaneously with the $\overline{MWB}$ signal and BTCR[7] is set, a module-based DMA transfer is performed.

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$\overline{\text{DEDLK}}$

Input: No
Output: Yes
Drive: 8 mA

The dead-lock indication signal. This signal is used to indicate a dead-lockcondition has occurred. This signal should be used by local logic to remove its request for the VMEbus. $\overline{\text{DEDLK}}$ remains asserted until the slave transaction is complete.

$\overline{\text{DEDLK}}$ is also asserted to indicate that a VMEbus master cycle is being attempted during the interleave period of a block transfer with local DMA, without the dual path feature enabled. In this case, $\overline{\text{DEDLK}}$ is asserted while $\overline{\text{MWB}}$ is asserted. If, during the interleave period, the $\overline{\text{MWB}}$ signal is asserted after the VMEbus has been re-obtained, the VIC068A will assert $\overline{\text{DEDLK}}$ for the duration of the burst.

$\overline{\text{IPL2}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL0}}$

Inputs: $\overline{\text{IPL0}}$ only
Output: Yes,open-collector
Drive: 8 mA

The local priority encoded interrupt request signals. These signals are asserted to interrupt the local processor. All local VIC068A interrupts are issued with these signals. These signals are meant to emulate the Motorola 68K interrupt algorithms. The assertion of one or more of these signals indicate a single interrupt with a priority given by the negative-logic value of the $\overline{\text{IPLi}}$ signals. Level 7 is the highest priority. These signals are open-collector to allow the wire-ORingof multiple interrupt sources.

During the assertion of $\overline{\text{IRESET}}$, $\overline{\text{IPL0}}$ becomes an input. If $\overline{\text{IPL0}}$ is asserted at this time, a global reset is performed.

$\overline{\text{LIRQ7}}$ – $\overline{\text{LIRQ1}}$

Input: Yes
Output: $\overline{\text{LIRQ2}}$ only
Drive: 8mA ($\overline{\text{LIRQ2}}$ only)

The local interrupt request signals. These signals serve as local interrupt request signals for the VIC068A. If enabled to handle the particular local interrupt, the VIC068A in turn issues a processor interrupt with the $\overline{\text{IPLi}}$ signals at the assertion of a $\overline{\text{LIRQi}}$. Extensive configuration of local interrupts is allowed through the Local Interrupt Configuration Registers.

$\overline{\text{LIRQ2}}$ may also be configured to issue periodic "heartbeat" interrupts at user defined intervals.

$\overline{\text{LIACKO}}$

Input: No
Output: Yes
Drive: 8 mA

The "autovectoring" indication signal. This signal is asserted when the VIC068A is configured to allow the interrupting device to place its status/ID vector on the local data bus in response to a VIC068A-handledlocal interrupt acknowledge. This signal may be used to signal a autovectored interrupt acknowledge cycle for 68020/30/40 processors. This signal may be connected directly to the AVEC signal for these processors.

$\overline{\text{IRESET}}$

Input: Yes
Output: No
Drive: None

The internal reset signal. This signal is used to issue both internal and global resets to the VIC068A. If asserted with $\overline{\text{IPL0}}$, a global reset is performed. If asserted without $\overline{\text{IPL0}}$, an internal reset is performed. All internal state machines and selected register bits are reset during the assertion of $\overline{\text{IRESET}}$. $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ are both asserted during the assertion of $\overline{\text{IRESET}}$. If configured as system controller, $\overline{\text{SYSRESET}}$ is also asserted during the assertion of $\overline{\text{IRESET}}$.

$\overline{\text{IRESET}}$ contains internal hysteresis to allow the connection of this signal to an external RC network for power-up resets.

$\overline{\text{SCON}}$

Input: Yes
Output: No
Drive: None

The system controller enabling signal. This signal is used to configure the VIC068A as VMEbus system controller. This signal must be strapped LOW at power-up and remain LOW for VIC068A to reliably assume the role of VMEbus system controller.

CLK64M

Input: Input
Output: No
Drive: None

The VIC068A master clock input. This 64-MHz clock input is used to clock internal arbitration, timing, and delay functions within the VIC068A.

Buffer Control Signals

These signals control the latching and enabling of the external address and data latches and buffers. For block transfers with local DMA, some of these signals are used to control the counting and enablingof external counters required for page boundary crossing.

$\overline{\text{ABEN}}$

Input: No
Output: Yes
Drive: 8 mA

The VMEbus Address Bus ENable signal. This signal is used to enable the external VMEbus address drivers for VMEbus master operations. It is typically connected to the OEAB input of a '543 addresstransceivers.

LAEN

Input: No
Output: Yes
Drive: 8 mA

The Local Address ENable signal. This signal is used to enable the external local address drivers for slave accesses. It is typically connected to the OEBA input of a '543 address transceivers through an inverter.

Note that this signal is an active-HIGH signal.

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LADO

Input: No
Output: Yes
Drive: 8 mA

The Latch ADdress Out signal. This signal is used to latch the outgoing VMEbus address for VMEbus master operations. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEAB input. LADO is very important for proper operation of master write posting and block transfers with interleave periods. For these operations, VIC068A may use LADO in combination with LADI and $\overline{\text{ABEN}}$ to temporarily store the contents of a VMEbus address during intervening slave accesses.

LADI

Input: No
Output: Yes
Drive: 8 mA

The Latch ADdress In signal. This signal is used to latch the incoming VMEbus address for slave accesses. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEBA input. LADI is used in conjunction with LADO to temporarily store outgoing VMEbus master transaction addresses during intervening slave accesses.

$\overline{\text{DENO}}$

Input: No
Output: Yes
Drive: 8mA

The Data ENable Out signal. This signal enables data onto the VMEbus data bus for master write and slave read cycles. This signal is typically connected to the OEAB input of the '543 data latches.

$\overline{\text{LWDENIN}}$

Input: No
Output: Yes
Drive: 8 mA

The Lower Word Data ENable IN signal. This signal enables data onto the lower word of the local data bus LD(15:8) for master read and slave write cycles. This signal is typically connected to the OEBA input of the '543 lower data latch.

$\overline{\text{UWDENIN}}$

Input: No
Output: Yes
Drive: 8 mA

The Upper Word Data ENable IN signal. This signal enables data onto the upper word of the local data bus LD(31:16) for master read and slave write cycles. This signal is typically connected to the OEBA input of the upper '543 data latches.

LEDO

T-52-33-55

Input: No
Output: Yes
Drive: 8 mA

The Latch Enable Data Out signal. This signal latches the outgoing VMEbus data for master write and slave read cycles. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEAB input. This signal is used in conjunction with LEDI to temporarily store outgoing master write post data (data switch-back).

LEDI

Input: No
Output: Yes
Drive: 8 mA

The Latch Enable Data In signal. This signal latches the incoming VMEbus data for master read and slave write cycles. When this signal is asserted (HIGH), it is assumed that the latches are in a latched state. When negated, the latches should be in a fall-through state. This allows direct connection to the '543 address driver LEBA input. This signal is used in conjunction with LEDO to temporarily store outgoing master write post data.

$\overline{\text{ISOBE}}$

Input: No
Output: Yes
Drive: 8 mA

The ISOlation Buffer Enable signal. This signal, along with the $\overline{\text{SWDEN}}$ signal, provides byte lane switching. This signal is typically connected to the EN input of the '245 isolation buffer.

$\overline{\text{SWDEN}}$

Input: No
Output: Yes
Drive: 8 mA

The SWap Data ENable signal. This signal, along with the $\overline{\text{ISOBE}}$ signal, provides byte lane switching. It provides for swapping LD(31:16) to LD(15:0). This signal is typically connected to the EN input of the '245 swap buffer.

DDIR

Input: No
Output: Yes
Drive: 8 mA

The Data DIRection signal. This signal provides the data direction (i.e., read/write) information to the isolation and swap buffers. When asserted, buffers should be configured in the local-to-VMEbus (A-to-B) direction. This signal is typically connected to the DIR input of the '245. isolation/swap buffers.

VIC068A Register Values After Reset Operations

T-52-33-55

Address (hex)	Name	Description	Global Reset	Internal Reset	System Reset
03	VIICR	VMEbus Interrupter Interrupt Control Register	11111000	11111***	11111***
07–1F	CICR1–7	VMEbus Interrupt Control Registers 1–7	11111***	11111***	11111***
23	DMASR	DMA Status Register	11111000	11111***	11111***
37–3F	LICR1–7	Local Interrupt Control Registers 1–7	1000X000	1***X***	1***X***
43	ICGSICR	ICGS Interrupt Control Register	11111000	11111***	11111***
47	ICMSICR	ICMS Interrupt Control Register	11111000	11111***	11111***
4B	EGICR	Error Group Interrupt Control Register	11111000	11111***	11111***
4F	ICGSVBR	ECGS Vector Base Register	00001111	00001111	00001111
53	ICMSVBR	ICGS Vector Base Register	00001111	00001111	00001111
57	LIVBR	Local Interrupt VEctor Base Register	00001111	00001111	00001111
5B	EGIVBR	Error Group Interrupt Vector Base Register	00001111	00001111	00001111
5F	ICSR	Interprocessor Communications Switch Register	00000000	****0000	00000000
63–73	ICR0–4	Interprocessor Communications Registers 0–4	00000000	00000000	00000000
77	ICR5	Interprocessor Communications Register 5	Version	Version	Version
7B	ICR6	Interprocessor Communications Register 6	X11111XX	X1111111	X1111110
7F	ICR7	Interprocessor Communications Register 7	00X00000	X0XXXXXX	00X00000
83	VIRSR	VMEbus Interrupt Request Status Register	00000000	*******0	00000000
87–9F	VIVBR1–7	VMEbus Interrupt Vector Base Regtisters 1–7	00001111	********	00001111
A3	TTR	Transfer Timeout Register	01101000	01101000	01101000
A7	LBTR	Local Bus Timing Register	00000000	********	********
AB	BTDR	Block Transfer Definition Register	00000000	00000000	00000000
AF	ICR	Interface Configuration Register	00000000	00000000	00000000
B3	ARCR	Arbiter/Requester Configuration Register	01100000	011*0000	011*0000
B7	AMSR	Address Modifier Source Register	00000000	00000000	00000000
BB	BESR	Bus Error Status Register	X0000000	X0000000	X0000000
BF	DMASR	DMA Status Register	00000000	00000000	00000000
C3	SS0CR0	Slave Select 0 Control Register 0	00000000	00******	00******
C7	SS0CR1	Slave Select 0 Control Register 1	00000000	********	********
CB	SS1CR0	Slave Select 1 Control Register 0	00000000	00******	00******
CF	SS1CR1	Slave Select 1 Control Register 1	00000000	********	********
D3	RCR	Release Control Register	00000000	00000000	00000000
D7	BTCR	Block Transfer Control Register	00000000	00000000	00000000
D8	CTLR0	Block Transfer Length Register 0	00000000	00000000	00000000
DF	BTLR1	Block Transfer Length Register 1	00000000	00000000	00000000
E3	SRR	Ssytem Reset Register	11111111	11111111	11111111
EB–FF		Reserved Locations	11111111	11111111	11111111

BUS

Theory of Operation

The VIC068A is an interface between a local CPU bus and the VMEbus. The local bus interface of the VIC068A emulates Motorola's family of 32-bit CISC processor interfaces. Other processors can easily be adapted to interface to the VIC068A using the appropriate logic.

Resetting the VIC068A

The VIC068A can be reset by any of three distinct reset conditions:

Internal Reset. This reset is the most common means of reseting the VIC068A. It resets select register values and all logic within the device.

System Reset. This reset provides a means of resetting the VIC068A through the VMEbus backplane. The VIC068A may also signal a $\overline{\text{SYSRESET}}$ by writing a configuration register.

Global Reset. This provides a complete reset of the VIC068A. This reset resets all of the VIC068A's configuration registers. This reset should be used with caution since SYSCLK is not driven while a global reset is in progress.

All three reset options are implemented in a different manner and have different effects on the VIC068A configuration registers.

VIC068A VMEbus System Controller

The VIC068A is capable of operating as the VMEbus system controller. It provides VMEbus arbitration functions, including:

- Priority, round-robin, and single-level arbitration schemes
- Driving $\overline{\text{IACK}}$ Daisy-Chain
- Driving $\overline{\text{BGiOUT}}$ Daisy-Chain (All four levels)
- Driving SYSCLK output
- VMEbus arbitration timeout timer

The System controller functions are enabled by the $\overline{\text{SCON}}$ pin of the VIC068A. When strapped LOW, the VIC068A functions as the VMEbus system controller.

VIC068A VMEbus Master Cycles

The VIC068A is capable of becoming the VMEbus master in response to a request from local resources. In this situation, the local resource requests that a VMEbus transfer is desired. The VIC068A makes a request for the VMEbus. When the VMEbus is granted to the VIC068A, it then performs the transfer and acknowledges the local resource and the cycle is complete. The VIC068A is capable of all four VMEbus request levels. The following release modes are supported:

- Release on request (ROR)
- Release when done (RWD)
- Release on clear (ROC)
- Release under $\overline{\text{RMC}}$ control
- Bus capture and hold (BCAP)

The VIC068A supports A32, A24, and A16, as well as user-defined addressspaces.

Master Write-Posting

The VIC068A is capable of performing master write-posting (bus decoupling). In this situation, the VIC068A acknowledges the local resource *immediately* after the request to the VIC068A is made, thus freeing the local bus. The VIC068A latches the local data to be written and performs the VMEbus transfer without the local resource having to wait for VMEbus arbitration.

Indivisible Cycles

Read-modify-write cycles and indivisible multiple-address cycles (IMACs) are easily performed using the VIC068A. Significant control is allowed to:

- Requesting the VMEbus on the assertion of $\overline{\text{RMC}}$ independent of $\overline{\text{MWB}}$ (this prevents any slave access from interrupting local indivisable cycles)
- Stretching the VMEbus $\overline{\text{AS}}$
- Making the above behaviors dependent on the local SIZi signals

Deadlock Condition

If a master operation is attempted when a slave operation to the same module is in progress, a deadlock condition has occurred. The VIC068A will signal a deadlock condition by asserting the $\overline{\text{DEDLK}}$ signal. This should be used by the local resource requesting the VMEbus to try the transfer after the slave access has completed.

Self-Access Condition

If the VIC068A, while it is VMEbus master, has a slave select signaled, a self access is said to have occurred. The VIC068A will issue a $\overline{\text{BERR}}$, which in turn will cause a $\overline{\text{LBERR}}$ to be asserted.

VIC068A VMEbus Slave Cycles

The VIC068A is capable of operating as a VMEbus slave controller. The VIC068A contains a highly programmable environment to allow for a wide variety of slave configurations. The VIC068A allows for:

- D32 or D16 configuration
- A32, A24, A16, or user-defined address spaces
- Programmable block transfer support including:
  - — DMA-type block transfer ($\overline{\text{PAS}}$ and $\overline{\text{DSACKi}}$ held asserted)
  - — non–DMA-type block transfer (toggle $\overline{\text{PAS}}$ and $\overline{\text{DSACKi}}$)
  - — No support for block transfer
- Programmable data acquisition delays
- Programmable $\overline{\text{PAS}}$ and $\overline{\text{DS}}$ timing
- Restricted slave accesses (supervisory accesses only)

When a slave access is required, the VIC068A will request the local bus. When local bus mastership is obtained, the VIC068A will read or write the data to/from the local resource and assert the $\overline{\text{DTACK}}$ signal to complete the transfer.

Slave Write-Posting

The VIC068A is capable of performing a slave write-post operation (bus decoupling). When enabled, the VIC068A latches the data to be written and acknowledge the VMEbus (asserts $\overline{\text{DTACK}}$) immediately thereafter. This prevents the VMEbus from having to wait for local bus access.

Address Modifier (AM) Codes

The VIC068A encodes and decodes the VMEbus address modifier codes. For VMEbus master accesses, the VIC068A encodes the appropriate AM codes through the VIC068A FCi and ASIZi signals, as well as the block transfer status. For slave accesses, the VIC068A decodes the AM codes and checks the slave select control registers to see if the slave request is to be supported with regard to address spaces, supervisory accesses, and block transfers. The VIC068A also supports user-defined AM codes; that is, the

VIC068A can be made to assert and respond to user-defined AM codes.

VIC068A VMEbus Block Transfers

The VIC068A is capable of both master and slave block transfers. The master VIC068A performs a block transfer in one of two modes:

- MOVEM-type Block Transfer
- Master Block Transfer with Local DMA

In addition to these VMEbus block transfers, the VIC068A is also capable of performing block transfers from one local resource to another in a DMA-like fashion. This is referred to as a Module-based DMA transfer.

The VMEbus specification restricts block transfers from crossing 256-byte boundaries without toggling the address strobe, in addition to restricting the maximum length of the transfer to 256 bytes. The VIC068A allows for easy implementation of block transfers that exceed the 256-byte restriction by releasing the VMEbus at the appropriate time and rearbitrating for the bus at a programmed time later (this in-between time is referred to as the interleave period), while at the same time holding both the local and VMEbus addresses with internal latches. All of this is performed without processor/software intervention until the transfer is complete.

The VIC068A contains two seperate address counters for the VMEbus and the local address buses. In addition, a seperate address is counter-provided for slave block transfers. The VIC068A address counters are 8-bit up-counters that provide for transfers up to 256 bytes. For transfers that exceed the 256-byte limit, the Cypress VAC068A or external counters and latches are required.

The VIC068A allows slave accesses to occur during the interleave period. Master accesses are also allowed during interleave with programming and external logic. This is referred to as the "dual path" option.

The VAC068A may be used in conjunction with the VIC068A to provide much of the external logic required for extended block transfer modes, such as the 256-byte boundary crossing and dual path. the VAC068A extends the 8-bit counters in the VIC068A to support full 32-bit incrementing addresses on both the local bus and VMEbus. The VAC068A also contains the latches required for extended address block transfers as well as those required for supporting the dual path feature. The VAC068A is not required to support block transfers, it simply enhances them.

MOVEM Master Block Transfer

This mode of block transfer provides the simplest implementation of VMEbus block transfers. For this mode, the local resource simply configures the VIC068A for a MOVEM block transfer and proceeds with the consecutive-address cycles (such as a 680X0 MOVEM instruction). The local resource continues as the local bus master in this mode.

Master Block Transfers with Local DMA

In this mode, the VIC068A becomes the local bus master and reads or writes the local data in a DMA-like fashion. This provides a much faster interface than the MOVEM block transfer, but with less control and fault tolerence.

VIC068A Slave Block Transfer

The process of receiving a block transfer is referred to as a slave block transfer. The VIC068A is capable of decoding the address modifier codes to determine that a slave block transfer is desired.

In this mode, the VIC068A captures the VMEbus address, and latches them into internal counters. For subsequent cycles, the VIC068A simply increments this counter for each transfer. The local protocol for slave block transfers can be configured in a full handshake mode by toggling both $\overline{PAS}$ and $\overline{DS}$ and expecting $\overline{DSACKi}$ to toggle, or in an accelerated mode in which only $\overline{DS}$ toggles and $\overline{PAS}$ is asserted throughout the cycle.

Module-based DMA Transfers

The VIC068A is capable of acting as a DMA controller between two local resources. This mode is similar to that of master block transfers with local DMA, with the exception that the VMEbus is not the second source or destination.

VIC068A Interrupt Generation and Handling Facilities

The VIC068A is capable of generating and handling a seven-level prioritized interrupt scheme similar to that used by the Motorola CISC processors. These interrupts include the seven VMEbus interrupts, seven local interrupts, five VIC068A error/status interrupts, and eight interprocessor communication interrupts.

The VIC068A can be configured to act as handler for any of the seven VMEbus interrupts. The VIC068A can generate the seven VMEbus interrupts as well as supplying a user-defined status/ID vector. The local priority level (IPL) for VMEbus interrupts is programmable. When configured as the system controller, the VIC068 will drive the IACK daisy-chain.

The local interrupts can be configured with the following:

- User-defined local interrupt priority level (IPL)
- Option for VIC068A to provide the status/ID vector
- Edge or level sensitivity
- Polarity (rising/falling edge, active HIGH/LOW)

The VIC068A is also capable of generating local interrupts on certain error or status conditions. These include:

- $\overline{ACFAIL}$ asserted
- $\overline{SYSFAIL}$ asserted
- Failed master write-post ($\overline{BERR}$ asserted)
- Local DMA completion for block transfers
- Arbitration timeout
- VMEbus interrupter interrupt

The VIC068A can also interrupt on the setting of a module or global switch in the interprocessor communication facilities.

Interprocessor Communication Facilities

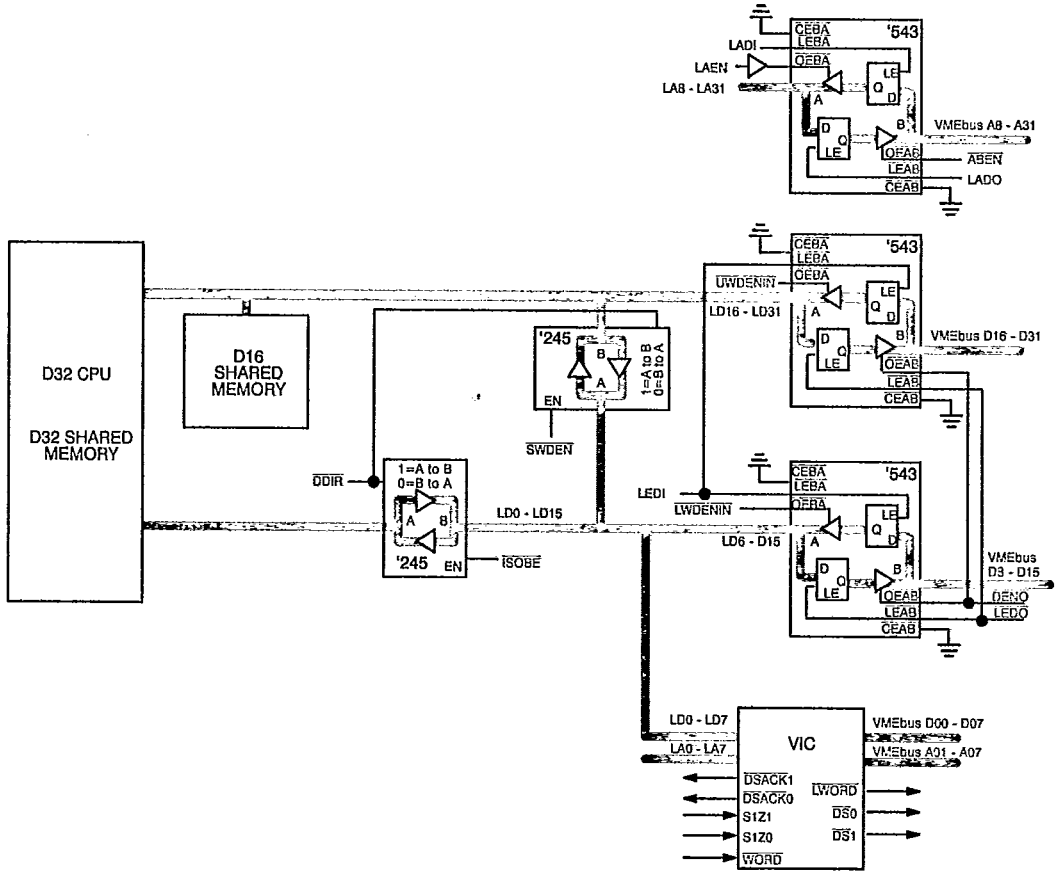
The VIC068A includes interprocessor registers and switches that can be written and read through VMEbus accesses. These are the only such registers that are directly accessible from the VMEbus. Included in the interprocessor communication facilities are:

- Four general purpose 8-bit registers
- Four module switches
- Four global switches
- VIC068A version/revision register (read-only)
- VIC068A Reset/Halt condition (read-only)
- VIC068A interprocessor communication register semaphores

When set through a VMEbus access, these switches can interrupt a local resource. The VIC068A includes module switches that are intended for a single module, and global switches which are intended to be used as a broadcast.

BUS

Buffer Control Signal for Shared Memory Implementation[1]



Note:
1. This configuration can support Slave Block Transfers and Master and Slave Write-Post Operation. This buffer configuration cannot support block transfers with DMA.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics (For guideline, not tested)

Parameters	Description	Test Conditions		Min.	Max.	Units
I_{CC}	V_{CC} Operating Supply Current	CLK 64M = 64 MHz	Commercial $T_A = -0°C$, $V_{CC} = 5.25V$		150	mA
			Industrial $T_A = -40°C$, $V_{CC} = 5.5V$		150	
			Military $T_A = -55°C$, $V_{CC} = 5.5V$		150	

For More Information

See the following documents:

VIC64 Datasheet
VAC068A Datasheet
CY7C964 Datasheet
VIC068A *User's Guide*
VAC068A User's Guide

Ordering Information

Ordering Code	Package Type	Operating Range
VIC068A–BC	B144	Commercial
VIC068A–GC	G145	
VIC068A–NC	N160	
VIC068A–UC	U162	
VIC068A–GI	G145	Industrial
VIC068A–UI	U162	
VIC068A–GM	G145	Military
VIC068A–UM	U162	

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BUS