μPD42532
32,768 x 8-Bit
Bidirectional Data Buffer

Description

The μPD42532 bidirectional data buffer features 32,768-word by 8-bit organization and CMOS dynamic circuitry that provides for high-speed, asynchronous, simultaneous write and read operation at a minimum cycle time of 100 ns. Two sets of write and read registers between the I/O pins and the storage cells enable all data to be parallel-transmitted as a single register group when the registers are either full or empty. The device's main application is data transmission between devices having different processing speeds, such as between a central processor and a disk.

Automatic refreshing by means of an internal capability is performed regularly for the μPD42532—without any influence on write and read operation. A built-in arbitration circuit performs each required read, write, or refresh operation sequentially (even if transparent refreshing overlaps with the transmission of data) to simplify the device's external timing requirements.

The μPD42532 operates from a single +5-volt power supply and is packaged in a 600-mil, 40-pin plastic DIP. Four FLAG pins, plus $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins, are provided to monitor the amount of data accumulated in storage.

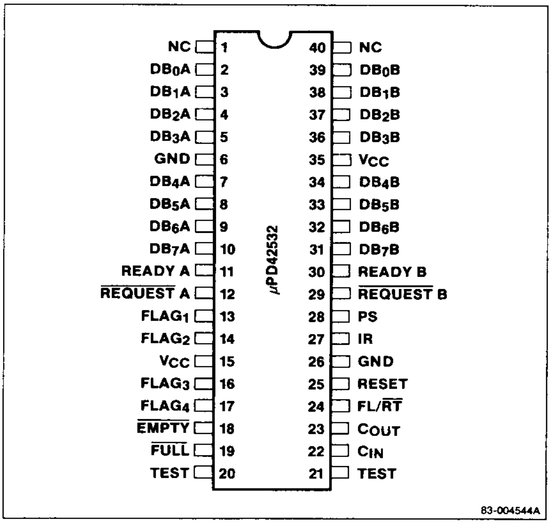
The μPD42532 is capable of bidirectional input/output by means of a port select function. Input and output pins are also supplied for cascade connection. Cascade connection allows any number of μPD42532s to be linked together so as to expand word width and length without limit.

Features

- ☐ 32,768-word by 8-bit organization
- ☐ CMOS technology
- ☐ Single +5-volt power supply
- ☐ Independent, asynchronous write/read operation
- ☐ Bidirectional transmission of input and output data (exchange of port functions)
- ☐ Automatic, regular refreshing
- ☐ Internal addressing
- ☐ Flag pin monitoring of accumulated data
- ☐ Unlimited expansion of word width and depth (cascade connection)
- ☐ Retransmit (re-read) function
- ☐ High-speed operation
  - — Access time: 50 ns maximum
  - — Cycle time: 100 ns minimum
- ☐ 600-mil, 40-pin plastic DIP packaging

Pin Configuration

40-Pin Plastic DIP



Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42532C-10	50 ns	100 ns	40-pin plastic DIP

Pin Identification

Symbol	Function
DB_0A-DB_7A	Port A input/output data buses
DB_0B-DB_7B	Port B input/output data buses
RESET	Reset input
$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B	Port A/Port B request input
READY A/READY B	Port A/Port B ready output
$\overline{\text{EMPTY}}$	Empty output
$FLAG_1$-$FLAG_4$	Flag outputs
$\overline{\text{FULL}}$	Full output
PS	Write/read port select input
IR	Interrupt read request input
FL/$\overline{\text{RT}}$	First load/retransmit input
C_{IN}	Cascade connection input
C_{OUT}	Cascade connection output
TEST	Test pin (connect to GND in system)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Functions

DB_0A-DB_7A/DB_0B-DB_7B. These pins function as 8-bit data buses for write input or read output depending on the status of the PS pin. The output drivers are three-state outputs.

RESET. This pin initializes the internal counters and pointers.

$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. To initiate a write or read cycle, the signal goes low for the respective port (if READY A or READY B is low, the corresponding $\overline{\text{REQUEST}}$ input is ignored internally). These pins can be connected to the WR and RD pins of a CPU.

READY A/READY B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. When a write or read cycle is possible, the READY signal is high for the respective port. These pins can be connected to the READY pins of a CPU or DMA controller.

$\overline{\text{EMPTY}}$. The signal from this pin is low whenever the amount of data accumulated is exactly 0 bytes, and high in all other cases.

$FLAG_1$-$FLAG_4$. These pins reflect the amount of data accumulated in the storage array. By combining the output signals, it is possible to monitor (in 2K byte steps) data quantities of up to 32K bytes.

$\overline{\text{FULL}}$. The signal from this pin is low when the storage cells are full of accumulated data, and high in all other cases.

PS. This pin is used to specify the direction of data transfer. When PS is high, Port A serves as the write port and Port B as the read port. When PS is low, the functions of the two ports are reversed.

IR. If the data accumulated in storage is less than 64 bytes (i.e., one register's capacity), the READY signal for the read port goes low to inhibit reading. However, forcing IR high makes it possible to read all stored data.

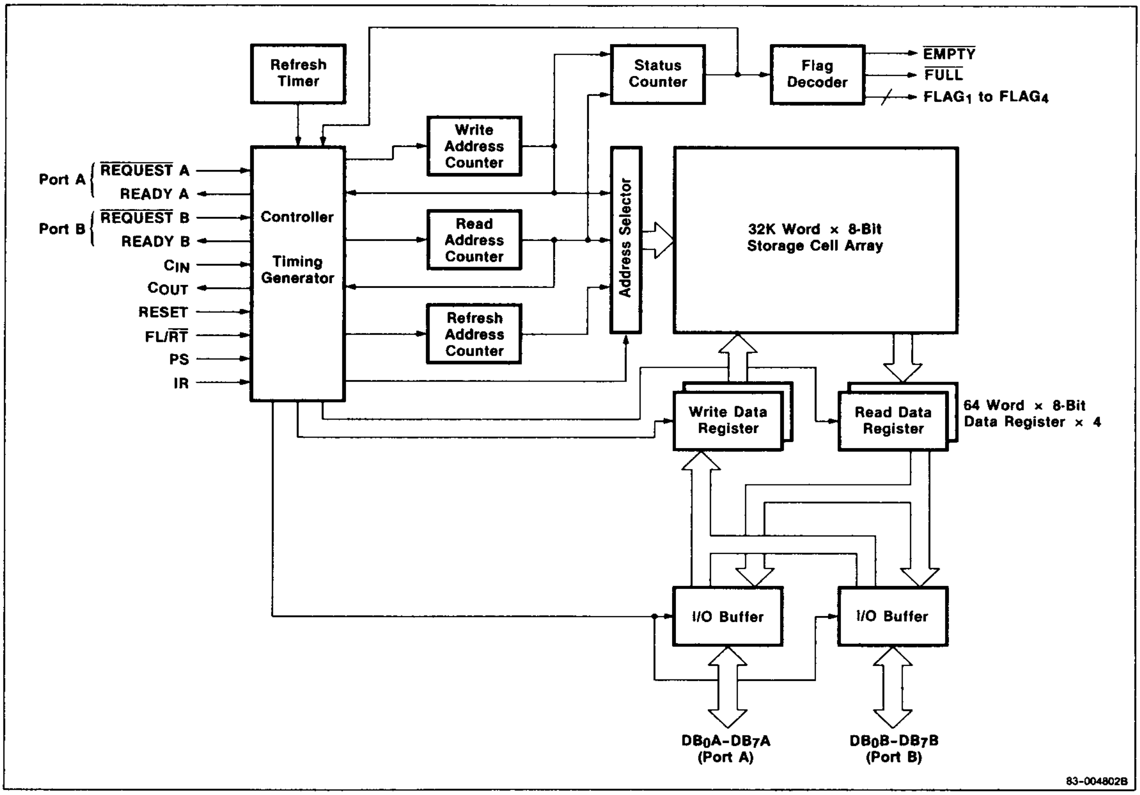
Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, all remaining data must be read using the interrupt read option.

FL/$\overline{\text{RT}}$. This pin designates the lead device when multiple devices are cascade connected. It is high only for that device and low for all others. If the device is not cascaded, a low FL/$\overline{\text{RT}}$ controls the retransmit (reread) function; other than during retransmission, FL/$\overline{\text{RT}}$ must be high.

C_{IN}. This pin is used to expand word depth and is connected to the C_{OUT} pin of the device preceding it in cascade connections. If word depth is not expanded, C_{IN} is connected to C_{OUT} of the same device.

C_{OUT}. This pin is used to expand word depth and is connected to the C_{IN} pin of the device following it in cascade connections. If word depth is not expanded, C_{OUT} is connected to C_{IN} of the same device.

Block Diagram



Operation

Reset Cycle

After power is applied to the μPD42532, it is necessary to clear the internal counters and initialize the write and read address pointers by executing a reset cycle. A reset cycle can be executed at any time by setting the RESET pin to a high logic level. However, once this cycle is initiated, RESET, REQUEST, and FL/RT must be kept high for a minimum time of t_{SW} before the RESET signal goes low again (see waveform for "Reset Cycle"). The RESET, REQUEST, and FL/RT signals are all high at the start of a reset, except in cascade connections, in which case a high FL/RT is required only in the first stage.

After a reset, the READY signal for the write port, READY (W), is driven high to prepare for a write cycle. Subsequently, the REQUEST signal for the write port, REQUEST (W), can be set low to commence writing.

A standard read cycle can be executed once data written to one of the 64-byte registers has filled that register and been transferred to the storage cells. The READY signal for the read port, READY (R), goes high to prepare for the cycle. Subsequently, the REQUEST signal for the read port, REQUEST (R), can be set low to commence reading.

Write Cycle

In a write cycle, data is written to one of two 64-byte write registers before being transferred to the storage cells. Whenever 64 bytes have been written into one register, write operation automatically shifts to the other and the contents of the first are transferred to storage. High-speed write cycles are thus executed continuously by alternating registers repeatedly. Write data must satisfy the requirements for setup and hold times as measured against the rising edge of REQUEST (W) [see waveform for "Write Cycle"].

A write cycle can be initiated any time READY (W) is high by setting $\overline{\text{REQUEST}}$ (W) low. To allow a write cycle to be executed in one port even while the other port may be executing a read cycle, READY (W) is always high after a reset, except in the following cases:

- Whenever the storage cells are full of accumulated data
- While the device is executing a forced read cycle (see **Interrupt Read Cycle**)
- When a retransmit operation is being performed (see **Retransmit Cycle**)

While READY (W) is off, the $\overline{\text{REQUEST}}$ (W) signal is ignored internally and no write cycle is executed.

Figure 1. Write Register Operation

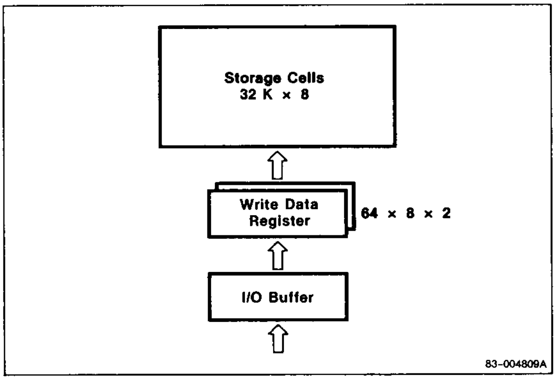
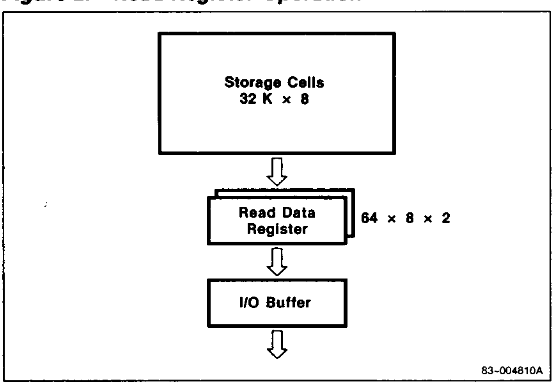


Figure 2. Read Register Operation



Read Cycle

In a read cycle, data is not read directly from the storage cells but rather from one of two 64-byte read registers. After 64 bytes of data have been read from one register, read operation automatically shifts to the other and the contents of the first are subsequently replaced by data from the storage cells. High-speed read cycles are thus executed continuously by alternating registers repeatedly.

Data is output after a maximum access time of t_{AC}, measured from the falling edge of $\overline{\text{REQUEST}}$ (R). When $\overline{\text{REQUEST}}$ (R) is high or READY (R) is low, the outputs are in a state of high impedance (see waveform for "Read Cycle").

A standard read cycle can be initiated any time READY (R) is high by setting $\overline{\text{REQUEST}}$ (R) low. To allow a read cycle to be executed in one port even while the other port may be executing a write cycle, the READY (R) signal is always high, except in the following cases:

- Whenever the data accumulated is less than 64 bytes
- While a retransmit operation is being performed (see **Retransmit Cycle**).

While READY (R) is low, $\overline{\text{REQUEST}}$ (R) is ignored internally and no read cycle is executed.

Flags

The μPD42532 supplies signals from the $\overline{\text{EMPTY}}$ pin, the $\overline{\text{FULL}}$ pin, and the four FLAG pins to indicate the amount of stored data in units of approximately 2K bytes. Accumulated data is reflected as the difference between the write address counter and the read address counter. Thus, if a total of 16K bytes have been read while 32K bytes have been written since the most recent reset, the amount of data in storage is 16K bytes.

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins are used to prevent overwriting and overreading. To control write operation on data units of register length (64 bytes), the $\overline{\text{FULL}}$ pin outputs a low signal when stored data reaches the 32,705- to 32,768-byte range. Whenever write cycles are executed continuously and the storage cells become full, $\overline{\text{REQUEST}}$ (W) is ignored and the signals of $\overline{\text{FULL}}$ and READY (W) are driven low to inhibit writing. Meanwhile if read cycles are executed and the data decreases to 32,704 bytes or less, READY (W) goes high again to enable write operation.

The $\overline{EMPTY}$ pin goes low whenever stored data is exactly 0 bytes. Since standard read cycles cannot be executed if the quantity of data drops below 64 bytes, READY (R) goes low to inhibit read operation. Whenever write cycles are executed and stored data increases to 64 bytes or more, READY (R) goes high again to enable read operation.

The status of the FLAG pins depends on the internal status of the write and read address counters. These counters are incremented as data is transferred to or from the storage array. Since the logic levels of the FLAG pins reflect movement of blocks of data on a 64-byte-register basis rather than on a single-byte basis, the status indicated by these pins can be in error by a maximum of 255 bytes with respect to the actual amount of data accumulated [i.e., the sum of the write register (63 bytes), the read registers (128 bytes), and the 64 bytes currently being transferred]. This discrepancy means that two adjacent ranges of stored data, as indicated by the FLAGs, can overlap by up to 191 bytes.

The following table shows the combination of signals output from these pins.

Table 1. Stored Data as Indicated by Flag Pins

Amount of Stored Data (bytes)	$\overline{FULL}$	$\overline{EMPTY}$	FLAG 1	FLAG 2	FLAG 3	FLAG 4
32705 to 32768	0	1	1	1	1	1
30721 to 32767	1	1	1	1	1	1
28673 to 30911	1	1	0	1	1	1
26625 to 28863	1	1	1	0	1	1
24577 to 26815	1	1	0	0	1	1
22529 to 24767	1	1	1	1	0	1
20481 to 22719	1	1	0	1	0	1
18433 to 20671	1	1	1	0	0	1
16385 to 18623	1	1	0	0	0	1
14337 to 16575	1	1	1	1	1	0
12289 to 14527	1	1	0	1	1	0
10241 to 12479	1	1	1	0	1	0
8193 to 10431	1	1	0	0	1	0
6145 to 8383	1	1	1	1	0	0
4097 to 6335	1	1	0	1	0	0
2049 to 4287	1	1	1	0	0	0
1 to 2239	1	1	0	0	0	0
0	1	0	0	0	0	0

Notes:

(1) 1 = high level

(2) 0 = low level

Interrupt Read Cycle

Whenever the amount of stored data drops below 64 bytes (i.e., one register's capacity), or 2K bytes for devices with process code K, READY (R) is driven low to inhibit reading. Any data remaining in a write register can only be read by means of an interrupt (or forced) read cycle.

An interrupt read cycle can be executed by forcing the IR pin high. At this point, data is transferred from the write register to one of the read registers via the storage array, and write operation is disabled until all stored data has been read. If this cycle is initiated after READY (R) goes low, read operation will be delayed until all data has been transferred to one of the read registers.

Once the device completes reading of its last address, the $\overline{EMPTY}$ and READY (R) signals are driven low and READY (W) goes high to enable write operation again (unless a retransmit cycle has been requested). Read cycles will be executed only after 64 bytes or more have been written and transferred to storage.

Retransmit Cycle

The μPD42532 will execute a retransmit cycle whenever a low-level pulse is applied to $\overline{RT}$. A retransmit cycle initializes the read address counter to starting address 0. Although retransmission can be executed at any time, $\overline{REQUEST}$ (W) and $\overline{REQUEST}$ (R) must be high before and after the low $\overline{RT}$ signal is applied.

During this cycle, the READY signals are pulsed low to temporarily inhibit writing and reading, and the FLAG and $\overline{EMPTY}$ signals vary in accordance with the amount of data in storage. After READY (W) goes high again, the retransmit preparation cycle is complete. Write operation can resume after an extra delay to ensure stability of the FLAG and $\overline{EMPTY}$ pins. If an interrupt read signal is applied during retransmission, the interrupt read cycle is executed after termination of the retransmit cycle.

The retransmit function is only useful in systems where less than 32K bytes of data are written between resets. If a retransmit cycle is executed after more than 32K bytes are written, old data cannot be retransmitted.

Since the $\overline{RT}$ pin is multiplexed as the first load (FL) pin in cascade connections, cascaded devices cannot be used for retransmission. In single-device configuration, this pin is always high except during a retransmit cycle.

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Port Select Function

The μPD42532 is able to change the direction of data transfer according to the logical level of the signal applied to the PS pin. When a high-level input is applied to PS, Port A becomes the write port and Port B the read port. When PS is low, the functions of the two ports are reversed. While port functions are being assigned, the $\overline{\text{REQUEST}}$ signals must be kept high.

Since register and storage cell data are preserved during port selection, data written to a particular port can also be read from that same port.

Cascade Connection

The μPD42532 can be used in a single-device, 32K by 8-bit configuration or it can be cascade connected by means of the C_{IN} and C_{OUT} pins to allow unlimited expansion of word width and length.

Single-Device Configuration. When using the μPD42532 as a single 32K by 8-bit data buffer, connect C_{OUT} to C_{IN} and set the FL pin to a high logic level (see figure 3).

Expanded Word Width. When using multiple devices to expand word width, connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals. Each C_{OUT} pin should be connected to its own C_{IN} pin (as in the single-device configuration) and a high-level input applied to each FL. The flag pins of a single μPD42532 can be used to represent the entire system (see figure 4).

Expanded Word Length. When using multiple devices to expand word length, set a high-level input to FL of the lead μPD42532 and a low-level input to FL of all the others. Each C_{OUT} pin should be connected to C_{IN} of the device following it; C_{OUT} on the last device should be connected to C_{IN} of the lead device. Connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals.

The $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY pins of each device, respectively, can be ORed together by external logic. 'OR' outputs are composite $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY signals for all data buffers (see figure 5).

Operation. To enable operation of μPD42532s in cascade connection, set the RESET signal(s) high to clear the internal counters and initialize the write and read address pointers. When the reset is complete, start writing to the lead device. While data is being written to the first, all other devices output low READY signals and ignore the $\overline{\text{REQUEST}}$ signals. When write operation in the first μPD42532 (n) reaches the last address, its C_{OUT} pin outputs a high-level signal and forces C_{IN} of the next device high. Write operation shifts to the next device in succession (n + 1). The READY (W) signal of the first device (n) is driven low, and the READY (W) signal of the succeeding device (n + 1) goes high.

If only write cycles are being executed, each data buffer outputs a low $\overline{\text{FULL}}$ signal as writing is completed for that device. At the point where the last device finishes writing to its last address, all μPD42532s output low-level $\overline{\text{FULL}}$ and READY (W) signals. The ORed composite of these signals should be used to inhibit write operation.

If write and read cycles are being executed simultaneously, and the storage cells in the lead device are not full of accumulated data when the last device completes writing to its last address, write operation shifts to the lead μPD42532 again. Writing continues in this manner until every data buffer is full.

Read cycles also begin with the lead device (n) and shift to the next (n + 1) once the last address has been read. When all devices have been completely emptied of data, the ORed composite of the $\overline{\text{EMPTY}}$ signals is low. If the expanded word length configuration has less than 64 bytes of data in a write register, $\overline{\text{EMPTY}}$ will not be at a low level; READY (R) will be low to indicate that standard read operation may not proceed. Forced read or dummy write cycles will be required to continue reading any accumulated data of less than 64 bytes.

Figure 3. Single-Device Configuration Block Diagram

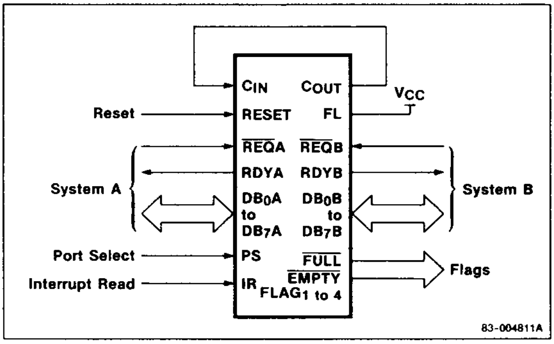


Figure 4. Expanded Word Width Block Diagram

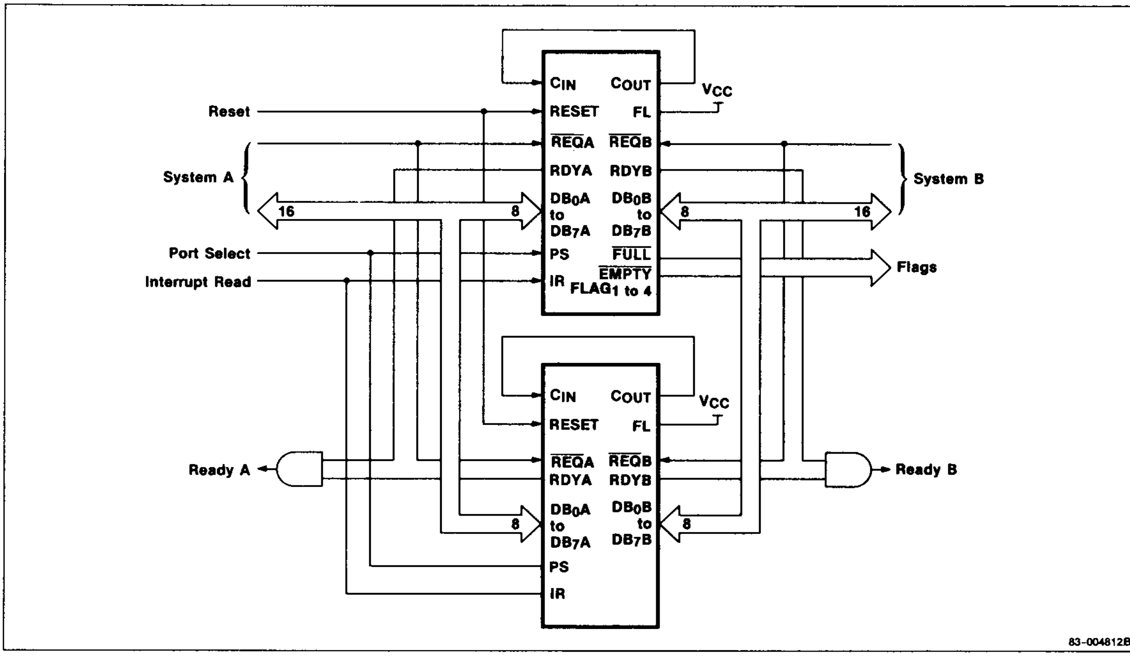
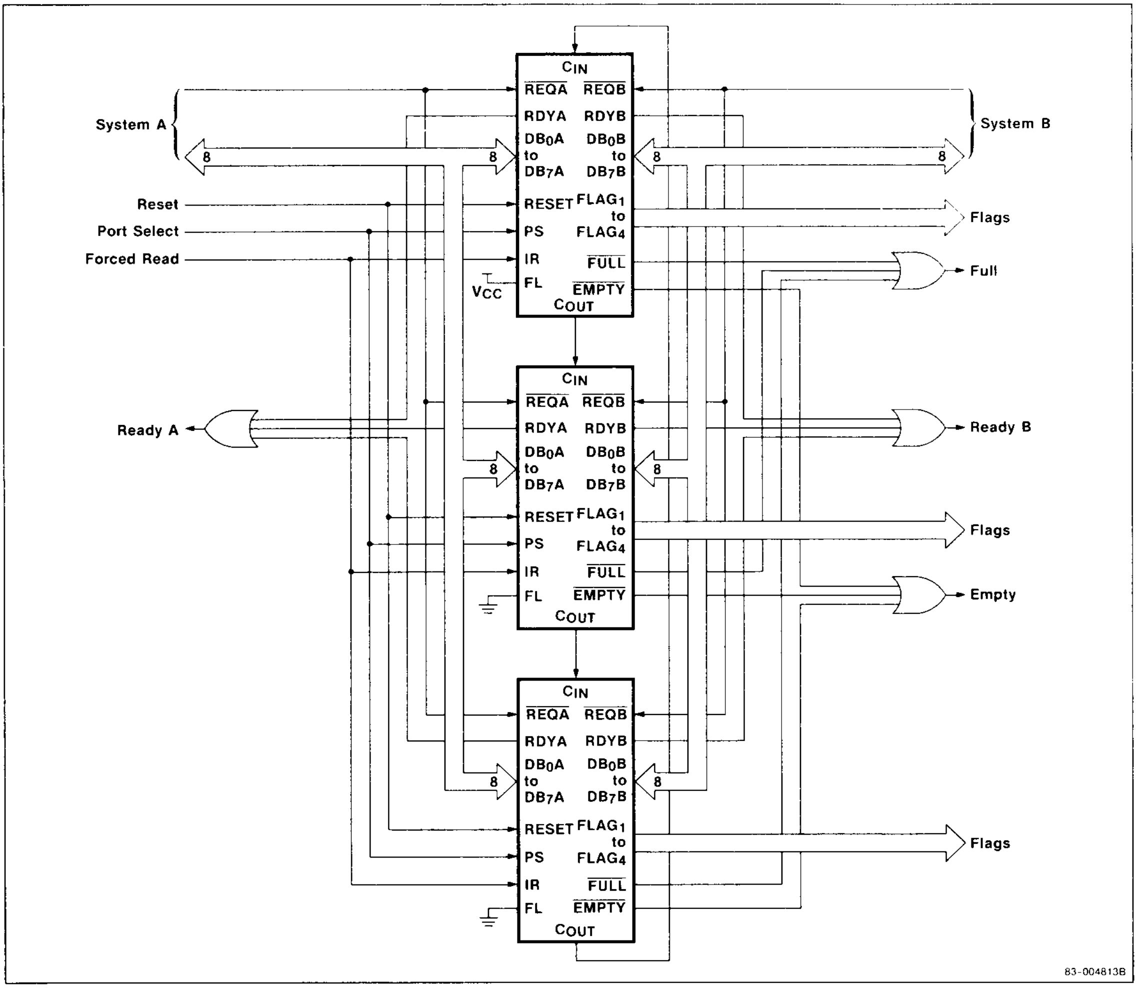


Figure 5. Expanded Word Length Block Diagram



Absolute Maximum Ratings

Terminal voltage, V_T	−1.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Output current, I_O	50 mA
Power supply voltage, V_{CC}	−1.5 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended DC Operating Conditions

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC1}			20	mA	$\overline{REQUEST}$ A, B = V_{IH}
Write/read cycle supply current	I_{CC2}			80	mA	t_{WC} = 100 ns; t_{RC} = 100 ns
Write cycle supply current	I_{CC3}			60	mA	t_{WC} = 100 ns; $\overline{REQUEST}$ (R) = V_{IH}
Read cycle supply current	I_{CC4}			60	mA	t_{RC} = 100 ns; $\overline{REQUEST}$ (W) = V_{IH}
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; other inputs = 0 V
Output leakage current	I_O	−10		10	μA	V_O = 0 to V_{CC}; output disabled
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4 mA

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			10	pF	$\overline{REQUEST}$, $\overline{RESET}$, PS, C_{IN}, IR, FL/$\overline{RT}$
Output capacitance	C_O			10	pF	READY, $FLAG_1$-$FLAG_4$, C_{OUT}, $\overline{FULL}$, $\overline{EMPTY}$
Input/output capacitance	$C_{I/O}$			10	pF	DB_0-DB_7

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Read cycle time	t_{RC}	100		ns	
$\overline{REQUEST}$ (R) pulse width	t_{RQW}	50	10000	ns	(Note 5)
$\overline{REQUEST}$ (R) precharge time	t_{RQP}	30		ns	
$\overline{REQUEST}$ (R) low hold time after READY (R) high	t_{RQN}	50	10000	ns	(Note 6)
READY (R) low output time	t_{RRF}		30	ns	(Note 14)
Access time	t_{AC}		50	ns	
Access time after READY (R) high	t_{ACR}		50	ns	
Output data hold time	t_{OH}	10		ns	
Output data off time	t_{OFF}		40	ns	
Low-impedance output delay	t_{LZ}	5		ns	
Low-impedance output delay after READY (R) high	t_{LZR}	0		ns	
READY (R) low time when empty	t_{SRR}		4800 + 64 t_{WC}	ns	(Note 8)
READY (R) low time when almost empty	t_{EMR}	0	4800 + 63 t_{WC}	ns	(Note 8)
Write cycle time	t_{WC}	100		ns	
$\overline{REQUEST}$ (W) pulse width	t_{WQW}	50	10000	ns	(Note 5)
$\overline{REQUEST}$ (W) precharge time	t_{WQP}	30		ns	
$\overline{REQUEST}$ (W) low hold time after READY (W) high	t_{WQN}	50	10000	ns	(Note 6)
READY (W) low output time	t_{WRF}		30	ns	
Write data setup time	t_{DW}	30		ns	
Write data hold time	t_{DH}	10		ns	
$\overline{REQUEST}$ high setup time	t_{QRP}	t_T + 30		ns	(Note 6)
READY (W) low time when full	t_{FLW}	0	3200 + 64 t_{RC}	ns	
$FLAG_1$-$FLAG_4$ output times	t_{FLO}		4800	ns	
$\overline{EMPTY}$ and $\overline{FULL}$ output valid times	t_{EFO}		40	ns	
$\overline{EMPTY}$ and $\overline{FULL}$ output hold times	t_{EFH}	0		ns	
$\overline{FULL}$ output off time	t_{FOF}		3200	ns	(Note 9)
C_{OUT} output off time when read request is executed	t_{COR}		40	ns	
C_{OUT} output on time when write request is executed	t_{COW}		40	ns	
C_{IN} setup time for $\overline{REQUEST}$ (R)	t_{CIR}	10		ns	
C_{IN} setup time for $\overline{REQUEST}$ (W)	t_{CIW}	10		ns	
Reset pulse width	t_{SW}	100		ns	
READY, $\overline{FULL}$, and $\overline{EMPTY}$ output times after reset	t_{SWR}		80	ns	
$FLAG_1$-$FLAG_4$ output times after reset	t_{SSF}		100	ns	
$\overline{REQUEST}$ precharge hold time after reset	t_{SWQ}	30		ns	
$\overline{RT}$ disable hold time after reset	t_{SRT}	800		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
C_{OUT} output low time after reset	t_{SWC}		100	ns	
READY (R) on time after interrupt read is executed	t_{FRR}	0	6400	ns	(Note 7)
READY (W) off time after interrupt read is executed	t_{FWR}		50	ns	(Note 7)
READY (W) on time after interrupt read	t_{IRW}		100	ns	(Note 11)
$\overline{REQUEST}$ (W) hold time after IR input	t_{FQA}	60		ns	(Note 13)
$\overline{REQUEST}$ (W) setup time before IR input	t_{FQB}	60		ns	
IR pulse width	t_{FW}	50	2000	ns	(Notes 4, 12, 13)
$\overline{REQUEST}$ hold time after PS input	t_{PAQ}	100		ns	
$\overline{REQUEST}$ setup time before PS input	t_{PBQ}	100		ns	
READY output time after port selection	t_{PSR}		50	ns	
$\overline{RT}$ pulse width	t_{RTW}	50	2000	ns	(Note 4)
$\overline{REQUEST}$ setup time before $\overline{RT}$ input	t_{BRT}	60		ns	(Note 10)
$\overline{REQUEST}$ hold time after $\overline{RT}$ input	t_{RTQ}	60		ns	
READY (R) on time after retransmit is executed	t_{RTR}		6400	ns	(Note 7)
READY (W) on time after retransmit is executed	t_{WRT}		4800	ns	(Note 7)
READY off time after retransmit is executed	t_{RRT}		50	ns	
$\overline{EMPTY}$ and $\overline{FULL}$ output hold times after retransmit is executed	t_{FSRT}	0		ns	
$\overline{EMPTY}$ reset time after retransmit is executed	t_{RTE}		3200	ns	
$FLAG_1$-$FLAG_4$ output valid times after retransmit is executed	t_{RTF}		8000	ns	
Input transition time	t_T	5	50	ns	

Notes:

(1) All voltages are referenced to GND.

(2) All ac measurements assume input pulse rise and fall times of 5 ns.

(3) The input voltage reference levels for timing ratings are V_{IH} (min) and V_{IL} (max). Transition time t_T is defined between V_{IH} and V_{IL}.

(4) IR and $\overline{RT}$ inputs cannot be applied simultaneously. A timing delay of at least 100 ns is required. See figures 6 and 7 for acceptable input methods.

(5) The maximum pulse width of 10,000 ns applies only when the READY signal is on.

(6) $\overline{REQUEST}$ cannot be raised to a high level during the t_{QRP} + t_{RQN} (or t_{WQN}) interval.

(7) If an $\overline{RT}$ (IR) pulse is applied during IR ($\overline{RT}$) operation, the $\overline{RT}$ (IR) operation is delayed until IR ($\overline{RT}$) operation is released.

(8) "Empty" is defined as the state where the amount of stored data is zero, and "almost empty" is defined as the state where the amount of data is 1 to 63 bytes.

(9) t_{FOF} is defined from the rising edge of the $\overline{REQUEST}$ (R) signal when the amount of stored data reaches the prescribed value (that is, the value at which the FULL signal changes from a low level to a high level as defined in Table 1).

(10) t_{BRT} = 4800 ns minimum for the devices with process code K.

Figure 6. Input Timing for IR and $\overline{RT}$: Method 1

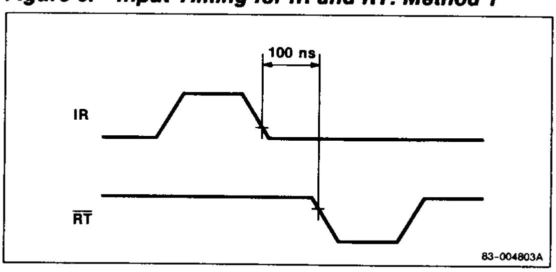
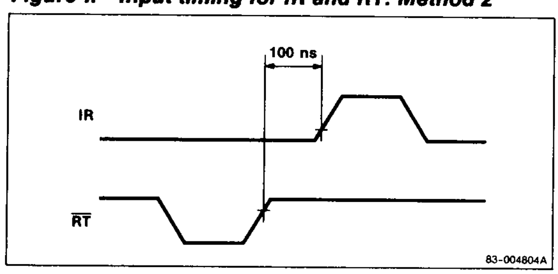


Figure 7. Input timing for IR and $\overline{RT}$: Method 2



AC Characteristics (cont)

Notes [cont]:

(11) After all data has been read in an IR cycle for devices with process code K, always input a $\overline{\text{RESET}}$ signal to initialize the internal circuitry before proceeding to the next operation. See figure 8.

(12) The IR signal is invalid whenever the $\overline{\text{EMPTY}}$ signal is low on devices with process code K.

(13) If an IR input signal is applied in a cascade connection for devices with process code K, the $\overline{\text{REQUEST}}$ (W) signal must stay at a high level until all data has been read.

(14) Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, read all of the remaining data using the interrupt read option.

Figure 8. Reset Pulse After IR Operation

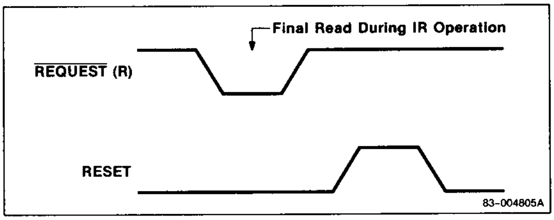


Figure 9. Input Timing

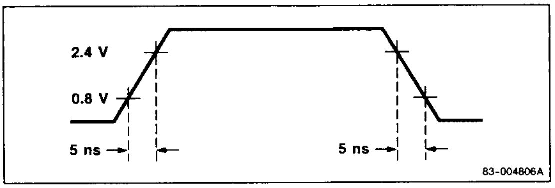


Figure 10. Output Timing

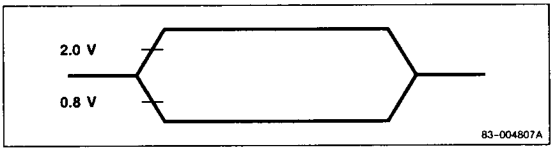
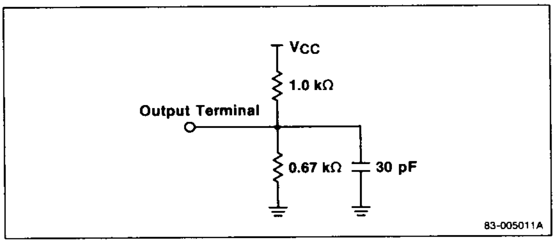
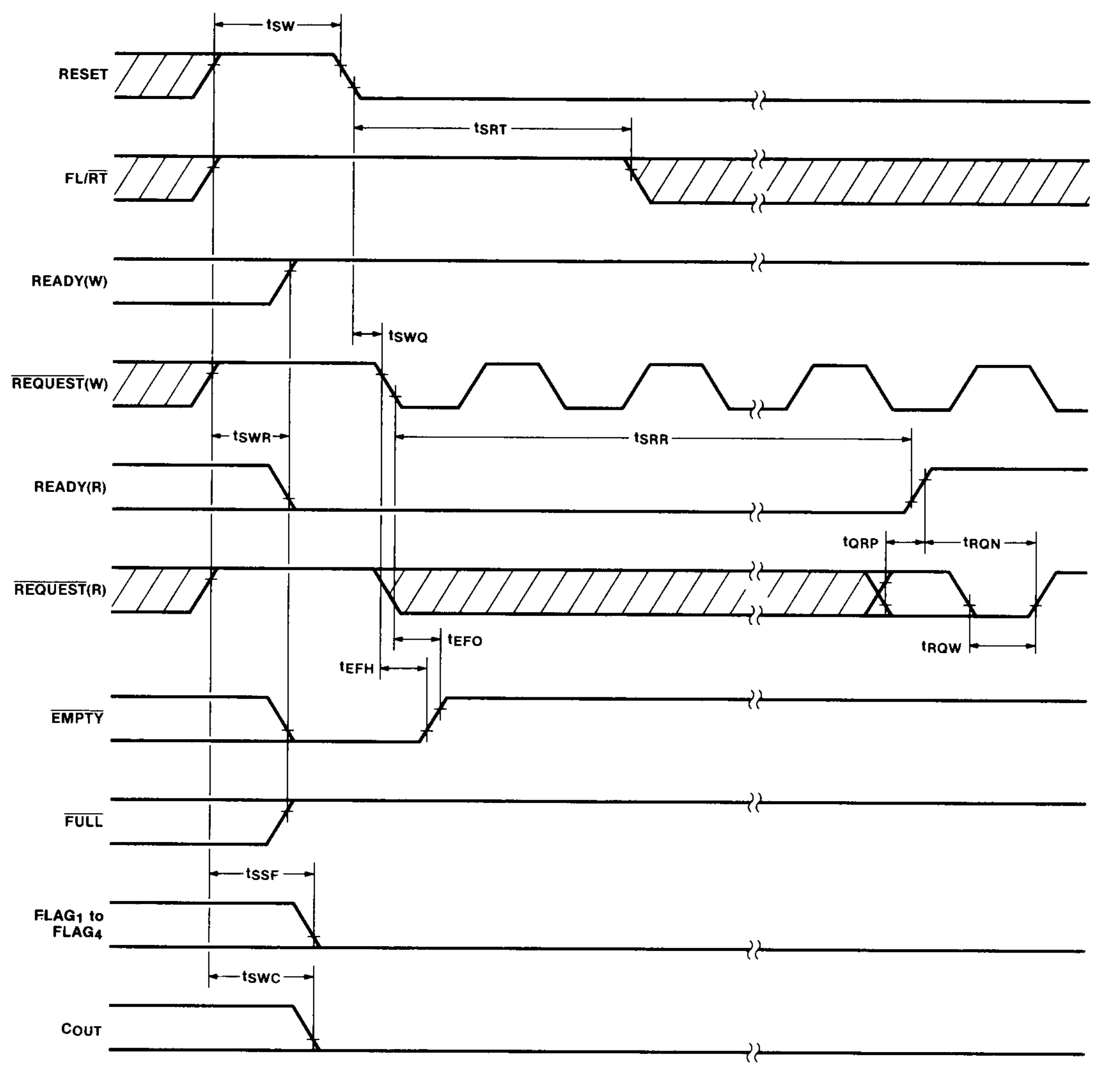


Figure 11. Output Loads



Timing Waveforms

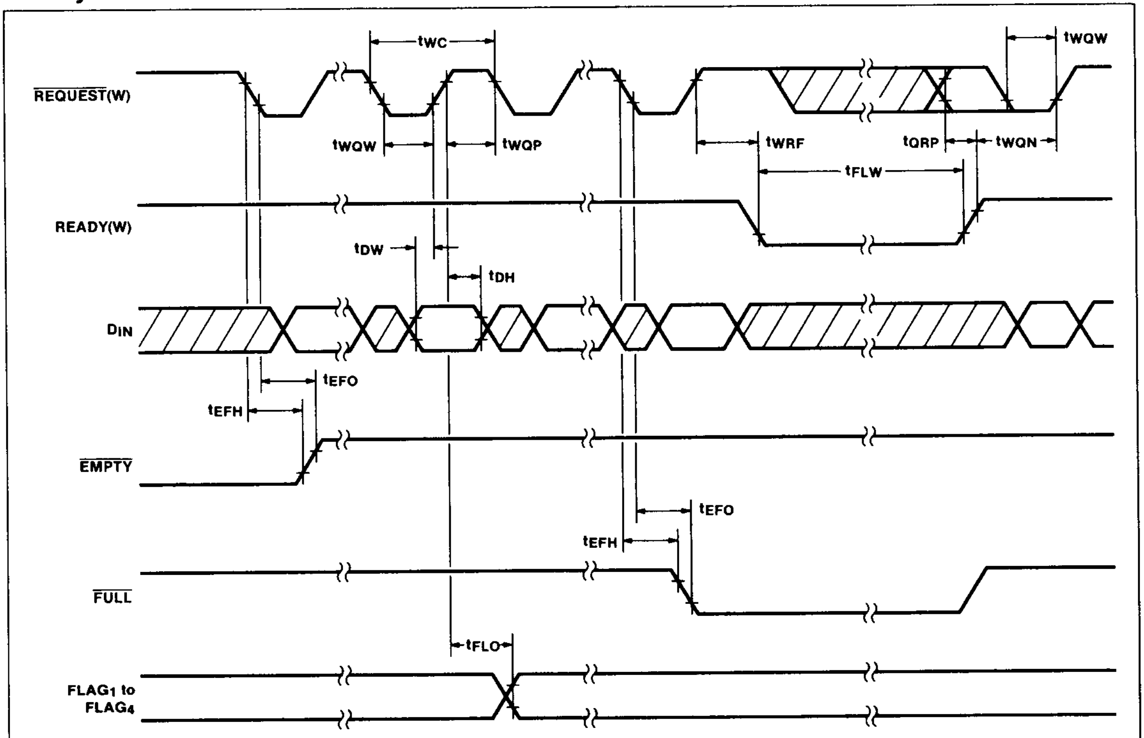
Reset Cycle



Notes:
(1) IR = low
(2) PS = high or low

Timing Waveforms (cont)

Write Cycle



Notes:

(1) IR = low

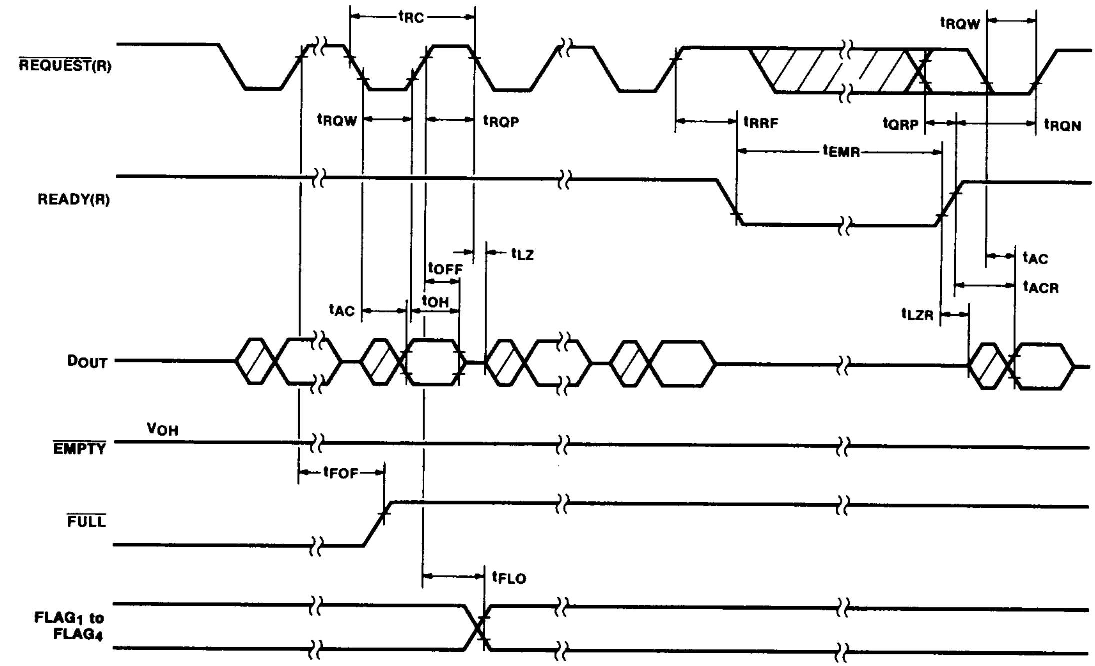
(2) FL/$\overline{RT}$ = high

(3) PS = high or low

(4) RESET = low

Timing Waveforms (cont)

Read Cycle



Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high
(3) PS = high or low
(4) RESET = low

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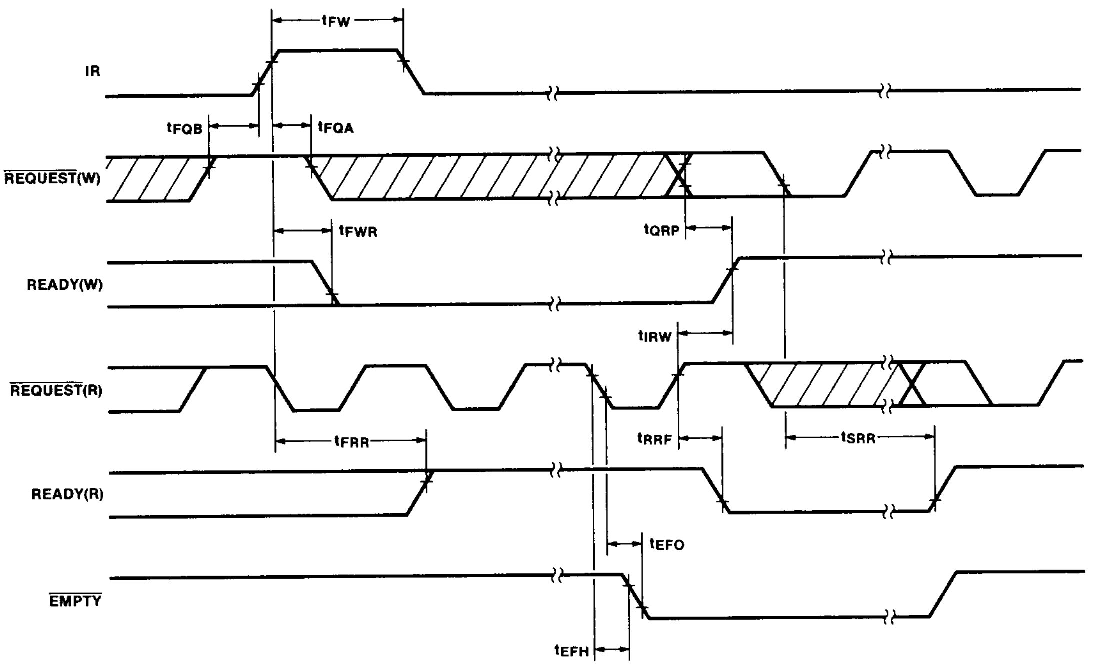
Timing Waveforms (cont)

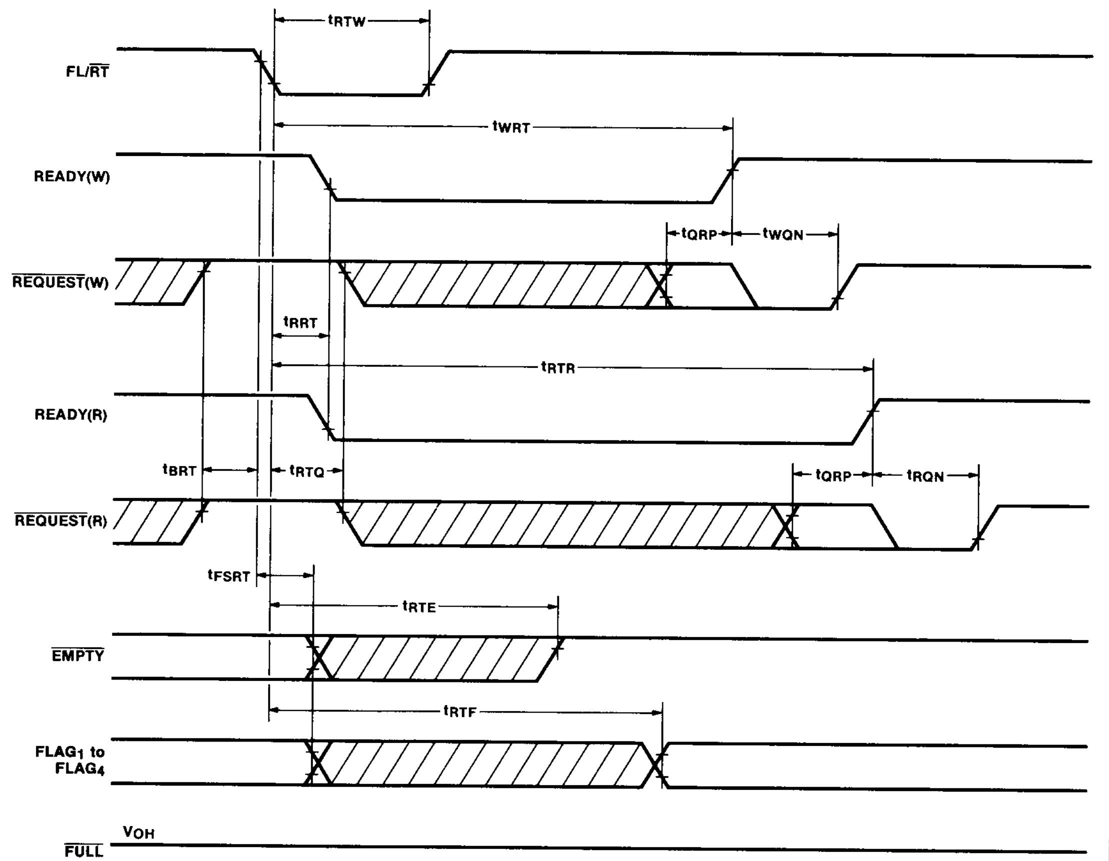
Interrupt Read Cycle



Notes:
(1) PS = high or low
(2) FL/RT = high
(3) RESET = low

Timing Waveforms (cont)

Retransmit Cycle



Notes:

(1) PS = high or low

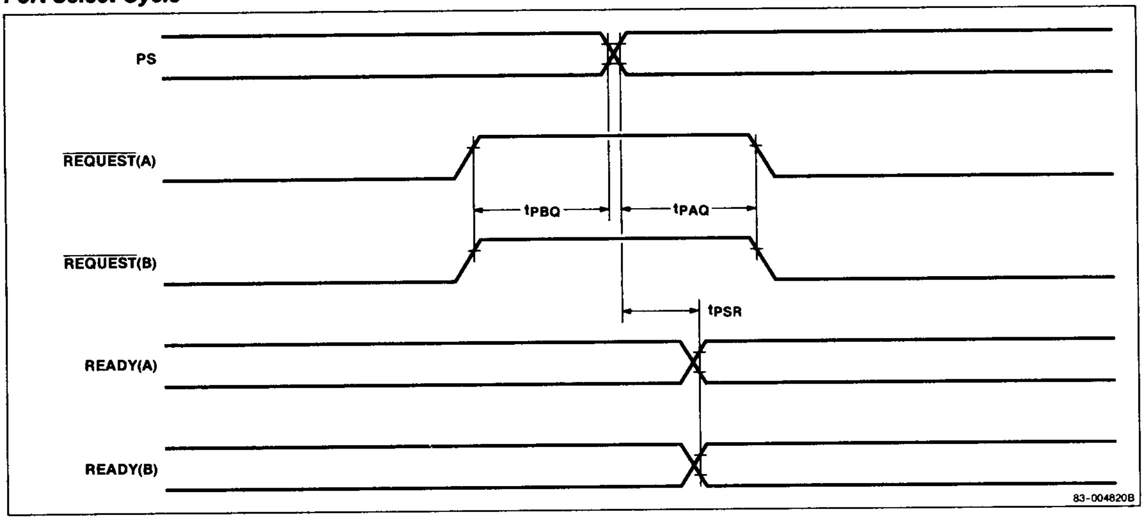
(2) IR = low

(3) RESET = low

NEC

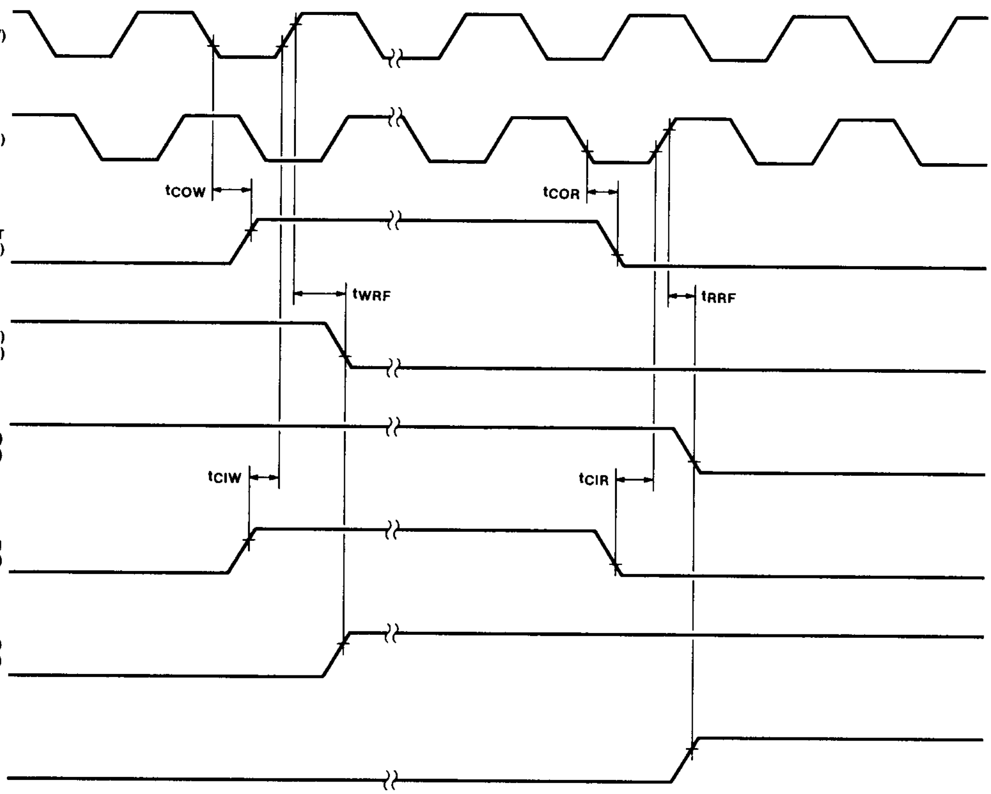
Timing Waveforms (cont)

Port Select Cycle



Timing Waveforms (cont)

Cascade Cycle



Notes:

(1) IR = low

(2) FL/$\overline{RT}$ = high or low

(3) PS = high or low

(4) RESET = low