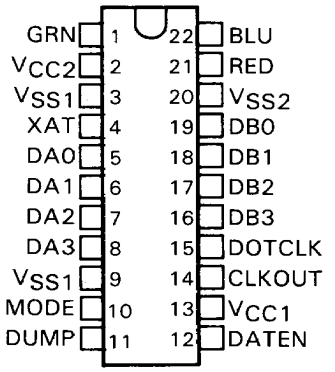
- Three 4-Bit Video-DAC Outputs Directly Drive 75-Ω Monitor Cables
- Sixteen 14-Bit Color Lookup Registers Support the Simultaneous Display of a Palette of 16 Colors Selected from an Available 4096 Colors
- Color Lookup Table Can Be Automatically Loaded with a New Set of Colors Prior to the Start of Each Horizontal Scan Line without Processor Intervention
- Device Can Be Used with a Variety of Controllers and Memory Types
- Real-Time Animation is Supported by the REP Attribute Bit, Which Facilitates Rapid Rendering of Scenes Composed of Polygons of Various Solid Colors
- Video Overlay Capability Is Supported by the EXT Attribute Bit, Which Is Used to Control External Circuitry
- Analog RGB Video Data Is Output from the Video-DAC Pins at Update Rates of Up to 66 MHz

N PACKAGE
(TOP VIEW)



- Digital Input and Output Logic Levels Are TTL-Compatible
- Separate 5-Volt Power Supply Pins Are Provided for Digital and Analog Functions
- Device Is Available in a 22-Pin, 400-Mil Plastic Dual-in-Line Package

description

The TMS34070 Color Palette is a monolithic integrated circuit containing a color lookup table and providing three channels of analog video output for RGB-type CRT monitors operating at video bandwidths up to 66 MHz. This corresponds to a display resolution of about 1024 by 768 pixels, assuming a non-interlaced display refreshed at 60 Hz. The TMS34070 supports graphics systems having up to four color planes and allows 16 of 4096 colors to be displayed simultaneously on the CRT monitor.

The three analog outputs of the TMS34070 — RED, GRN, and BLU — are used to drive the R (red), G (green), and B (blue) inputs of a color CRT. Each of the analog output pins is driven by a four-bit digital-to analog converter (DAC). Each DAC provides 16 levels of intensity in its respective color.

The TMS34070 supports frame-buffer memories of up to four bits per pixel. The sixteen 14-bit registers of the color lookup table are loaded directly from the video memory, eliminating the need for a separate processor interface through which the registers can be loaded. During each output clock period, two 4-bit pixel values are input in parallel on eight data pins and are multiplexed internally to provide analog R, G, and B video signals output at the dot clock frequency.

Each of the 16 registers of the color lookup table contains 12 color bits and two attribute bits. The color bits are assigned as four bits of red intensity, four bits of green intensity, and four bits of blue intensity. The two attribute bits are named EXT (external pixel attribute) and REP (repeat color command). The EXT bit provides a convenient means for controlling external devices and supports the overlaying of external video with a graphics image. The REP bit provides a means of repeating the previous color rather than specifying a new color and supports real-time animation of scenes composed of colored polygons.

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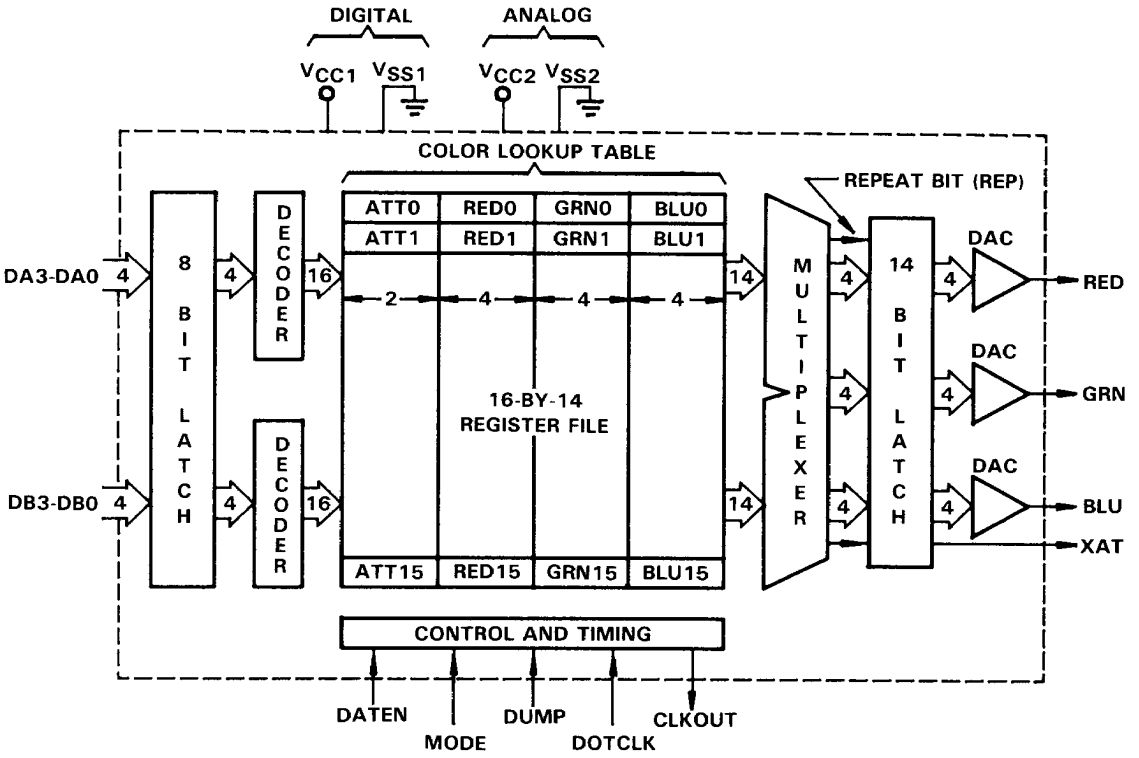
functional block diagram



pin descriptions

PIN NAME	PIN NO.	I/O	DESCRIPTION
DOTCLK	15	I	Dot Clock. The dot clock controls the rate at which analog video data is output at the analog outputs (RED, GRN and BLU) and the digital output, XAT. All on-chip timing is generated from this clock.
CLKOUT	14	O	Output Clock. The signal at pin CLKOUT is a nominal 50-percent-duty-cycle, TTL-level clock. Its frequency is half that of the input clock, DOTCLK. Data input at the DA3-DA0 and DB3-DB0 pins are latched internally at the low-to-high transition of CLKOUT. The high phase of the clock is referred to as phase A, and the low phase of the clock is referred to as phase B.
DA0-DA3	5-8	I/O	Bidirectional Data Pins, Phase A. DA0-DA3 are digitally-encoded data used to index into the color lookup table. The color value selected from the lookup table is then converted to the analog signals output on the RED, GRN and BLU pins during phase A of CLKOUT. These pins are typically used as inputs only but can be converted to outputs under control of the signal input at the DUMP pin. DA0 is the LSB.

Continued next page.

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pin descriptions (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
DB3-DB0	16-19	I/O	Bidirectional Data Pins, Phase B. DB3-DB0 are digitally-encoded data used to index into the color lookup table. The color value selected from the lookup table is then converted to the analog signals output on the RED, GRN and BLU pins during phase B of CLKOUT. These pins are typically used as inputs only but can be converted to outputs under control of the signal input at the DUMP pin. DB0 is the LSB.
DATEN	12	I	Data Transfer Enable. The DATEN input is driven active-high to indicate that a transfer of data is currently taking place at pins DA3-DA0 and DB3-DB0. DATEN must be high to enable the translation of the digital data input on DA3-DA0 and DB3-DB0 into the analog signals output at the RED, GRN and BLU pins. When DATEN is driven inactive-low, the three on-chip DACs drive the RED, GRN and BLU outputs to the voltage level corresponding to black. DATEN is specified in a manner allowing it to be conveniently driven by the composite blanking signal from an external CRT timing generator.
MODE	10	I	Select Mode of Operation. The signal input on the MODE pin configures the device to one of several modes of operation. For example, the MODE pin can be connected to the active-low vertical sync signal from an external video timing generator to enable loading of a new table of 16 colors prior to the start of each frame. Alternately, MODE is tied to ground to enable the loading of a new table prior to the display of each active scan line. Finally, MODE can be held at a logic-high level for as long as necessary to disable loading. In this last case, the set of 16 colors displayed are the values loaded into the table during the last load operation.
DUMP	11	I	Dump Enable. The DUMP signal is used to enable a dump back to memory of the color lookup table for both test and diagnostic purposes. During a dump operation, the DA3-DA0 and DB3-DB0 pins are configured as outputs rather than as inputs.
XAT	4	O	External Pixel Attribute. The XAT signal is used to enable an external function controlled by the external attribute value stored in each color register. While operating in display mode, the external attribute bit of the currently-selected register is output at the XAT pin. During times other than the active portion of each scan line, XAT is forced to the logic-low level.
RED	21	O	Red Video Signal. RED is the analog signal used to drive the amplifier controlling the red gun of an RGB video monitor.
GRN	1	O	Green Video Signal. GRN is the analog signal used to drive the amplifier controlling the green gun of an RGB video monitor.
BLU	22	O	Blue Video Signal. BLU is the analog signal used to drive the amplifer controlling the blue gun of an RGB video monitor.

Continued next page.

pin descriptions (concluded)

PIN NAME	PIN NO.	I/O	DESCRIPTION
V_{CC1}	13	I	+5-volt power supply for digital circuitry.
V_{CC2}	2	I	+5-volt power supply for analog circuitry.
V_{SS1}	3,9	I	Ground pins for digital circuitry.
V_{SS2}	20	I	Ground pin for analog circuitry.

internal registers

The color lookup table within the TMS34070 Video Palette contains 16 registers numbered 0 through 15. Each register contains 14 bits of data as shown in Figure 1. The registers are loaded from locations in the frame-buffer memory. During a load operation, the 16 registers are loaded in the order 0, 1, . . . ,15. The data is input on pins DA3-DA0 and DB3-DB0 and loaded into each register in the manner indicated in Figure 1. Two successive CLKOUT periods are required to load each register. The left half of the register, consisting of the four red bits and two attribute bits, is loaded first. The right half of the register, consisting of the four blue bits and four green bits, is loaded next, one CLKOUT period later.

Each of the sixteen 14-bit registers contains two attribute bits in addition to the 12 bits of color information. Each color register contains a REP bit. When one of the 16 color registers is displayed, its REP bit controls the latching of its 12 color bits at the inputs to the three 4-bit DACs. If REP is zero, the register's content replaces the old values latched at the DAC inputs. If REP is one, latching is disabled for one dot clock period, and the color output during the preceding pixel is repeated. Immediately following a blanking interval, the content of the latches at the DAC inputs is undefined. A repeat color command occurring in the first pixel of a new line will result in an undefined color.

Each color register also contains an EXT bit. When any one of the 16 color registers is displayed, the value of its EXT bit is output at the XAT pin. If the EXT bit in the selected color register is one, the XAT pin is driven to the logic-high level. If the EXT bit in the register is zero, the next XAT pin is driven to the logic low-level. This bit is useful for controlling devices external to the TMS34070.

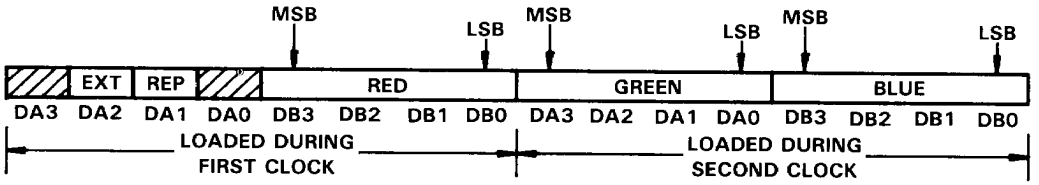

FIGURE 1. COLOR LOOKUP TABLE REGISTER

interface operation

The TMS34070 loads its color lookup table directly from the frame-buffer memory. The loading is performed automatically, without processor intervention, according to one of several programmable modes.

The TMS34070 supports several methods of loading the color lookup table to accommodate the system needs of various applications. Also provided is the ability to dump (output) the contents of the color lookup table for diagnostic purposes. Four typical methods of operation are listed in Table 1.

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TABLE 1. TYPICAL METHODS OF OPERATION

METHOD	DESCRIPTION
Frame-Load	Load table from video memory prior to start of each frame.
Command-Load	Do not load table except when an explicit load command is given.
Line-Load	Load table from video memory prior to start of each individual scan line.
Dump	Output contents of table to memory during a selected scan line.

The TMS34070 is easily configured to support the frame-load and line-load methods of operation without additional logic. Frame-load operation is configured as follows:

1. Connect DATEN to active-low blanking signal from external CRT timing generator.
2. Connect MODE to active-low vertical sync signal.
3. Strap DUMP to ground.

Line-load operation is configured as follows:

1. Connect DATEN to active-low blanking signal.
2. Strap both MODE and DUMP to ground.

While a load is in progress, the TMS34070 automatically blanks the screen to avoid the display of spurious data. The designer can also generate logic to control the MODE signal providing a load operation that can be enabled by the user as required.

During a dump operation the contents of the color lookup table are dumped back to memory. This operation is primarily used for system diagnostics. The following sequence of events occurs during a dump operation:

1. During the first nine clocks (CLKOUT periods) following the DATEN rising edge, DA3-DA0 and DB3-DB0 remain in high impedance.
2. During the next 64 clocks, the contents of the 16 color registers are output to DA3-DA0 and DB3-DB0.
3. Thereafter, DA3-DA0 and DB3-DB0 are driven to high impedance until the next low-to-high transition of DATEN.

Four clocks are required to output each of the 16 registers during the dump operation. Register 0 is the first to be output and register 15 is the last. An internal 4-bit counter points to the register currently being output and is incremented once every four clocks through the sequence 0,1 . . . ,15. A total of 64 clocks is required to complete the dump of all 16 registers in the color lookup table.

DAC functional characteristics

The functional characteristics of the DACs that drive the analog RED, GRN, and BLU outputs are summarized in Table 2.

TABLE 2. DAC FUNCTIONAL CHARACTERISTICS

PARAMETER	VALUE
Analog outputs DAC resolution	4 bits
Palette colors	4096 colors
Dynamic characteristics of each analog output:	
Update rate†	66.67 MHz
Data inputs:	
Compatibility	TTL
Coding	Binary

†Due to internal multiplexing, the rate at which the analog outputs can be updated is twice the frequency of the output clock (CLKOUT).

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Off-state output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to network ground terminal V_{SS1} for V_{CC1} and V_{SS2} for V_{CC2}. V_{SS1} and V_{SS2} must be tied to the same potential to ensure proper operation and device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	All inputs except DOTCLK	2		$V_{CC1}+0.5$	V
		DOTCLK	2.4		$V_{CC1}+0.5$	V
V_{IL}	Low-level input voltage	All inputs except DOTCLK	0		0.8	V
		DOTCLK	0		0.6	V
V_{CC1}	Supply voltage (digital circuitry)		4.75	5	5.25	V
V_{CC2}	Supply voltage (analog circuitry)†		4.75	5	5.25	V
V_{SS1}	Supply voltage (digital circuitry)‡			0		V
V_{SS2}	Supply voltage (analog circuitry)‡			0		V
I_{OH}	High-level output current (TTL)				−400	μA
I_{OL}	Low-level output current (TTL)				2	mA
T_A	Operating free-air temperature		0		70	°C

†Voltage levels at DAC outputs vary directly in proportion to variations in V_{CC2} from the nominal 5-V power supply level.
‡All voltage values are measured with respect to V_{SS1} and V_{SS2}, which are tied together during test.

electrical characteristics over recommended free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = max	2.4	3.2		V
V_{OL}	Low-level output voltage		I_{OL} = max		0.2	0.6	V
I_{OZH}	Off-state output current with high-level voltage applied	DA3-DA0 and DB3-DB0	V_O = 2.4 V		1	100	μA
I_{OZL}	Off-state output current with low-level voltage applied	DA3-DA0 and DB3-DB0	V_O = 0.6 V		−1	−100	μA
I_{IH}	High-level input current	All inputs except DOTCLK	V_I = 5.25 V, All other pins at 0 V			10	μA
		DOTCLK				100	μA
I_{IL}	Low-level input current	All inputs except DOTCLK	V_I = 0 V, All other pins at 0 V			−10	μA
		DOTCLK				−100	μA
I_{CC}†	Average supply current from V_{CC1} and V_{CC2}	Continuous black levels output at analog pins	R_L = 75 Ω, V_{CC1} = 5.25 V, V_{CC2} = 5.25 V, $t_{c(DC)}$ = 15 ns		130	195	mA
		Continuous white levels output at analog pins			210	275	mA
C_I	Input capacitance	Data inputs			15‡		pF
		All other inputs			7‡		pF
C_O	Output capacitance	Data outputs			15‡		pF
		XAT			15‡		pF
		Analog outputs			14‡		pF
R_O	Output resistance at analog outputs		R_L = 75 Ω, V_{CC2} = 5 V		25§		Ω
V_{WHITE}	Voltage level of analog video outputs		R_L = 75 Ω, V_{CC2} = 5 V	1.95	2.3	2.65	V
V_{BLACK}	Voltage level of video analog outputs		R_L = 75 Ω, V_{CC2} = 5 V	0.35	0.65	0.95	V
$V_{WHITE} - V_{BLACK}$	Voltage output difference for analog video outputs		R_L = 75 Ω, V_{CC2} = 5 V	1.45	1.65	1.85	V
$\left\lvert \frac{V_{(n)} - V_{(n-1)}}{V_{WHITE} - V_{BLACK}} - \frac{1}{15} \right\rvert$	Monotonicity of any analog output measured for any 2 successive digital codes, n − 1 and n, from 0 to 15		R_L = 75 Ω, V_{CC2} = 5 V			0.033	
$\left\lvert \frac{2\,(V_{BLACK1} - V_{BLACK2})}{(V_{WHITE1} - V_{BLACK1}) + (V_{WHITE2} - V_{BLACK2})} \right\rvert$	Difference between black levels for any pair of analog outputs, 1 and 2		R_L = 75 Ω, V_{CC2} = 5 V			0.033	
$\left\lvert \frac{2\,(V_{WHITE1} - V_{WHITE2})}{(V_{WHITE1} - V_{BLACK1}) + (V_{WHITE2} - V_{BLACK2})} \right\rvert$	Difference between white levels for any pair of analog outputs, 1 and 2		R_L = 75 Ω, V_{CC2} = 5 V			0.033	
$\left\lvert \frac{2[(V_{WHITE1} - V_{BLACK1}) - (V_{WHITE2} - V_{BLACK2})]}{(V_{WHITE1} - V_{BLACK1}) + (V_{WHITE2} - V_{BLACK2})} \right\rvert$	Difference in black-to-white voltage ranges for any pair of analog outputs, 1 and 2		R_L = 75 Ω, V_{CC2} = 5 V			0.033	

†I_{CC} includes current shunted to loads at analog outputs.
‡These values are based on a sample characterization.
§This value is based on computer simulation.

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interface timing parameters

PARAMETER		MIN	MAX	UNIT
$t_{c(DC)}$	Period of DOTCLK input	15	200	ns
$t_{c(CO)}$	Period of CLKOUT output	$2t_{c(DC)}$		ns
$t_{d(COH-RGB)}$	Delay from CLKOUT high to stable analog data (Note 2)		25	ns
$t_{d(COL-RGB)}$	Delay from CLKOUT low to stable analog data (Note 2)		25	ns
$t_{d(COH-DV)}$	Delay from CLKOUT high to valid data output, dump operation		45	ns
$t_{d(COH-DZ)}$	Delay from CLKOUT high to data high impedance, end of dump		25†	ns
$t_{d(COH-XV)}$	Delay from CLKOUT high to valid XAT output (Note 3)		50	ns
$t_{d(COL-XV)}$	Delay from CLKOUT low to valid XAT output (Note 3)		50	ns
$t_{d(DC-OC)}$	Delay from DOTCLK high to CLKOUT high or low		35	ns
$t_{d(RGB-RGB)}$	Delay from RED, GRN, or BLU no longer stable to RED, GRN, and BLU again stable		7.5	ns
$t_{f(A)}$	Fall time of analog outputs		7.5	ns
$t_{h(COH-RGB)}$	Hold time of stable analog data after CLKOUT no longer high (Note 2)	0†		ns
$t_{h(COL-RGB)}$	Hold time of stable analog data after CLKOUT no longer low (Note 2)	0†		ns
$t_{h(COH-DE)}$	Hold time of valid DATEN input after CLKOUT high	0†		ns
$t_{h(COH-DU)}$	Hold time of valid DUMP input after CLKOUT high	0†		ns
$t_{h(COH-MO)}$	Hold time of valid MODE input after CLKOUT high	0†		ns
$t_{h(COH-DI)}$	Hold time of valid input data after CLKOUT high, load or display operation	0†		ns
$t_{h(COH-XV)}$	Hold time of valid XAT output after CLKOUT no longer high	0		ns
$t_{h(COL-DV)}$	Hold time of valid data input after CLKOUT no longer low, dump operation	3		ns
$t_{h(COL-DZ)}$	Hold time of data high impedance after CLKOUT no longer low, start of dump operation	0†		ns
$t_{h(COL-XV)}$	Hold time of valid XAT output after CLKOUT no longer low	0		ns
$t_{h(DC-OC)}$	Hold time of CLKOUT high or low after DOTCLK no longer low	0		ns
$t_{h(DEH-DU)}$	Hold time of DUMP input after DATEN high, asynchronous timing requirement	$t_{c(CO)} + 25$		ns
$t_{h(DEH-MO)}$	Hold time of MODE input after DATEN high, asynchronous timing requirement	$t_{c(CO)} + 25$		ns
$t_{h(DEL-MOH)}$	Hold time of MODE high after DATEN low, asynchronous timing, load and blank entire line	0		ns
$t_{r(A)}$	Rise time of analog outputs		7.5	ns
$t_{su(DE-COL)}$	Setup time of valid DATEN input to CLKOUT no longer low	13.5		ns
$t_{su(DU-COL)}$	Setup time of valid DUMP input to CLKOUT no longer low	13.5		ns
$t_{su(MO-COL)}$	Setup time of valid MODE input to CLKOUT no longer low	13.5		ns
$t_{su(MO-DEL)}$	Setup time of valid MODE input to DATEN no longer low, asynchronous timing requirement	0		ns
$t_{su(DU-DEL)}$	Setup time of valid DUMP input to DATEN no longer low, asynchronous timing requirement	0		ns
$t_{su(DI-COL)}$	Setup time of valid input data to CLKOUT no longer low, load or display operation	13.5		ns

Continued next page.

NOTES: 2. Analog outputs are termed stable when they are within 10% of their final value.
3. At DOTCLK periods <62ns, XAT may not be valid before the next DOTCLK edge.
4. Variations from the ideal 75 Ω analog load resistors due to resistor tolerance can cause small deviations in the voltage levels at the RED, BLUE, and GREEN analog outputs. When 5% tolerance resistors are incorporated, the white level varies by approximately ⅛ LSB with respect to the black level. This data is provided for the designer's information and is not tested.

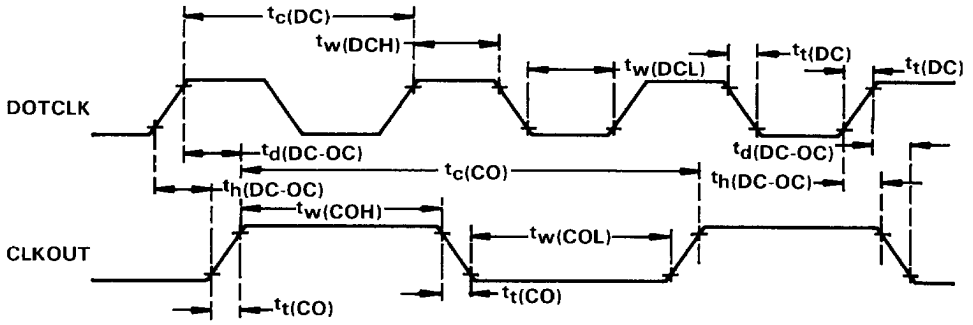
†These values were derived from characterization and are not tested.

interface timing parameters (concluded)

PARAMETER		MIN	MAX	UNIT
$t_{t(CO)}$	Transition time (rise or fall) of CLKOUT output		5	ns
$t_{t(DC)}$	Transition time (rise or fall) of DOTCLK input		5‡	ns
$t_{w(COH)}$	Pulse duration of CLKOUT high	$t_{c(DC)}$ – 9		ns
$t_{w(COL)}$	Pulse duration of CLKOUT low	$t_{c(DC)}$ – 6		ns
$t_{w(DCH)}$	Pulse duration of DOTCKL high	4		ns
$t_{w(DCL)}$	Pulse duration of DOTCLK low	4		ns
$t_{w(MOL)}$	Pulse duration of MODE low, asynchronous timing, load and blank entire line	$t_{c(CO)}$ + 15		ns

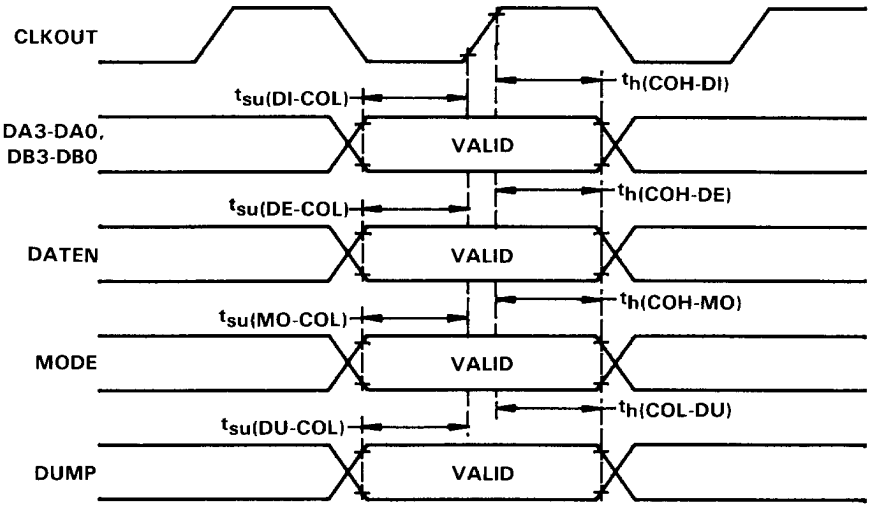
‡Due to tester limitations, this parameter can not be checked at test. Value is based on computer simulation.

timing for input and output clocks



NOTE 5: Measurement points for DOTCLK input are 0.6 and 2.4 volts. Measurement points for all other digital signals are 0.8 and 2.0 volts.

digital input timing



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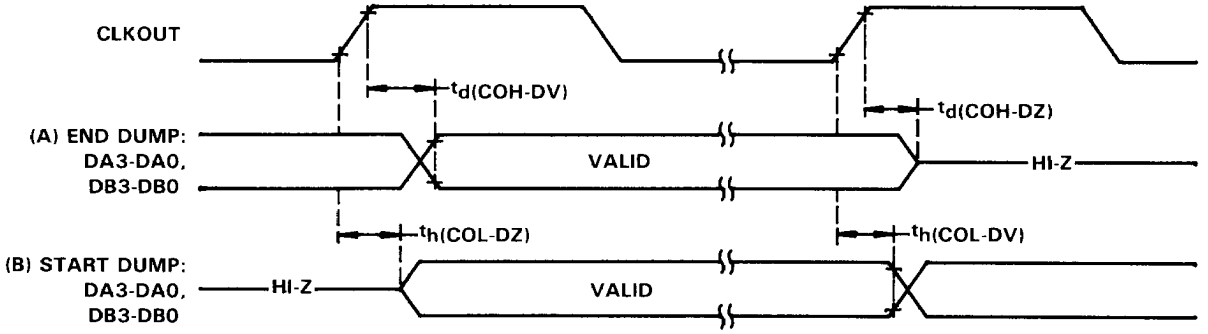
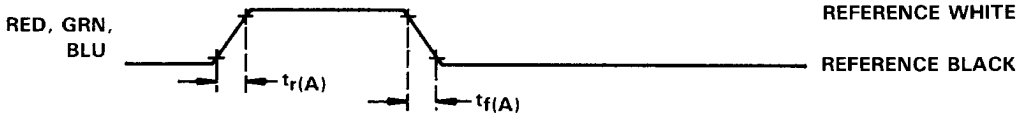
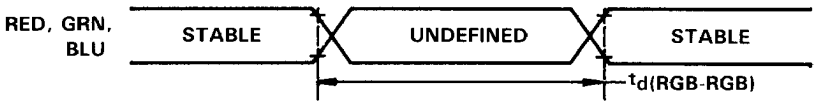
digital data output timing



analog output transition timing



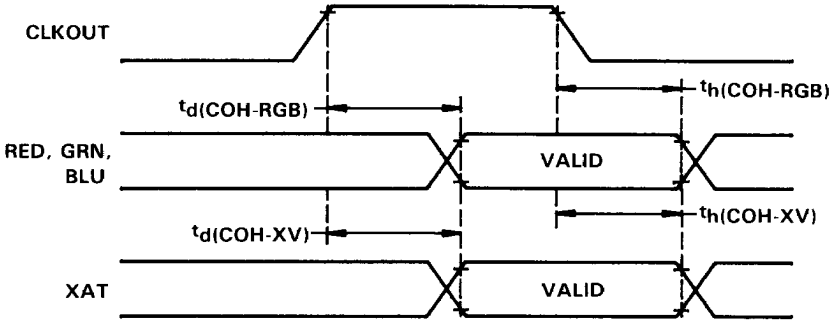
(a) RISE AND FALL TIMES FOR AN INDIVIDUAL ANALOG OUTPUT



NOTE 6: Measurement points for analog output transitions are at 10% and 90% of the interval from the starting level to the final level.

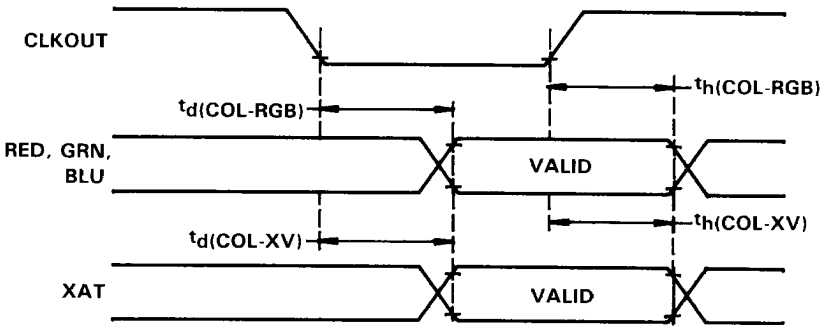
(b) TRANSITION OF ALL ANALOG OUTPUTS

video output delay timing



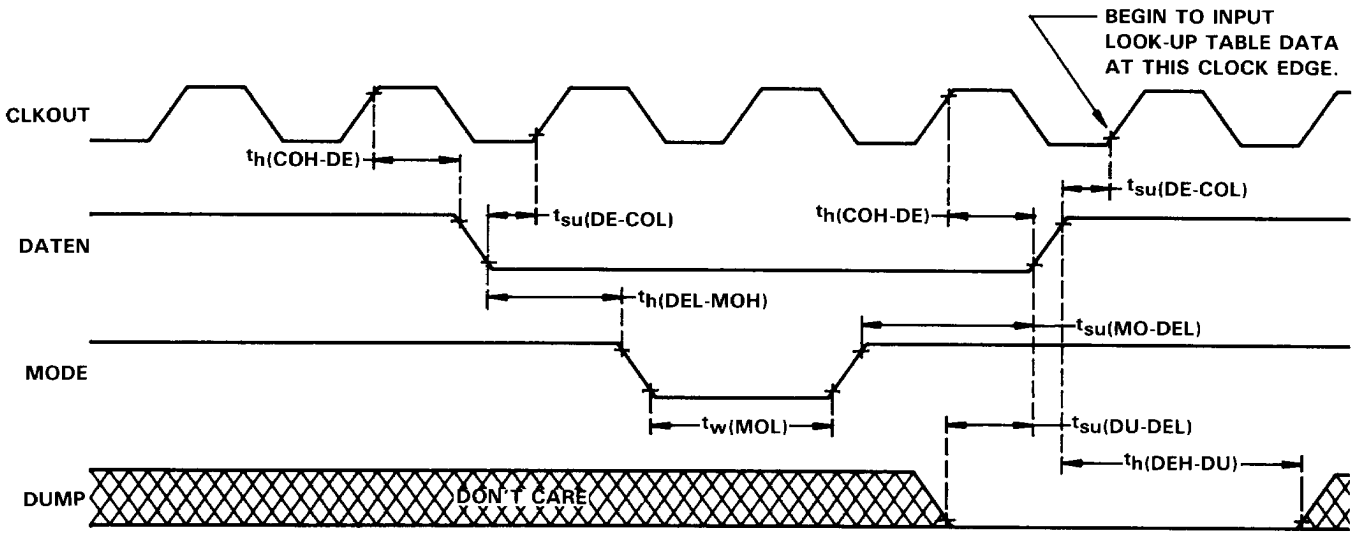
(a) PHASE A VIDEO OUTPUTS

video output delay timing (concluded)



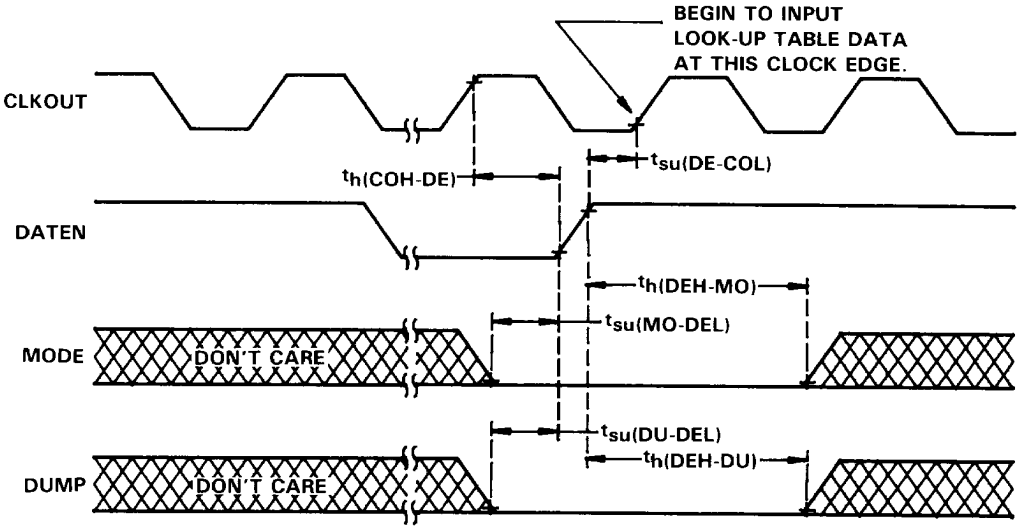
(b) PHASE B VIDEO OUTPUTS

asychronous control inputs

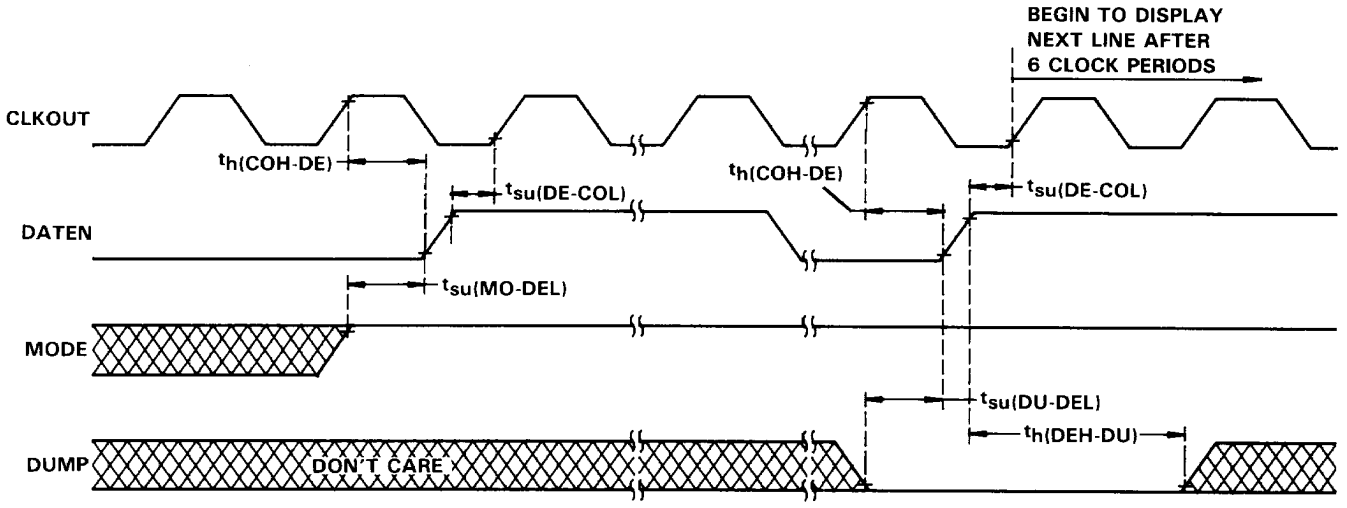


(a) PERFORM LOAD: BLANK ENTIRE LINE

asychronous control inputs (continued)

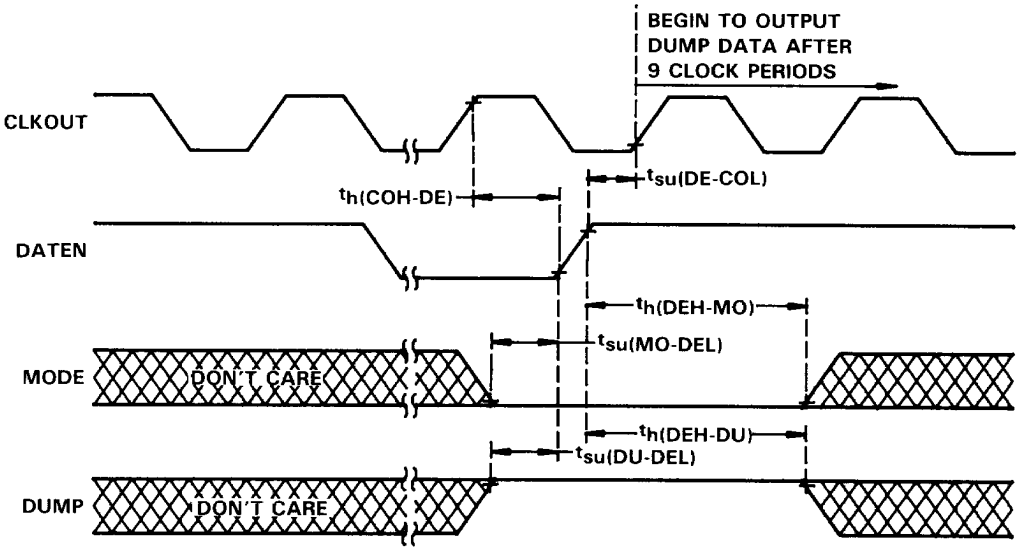


(b) PERFORM LOAD: DISPLAY REMAINDER OF LINE



(c) DISPLAY ENTIRE LINE (NO LOAD)

asynchronous control inputs (concluded)



(d) DUMP OPERATION

NOTES: 7. High-to-low and low-to-high transitions of the MODE and DUMP inputs are permitted to be asynchronous to CLKOUT as long as the timing requirements relating MODE and DUMP to DATEN transitions are met. In other words, MODE and DUMP transitions can occur at any time relative to CLKOUT, including during a CLKOUT low-to-high transition, as long as the setup and hold requirements with respect to DATEN transitions are met.

8. Asynchronous timing requirements for MODE and DUMP are given in terms of the CLKOUT cycle time, $t_{c(CO)}$.

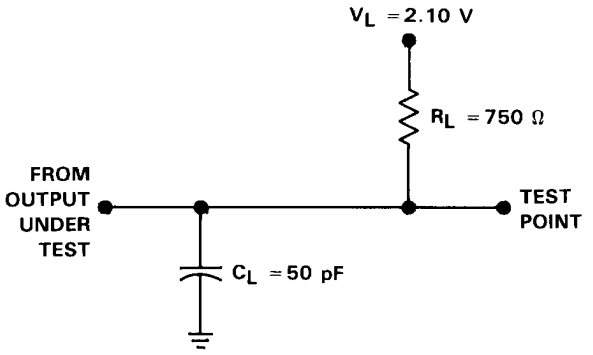


FIGURE 2. TEST LOAD CIRCUIT—DIGITAL OUTPUTS

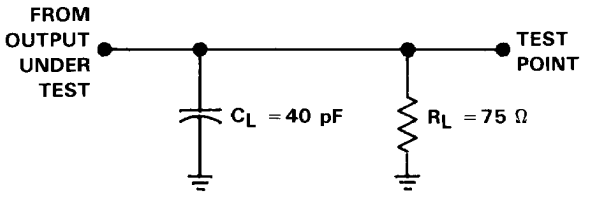


FIGURE 3. TEST LOAD CIRCUIT—ANALOG OUTPUTS

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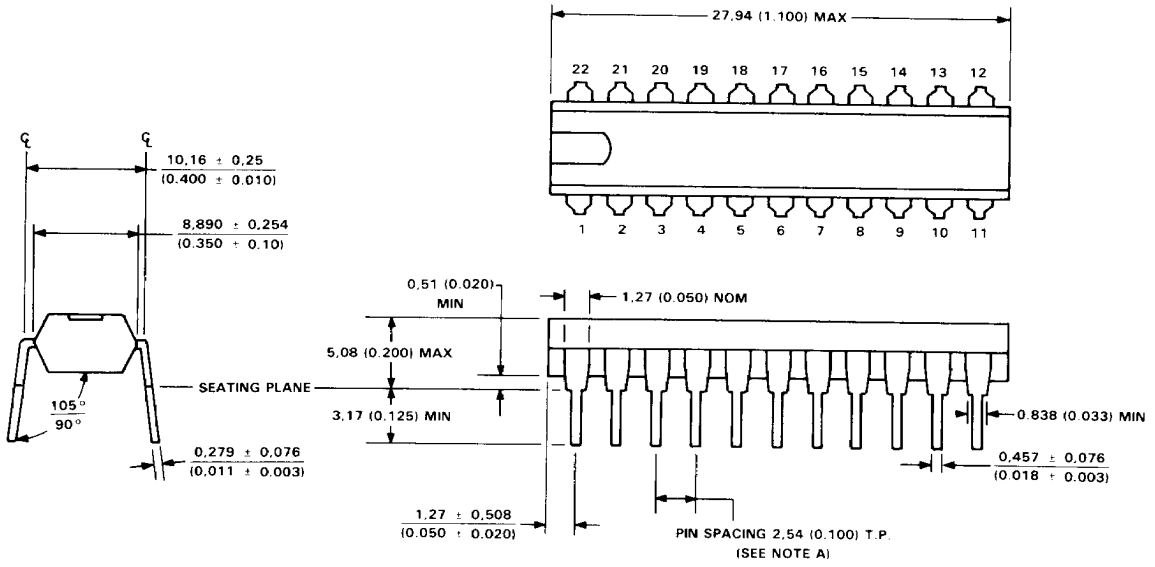
MECHANICAL DATA

22-pin N dual-in-line package



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.