S6D0110

Preliminary

132 RGB Source & 176 Gate Driver With Internal GRAM
FOR 65,536 Colors TFT-LCD

July 9, 2002

Ver. 0.4

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S6D0110 Specification Revision History			
Version	**Content**	**Author**	**Date**
0.0	Original	G. H. Jung	March 16 , 2002
0.1	Modified descriptions for operating voltage. (page 4) Modified figure for pad configuration. (page 6) Added descriptions for IM2-0 pin mode setting. (page 10) Added descriptions for /RD pin. (page 10) Modified table for register selection. (page 12) Added table for GRAM address. (page 17-18) Modified table for Instruction. (page 20) Modified descriptions for R00h. (page 22) Added descriptions for SM bit in R01h. (page 23) Modified descriptions for BT2-0 bits in R03h. (page 26) Modified descriptions for CAD bit in R04h. (page 28) Modified descriptions for VDV4-0 bits in R0Eh. (page 30) Added descriptions for R08h, R09h. (page 36) Modified figure for window address setting range. (page 41) Modified table for GRAM data and grayscale level. (page 43) Modified figure for voltage regulation function. (page 47) Added descriptions and table for system interface.(page 48) Modified figure for high-speed RAM write in window address range. (page 56) Added descriptions and figure for gate driver scan mode setting. (page 69) Modified figure for setup procedure of 8color display mode.(page 83) Modified figure for instruction setup flow. (page 85-86) Modified figure for interlaced drive. (page 89) Modified descriptions for restriction on the 1st/2nd screen driving position register setting. (page 93)	M. S. Song	April 1 , 2002
0.2	Modified descriptions for introduction. (page 3) Modified descriptions for Features. (page 4) Modified figure for block diagram. (page 5) Modified figure for pad configuration. (page 6) Added table for pad dimension. (page 7) Added figure for align key configuration and its coordinate. (page 8-9) Added table for pad center coordinates. (page 10-13) Modified and Added descriptions for pin description. (page 14-18) Modified descriptions for power supply circuit. (page 21) Modified figure for voltage setting. (page 22) Added figure for application circuit. (page 102)	M. S. Song	April 12 , 2002
0.3	Modified table for pad dimension. (page 7) Added table for blanking period setting. (page 43) Modified descriptions for reset function. (page 53)	M. S. Song	April 30 , 2002
0.4	Modified descriptions for VC2-0 and VRL3-0 bit. (page 36) Added descriptions and table contents for BGR bit. (page 39-40)	M. S. Song	July 9, 2002

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INTRODUCTION

The S6D0110 is 1-chip solution for TFT-LCD panel: source driver with built-in memory, gate driver, power IC are integrated on one chip. This IC can display to a maximum of 132-RGB x 176-dot graphics on 65k-color TFT panel.

The S6D0110 also supports bit-operation functions, 8/16-bit high-speed bus interface, and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the internal GRAM.

The moving picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively so that moving picture is able to displayed simultaneously independent of still picture area.

The S6D0110 has various functions for reducing the power consumption of a LCD system: It operates at low voltage (minimum 1.8V) and the IC has an internal GRAM to store 132-RGB x 176-dot 65k-color image. In addition, it has the internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

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FEATURES

132-RGB x 176-dot TFT-LCD display controller/driver IC for 65,536 colors (396ch-source driver/176ch-gate driver)

16-/8-bit high-speed bus interface and serial peripheral interface (SPI)

High-speed burst-RAM write function

Writing to a window-RAM address area by using a window-address function

Bit-operation functions for graphic processing

- Write-data mask functions in bit units
- Logical operation in pixel unit and conditional write function

Various color-display control functions

- 65,536 colors can be displayed at the same time (gamma adjust included)
- Vertical scroll display function in raster-row units

Internal RAM capacity: 132 x 16 x 176 = 371,712 bits

Low-power operation supports:

- Power-save functions such as the standby mode and sleep mode
- Partial LCD drive of two screens in any position
- Maximum 12-times step-up circuit for liquid crystal drive voltage
- Voltage followers to decrease direct current flow in the LCD drive breeder-resistors
- Equalizing function for the switching performance of step-up circuits and operational amplifiers

N-raster row inversion drive (Reverse the polarity of driving voltage in every selected raster row is possible)

Internal oscillation and hardware reset

Structure for TFT-display retention volume (Cst/Cadd structure)

Alternating functions for TFT-display counter-electrode power supply

- N-line alternating drive of Vcom (Vgoff is also available for N-line alternating drive for Cadd)

Internal power supply circuit

- Step-up circuit: five to nine times, positive-polarity inversion
- Adjustment of Vcom(Vgoff) amplitude: internal 22-level digital potentiometer

Operating voltage

- Applying voltage
  - VDD to VSS = 1.8 to 2.5 V (non-regulating) (logic voltage range – non-regulated)
    VDD3 to VSS = 2.3 to 3.3 V (regulating) (logic voltage range – regulated)
  - Vci to VSS = 2.5 to 3.3 V (internal reference power-supply voltage)
  - Vci1 to VSS = 1.7 to 2.75 V (2.5 x 0.68 ~ 2.75) (power supply for step-up circuits)
- Generating voltage
  - For the source driver: AVDD to VSS = 3.5 to 5.5V (power supply for liquid crystal output circuits)
    GVDD to VSS = 3.0 to 5.0V (reference power supply for grayscale voltages)
  - For the gate driver: VGH to VGL = 14 to 30 V, VGH to VSS = +7.0 to +20 V,
    VgoffL = (VGL+0.5) to –7.5V, VgoffH = ~ to -1.5V
  - For the TFT-display counter electrode: Vcom amplitude(max) = 6V, VcomH to VSS(max) = GVDD
    VcomL to VSS(max) = 1.0 V to -Vci + 0.5 V

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BLOCK DIAGRAM

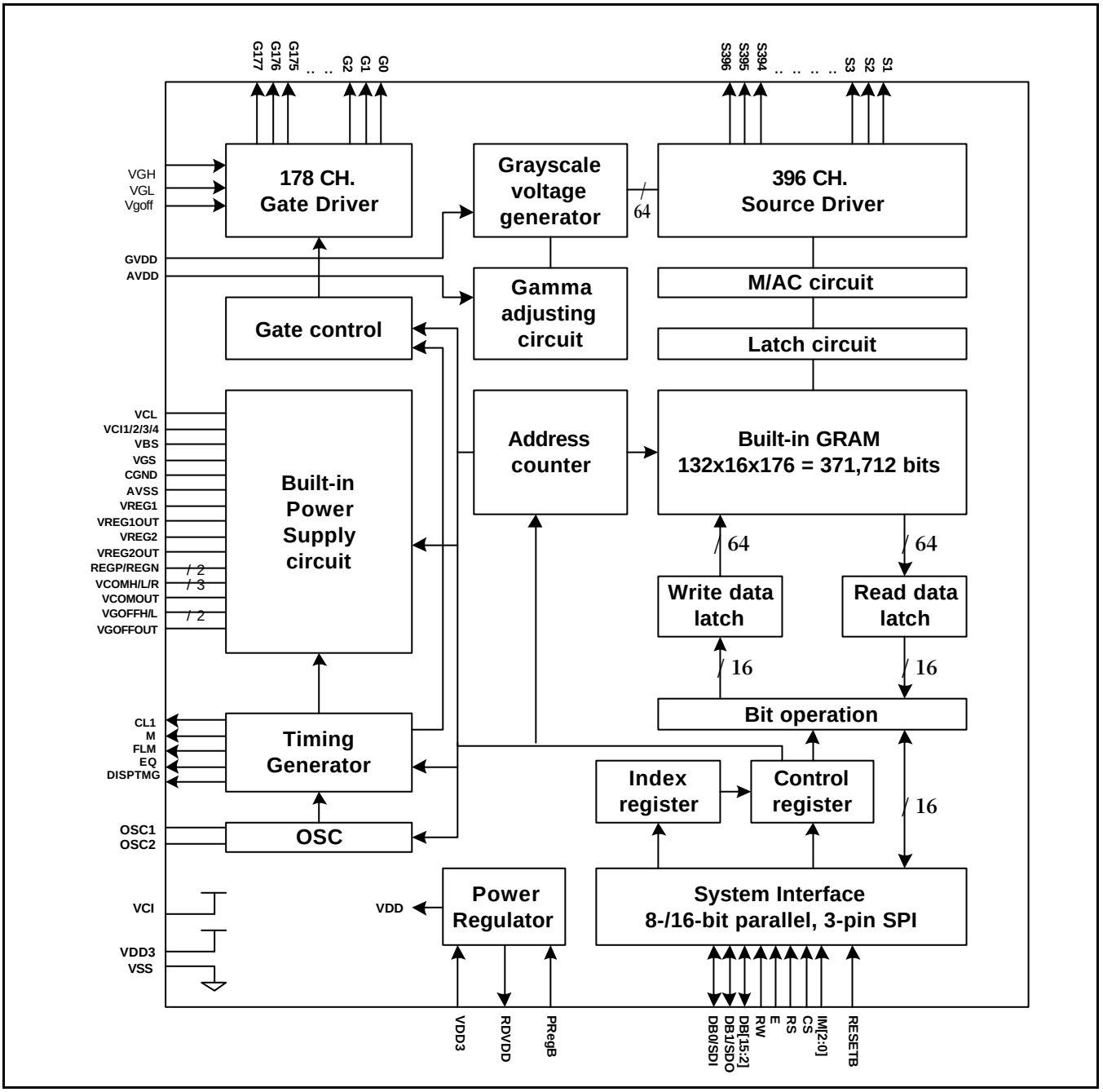

Figure 1. Block Diagram

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PAD CONFIGURATION

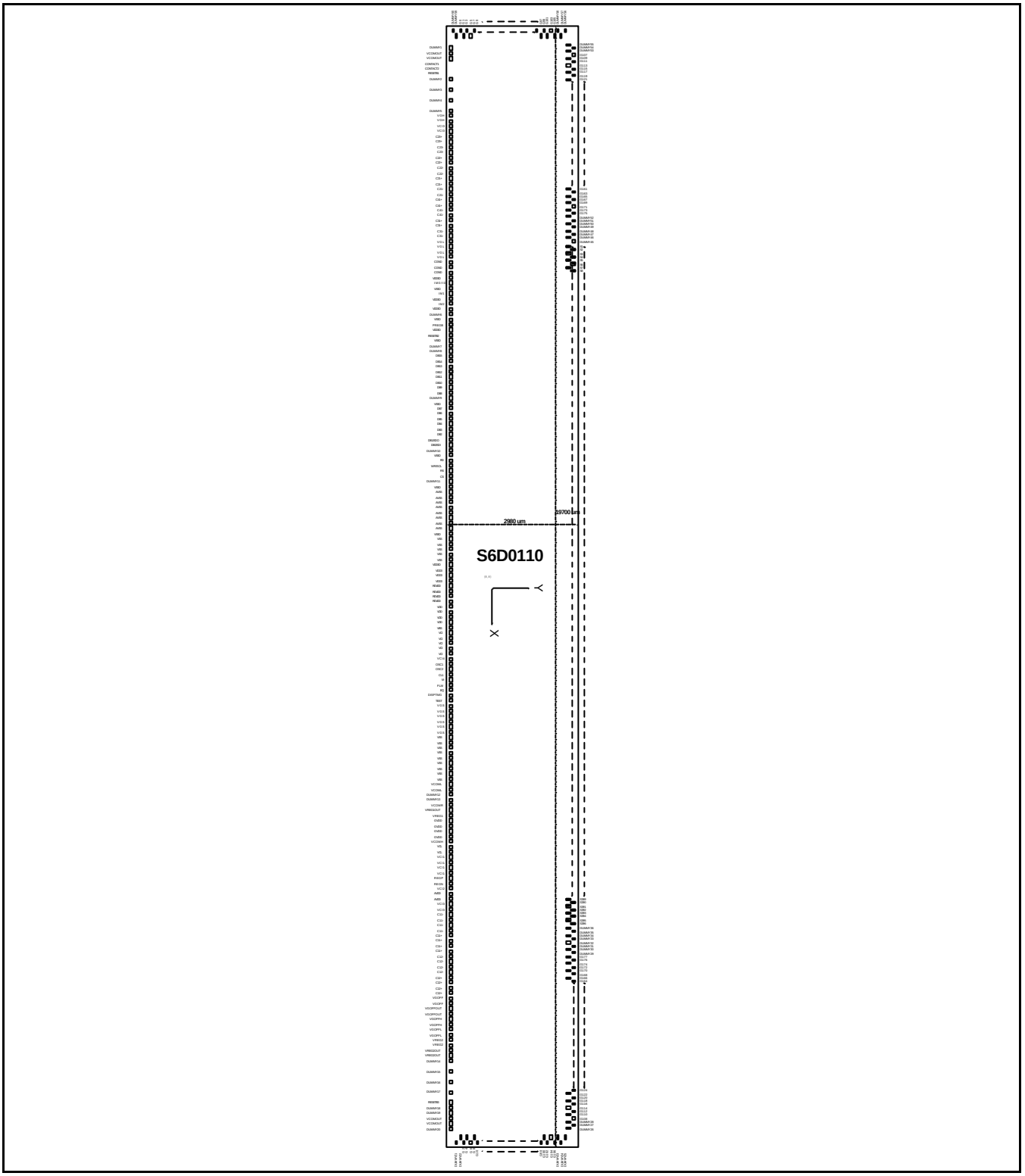

Figure 2. Pad Configuration

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Table 1. S6D0110 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size[1)]	-	19580	2860	um
Pad size	INPUT PAD	54	100	
	OUTPUT PAD	36	70	

NOTES:

1. Scribe line is not included in this chip size (Scribe line: 120um)

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ALIGN KEY CONFIGURATION AND COORDINATE

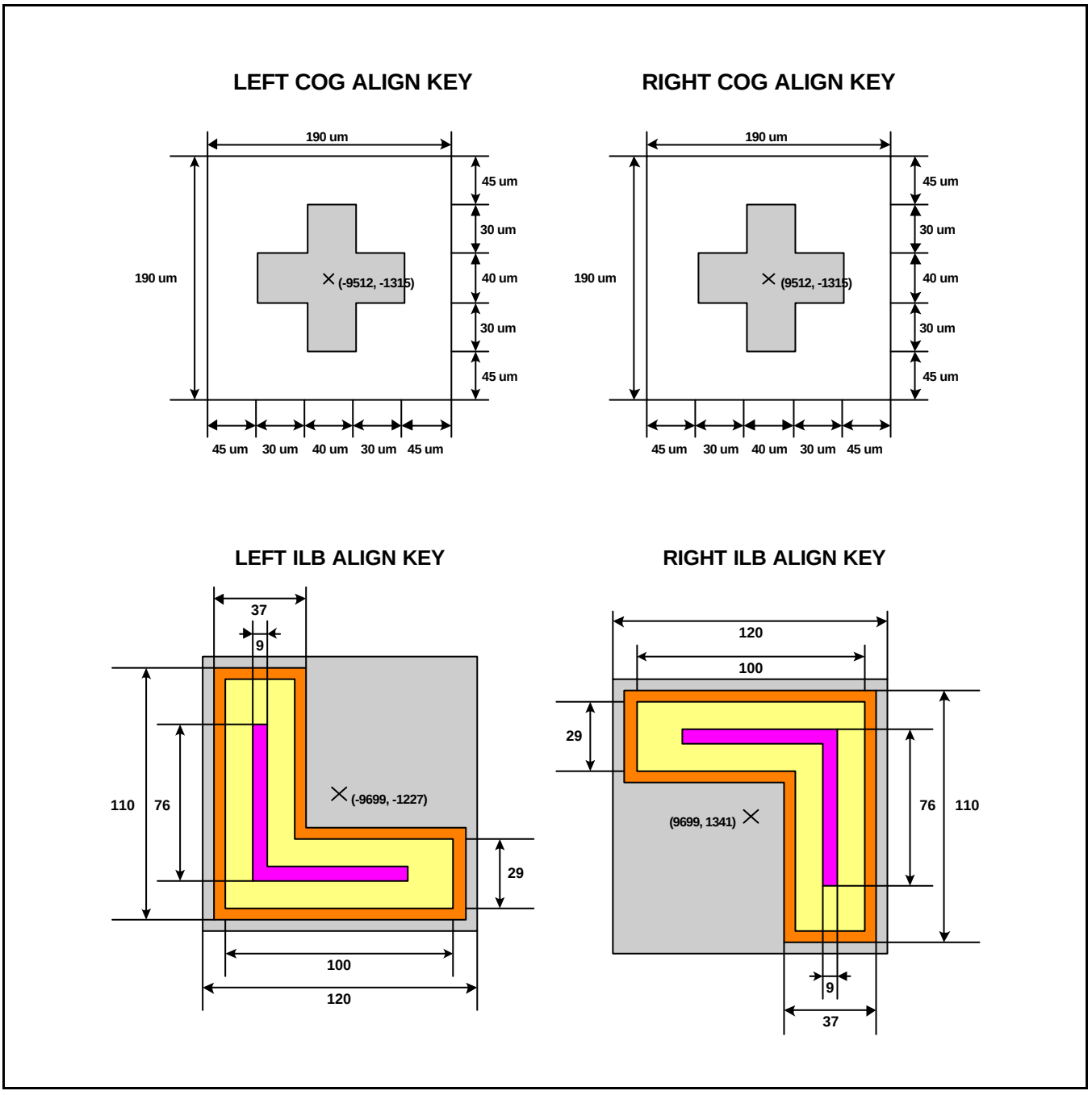

Figure 3. COG and ILB align key

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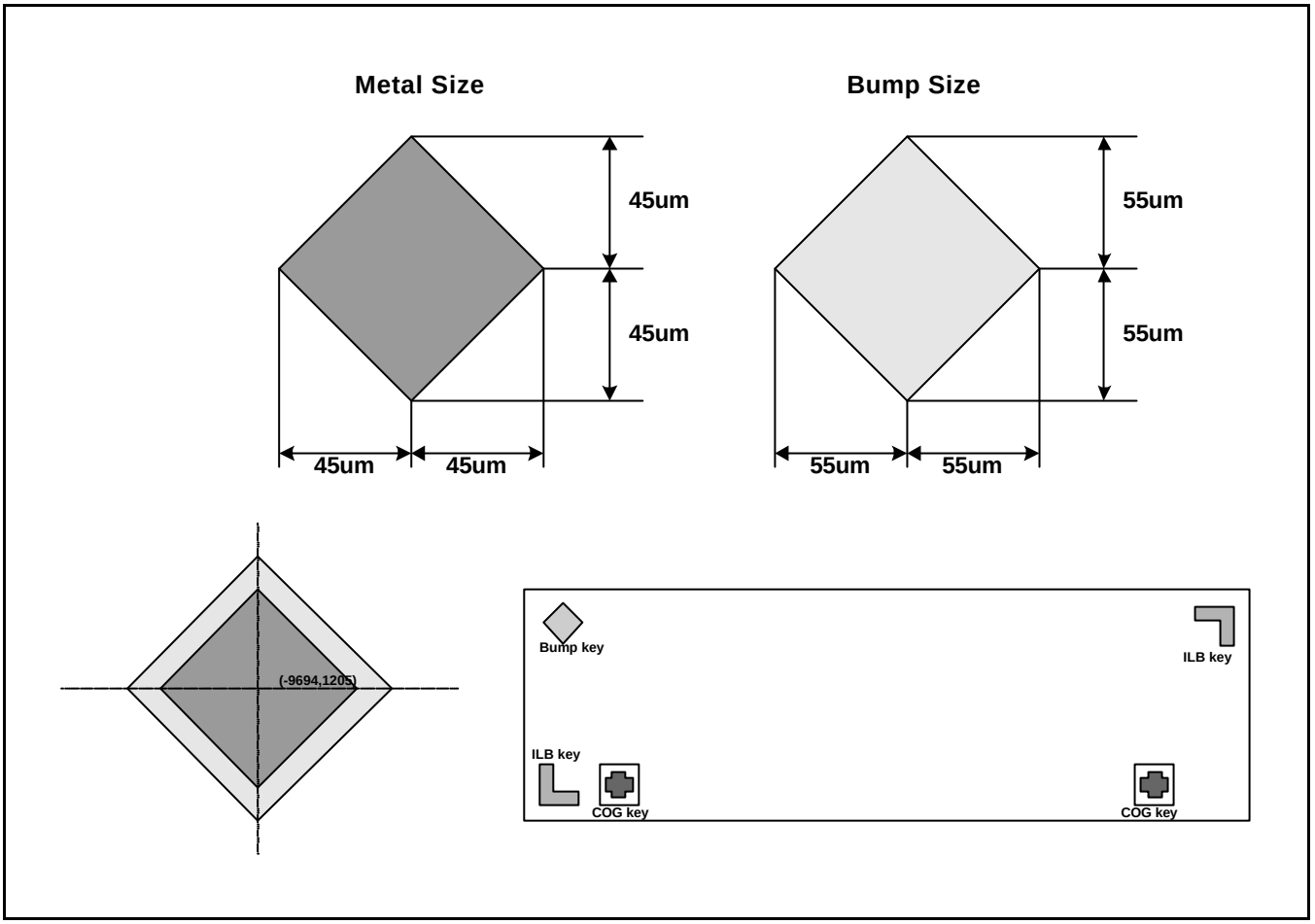

Figure 4. Bump align key and align key configuration

NOTES:

2. Gold bump height: 15um(typ.)
2. Wafer thickness: 470um

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PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: um]

NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y
1	DUMMY<1>	-9360	-1356	61	DB<11>	-3200	-1356	121	EQ	1600	-1356	181	VGOFF	6400	-1356
2	VCOMOUT	-9280	-1356	62	DB<10>	-3120	-1356	122	DISPTMG	1680	-1356	182	VGOFFOUT	6480	-1356
3	VCOMOUT	-9200	-1356	63	DB<9>	-3040	-1356	123	TEST	1760	-1356	183	VGOFFOUT	6560	-1356
4	CONTACT1	-9120	-1356	64	DB<8>	-2960	-1356	124	VGS	1840	-1356	184	VGOFFH	6640	-1356
5	CONTACT2	-9040	-1356	65	DUMMY<9>	-2880	-1356	125	VGS	1920	-1356	185	VGOFFH	6720	-1356
6	RESETB1	-8960	-1356	66	VSSO	-2800	-1356	126	VGS	2000	-1356	186	VGOFFL	6800	-1356
7	DUMMY<2>	-8880	-1356	67	DB<7>	-2720	-1356	127	VGS	2080	-1356	187	VGOFFL	6880	-1356
8	DUMMY<3>	-8280	-1356	68	DB<6>	-2640	-1356	128	VGS	2160	-1356	188	VREG2	6960	-1356
9	DUMMY<4>	-7780	-1356	69	DB<5>	-2560	-1356	129	VGS	2240	-1356	189	VREG2	7040	-1356
10	DUMMY<5>	-7280	-1356	70	DB<4>	-2480	-1356	130	VSS	2320	-1356	190	VREG2OUT	7120	-1356
11	VGH	-7200	-1356	71	DB<3>	-2400	-1356	131	VSS	2400	-1356	191	VREG2OUT	7200	-1356
12	VGH	-7120	-1356	72	DB<2>	-2320	-1356	132	VSS	2480	-1356	192	DUMMY<14>	7280	-1356
13	VCI3	-7040	-1356	73	DB1/SDO	-2240	-1356	133	VSS	2560	-1356	193	DUMMY<15>	7780	-1356
14	VCI3	-6960	-1356	74	DB0/SDI	-2160	-1356	134	VSS	2640	-1356	194	DUMMY<16>	8280	-1356
15	C23+	-6880	-1356	75	DUMMY<10>	-2080	-1356	135	VSS	2720	-1356	195	DUMMY<17>	8880	-1356
16	C23+	-6800	-1356	76	VSSO	-2000	-1356	136	VSS	2800	-1356	196	RESETB3	8960	-1356
17	C23-	-6720	-1356	77	R/W	-1920	-1356	137	VSS	2880	-1356	197	DUMMY<18>	9040	-1356
18	C23-	-6640	-1356	78	E	-1840	-1356	138	VSS	2960	-1356	198	DUMMY<19>	9120	-1356
19	C22+	-6560	-1356	79	RS	-1760	-1356	139	VCOML	3040	-1356	199	VCOMOUT	9200	-1356
20	C22+	-6480	-1356	80	CSB	-1680	-1356	140	VCOML	3120	-1356	200	VCOMOUT	9280	-1356
21	C22-	-6400	-1356	81	DUMMY<11>	-1600	-1356	141	DUMMY<12>	3200	-1356	201	DUMMY<20>	9360	-1356
22	C22-	-6320	-1356	82	VSSO	-1520	-1356	142	DUMMY<13>	3280	-1356	202	DUMMY<21>	9720	-1078
23	C21+	-6240	-1356	83	AVSS	-1440	-1356	143	VCOMR	3360	-1356	203	DUMMY<22>	9610	-1040
24	C21+	-6160	-1356	84	AVSS	-1360	-1356	144	VREG1OUT	3440	-1356	204	G<2>	9720	-1002
25	C21-	-6080	-1356	85	AVSS	-1280	-1356	145	VREG1	3520	-1356	205	G<4>	9610	-964
26	C21-	-6000	-1356	86	AVSS	-1200	-1356	146	GVDD	3600	-1356	206	G<6>	9720	-926
27	C41+	-5920	-1356	87	AVSS	-1120	-1356	147	GVDD	3680	-1356	207	G<8>	9610	-888
28	C41+	-5840	-1356	88	AVSS	-1040	-1356	148	GVDD	3760	-1356	208	G<10>	9720	-850
29	C41-	-5760	-1356	89	AVSS	-960	-1356	149	GVDD	3840	-1356	209	G<12>	9610	-812
30	C41-	-5680	-1356	90	AVSS	-880	-1356	150	VCOMH	3920	-1356	210	G<14>	9720	-774
31	C31+	-5600	-1356	91	VSS*	-800	-1356	151	VCL	4000	-1356	211	G<16>	9610	-736
32	C31+	-5520	-1356	92	VSS	-720	-1356	152	VCL	4080	-1356	212	G<18>	9720	-698
33	C31-	-5440	-1356	93	VSS	-640	-1356	153	VCI1	4160	-1356	213	G<20>	9610	-660
34	C31-	-5360	-1356	94	VSS	-560	-1356	154	VCI1	4240	-1356	214	G<22>	9720	-622
35	VGL	-5280	-1356	95	VSS	-480	-1356	155	VCI1	4320	-1356	215	G<24>	9610	-584
36	VGL	-5200	-1356	96	VSS	-400	-1356	156	VCI1	4400	-1356	216	G<26>	9720	-546
37	VGL	-5120	-1356	97	VDD3*	-320	-1356	157	REGP	4480	-1356	217	G<28>	9610	-508
38	VGL	-5040	-1356	98	VDD3	-240	-1356	158	REGN	4560	-1356	218	G<30>	9720	-470
39	CGND	-4960	-1356	99	VDD3	-160	-1356	159	VCI2	4640	-1356	219	G<32>	9610	-432
40	CGND	-4880	-1356	100	VDD3	-80	-1356	160	AVDD	4720	-1356	220	G<34>	9720	-394
41	CGND	-4800	-1356	101	RDVDD	0	-1356	161	AVDD	4800	-1356	221	G<36>	9610	-356
42	VDD3O	-4720	-1356	102	RDVDD	80	-1356	162	VCI3	4880	-1356	222	G<38>	9720	-318
43	IM<0>	-4640	-1356	103	RDVDD	160	-1356	163	VCI3	4960	-1356	223	G<40>	9610	-280
44	VSSO	-4560	-1356	104	RDVDD	240	-1356	164	C11-	5040	-1356	224	G<42>	9720	-242
45	IM<1>	-4480	-1356	105	VDD	320	-1356	165	C11-	5120	-1356	225	G<44>	9610	-204
46	VDD3O	-4400	-1356	106	VDD	400	-1356	166	C11-	5200	-1356	226	G<46>	9720	-166
47	IM<2>	-4320	-1356	107	VDD	480	-1356	167	C11-	5280	-1356	227	G<48>	9610	-128
48	VDD3O	-4240	-1356	108	VDD	560	-1356	168	C11+	5360	-1356	228	G<50>	9720	-90
49	DUMMY<6>	-4160	-1356	109	VBS	640	-1356	169	C11+	5440	-1356	229	G<52>	9610	-52
50	VSSO	-4080	-1356	110	VCI	720	-1356	170	C11+	5520	-1356	230	G<54>	9720	-14
51	PREGB	-4000	-1356	111	VCI	800	-1356	171	C11+	5600	-1356	231	G<56>	9610	24
52	VDD3O	-3920	-1356	112	VCI	880	-1356	172	C12-	5680	-1356	232	G<58>	9720	62
53	RESETB2	-3840	-1356	113	VCI	960	-1356	173	C12-	5760	-1356	233	G<60>	9610	100
54	VSSO	-3760	-1356	114	VCI	1040	-1356	174	C12-	5840	-1356	234	G<62>	9720	138
55	DUMMY<7>	-3680	-1356	115	VCI4	1120	-1356	175	C12-	5920	-1356	235	G<64>	9610	176
56	DUMMY<8>	-3600	-1356	116	OSC1	1200	-1356	176	C12+	6000	-1356	236	G<66>	9720	214
57	DB<15>	-3520	-1356	117	OSC2	1280	-1356	177	C12+	6080	-1356	237	G<68>	9610	252
58	DB<14>	-3440	-1356	118	CL1	1360	-1356	178	C12+	6160	-1356	238	G<70>	9720	290
59	DB<13>	-3360	-1356	119	M	1440	-1356	179	C12+	6240	-1356	239	G<72>	9610	328
60	DB<12>	-3280	-1356	120	FLM	1520	-1356	180	VGOFF	6320	-1356	240	G<74>	9720	366

Notes: No. 91 & 92, No.97 & 98 PAD must be short by external wiring.

Table 3. Pad Center Coordinates (continued)

[Unit: um]

NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y
241	G<76>	9610	404	301	DUMMY<31>	7914	1362	361	S<342>	5634	1362	421	S<282>	3354	1362
242	G<78>	9720	442	302	DUMMY<32>	7876	1252	362	S<341>	5596	1252	422	S<281>	3316	1252
243	G<80>	9610	480	303	DUMMY<33>	7838	1362	363	S<340>	5558	1362	423	S<280>	3278	1362
244	G<82>	9720	518	304	DUMMY<34>	7800	1252	364	S<339>	5520	1252	424	S<279>	3240	1252
245	G<84>	9610	556	305	DUMMY<35>	7762	1362	365	S<338>	5482	1362	425	S<278>	3202	1362
246	G<86>	9720	594	306	DUMMY<36>	7724	1252	366	S<337>	5444	1252	426	S<277>	3164	1252
247	G<88>	9610	632	307	S<396>	7686	1362	367	S<336>	5406	1362	427	S<276>	3126	1362
248	G<90>	9720	670	308	S<395>	7648	1252	368	S<335>	5368	1252	428	S<275>	3088	1252
249	G<92>	9610	708	309	S<394>	7610	1362	369	S<334>	5330	1362	429	S<274>	3050	1362
250	G<94>	9720	746	310	S<393>	7572	1252	370	S<333>	5292	1252	430	S<273>	3012	1252
251	G<96>	9610	784	311	S<392>	7534	1362	371	S<332>	5254	1362	431	S<272>	2974	1362
252	G<98>	9720	822	312	S<391>	7496	1252	372	S<331>	5216	1252	432	S<271>	2936	1252
253	G<100>	9610	860	313	S<390>	7458	1362	373	S<330>	5178	1362	433	S<270>	2898	1362
254	G<102>	9720	898	314	S<389>	7420	1252	374	S<329>	5140	1252	434	S<269>	2860	1252
255	G<104>	9610	936	315	S<388>	7382	1362	375	S<328>	5102	1362	435	S<268>	2822	1362
256	G<106>	9720	974	316	S<387>	7344	1252	376	S<327>	5064	1252	436	S<267>	2784	1252
257	DUMMY<23>	9610	1012	317	S<386>	7306	1362	377	S<326>	5026	1362	437	S<266>	2746	1362
258	DUMMY<24>	9720	1050	318	S<385>	7268	1252	378	S<325>	4988	1252	438	S<265>	2708	1252
259	DUMMY<25>	9610	1088	319	S<384>	7230	1362	379	S<324>	4950	1362	439	S<264>	2670	1362
260	DUMMY<26>	9472	1252	320	S<383>	7192	1252	380	S<323>	4912	1252	440	S<263>	2632	1252
261	DUMMY<27>	9434	1362	321	S<382>	7154	1362	381	S<322>	4874	1362	441	S<262>	2594	1362
262	DUMMY<28>	9396	1252	322	S<381>	7116	1252	382	S<321>	4836	1252	442	S<261>	2556	1252
263	G<108>	9358	1362	323	S<380>	7078	1362	383	S<320>	4798	1362	443	S<260>	2518	1362
264	G<110>	9320	1252	324	S<379>	7040	1252	384	S<319>	4760	1252	444	S<259>	2480	1252
265	G<112>	9282	1362	325	S<378>	7002	1362	385	S<318>	4722	1362	445	S<258>	2442	1362
266	G<114>	9244	1252	326	S<377>	6964	1252	386	S<317>	4684	1252	446	S<257>	2404	1252
267	G<116>	9206	1362	327	S<376>	6926	1362	387	S<316>	4646	1362	447	S<256>	2366	1362
268	G<118>	9168	1252	328	S<375>	6888	1252	388	S<315>	4608	1252	448	S<255>	2328	1252
269	G<120>	9130	1362	329	S<374>	6850	1362	389	S<314>	4570	1362	449	S<254>	2290	1362
270	G<122>	9092	1252	330	S<373>	6812	1252	390	S<313>	4532	1252	450	S<253>	2252	1252
271	G<124>	9054	1362	331	S<372>	6774	1362	391	S<312>	4494	1362	451	S<252>	2214	1362
272	G<126>	9016	1252	332	S<371>	6736	1252	392	S<311>	4456	1252	452	S<251>	2176	1252
273	G<128>	8978	1362	333	S<370>	6698	1362	393	S<310>	4418	1362	453	S<250>	2138	1362
274	G<130>	8940	1252	334	S<369>	6660	1252	394	S<309>	4380	1252	454	S<249>	2100	1252
275	G<132>	8902	1362	335	S<368>	6622	1362	395	S<308>	4342	1362	455	S<248>	2062	1362
276	G<134>	8864	1252	336	S<367>	6584	1252	396	S<307>	4304	1252	456	S<247>	2024	1252
277	G<136>	8826	1362	337	S<366>	6546	1362	397	S<306>	4266	1362	457	S<246>	1986	1362
278	G<138>	8788	1252	338	S<365>	6508	1252	398	S<305>	4228	1252	458	S<245>	1948	1252
279	G<140>	8750	1362	339	S<364>	6470	1362	399	S<304>	4190	1362	459	S<244>	1910	1362
280	G<142>	8712	1252	340	S<363>	6432	1252	400	S<303>	4152	1252	460	S<243>	1872	1252
281	G<144>	8674	1362	341	S<362>	6394	1362	401	S<302>	4114	1362	461	S<242>	1834	1362
282	G<146>	8636	1252	342	S<361>	6356	1252	402	S<301>	4076	1252	462	S<241>	1796	1252
283	G<148>	8598	1362	343	S<360>	6318	1362	403	S<300>	4038	1362	463	S<240>	1758	1362
284	G<150>	8560	1252	344	S<359>	6280	1252	404	S<299>	4000	1252	464	S<239>	1720	1252
285	G<152>	8522	1362	345	S<358>	6242	1362	405	S<298>	3962	1362	465	S<238>	1682	1362
286	G<154>	8484	1252	346	S<357>	6204	1252	406	S<297>	3924	1252	466	S<237>	1644	1252
287	G<156>	8446	1362	347	S<356>	6166	1362	407	S<296>	3886	1362	467	S<236>	1606	1362
288	G<158>	8408	1252	348	S<355>	6128	1252	408	S<295>	3848	1252	468	S<235>	1568	1252
289	G<160>	8370	1362	349	S<354>	6090	1362	409	S<294>	3810	1362	469	S<234>	1530	1362
290	G<162>	8332	1252	350	S<353>	6052	1252	410	S<293>	3772	1252	470	S<233>	1492	1252
291	G<164>	8294	1362	351	S<352>	6014	1362	411	S<292>	3734	1362	471	S<232>	1454	1362
292	G<166>	8256	1252	352	S<351>	5976	1252	412	S<291>	3696	1252	472	S<231>	1416	1252
293	G<168>	8218	1362	353	S<350>	5938	1362	413	S<290>	3658	1362	473	S<230>	1378	1362
294	G<170>	8180	1252	354	S<349>	5900	1252	414	S<289>	3620	1252	474	S<229>	1340	1252
295	G<172>	8142	1362	355	S<348>	5862	1362	415	S<288>	3582	1362	475	S<228>	1302	1362
296	G<174>	8104	1252	356	S<347>	5824	1252	416	S<287>	3544	1252	476	S<227>	1264	1252
297	G<176>	8066	1362	357	S<346>	5786	1362	417	S<286>	3506	1362	477	S<226>	1226	1362
298	G<177>	8028	1252	358	S<345>	5748	1252	418	S<285>	3468	1252	478	S<225>	1188	1252
299	DUMMY<29>	7990	1362	359	S<344>	5710	1362	419	S<284>	3430	1362	479	S<224>	1150	1362
300	DUMMY<30>	7952	1252	360	S<343>	5672	1252	420	S<283>	3392	1252	480	S<223>	1112	1252

Table 4. Pad Center Coordinates (continued)

[Unit: um]

NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y
481	S<222>	1074	1362	541	S<170>	-1206	1362	601	S<110>	-3486	1362	661	S<50>	-5766	1362
482	S<221>	1036	1252	542	S<169>	-1244	1252	602	S<109>	-3524	1252	662	S<49>	-5804	1252
483	S<220>	998	1362	543	S<168>	-1282	1362	603	S<108>	-3562	1362	663	S<48>	-5842	1362
484	S<219>	960	1252	544	S<167>	-1320	1252	604	S<107>	-3600	1252	664	S<47>	-5880	1252
485	S<218>	922	1362	545	S<166>	-1358	1362	605	S<106>	-3638	1362	665	S<46>	-5918	1362
486	S<217>	884	1252	546	S<165>	-1396	1252	606	S<105>	-3676	1252	666	S<45>	-5956	1252
487	S<216>	846	1362	547	S<164>	-1434	1362	607	S<104>	-3714	1362	667	S<44>	-5994	1362
488	S<215>	808	1252	548	S<163>	-1472	1252	608	S<103>	-3752	1252	668	S<43>	-6032	1252
489	S<214>	770	1362	549	S<162>	-1510	1362	609	S<102>	-3790	1362	669	S<42>	-6070	1362
490	S<213>	732	1252	550	S<161>	-1548	1252	610	S<101>	-3828	1252	670	S<41>	-6108	1252
491	S<212>	694	1362	551	S<160>	-1586	1362	611	S<100>	-3866	1362	671	S<40>	-6146	1362
492	S<211>	656	1252	552	S<159>	-1624	1252	612	S<99>	-3904	1252	672	S<39>	-6184	1252
493	S<210>	618	1362	553	S<158>	-1662	1362	613	S<98>	-3942	1362	673	S<38>	-6222	1362
494	S<209>	580	1252	554	S<157>	-1700	1252	614	S<97>	-3980	1252	674	S<37>	-6260	1252
495	S<208>	542	1362	555	S<156>	-1738	1362	615	S<96>	-4018	1362	675	S<36>	-6298	1362
496	S<207>	504	1252	556	S<155>	-1776	1252	616	S<95>	-4056	1252	676	S<35>	-6336	1252
497	S<206>	466	1362	557	S<154>	-1814	1362	617	S<94>	-4094	1362	677	S<34>	-6374	1362
498	S<205>	428	1252	558	S<153>	-1852	1252	618	S<93>	-4132	1252	678	S<33>	-6412	1252
499	S<204>	390	1362	559	S<152>	-1890	1362	619	S<92>	-4170	1362	679	S<32>	-6450	1362
500	S<203>	352	1252	560	S<151>	-1928	1252	620	S<91>	-4208	1252	680	S<31>	-6488	1252
501	S<202>	314	1362	561	S<150>	-1966	1362	621	S<90>	-4246	1362	681	S<30>	-6526	1362
502	S<201>	276	1252	562	S<149>	-2004	1252	622	S<89>	-4284	1252	682	S<29>	-6564	1252
503	S<200>	238	1362	563	S<148>	-2042	1362	623	S<88>	-4322	1362	683	S<28>	-6602	1362
504	S<199>	200	1252	564	S<147>	-2080	1252	624	S<87>	-4360	1252	684	S<27>	-6640	1252
505	S<198>	162	1362	565	S<146>	-2118	1362	625	S<86>	-4398	1362	685	S<26>	-6678	1362
506	S<197>	124	1252	566	S<145>	-2156	1252	626	S<85>	-4436	1252	686	S<25>	-6716	1252
507	S<196>	86	1362	567	S<144>	-2194	1362	627	S<84>	-4474	1362	687	S<24>	-6754	1362
508	S<195>	48	1252	568	S<143>	-2232	1252	628	S<83>	-4512	1252	688	S<23>	-6792	1252
509	S<194>	10	1362	569	S<142>	-2270	1362	629	S<82>	-4550	1362	689	S<22>	-6830	1362
510	S<193>	-28	1252	570	S<141>	-2308	1252	630	S<81>	-4588	1252	690	S<21>	-6868	1252
511	DUMMY<37>	-66	1362	571	S<140>	-2346	1362	631	S<80>	-4626	1362	691	S<20>	-6906	1362
512	DUMMY<38>	-104	1252	572	S<139>	-2384	1252	632	S<79>	-4664	1252	692	S<19>	-6944	1252
513	DUMMY<39>	-142	1362	573	S<138>	-2422	1362	633	S<78>	-4702	1362	693	S<18>	-6982	1362
514	DUMMY<40>	-180	1252	574	S<137>	-2460	1252	634	S<77>	-4740	1252	694	S<17>	-7020	1252
515	DUMMY<41>	-218	1362	575	S<136>	-2498	1362	635	S<76>	-4778	1362	695	S<16>	-7058	1362
516	DUMMY<42>	-256	1252	576	S<135>	-2536	1252	636	S<75>	-4816	1252	696	S<15>	-7096	1252
517	DUMMY<43>	-294	1362	577	S<134>	-2574	1362	637	S<74>	-4854	1362	697	S<14>	-7134	1362
518	DUMMY<44>	-332	1252	578	S<133>	-2612	1252	638	S<73>	-4892	1252	698	S<13>	-7172	1252
519	S<192>	-370	1362	579	S<132>	-2650	1362	639	S<72>	-4930	1362	699	S<12>	-7210	1362
520	S<191>	-408	1252	580	S<131>	-2688	1252	640	S<71>	-4968	1252	700	S<11>	-7248	1252
521	S<190>	-446	1362	581	S<130>	-2726	1362	641	S<70>	-5006	1362	701	S<10>	-7286	1362
522	S<189>	-484	1252	582	S<129>	-2764	1252	642	S<69>	-5044	1252	702	S<9>	-7324	1252
523	S<188>	-522	1362	583	S<128>	-2802	1362	643	S<68>	-5082	1362	703	S<8>	-7362	1362
524	S<187>	-560	1252	584	S<127>	-2840	1252	644	S<67>	-5120	1252	704	S<7>	-7400	1252
525	S<186>	-598	1362	585	S<126>	-2878	1362	645	S<66>	-5158	1362	705	S<6>	-7438	1362
526	S<185>	-636	1252	586	S<125>	-2916	1252	646	S<65>	-5196	1252	706	S<5>	-7476	1252
527	S<184>	-674	1362	587	S<124>	-2954	1362	647	S<64>	-5234	1362	707	S<4>	-7514	1362
528	S<183>	-712	1252	588	S<123>	-2992	1252	648	S<63>	-5272	1252	708	S<3>	-7552	1252
529	S<182>	-750	1362	589	S<122>	-3030	1362	649	S<62>	-5310	1362	709	S<2>	-7590	1362
530	S<181>	-788	1252	590	S<121>	-3068	1252	650	S<61>	-5348	1252	710	S<1>	-7628	1252
531	S<180>	-826	1362	591	S<120>	-3106	1362	651	S<60>	-5386	1362	711	DUMMY<45>	-7666	1362
532	S<179>	-864	1252	592	S<119>	-3144	1252	652	S<59>	-5424	1252	712	DUMMY<46>	-7704	1252
533	S<178>	-902	1362	593	S<118>	-3182	1362	653	S<58>	-5462	1362	713	DUMMY<47>	-7742	1362
534	S<177>	-940	1252	594	S<117>	-3220	1252	654	S<57>	-5500	1252	714	DUMMY<48>	-7780	1252
535	S<176>	-978	1362	595	S<116>	-3258	1362	655	S<56>	-5538	1362	715	DUMMY<49>	-7818	1362
536	S<175>	-1016	1252	596	S<115>	-3296	1252	656	S<55>	-5576	1252	716	DUMMY<50>	-7856	1252
537	S<174>	-1054	1362	597	S<114>	-3334	1362	657	S<54>	-5614	1362	717	DUMMY<51>	-7894	1362
538	S<173>	-1092	1252	598	S<113>	-3372	1252	658	S<53>	-5652	1252	718	DUMMY<52>	-7932	1252
539	S<172>	-1130	1362	599	S<112>	-3410	1362	659	S<52>	-5690	1362	719	G<175>	-7970	1362
540	S<171>	-1168	1252	600	S<111>	-3448	1252	660	S<51>	-5728	1252	720	G<173>	-8008	1252

Table 5. Pad Center Coordinates (continued)

[Unit: um]

NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y	NO.	PAD name	X	Y
721	G<171>	-8046	1362	781	G<63>	-9720	176								
722	G<169>	-8084	1252	782	G<61>	-9610	138								
723	G<167>	-8122	1362	783	G<59>	-9720	100								
724	G<165>	-8160	1252	784	G<57>	-9610	62								
725	G<163>	-8198	1362	785	G<55>	-9720	24								
726	G<161>	-8236	1252	786	G<53>	-9610	-14								
727	G<159>	-8274	1362	787	G<51>	-9720	-52								
728	G<157>	-8312	1252	788	G<49>	-9610	-90								
729	G<155>	-8350	1362	789	G<47>	-9720	-128								
730	G<153>	-8388	1252	790	G<45>	-9610	-166								
731	G<151>	-8426	1362	791	G<43>	-9720	-204								
732	G<149>	-8464	1252	792	G<41>	-9610	-242								
733	G<147>	-8502	1362	793	G<39>	-9720	-280								
734	G<145>	-8540	1252	794	G<37>	-9610	-318								
735	G<143>	-8578	1362	795	G<35>	-9720	-356								
736	G<141>	-8616	1252	796	G<33>	-9610	-394								
737	G<139>	-8654	1362	797	G<31>	-9720	-432								
738	G<137>	-8692	1252	798	G<29>	-9610	-470								
739	G<135>	-8730	1362	799	G<27>	-9720	-508								
740	G<133>	-8768	1252	800	G<25>	-9610	-546								
741	G<131>	-8806	1362	801	G<23>	-9720	-584								
742	G<129>	-8844	1252	802	G<21>	-9610	-622								
743	G<127>	-8882	1362	803	G<19>	-9720	-660								
744	G<125>	-8920	1252	804	G<17>	-9610	-698								
745	G<123>	-8958	1362	805	G<15>	-9720	-736								
746	G<121>	-8996	1252	806	G<13>	-9610	-774								
747	G<119>	-9034	1362	807	G<11>	-9720	-812								
748	G<117>	-9072	1252	808	G<9>	-9610	-850								
749	G<115>	-9110	1362	809	G<7>	-9720	-888								
750	G<113>	-9148	1252	810	G<5>	-9610	-926								
751	G<111>	-9186	1362	811	G<3>	-9720	-964								
752	G<109>	-9224	1252	812	G<1>	-9610	-1002								
753	G<107>	-9262	1362	813	G<0>	-9720	-1040								
754	DUMMY<53>	-9300	1252	814	DUMMY<59>	-9610	-1078								
755	DUMMY<54>	-9338	1362	815	DUMMY<60>	-9720	-1116								
756	DUMMY<55>	-9376	1252												
757	DUMMY<56>	-9720	1088												
758	DUMMY<57>	-9610	1050												
759	DUMMY<58>	-9720	1012												
760	G<105>	-9610	974												
761	G<103>	-9720	936												
762	G<101>	-9610	898												
763	G<99>	-9720	860												
764	G<97>	-9610	822												
765	G<95>	-9720	784												
766	G<93>	-9610	746												
767	G<91>	-9720	708												
768	G<89>	-9610	670												
769	G<87>	-9720	632												
770	G<85>	-9610	594												
771	G<83>	-9720	556												
772	G<81>	-9610	518												
773	G<79>	-9720	480												
774	G<77>	-9610	442												
775	G<75>	-9720	404												
776	G<73>	-9610	366												
777	G<71>	-9720	328												
778	G<69>	-9610	290												
779	G<67>	-9720	252												
780	G<65>	-9610	214												

Preliminary

PIN DESCRIPTION

Table 6. Power supply pin description

Symbol	I/O	Description
VDD	Power	System power supply. As S6D0110 have internal regulator, VDD range varies with each mode. Non-regulated(PregB = 1) : +1.8 ~ +2.5 V Regulated (PregB = 0) : +1.9V
VDD3	Power	System power supply for internal regulator as external power. (VDD3: +2.5 to +3.3 V)
VSS	Power	System ground(0V)
CGND	Power	System ground level for step up circuit block.
AVSS	Power	System ground level for analog circuit block.
VCI	Power	An internal reference power supply for VREG1OUT/VREG2OUT. Connect VDD when VDD = 2.5 to 3.3 V. Connect a 2.5 to 3.3 V external-voltage power supply when VDD = 1.8 to 2.5 V.
AVDD	O	A power output pin for source driver that is generated from power block. Connect a capacitor for stabilization. (AVDD: 3.5 to 5.5 V) Interconnect this pin to VCI2 pin.
GVDD	O	A Standard level for grayscale voltage generator. Connect a capacitor for stabilization.
VGS	I	Reference voltage for grayscale voltage generator.
VCI1	I	A reference voltage for step-up circuit 1.
VCI2	I	A reference voltage for step-up circuit 2.
VCI3	I	A reference voltage in step-up circuit 3.
VCI4	I	A reference voltage in step-up circuit 4. Connect VCI, VDD, or an external power supply lower than 3.3 V.
VCL	O	A power supply pin for generating VcomL. When VcomL is higher than VSS, outputs VSS level.

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Table 7. Power supply pin description (continued)

Symbol	I/O	Description
VBS	I	Reference voltage for step-up circuit3. When VGH (max) = 20V, connect this pin to VCI. When VGH (max) = 15V, connect this pin to VSS.
REGN, REGP	I/O	Input pins for reference voltages of VREG1OUT, and VREG2OUT when the internal reference-voltage generation circuit is not used. Leave these pins open when the internal reference-voltage generation circuit is used.
VREG1OUT	O	This pin outputs a reference voltage for VREG1 between AVDD(DDVDH) and VSS. When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGP. Connect this pin to VREG1 and a capacitor for stabilization. When this pin is not used, leave it open.
VREG2OUT	O	This pin outputs a reference voltage for VREG2 between VSS and VGL When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGN. Connect this pin to VREG2 and a capacitor for stabilizatio0n. When this pin is not used, leave it open.
VcomOUT	O	A power supply for the TFT-display counter electrode. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display counter electrode. This pin is also used as equalizing function: When EQ = "High" period, all source driver's outputs (S1 to S396) are short to Vcom level (Hi-z). In case of VcomL < 0V, equalizing function must not be used. (Set EQ bit (R07h) to be "00" for preventing the abnormal function.)
VcomR	I	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VGH	O	A positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. Interconnect this pin to VCI3 pin.
VGL	O	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. When internal VGL generator is not used, connect an external-voltage power supply higher than -15.0 V.

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Table 8. Power supply pin description (continued)

Symbol	I/O	Description
Vgoff	I	Power supply pin for off level for gate of TFT. Connect this pin to VgoffOUT.
VgoffOUT	O	An power output pin for gate driver. This pin is a negative voltage for the gate off level. Alternation can be synchronized by M pin. Set the internal register according to the structure of the TFT-display retention volume. For the amplitude at the alternation driving, this pin outputs a voltage between VcomH and VcomL with the VgoffL reference voltage..
VgoffH	O	When the Vgoff alternation is driven, this pin indicates a high level of Vgoff. Connect a capacitor for stabilization. When the CAD bit is low, the VgoffH output stops and a capacitor for stabilization is not needed.
VgoffL	O	When the Vgoff alternation is driven, this pin indicates a low level of Vgoff. Connect a capacitor for stabilization. An internal register can be used to adjust the voltage.
C11+,C11- to C23+,C23-	-	Connect the step-up capacitor according to the step-up factor.
C31+, C31-	-	Connect a step-up capacitor for generating the VGL level.
C41+, C41-	-	Connect a step-up capacitor for generating the -VCL level.

Preliminary

Table 9. System interface pin description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="9">IM2-1,
IM0/ID</td><td rowspan="9">I</td><td colspan="4">Selects the MPU interface mode:</td></tr>
<tr><td>IM2</td><td>IM1</td><td>IM0/ID</td><td>MPU interface mode</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 16-bit bus interface</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 8bit bus interface</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 16bit bus interface</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 8bit bus interface</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>ID</td><td>Serial peripheral interface (SPI)</td></tr>
<tr><td colspan="4">When a SPI mode is selected, the IM0 pin is used as the ID setting for a device code.</td></tr>
<tr><td>CSB</td><td>I</td><td colspan="4">Chip select pin.
Low: S6D0110 is selected and can be accessed
High: S6D0110 is not selected and cannot be accessed
Must be fixed at VSS level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td colspan="4">Register select pin.
Low: Index/status, High: Control</td></tr>
<tr><td rowspan="4">E
(/WR,SCL)</td><td rowspan="4">I</td><td>IM2</td><td>IM1</td><td>Pin func.</td><td>Pin description</td></tr>
<tr><td>VSS</td><td>VSS</td><td>E</td><td>For a 68-system bus interface, serves as an enable signal to activate data read/write operation.</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>/WR</td><td>For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>SCL</td><td>For a serial peripheral interface, serves as the synchronous clock signal.</td></tr>
<tr><td rowspan="4">R/W
(/RD)</td><td rowspan="4">I</td><td>IM2</td><td>IM1</td><td>Pin func.</td><td>Pin description</td></tr>
<tr><td>VSS</td><td>VSS</td><td>R/W</td><td>For a 68-system bus interface, serves as a signal to select data read/write operation.
Low: Write , High: Read</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>/RD</td><td>For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.</td></tr>
<tr><td colspan="4">When SPI mode is selected, fix this pin at “VSS” level.</td></tr>
<tr><td>DB0/SDI</td><td>I/O</td><td colspan="4">Bi-directional data input pin for the first bit of 16-bit data bus or serial data of SPI.
For an 8-bit bus interface, data bus uses DB15-DB8; fix unused DB7-DB0 to the VDD3 or VSS level.
For a serial peripheral interface (SPI), The input data is fetched at the rising edge of the SCL signal.</td></tr>
<tr><td>DB1/SDO</td><td>I/O</td><td colspan="4">Serves as a 16-bit bi-directional data bus.
For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the VDD3 or VSS level.
For a serial peripheral interface (SPI), serves as the serial data output pin(SDO). Successive bit values are output on the falling edge of the SCL signal.</td></tr>
<tr><td>DB2-DB15</td><td>I/O</td><td colspan="4">Serves as a 16-bit bi-directional data bus.
For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the VDD3 or VSS level.</td></tr>
<tr><td>RESETB1/
RESETB2/
RESETB3</td><td>I</td><td colspan="4">Reset pin. Initializes the LSI when low. Must be reset after power-on.</td></tr>
</table>

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Table 10. Display pin description

Symbol	I/O	Description
S1 - S396	O	Source driver output pins. The SS bit can change the shift direction of the source signal. For example, if SS = 0, RAM address 0000 is output from S1. If SS = 1, it is output from S396. S1, S4, S7, ... S(3n-1) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-2) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
G1 - G176	O	Gate driver output pins. The output of driving circuit is whether VGH, output gate selecting level or Vgoff, gate non-selecting level.
G0, G177	O	Gate driver output pins for IC maker's testing. Please, leave it disconnected.
CL1	O	Output pin for one-raster-row-cycle pulse.
M	O	Output pin for AC-cycle signal.
FLM	O	Output pin for frame-start pulse.
EQ	O	Output pin for timing for equalizing Low : Normal display, High : Equalizing
DISPTMG	O	Gate off signal in the partial display Low : Non-display, High : Normal output

Table 11. Oscillator and internal power regulator pin description

Symbol	I/O	Description
OSC1/ OSC2	I/O	Connect an external resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2.
PregB	I	Internal power regulator control input pin. When the internal regulated power (RDVDD) is used as VDD, PregB is fixed to "low" level. When the external logic power(VDD3) is used as VDD, PregB is fixed to "high" level.
RDVDD	O	Internal power regulated-VDD output (typ. 1.9V). When PregB is "low", RDVDD is connected to VDD pin. When PRegB is "high", leave this pin open.

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FUNCTIONAL DESCRIPTION

System Interface

The S6D0110 has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a serial interface (SPI: Serial Peripheral Interface port). The IM2-0 pins select the interface mode.
The S6D0110 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information for control register and GRAM. The WDR temporarily stores data to be written into control register and GRAM. The RDR temporarily stores data read from GRAM. Data written into the GRAM from the MPU is first written into the WDR and then written into the GRAM by internal operation automatically. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are valid.
When a logic operation is performed inside of the S6D0110 by using the display data stored in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.
Execution time for instruction, except oscillation start, is 0-clock cycle so that instructions can be written in succession.

Table 12. Register Selection (80-system 8/16 Parallel Interface)

/WR	/RD	RS	Operations
0	1	0	Write indexes into IR
1	0	0	Reads internal status
0	1	1	Writes into control registers and GRAM through WDR
1	0	1	Reads from GRAM through RDR

Table 13. Register Selection (Serial Peripheral Interface)

R/W Bits	RS Bits	Operations
0	0	Writes index into IR
1	0	Reads internal status
0	1	Writes data into control registers and GRAM through WDR
1	1	Reads data from GRAM through RDR

Bit Operation

The S6D0110 supports the following functions: a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assign addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.
After writing into the GRAM, the AC is automatically increased/decreased by 1 according to ID1-0 bit of control register. After reading data from GRAM, the AC is not updated. A window address function allows data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has sixteen bits/pixel and stores the bit-pattern data for 132 RGB x 176 dot display.

Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale ϒ-adjusting resistor. 65,536 colors can be displayed at the same time. For details, see the ϒ-adjusting resistor section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as GRAM.
The RAM read timing for display and the internal operation timing for MPU access is generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, CL1, EQ, DISPTMG).

Oscillation Circuit (OSC)

The S6D0110 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Source Driver Circuit

This liquid crystal display source driver circuit consists of 396 source drivers (S1 to S396).
Display pattern data is latched when 396-bit data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The SS bit can change the shift direction of 396-bit data by selecting an appropriate direction for the device-mounted configuration.

Gate Driver Circuit

This liquid crystal display gate driver circuit consists of 178 gate drivers (G0 to G177).
The VGH or Vgoff level is output by the signal from the gate control circuit.
G0 and G177 are IC maker' s test pins.

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Power Supply Circuit

Figure 2 shows a configuration of the voltage generation circuit for S6D0110. The step-up circuits consist of step-up circuits 1 to 4. Step-up circuit 1 doubles or triples the voltage supplied to Vci1, and that voltage is doubled, tripled, or quadrupled in step-up circuit 2. Step-up circuit 3 reverses the VGH level with reference to VSS or VBS and generates the VGL level. Step-up circuit 4 reverses the Vci level with reference to VSS and generates the VCL level. These step-up circuits generate power supplies AVDD, GVDD, VGH, VGL, Vgoff, and Vcom. Reference voltages GVDD, Vcom, and Vgoff for the grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit or the REGP or REGN voltage, and generate each level depending on that voltage. Connect Vcom to the TFT panel.

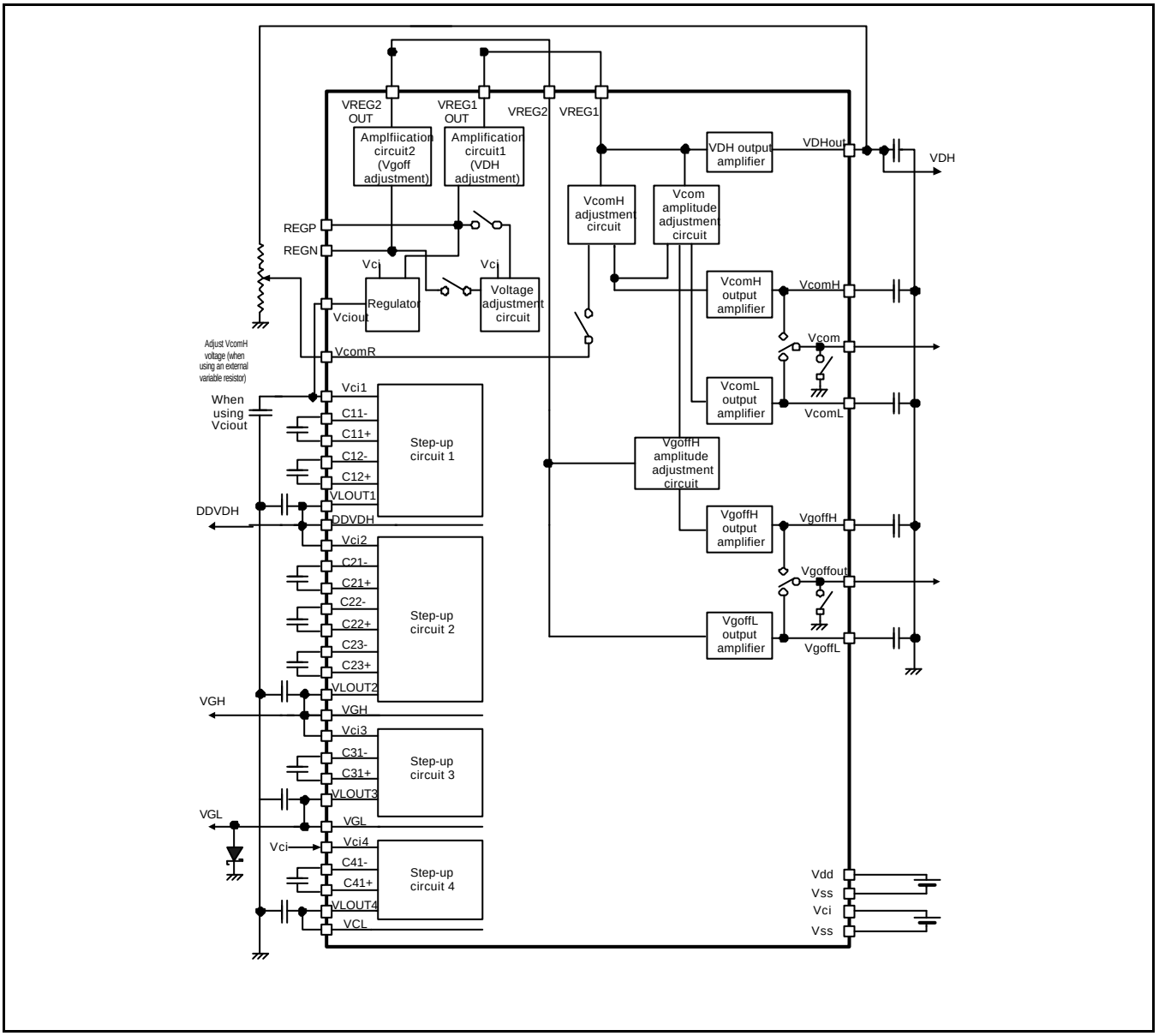


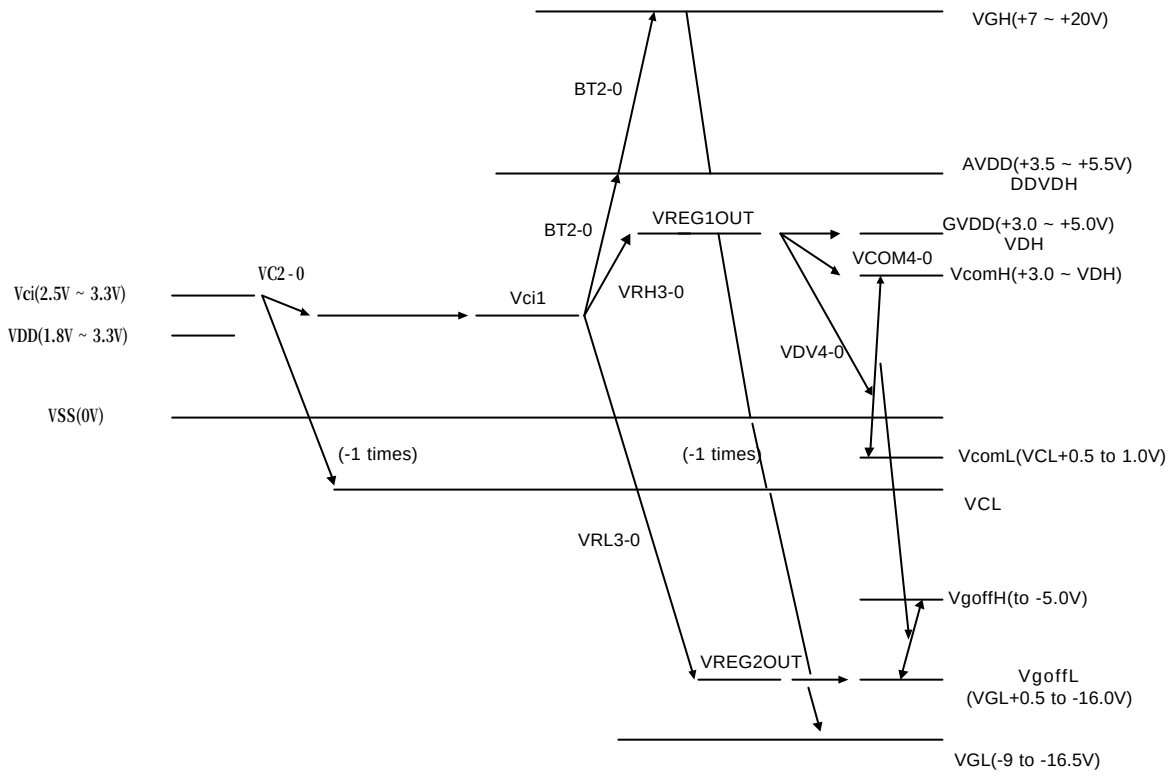
Figure 5. Configuration of the Internal Power-Supply Circuit

Notes:

Use the 1uF capacitor.

Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note:
Adjust the conditions of AVDD-GVDD>0.5V, VcomL-VCL>0.5V, and Vgoff-VGL>0.5V with loads because they differ depending on the display load to be driven. In addition, Vci can be directly input to Vci1.

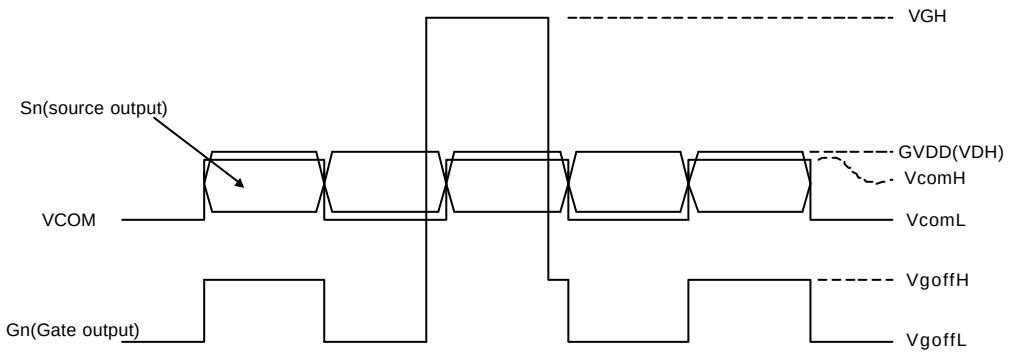


Figure 6. Pattern diagram and an example of waveforms

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Set up Flow of Power Supply

Apply the power in a sequence as shown in Figure 7. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.

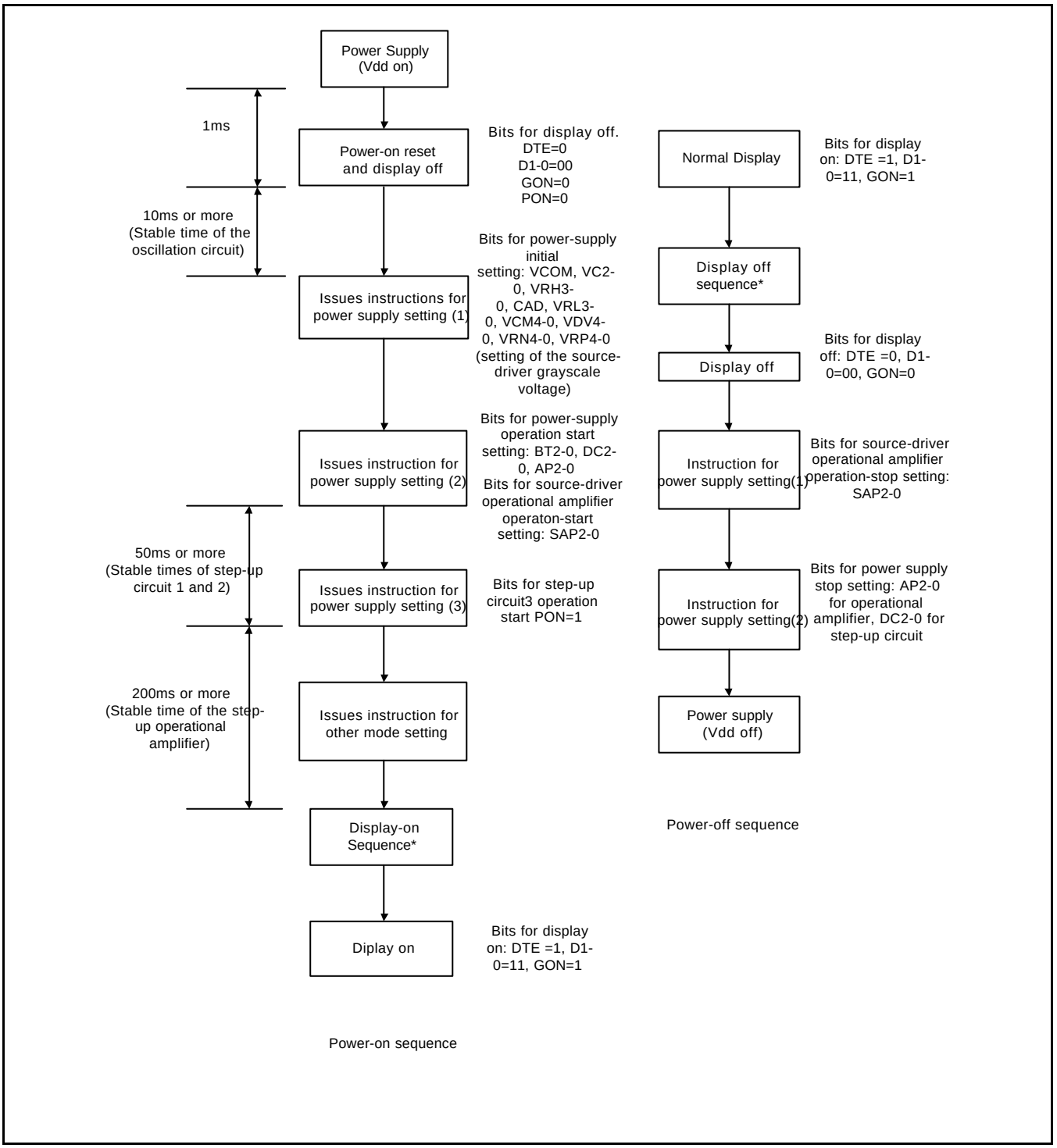

Figure 7. Set up Flow of Power Supply

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GRAM ADDRESS

Table 14. GRAM address (SS="0")

S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB 15 ..... DB 0			DB 15 ..... DB 0			DB 15 ..... DB 0			DB 15 ..... DB 0				DB 15 ..... DB 0			DB 15 ..... DB 0			DB 15 ..... DB 0			DB 15 ..... DB 0		
G1	G176	"0000"H			"0001"H			"0002"H			"0003"H			.....	"0080"H			"0081"H			"0082"H			"0083"H		
G2	G175	"0100"H			"0101"H			"0102"H			"0103"H			.....	"0180"H			"0181"H			"0182"H			"0183"H		
G3	G174	"0200"H			"0201"H			"0202"H			"0203"H			.....	"0280"H			"0281"H			"0282"H			"0283"H		
G4	G173	"0300"H			"0301"H			"0302"H			"0303"H			.....	"0380"H			"0381"H			"0382"H			"0383"H		
G5	G172	"0400"H			"0401"H			"0402"H			"0403"H			.....	"0480"H			"0481"H			"0482"H			"0483"H		
G6	G171	"0500"H			"0501"H			"0502"H			"0503"H			.....	"0580"H			"0581"H			"0582"H			"0583"H		
G7	G170	"0600"H			"0601"H			"0602"H			"0603"H			.....	"0680"H			"0681"H			"0682"H			"0683"H		
G8	G169	"0700"H			"0701"H			"0702"H			"0703"H			.....	"0780"H			"0781"H			"0782"H			"0783"H		
G9	G168	"0800"H			"0801"H			"0802"H			"0803"H			.....	"0880"H			"0881H			"0882"H			"0883"H		
G10	G167	"0900"H			"0901"H			"0902"H			"0903"H			.....	"0980"H			"0981"H			"0982"H			"0983"H		
G11	G166	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0A80"H			"0A81"H			"0A82"H			"0A83"H		
G12	G165	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0B80"H			"0B81"H			"0B82"H			"0B83"H		
G13	G164	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0C80"H			"0C81"H			"0C82"H			"0C83"H		
G14	G163	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0D80"H			"0D81"H			"0D82"H			"0D83"H		
G15	G162	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0E80"H			"0E81"H			"0E82"H			"0E83"H		
G16	G161	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0F80"H			"0F81"H			"0F82"H			"0F83"H		
G17	G160	"1000"H			"1001"H			"1002"H			"1003"H			.....	"1080"H			"1081"H			"1082"H			"1083"H		
G18	G159	"1100"H			"1101"H			"1102"H			"1103"H			.....	"1180"H			"1181"H			"1182"H			"1183"H		
G19	G158	"1200"H			"1201"H			"1202"H			"1203"H			.....	"1280"H			"1281"H			"1282"H			"1283"H		
G20	G157	"1300"H			"1301"H			"1302"H			"1303"H			.....	"1380"H			"1381"H			"1382"H			"1383"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G169	G168	"A800"H			"A801"H			"A802"H			"A803"H			.....	"A880"H			"A881"H			"A880"H			"A883"H		
G170	G167	"A900"H			"A901"H			"A902"H			"A903"H			.....	"A980"H			"A981"H			"A980"H			"A983"H		
G171	G166	"AA00"H			"AA01"H			"AA02"H			"AA03"H			.....	"AA80"H			"AA81"H			"AA80"H			"AA83"H		
G172	G165	"AB00"H			"AB01"H			"AB02"H			"AB03"H			.....	"AB80"H			"AB81"H			"AB80"H			"AB83"H		
G173	G164	"AC00"H			"AC01"H			"AC02"H			"AC03"H			.....	"AC80"H			"AC81"H			"AC80"H			"AC83"H		
G174	G163	"AD00"H			"AD01"H			"AD02"H			"AD03"H			.....	"AD80"H			"AD81"H			"AD80"H			"AD83"H		
G175	G162	"AE00"H			"AE01"H			"AE02"H			"AE03"H			.....	"AE80"H			"AE81"H			"AE80"H			"AE83"H		
G176	G161	"AF00"H			"AF01"H			"AF02"H			"AF03"H			.....	"AF80"H			"AF81"H			"AF80"H			"AF83"H		

Table 15. GRAM address (SS="1")

S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB 15 ..... DB 0																								
G1	G176	"0083"H			"0082"H			"0081"H			"0080"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G175	"0183"H			"0182"H			"0181"H			"0180"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G174	"0283"H			"0282"H			"0281"H			"0280"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G173	"0383"H			"0382"H			"0381"H			"0380"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G172	"0483"H			"0482"H			"0481"H			"0480"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G171	"0583"H			"0582"H			"0581"H			"0580"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G170	"0683"H			"0682"H			"0681"H			"0680"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G169	"0783"H			"0782"H			"0781"H			"0780"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G168	"0883"H			"0882"H			"0881H			"0880"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G167	"0983"H			"0982"H			"0981"H			"0980"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G166	"0A83"H			"0A82"H			"0A81"H			"0A80"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G165	"0B83"H			"0B82"H			"0B81"H			"0B80"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G164	"0C83"H			"0C82"H			"0C81"H			"0C80"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G163	"0D83"H			"0D82"H			"0D81"H			"0D80"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G162	"0E83"H			"0E82"H			"0E81"H			"0E80"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G161	"0F83"H			"0F82"H			"0F81"H			"0F80"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G160	"1083"H			"1082"H			"1081"H			"1080"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G159	"1183"H			"1182"H			"1181"H			"1180"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G158	"1283"H			"1282"H			"1281"H			"1280"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G157	"1383"H			"1382"H			"1381"H			"1380"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G169	G168	"A883"H			"A880"H			"A881"H			"A880"H			.....	"A803"H			"A802"H			"A801"H			"A800"H		
G170	G167	"A983"H			"A980"H			"A981"H			"A980"H			.....	"A903"H			"A902"H			"A901"H			"A900"H		
G171	G166	"AA83"H			"AA80"H			"AA81"H			"AA80"H			.....	"AA03"H			"AA02"H			"AA01"H			"AA00"H		
G172	G165	"AB83"H			"AB80"H			"AB81"H			"AB80"H			.....	"AB03"H			"AB02"H			"AB01"H			"AB00"H		
G173	G164	"AC83"H			"AC80"H			"AC81"H			"AC80"H			.....	"AC03"H			"AC02"H			"AC01"H			"AC00"H		
G174	G163	"AD83"H			"AD80"H			"AD81"H			"AD80"H			.....	"AD03"H			"AD02"H			"AD01"H			"AD00"H		
G175	G162	"AE83"H			"AE80"H			"AE81"H			"AE80"H			.....	"AE03"H			"AE02"H			"AE01"H			"AE00"H		
G176	G161	"AF83"H			"AF80"H			"AF81"H			"AF80"H			.....	"AF03"H			"AF02"H			"AF01"H			"AF00"H		

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INSTRUCTIONS

The S6D0110 uses the 16-bit bus architecture. Before the internal operation of the S6D0110 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the S6D0110 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the S6D0110 instructions.
There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the gate driver and power supply IC

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. As instructions are executed in 0 cycles, they can be written in succession.

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INSTRUCTION TABLE

Table 16. Instruction table 1

Reg. No	R/W	RS	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Register Name / Description
IR	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	**Status read /** Reads the driving raster-row position
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**Start oscillation /** Starts the oscillation circuit
	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	**Device code read /** Read 0110H
R01h	0	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0	**Driver output control /** SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction NL4-0: number of driving lines
R02h	0	1	0	0	0	0	FLD1	FDL0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	**LCD-Driving-waveform control /** FLD1-0: number of interlaced field B/C: LCD drive AC waveform NW5-0: number of n-raster-row of C-pattern
R03h	0	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB	**Power control 1 /** SAP2-0: BT2-0: DC2-0: AP2-0: SLP: STB:
R04h	0	1	CAD	0	0	VRN4	VRN3	VRN2	VRN1	VRN0	0	0	0	VRP4	VRP3	VRP2	VRP1	VRP0	**Power control 2 /** CAD: VRN4-0: VRP4-0:
R05h	0	1	0	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	**Entry mode /** BGR: HWM: I/D1-0: AM: LG2-0:
R06h	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	**Compare register /**
R07h	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0	**Display control /** PT1-0: VLE2-1: SPT: GON: DTE: CL: REV: D1-0:
R08h	0	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0	**Blank period control 1/ BP3-0: Back porch setting FP3-0: Front porch setting**
R09h	0	1	0	0	0	0	BLP13	BLP12	BLP11	BLP10	BLP23	BLP22	BLP21	BLP20	0	0	0	0	**Blank period control 2/**
R0Bh	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	**Frame cycle control /** NO1-0: SDT1-0: EQ1-0: DVI1-0: RTN3-0:
R0Ch	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	**Power control 3 /** VC2-0:
R0Dh	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0	**Power control 4 /** VRL3-0: PON: VRH3-0:
R0Eh	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0	**Power control 5 /** VCOMG: VDV4-0: VCM4-0:
R0Fh	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0	**Gate scan position /** SCN4-0: scan starting position of gate

Preliminary

Table 17. Instruction table 2

Reg. No	R/W	RS	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Register Name / Description
R11h	0	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	**Vertical scroll control /** VL7-0:
R14h	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	**1st screen driving position /** SE17-10: SS17-10
R15h	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	**2nd screen driving position /** SE27-20: SS27-20
R16h	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**Horizontal RAM Address position /** HEA7-0: HSA7-0
R17h	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	**Vertical RAM Address position /** HEA7-0: HSA7-0
R20h	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	**RAM write data mask /** WM15-0:
R21h	0	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	**RAM address set /** AD15-0:
R22h	0	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	**Write data to GRAM /** WD15-0:
	1	1	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**Read data from GRAM /** RD15-0:
R30h	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00	**Gamma control 1 /** Adjust Gamma voltage
R31h	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20	**Gamma control 2 /** Adjust Gamma voltage
R32h	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40	**Gamma control 3 /** Adjust Gamma voltage
R33h	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00	**Gamma control 4 /** Adjust Gamma voltage
R34h	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00	**Gamma control 5 /** Adjust Gamma voltage
R35h	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20	**Gamma control 6 /** Adjust Gamma voltage
R36h	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40	**Gamma control 7 /** Adjust Gamma voltage
R37h	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00	**Gamma control 8 /** Adjust Gamma voltage

INSTRUCTION DESCRIPTIONS

Index

The index instruction specifies the RAM control indexes (R00h to R3Fh). It sets the register number in the range of 00000 to 111111 in binary form. However, R40 to R44 are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction read out the internal status of the IC.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the Halt State in the standby mode. After this instruction, wait at least 10 ms for oscillation to stabilize before giving the next instruction. (See the Standby Mode section)
If this register is read forcibly, *0110H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G176. When GS = 1, G176 shifts to G1.

SM: Select the division drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S396. When SS = 1, S396 shifts to S1. When SS = 0, <R><G><B> color is assigned from S1. When SS = 1, <R><G><B> color is assigned from S396. Re-write to the RAM when intending to change the SS bit.

NL4–0: Specify number of lines for the LCD drive. Number of lines for the LCD drive can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio. Select the set value for the panel size or higher.

Table 18. NL bit and Drive Duty (SCN4-0=00000)

NL4	NL3	NL2	NL1	NL0	Display size	Number of LCD driver lines	Gate driver used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	396 X 16 dots	16	G1 to G16
0	0	0	1	0	396 X 24 dots	24	G1 to G24
0	0	0	1	1	396 X 32 dots	32	G1 to G32
0	0	1	0	0	396 X 40 dots	40	G1 to G40
0	0	1	0	1	396 X 48 dots	48	G1 to G48
0	0	1	1	0	396 X 56 dots	56	G1 to G56
0	0	1	1	1	396 X 64 dots	64	G1 to G64
0	1	0	0	0	396 X 72 dots	72	G1 to G72
0	1	0	0	1	396 X 80 dots	80	G1 to G80
0	1	0	1	0	396 X 88 dots	88	G1 to G88
0	1	0	1	1	396 X 96 dots	96	G1 to G96
0	1	1	0	0	396 X 104 dots	104	G1 to G104
0	1	1	0	1	396 X 112 dots	112	G1 to G112
0	1	1	1	0	396 X 120 dots	120	G1 to G120
0	1	1	1	1	396 X 128 dots	128	G1 to G128
1	0	0	0	0	396 X 136 dots	136	G1 to G136
1	0	0	0	1	396 X 144 dots	144	G1 to G144
1	0	0	1	0	396 X 152 dots	152	G1 to G152
1	0	0	1	1	396 X 160 dots	160	G1 to G160
1	0	1	0	0	396 X 168 dots	168	G1 to G168
1	0	1	0	1	396 X 176 dots	176	G1 to G176

NOTE: Blank period (All gates output Vgoff level) have to be inserted after all gates are scanned.

LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	FLD 1	FLD 0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

FLD1-0: These bits are for the set up of the interlaced driver' s n raster-row. See the following table and figure for the set up value and field raster-row and scanning method.

Table 19. Association chart for scanning FLD1-0 and n raster-row

FLD1	FLD0	Scanning method
0	0	Set up disabled
0	1	1 field
1	0	Set up disabled
1	1	3 field (interlaced)

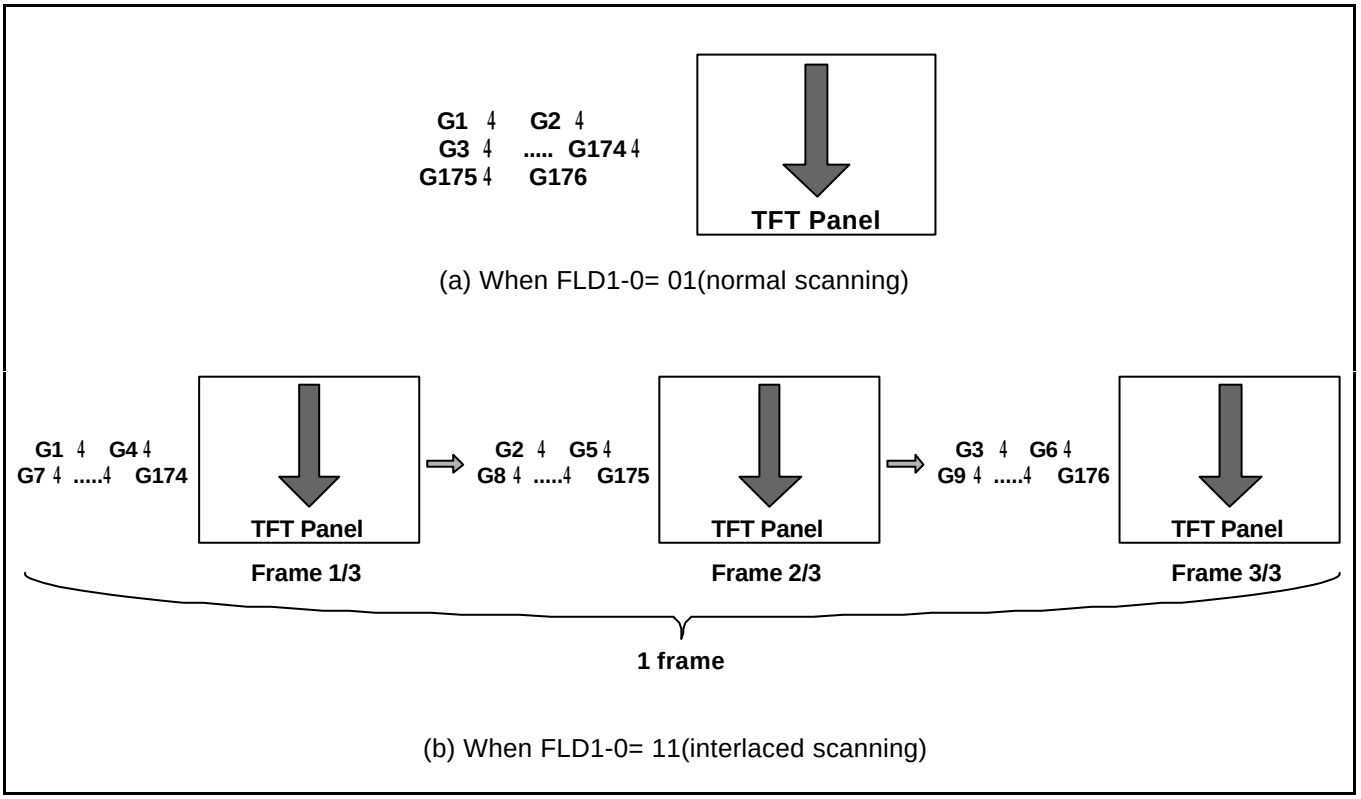


Figure 8. n raster-row interlaced scanning method

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a n raster-row waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register (R02h). For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed(Exclusive-OR) for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive raster-row and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows that will alternate in the C-pattern waveform setting (B/C = 1).
NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Power Control 1 (R03h)
Power Control 2 (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	SAP 2	SAP 1	SAP 0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
W	1	CAD	0	0	VRN 4	VRN 3	VRN 2	VRN 1	VRN 0	0	0	0	VRP 4	VRP 3	VRP 2	VRP 1	VRP 0

SAP2-0: The amount of fixed current from the fixed current source in the operational amplifier for the source driver is adjusted. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when SAP2-0 = "000", the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SAP2	SAP1	SAP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier and step-up circuit stops.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

BT2–0: The output factor of step-up is switched. Adjust scale factor of the step-up circuit by the voltage used. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

BT2	BT1	BT0	VLOUT1 Output	VLOUT2 Output	Notes*
0	0	0	2 X Vci1	3 X Vci2	VLOUT2 = Vci1 X six times
0	0	1	2 X Vci1	4 X Vci2	VLOUT2 = Vci1 X eight times
0	1	0	3 X Vci1	3 X Vci2	VLOUT2 = Vci1 X nine times
0	1	1	3 X Vci1	2 X Vci2	VLOUT2 = Vci1 X six times
1	0	0	2 X Vci1	Vci1 + 2 X Vci2	VLOUT2 = Vci1 X five times
1	0	1	2 X Vci1	Vci1 + 3 X Vci2	VLOUT2 = Vci1 X seven times
1	1	0	Step-up stopped	3 X Vci2	VLOUT2 = Vci2 X three times
1	1	1	Step-up stopped	4 X Vci2	VLOUT2 = Vci2 X four times

Notes: The step-up factors of VLOUT2 are derived from Vci1 when VLOUT1 and Vci2 are shorted. The conditions of VLOUT1 5.5V and VLOUT2 15.0V must be satisfied.

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit1	Step-up Cycle in Step-up Circuit 2/3/4
0	0	0	DCCLK / 1	DCCLK / 4
0	0	1	DCCLK / 2	DCCLK / 4
0	1	0	DCCLK / 4	DCCLK / 4
0	1	1	DCCLK / 2	DCCLK / 16
1	0	0	DCCLK	DCCLK / 8
1	0	1	DCCLK / 2	DCCLK / 8
1	1	0	DCCLK / 4	DCCLK / 8
1	1	1	DCCLK / 4	DCCLK / 16

AP2–0: The amount of fixed current in the operational amplifier for the power supply can be adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = "000", the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier and step-up circuit stops.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

SLP: When SLP = 1, the S6D0110 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

– Power control (BT2–0, DC3–0, AP2–0, SLP, STB, VC2-0, CAD, VR3-0, VRL3-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained and G1 to G228 output is fixed to VSS level, and register set-up is protected (maintained).

STB: When STB = 1, the S6D0110 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

- Standby mode cancel(STB = " 0')
- Start oscillation

CAD: Set this bit according to the structure for the TFT-display retention volume.
CAD = 0: Set this bit when the Cst retention volume is structured. In this case, Vgoff level is fixed to VgoffL level regardless of the Vcom alternating drive.
CAD = 1: Set this bit when the Cadd retention volume is structured. At the Vcom alternating drive, the Vgoff voltage is output in the VgoffL voltage reference by the amount of Vcom alternating amplitude.

VRP4-0: Control oscillation (positive polarity) of 64-grayscale. For details, see the Oscillation Adjusting Circuit section.

VRN4-0: Control oscillation (negative polarity) of 64-grayscale. For details, see the Oscillation Adjusting Circuit section.

Power Control 3 (R0Ch)
Power Control 4 (R0Dh)
Power Control 5 (R0Eh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	Vc0
W	1	0	0	0	0	VRL 3	VRL 2	VRL 1	VRL 0	0	0	0	PON	VRH 3	VRH 2	VRH 1	VRH 0
W	1	0	0	VCO MG	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0

VC2-0: Adjust reference voltage of VREG1, VREG2OUT and Vciout to optional rate of Vci. Also, when VC2 = " 1", it is possible to stop the internal reference voltage generator. This leads to optional power on for VREG1OUT/Vciout with REGP and VREG2OUT with REGN externally.

VC2	VC1	VC0	Internal Reference Voltage (REGP) of VREG1OUT and Vciout	Internal Reference Voltage (REGN) of VREG2OUT
0	0	0	0.92 X Vci	0.08 X Vci
0	0	1	0.83 X Vci	0.17 X Vci
0	1	0	0.73 X Vci	0.27 X Vci
0	1	1	0.68 X Vci	0.32 X Vci
1	0	0	Vci	VSS
1	*	*	Stops generation of the internal reference voltages of VREG1OUT and Vciout (REGP can be input externally)	Stops generation of the internal reference voltage of VREG2OUT (REGN can be input externally).

Notes: Leave these settings open because the voltage other than that for halting the internal circuit is output for REGP and REGN.

VRL3-0: Set magnification of amplification for VREG2OUT voltage (voltage for the reference voltage, VREG2 while generating Vgoffout.) It allows magnifying the amplification of REGN from 2 to 8.5 times.

VRL 3	VRL 2	VRL 1	VRL 0	VREG2OUT Voltage	VRL 3	VRL 2	VRL 1	VRL 0	VREG2OUT Voltage
0	0	0	0	-(Vci – REGN) X 3.0	1	0	0	0	-(Vci – REGN) X 6.5
0	0	0	1	-(Vci – REGN) X 3.5	1	0	0	1	-(Vci – REGN) X 7.0
0	0	1	0	-(Vci – REGN) X 4.0	1	0	1	0	-(Vci – REGN) X 7.5
0	0	1	1	-(Vci – REGN) X 4.5	1	0	1	1	-(Vci – REGN) X 8.0
0	1	0	0	-(Vci – REGN) X 5.0	1	1	0	0	-(Vci – REGN) X 8.5
0	1	0	1	-(Vci – REGN) X 5.5	1	1	0	1	-(Vci – REGN) X 9.0
0	1	1	0	-(Vci – REGN) X 6.0	1	1	1	0	-(Vci – REGN) X 9.5
0	1	1	1	Stopped	1	1	1	1	Stopped

Notes:
1. These settings apply when the internal reference-voltage generation circuit is stopped and the VREG2OUT voltage is generated specifying REGN as the reference voltage.
2. Adjust the settings between the voltage set by (Vci – VC2-0) or the (Vci – REGN) voltage and VRL0 to VRL3 so that the VREG2OUT voltage is higher than –16.0 V.
3. The VREG2OUT voltage is the factor when Vci is the reference voltage.

PON: This is an operation-starting bit for the booster circuit 4. PON = 0 is to stop and PON = 1 to start operation. For further information about timing for adjusting to the PON = 1, please refer to the set up flow of power supply circuit.

VRH3-0: Set the amplified factor of the VREG1OUT voltage (the voltage for the reference voltage, VREG2 while generating VgoffOUT). It allows to amplify from 1.45 to 2.85 times of REGN input voltage.

VRH 3	VRH 2	VRH 1	VRH 0	VREG1OUT Voltage	VRH 3	VRH 2	VRH 1	VRH 0	VREG1OUT Voltage
0	0	0	0	REGP X 1.45 times	1	0	0	0	REGP X 2.175 times
0	0	0	1	REGP X 1.55 times	1	0	0	1	REGP X 2.325 times
0	0	1	0	REGP X 1.65 times	1	0	1	0	REGP X 2.475 times
0	0	1	1	REGP X 1.75 times	1	0	1	1	REGP X 2.625 times
0	1	0	0	REGP X 1.80 times	1	1	0	0	REGP X 2.700 times
0	1	0	1	REGP X 1.85 times	1	1	0	1	REGP X 2.775 times
0	1	1	0	REGP X 1.90 times	1	1	1	0	REGP X 2.850 times
0	1	1	1	Stopped	1	1	1	1	Stopped

Notes:

1. These settings apply when the internal reference-voltage generation circuit is stopped and the VREG1OUT voltage is generated specifying REGP as the reference voltage.
2. Adjust the settings between the voltage set by VC2-0 or the REGP voltage and VRH0 to VRH3 so that the VREG1OUT voltage is lower than 5.0 V.

VCOMG: When VCOMG = 1, VcomL voltage can output to negative voltage (-5V).
When VCOMG = 0, VcomL voltage becomes VSS and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, When VCOMG = 0 and when Vcom is driven in A/C, set up of the VDV4-0 is invalid. In this case, adjustment of Vcom/Vgoff A/C oscillation must be adjusted VcomH with VCM4-0.

VDV4-0: Set the alternating amplitudes of Vcom and Vgoff at the Vcom alternating drive. These bits amplify Vcom and Vgoff 0.6 to 1.23 times the VREG1 voltage. When the Vcom alternation is not driven, the settings become invalid.

VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	Vcom Amplitude	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	Vcom Amplitude
0	0	0	0	0	VREG1 X 0.60	1	0	0	0	1	VREG1 X 1.08
0	0	0	0	1	VREG1 X 0.63	1	0	0	1	0	VREG1 X 1.11
0	0	0	1	0	VREG1 X 0.66	1	0	0	1	1	VREG1 X 1.14
:	:	:	:	:	:	1	0	1	0	0	VREG1 X 1.17
0	1	1	0	0	VREG1 X 0.96	1	0	1	0	1	VREG1 X 1.20
0	1	1	0	1	VREG1 X 0.99	1	0	1	1	0	VREG1 X 1.23
0	1	1	1	0	VREG1 X 1.02	1	0	1	1	1	Setting Inhibited
0	1	1	1	1	Setting Inhibited	1	1	*	*	*	Setting Inhibited
1	0	0	0	0	VREG1 X 1.05						

Notes : Adjust the settings between VREG1 and VDV0 to VDV4 so that the Vcom and Vgoff amplitudes are lower than 6.0 V.

VCM4-0: Set the VcomH voltage (a high-level voltage at the Vcom alternating drive). These bits amplify the VcomH voltage 0.4 to 0.98 times the VREG1 voltage. When VCOM4-0 = 1, the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH Voltage
0	0	0	0	0	VREG1 X 0.40 times
0	0	0	0	1	VREG1 X 0.42 times
0	0	0	1	0	VREG1 X 0.44 times
:	:	:	:	:	:
0	1	1	0	0	VREG1 X 0.64 times
0	1	1	0	1	VREG1 X 0.66 times
0	1	1	1	0	VREG1 X 0.68 times
0	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.
1	0	0	0	0	VREG1 X 0.70 times
1	0	0	0	1	VREG1 X 0.72 times
1	0	0	1	0	VREG1 X 0.74 times
:	:	:	:	:	:
1	1	1	0	0	VREG1 X 0.94 times
1	1	1	0	1	VREG1 X 0.96 times
1	1	1	1	0	VREG1 X 0.98 times
1	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.

Notes: Adjust the settings between VREG1 and VCM0 to VCM4 so that the VcomH voltage is lower than GVDD.

Preliminary

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

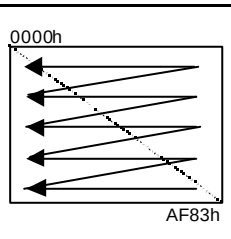
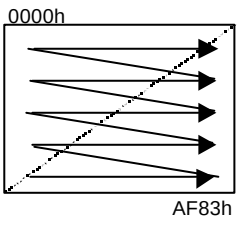
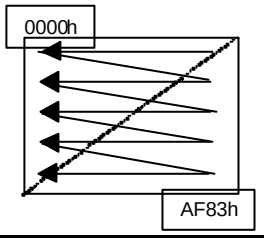
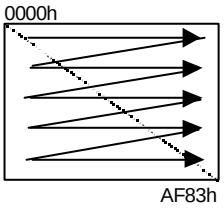
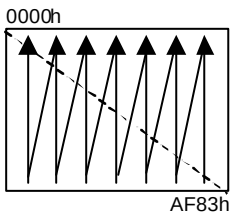
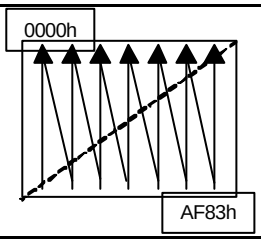
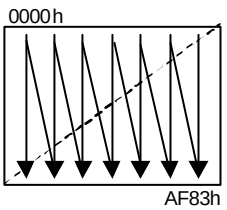
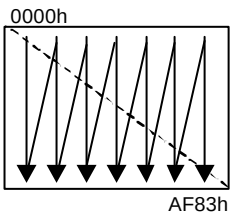
The write date sent from the microcomputer is modified in the S6D0110 written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation at the writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see the High Speed RAM Write Mode section.

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decreased by 1 after the data is written to the GRAM. Automatic address counter updating is not performed when reading data from GRAM. The increment/decrement setting of the address counter by I/D1-0 is performed independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the GRAM is written.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

Table 20. Address Direction Setting

	I/D1-0=" 00" H: decrement V: decrement	I/D1-0=" 01" H: increment V: increment	I/D1-0=" 10" H: decrement V: increment	I/D1-0=" 11" H: increment V: increment
AM=0 Horizontal				
AM=1 Vertical				

Preliminary

BGR: When 16-bit data is written to GRAM, bit-order of the data can be reversed by use of this bit. Therefore, bit-order of the data is set to be <R><G><B> when BGR is 0, <B><G><R> when BGR is 1.
Please be aware that setting BGR to 1 will convert the order of the CP15-0 and WM15-0 bits in the same way.

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP7–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP15–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

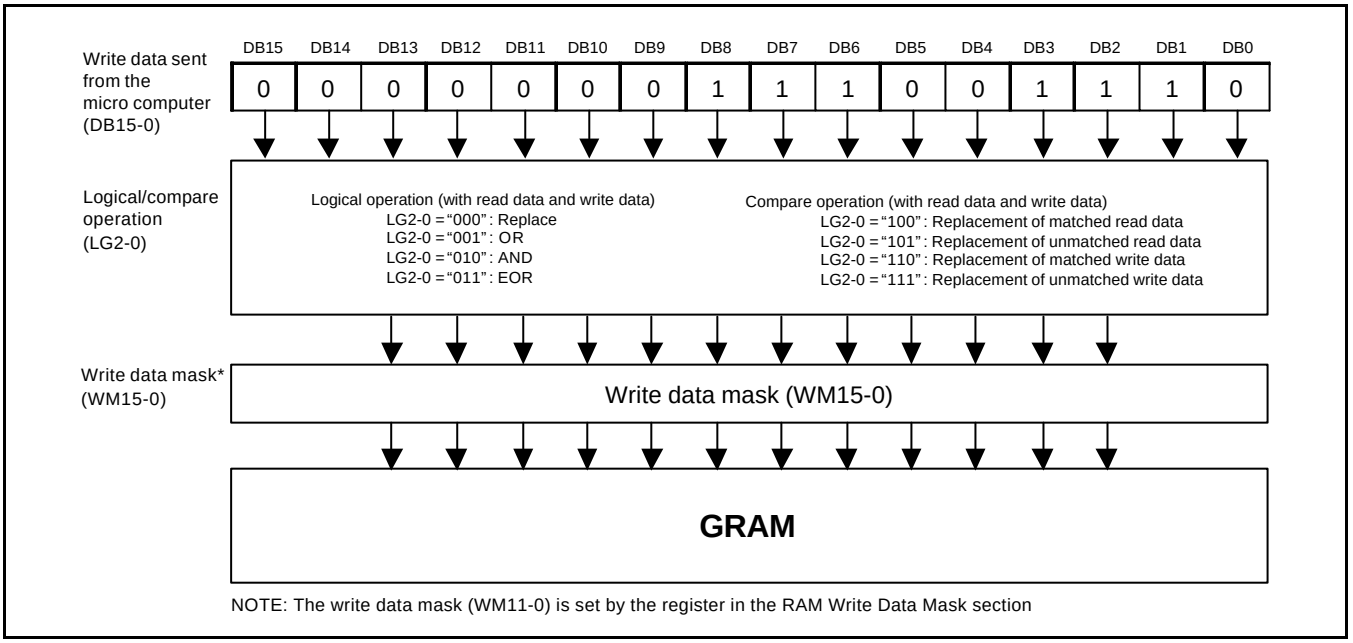


Figure 9. Logical/compare operation

Display Control (R07h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the Screen-division Driving Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll display
1	0	Scroll display	Fixed display
1	1	Setting disabled	Setting disabled

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

GON: Gate off level is set to be VSS when GON = 0.
When GON= 0 and DISPTMG= 0, G1 to G176 output is fixed to VSS level. When GON= 1, G1 to G176 output is fixed to VGH or Vgoff level. See the instruction set up flow for further description on the display on/off flow.

GON	Gate output
0	VGH/VSS
1	VGH/Vgoff

DTE: DISPTMG output is fixed to VSS when DTE = 0.

DTE	DISPTMG output
0	Halt (VSS)
1	Operation (VDD/VSS)

CL: When CL = 1, number of display is 8-color mode. For details, see the 8-color Display Mode.

CL	Number of display colors
0	65,536 colors
1	8 colors

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

1) Combination with the partial display

REV	GRAM data	Source output level							
		Display data		Non-display area					
				PT1-0=(0,1)		PT1-0=(1,0)		PT1-0=(1,1)	
		Vcom=L	Vcom=H	Vcom=L	Vcom=H	Vcom=L	Vcom=H	Vcom=L	Vcom=H
0	16'h0000 : 16'hFFFF	V63 : V0	V0 : V63	V63	V0	VSS	VSS	Hi-z	Hi-z
1	16'h0000 : 16'hFFFF	V0 : V63	V63 : V0	V63	V0	VSS	VSS	Hi-z	Hi-z

2) Combination with the D1-0

REV	GRAM data	Source output level							
		D1-0=(1,1)		D1-0=(1,0)		D1-0=(0,1)		D1-0=(0,0)	
		Vcom=L	Vcom=H	Vcom=L	Vcom=H	Vcom=L	Vcom=H	Vcom=L	Vcom=H
0	16'h0000 : 16'hFFFF	V63 : V0	V0 : V63	V63	V0	VSS	VSS	VSS	VSS
1	16'h0000 : 16'hFFFF	V0 : V63	V63 : V0	V63	V0	VSS	VSS	VSS	VSS

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0110 can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE. For details, see the Instruction Set Up Flow.

When D1–0 = 01, the internal display of the S6D0110 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	Source output	S6D0110 internal display operation	Master/slave signal (CL1, FLM, M, DISPTMG)
0	0	VSS	Halt	Halt
0	1	VSS	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Notes:

1. Writing from the microcomputer to the GRAM is independent from D1–0.
2. In sleep and standby mode, D1–0 = 00. However, the register contents of D1–0 are not modified.

Preliminary

Blanking period control 1 (R08h)

Blanking period control 2 (R09h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
W	1	0	0	0	0	BLP13	BLP12	BLP11	BLP10	BLP23	BLP22	BLP21	BLP20	0	0	0	0

The blanking period in the front and end of the display area can be defined using this register.
When N-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h). In interlace drive mode, Blank period can be adjusted using BLP13-0 and BLP23-0 bit (R09h).the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

FP3	FP2	FP1	FP0	Blanking period	BP3	BP2	BP1	BP0	Blanking period
0	0	0	0	0 raster-row	0	0	0	0	0 raster-row
0	0	0	1	1 raster-row	0	0	0	1	1 raster-row
0	0	1	0	2 raster-row	0	0	1	0	2 raster-row
0	0	1	1	3 raster-row	0	0	1	1	3 raster-row
0	1	0	0	4 raster-row	0	1	0	0	4 raster-row
0	1	0	1	5 raster-row	0	1	0	1	5 raster-row
0	1	1	0	6 raster-row	0	1	1	0	6 raster-row
0	1	1	1	7 raster-row	0	1	1	1	7 raster-row
1	0	0	0	8 raster-row	1	0	0	0	8 raster-row
1	0	0	1	9 raster-row	1	0	0	1	9 raster-row
1	0	1	0	10 raster-row	1	0	1	0	10 raster-row
1	0	1	1	11raster-row	1	0	1	1	11raster-row
1	1	0	0	12 raster-row	1	1	0	0	12 raster-row
1	1	0	1	13 raster-row	1	1	0	1	13 raster-row
1	1	1	0	14 raster-row	1	1	1	0	14 raster-row
1	1	1	1	15 raster-row	1	1	1	1	15 raster-row

BLP13	BLP12	BLP11	BLP10	Blanking period	BLP23	BLP22	BLP21	BLP20	Blanking period
0	0	0	0	0 raster-row	0	0	0	0	0 raster-row
0	0	0	1	1 raster-row	0	0	0	1	1 raster-row
0	0	1	0	2 raster-row	0	0	1	0	2 raster-row
0	0	1	1	3 raster-row	0	0	1	1	3 raster-row
0	1	0	0	4 raster-row	0	1	0	0	4 raster-row
0	1	0	1	5 raster-row	0	1	0	1	5 raster-row
0	1	1	0	6 raster-row	0	1	1	0	6 raster-row
0	1	1	1	7 raster-row	0	1	1	1	7 raster-row
1	0	0	0	8 raster-row	1	0	0	0	8 raster-row
1	0	0	1	9 raster-row	1	0	0	1	9 raster-row
1	0	1	0	10 raster-row	1	0	1	0	10 raster-row
1	0	1	1	11raster-row	1	0	1	1	11raster-row
1	1	0	0	12 raster-row	1	1	0	0	12 raster-row
1	1	0	1	13 raster-row	1	1	0	1	13 raster-row
1	1	1	0	14 raster-row	1	1	1	0	14 raster-row
1	1	1	1	15 raster-row	1	1	1	1	15 raster-row

Frame Cycle Control (R0Bh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the 1H period.

RTN3	RTN2	RTN1	RTN0	Clock cycles per raster row
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
. . .	. . .	. . .	. . .	. . .
1	1	1	0	30
1	1	1	1	31

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks, which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing number of the drive cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

DIV1	DIV0	Division Ratio	Internal operation clock frequency
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

*fosc = R-C oscillation frequency

EQ1-0: EQ period is sustained for the number of clock cycle which is set on EQ1-0. When VcomL<0, set these bits as "00" for preventing the abnormal function.

EQ1	EQ0	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc} : R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 10. Formula for the frame frequency

SDT1-0: Set delay amount from gate edge (end) to source output.

SDT1	SDT0	Delay amount of the source output
0	0	1 clock cycle
0	1	2 clock cycle
1	0	3 clock cycle
1	1	4 clock cycle

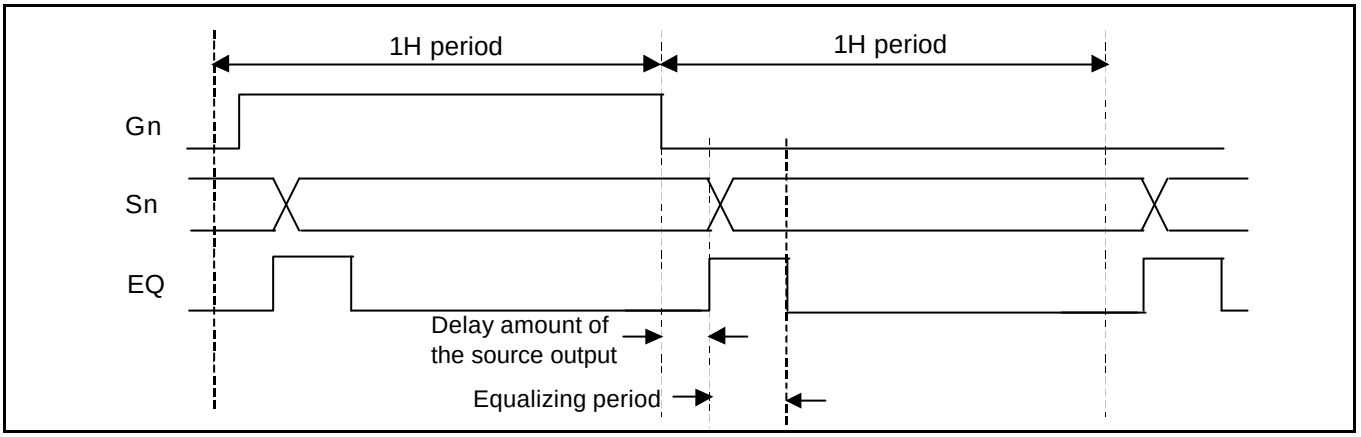


Figure 11. Set Delay from Gate Output to Source Output

NO1-0: Set amount of non-overlay for the gate output.

NO1	NO0	Amount of non-overlab
0	0	0 clock cycle
0	1	4 clock cycle
1	0	6 clock cycle
1	1	8 clock cycle

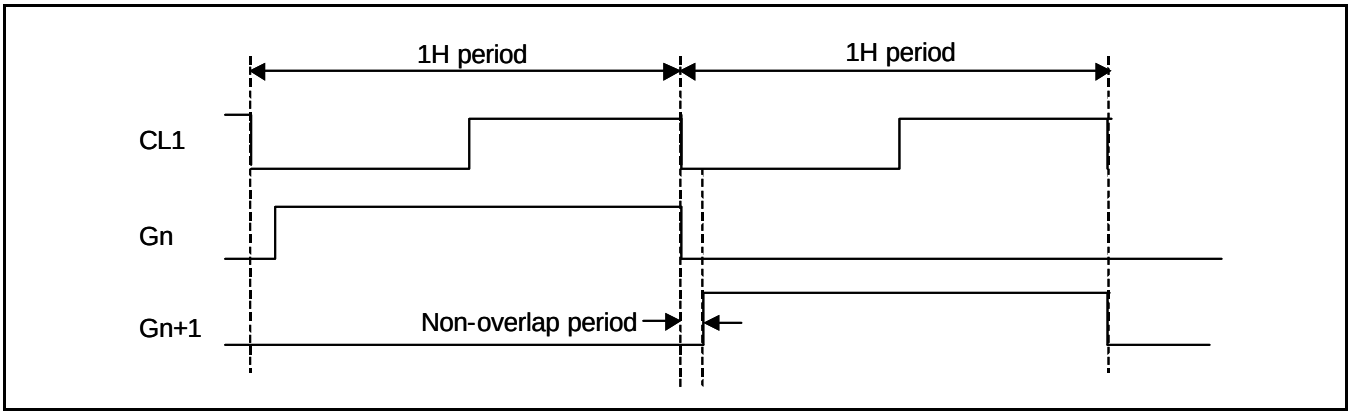


Figure 12. Non-overlap Period

Gate Scan Position (R0fh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	NO1	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN 4-0: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning start position	
					GS=0	GS=1
0	0	0	0	0	G1	G176
0	0	0	0	1	G9	G168
0	0	0	1	0	G17	G160
:	:	:	:	:	:	:
1	0	0	1	1	G153	G24
1	0	1	0	0	G161	G16
1	0	1	0	1	G169	G8

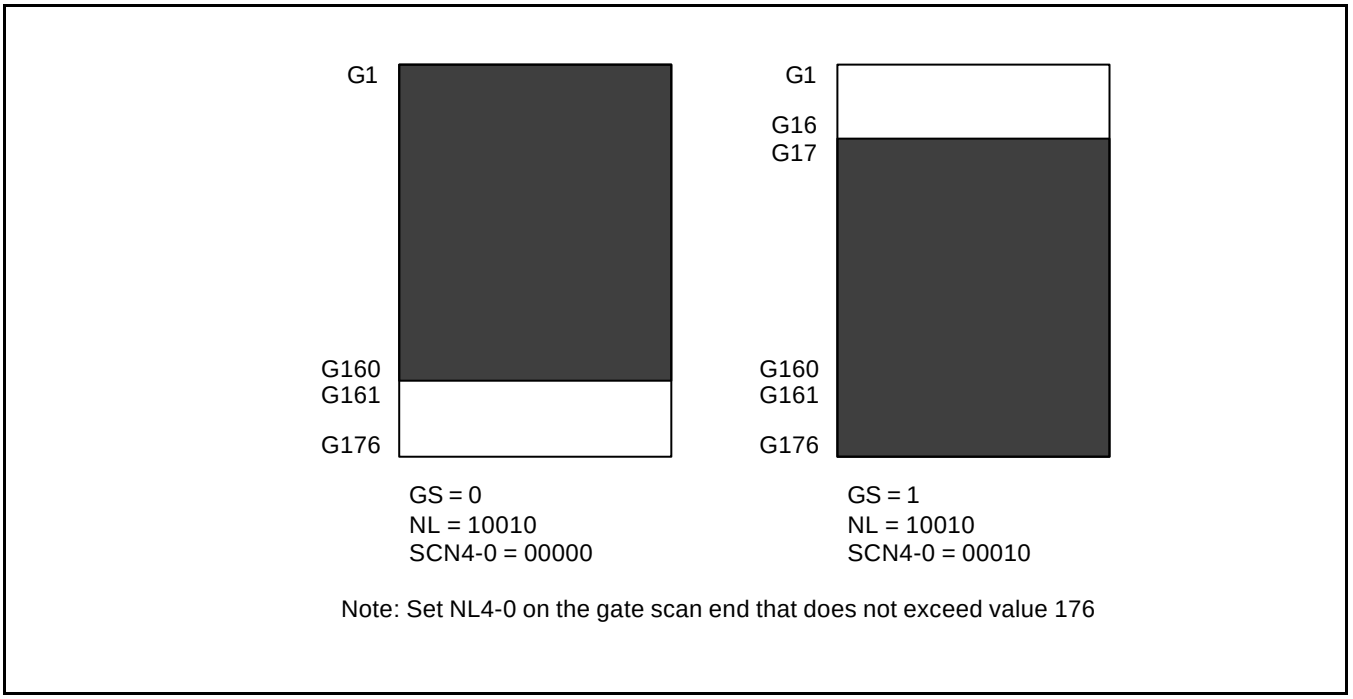


Figure 13. Relationship between NL and SCN set up value

Vertical Scroll Control (R11h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 176th can be scrolled for the number of the raster-row. After 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL7-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll length
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-row
				.				.
				.				.
				.				.
1	0	1	0	1	1	1	0	174 raster-row
1	0	1	0	1	1	1	1	175 raster-row

Note: Don't set any higher raster-row than 175 ("AF"H)

1st Screen Driving Position (R14h)
2nd Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS17–10: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value +1' common driver.

SE17–10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS17–10 = 07h and SE17–10 = 10h are set, the LCD driving is performed from G8 to G17, and black display driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFh. For details, see the Screen-division Driving Function section.

SS27–10: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver. The second screen is driven when SPT = 1.

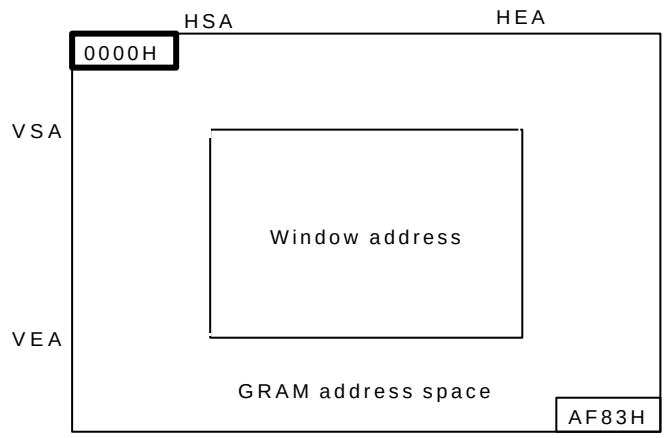
SE27–20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SPT = 1, SS27–20 = 20h, and SE27–20 = AFh are set, the LCD driving is performed from G33 to G80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ AFh. For details, see the Screen-division Driving Function section.

Horizontal Ram Address Position (R16h)
Vertical Ram Address Position (R17h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA 7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ 83h.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ AFh.



Window address setting range

"00"h £ HSA7-0 ≤ HEA7-0 ≤ "83"h
"00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"h

NOTE: 1. Ensure that the window address area is within the GRAM address space
2. In high-speed write mode, data are written to GRAM in four-words.
Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section

Figure 14. Window address setting range

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM15	WB14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14 to 0 bits mask the write data of DB14 to 0 in a bit unit. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting address. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address

AD15 to AD0	GRAM setting
"0000H" to "0083" H	Bitmap data for G1
"0100H" to "0183" H	Bitmap data for G2
"0200H" to "0283" H	Bitmap data for G3
"0300H" to "0383" H	Bitmap data for G4
: : :	: : :
"AC00H" to "AC83" H	Bitmap data for G173
"AD00H" to "AD83" H	Bitmap data for G174
"AE00H" to "AE83" H	Bitmap data for G175
"AF00H" to "AF83" H	Bitmap data for G176

Write Data to Gram (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

WD15-0: Write 16-bit data to the GRAM. This data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. During the standby mode, the GRAM cannot be accessed.

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1 pixel															

Figure 15. Write data to GRAM

Table 21. GRAM Data and Grayscale Level

GRAM data setup		Selected grayscale		GRAM data setup		Selected grayscale		GRAM data setup		Selected grayscale		GRAM data setup		Selected grayscale	
G	R/B	N	P	G	R/B	N	P	G	R/B	N	P	G	R/B	N	P
000000	00000	V0	V63	010000	01000	V16	V47	100000	-	V32	V31	110000	-	V48	V15
000001	-	V1	V62	010001	-	V17	V46	100001	10000	V33	V30	110001	11000	V49	V14
000010	00001	V2	V61	010010	01001	V18	V45	100010	-	V34	V29	110010	-	V50	V13
000011	-	V3	V60	010011	-	V19	V44	100011	10001	V35	V28	110011	11001	V51	V12
000100	00010	V4	V59	010100	01010	V20	V43	100100	-	V36	V27	110100	-	V52	V11
000101	-	V5	V58	010101	-	V21	V42	100101	10010	V37	V26	110101	11010	V53	V10
000110	00011	V6	V57	010110	01011	V22	V41	100110	-	V38	V25	110110	-	V54	V9
000110	-	V7	V56	010110	-	V23	V40	100110	10011	V39	V24	110110	11011	V55	V8
001000	00100	V8	V55	011000	01100	V24	V39	101000	-	V40	V23	111000	-	V56	V7
001001	-	V9	V54	011001	-	V25	V38	101001	10100	V41	V22	111001	11100	V57	V6
001010	00101	V10	V53	011010	01101	V26	V37	101010	-	V42	V21	111010	-	V58	V5
001011	-	V11	V52	011011	-	V27	V36	101011	10101	V43	V20	111011	11101	V59	V4
001100	00110	V12	V51	011000	01100	V28	V35	101100	-	V44	V19	111100	-	V60	V3
001101	-	V13	V50	011001	-	V29	V34	101101	10110	V45	V18	111101	11110	V61	V2
001100	00110	V14	V49	011010	01101	V30	V33	101100	-	V46	V17	111110	-	V62	V1
001101	-	V15	V48	011011	-	V31	V32	101101	10111	V47	V16	111111	11111	V63	V0

Read Data from GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

RD11–0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the S6D0110, only one read can be processed since the latched data in the first word is used.

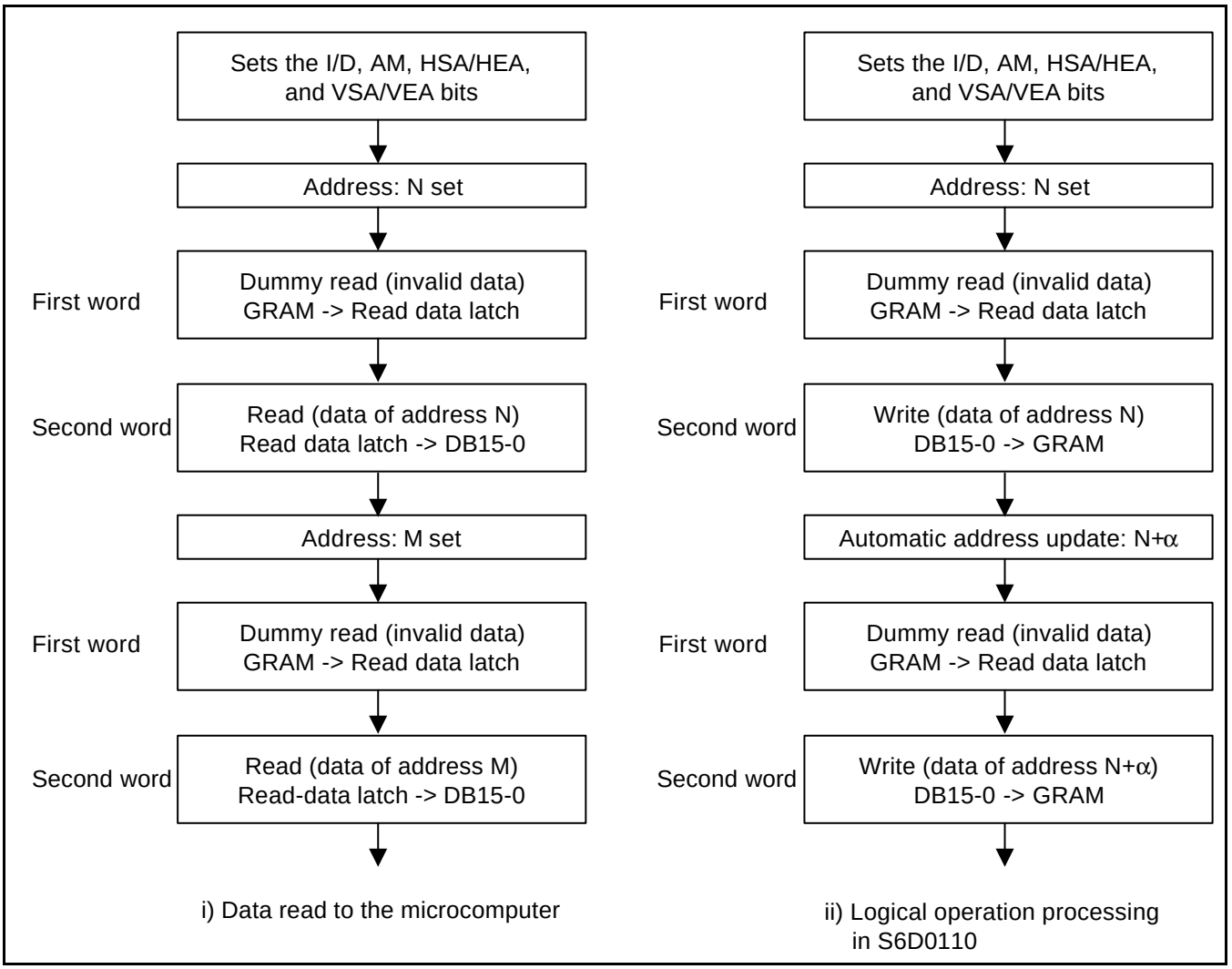


Figure 16. GRAM read sequence

Gamma Control (R30h To R37h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

PRN12-00: Gradient adjustment register for the negative polarity output

For details, see the Gamma Adjustment Function.

Preliminary

RESET FUNCTION

The S6D0110 is internally initialized by RESET input. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SS = 0, CS = 0)
3. B-pattern waveform AC drive (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Power control 1 (SAP2-0 = 000, BT2-0 = 000, DC2–0 = 000, AP2–0 = 000: LCD power off, SLP = 0, STB = 0: Standby mode off)
5. Power control 2 (CAD = 0, VRN4-0 = 00000, VRP4-0 = 00000)
6. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP15–0: 0000000000000000)
8. Display control (PT1-0 = 00, VLE2–1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL = 0: 65536 color mode, REV = 0, D1–0 = 00: Display off)
9. Display control (FP3-0=0101, BP3-0=0011, BLP13-0=0010, BLP23-0=0010)
10. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, EQ1-0 = 00: no equalizer, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clock cycle in 1H period)
11. Power control 3 (VC2-0 = 000)
12. Power control 4 (VRL3-0 = 0000, PON=0, VRH3-0 = 0000)
13. Power control 5 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
14. Gate scanning starting position (SCN4-0 = 00000)
15. Vertical scroll (VL7–0 = 0000000)
16. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
17. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
18. Horizontal RAM address position (HEA7-0 = 10000011, HSA7-0 = 00000000)
19. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
20. RAM write data mask (WM15–0 = 0000h: No mask)
21. RAM address set (AD15–0 = 0000h)
22. Gamma control
    (PKP02–00 = 000, PKP12–10 = 000, PKP22–20 = 000, PKP32–30 = 000,
    PK42–40 = 000, PKP52–50 = 000, PRP02–00 = 000, PRP12–10 = 000)
    (PKN02–00 = 000, PKN12–10 = 000, PKN22–20 = 000, PKN32–30 = 000,
    PKN42–40 = 000, PKN52–50 = 000, PRN02–00 = 000, PRN12–10 = 000)

GRAM Data Initialization

GRAM is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

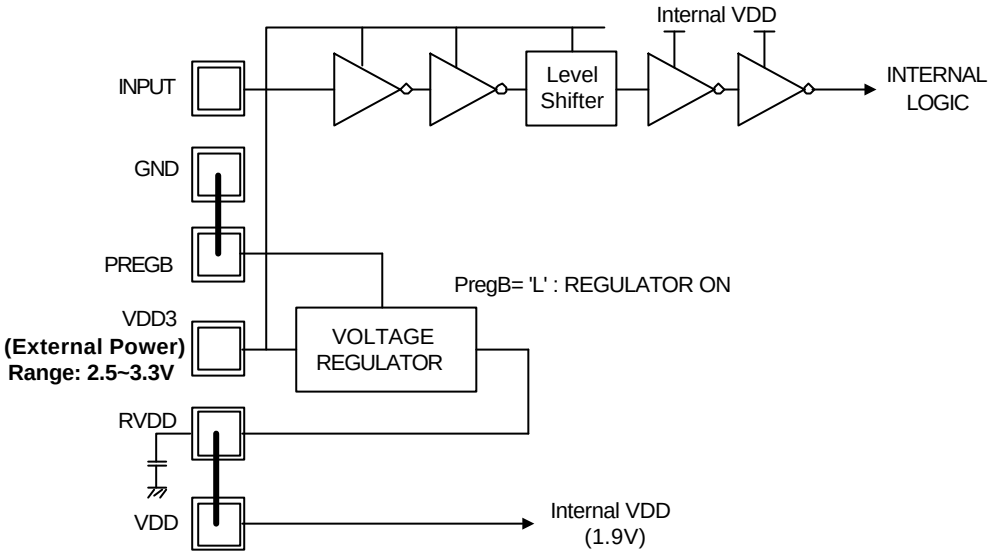
Output Pin Initialization

1. LCD driver output pins (Source output) : Output VSS level
   (Gate output) : Output Vgoff level
2. Oscillator output pin (OSC2): Outputs oscillation sign

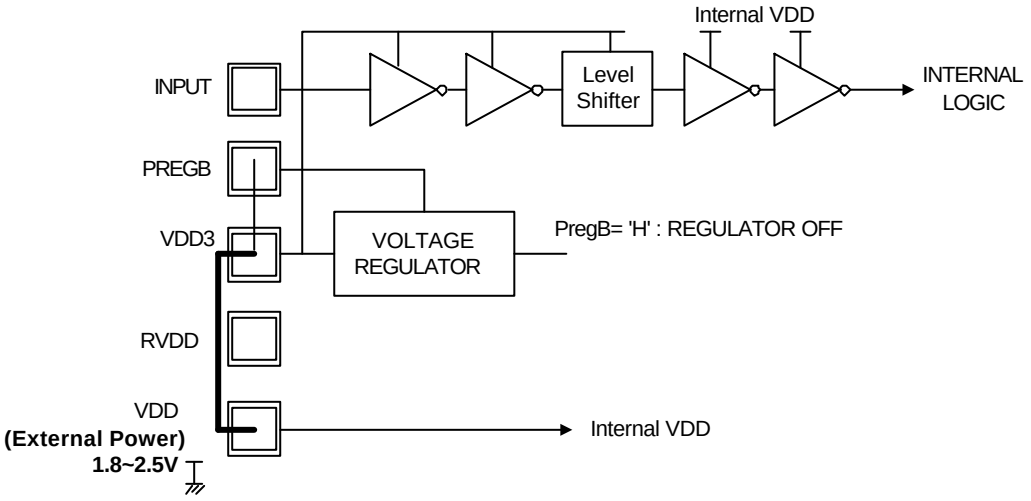
Preliminary

VOLTAGE REGULATION FUNCTION

The S6D0110 have internal voltage regulator. Voltage regulation function is controlled by PregB pin.
If PregB= " H", voltage regulation is stopped. PregB= " L" enables internal voltage regulation function.
By use of this function, internal logic circuit damage can be prohibited. Furthermore, power consumption also be obtained. Detailed function description and application setup is described in the following diagram.



(a) Voltage regulation function enabled



(b) Voltage regulation function disabled

Figure 13. Voltage regulation function

Preliminary

SYSTEM INTERFACE

System interface mode of S6D0110 can be fixed by use of IM2/1/0 pin. Instruction setting and GRAM access is executed via system interface.

Table 22. IM bits and System Interface

IM2	IM1	IM0	System Interface	DB Pin
0	0	0	68-system 16-bit interface	DB15 ~ 0
0	0	1	68-system 8-bit interface	DB15 ~ 8
0	1	0	80-system 16-bit interface	DB15 ~ 0
0	1	1	80-system 8-bit interface	DB15 ~ 8
1	0	*	Serial peripheral interface (SPI)	DB1 ~ 0
1	1	*	Setting disabled	-
*	*	*	Setting disabled	-

PARALLEL DATA TRANSFER

16-BIT BUS INTERFACE

Setting the IM2/1/0 (interface mode) to the VSS/VSS/VSS level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the VSS/VDD3/VSS level allows 80-system 16-bit parallel data transfer. When the number of bus or the mounting area is limited, use an 8-bit bus interface.

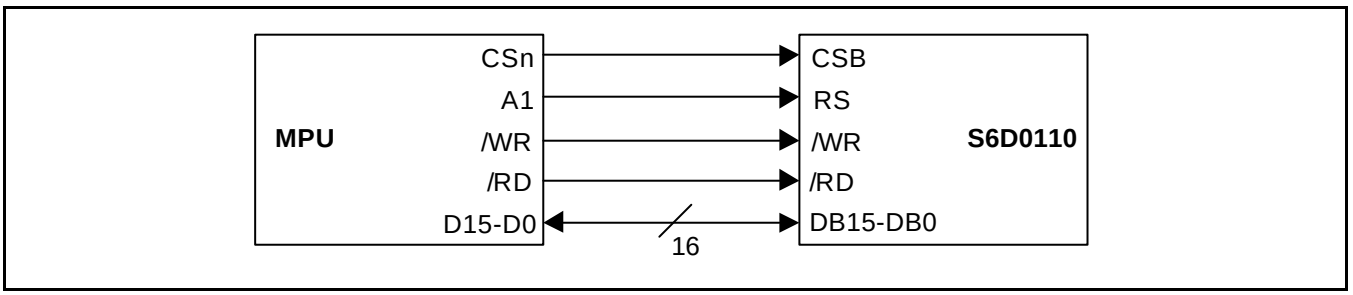


Figure 17. Interface to 16-bit microcomputer

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8-BIT BUS INTERFACE

Setting the IM2/1/0 (interface mode) to the VSS/VSS/VDD3 level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM2/1/0 to the VSS/VDD3/VDD3 level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into upper/lower eight bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the VDD3 or VSS level. Note that the upper bytes must also be written when the index register is written.

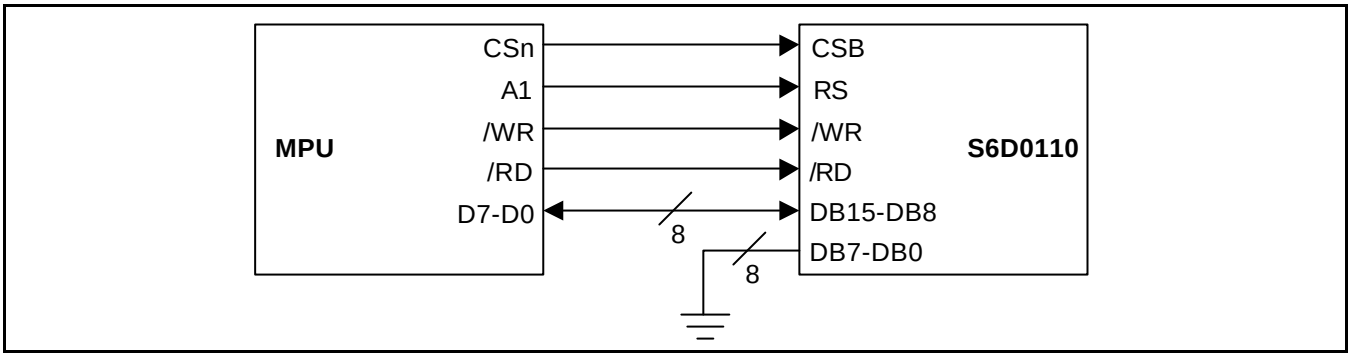

Figure 18. Interface to 8-bit microcomputer

Note: The S6D0110 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system

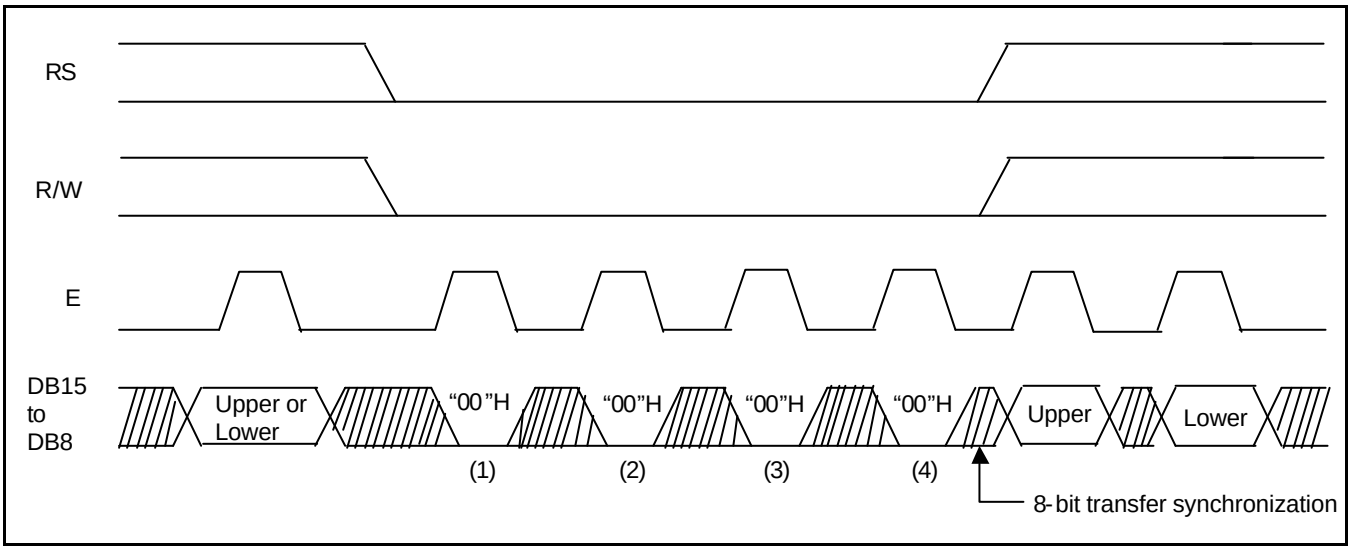

Figure 19. 8-bit transfer synchronization

Preliminary

SERIAL DATA TRANSFER

Setting the IM2/1 pin to the VDD3/VSS level allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins that are not used must be fixed at VDD3 or VSS.

The S6D0110 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The S6D0110 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the S6D0110. When selected, the S6D0110 receives the subsequent data string. The LSB of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single S6D0110 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the S6D0110 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All S6D0110 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The S6D0110 starts to read correct RAM data from the fifth byte.

Table 23. Start Byte Format

Transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

NOTE: ID bit is selected by the IM0/ID pin.

Table 24. RS and R/W Bit Function

RS	RW	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

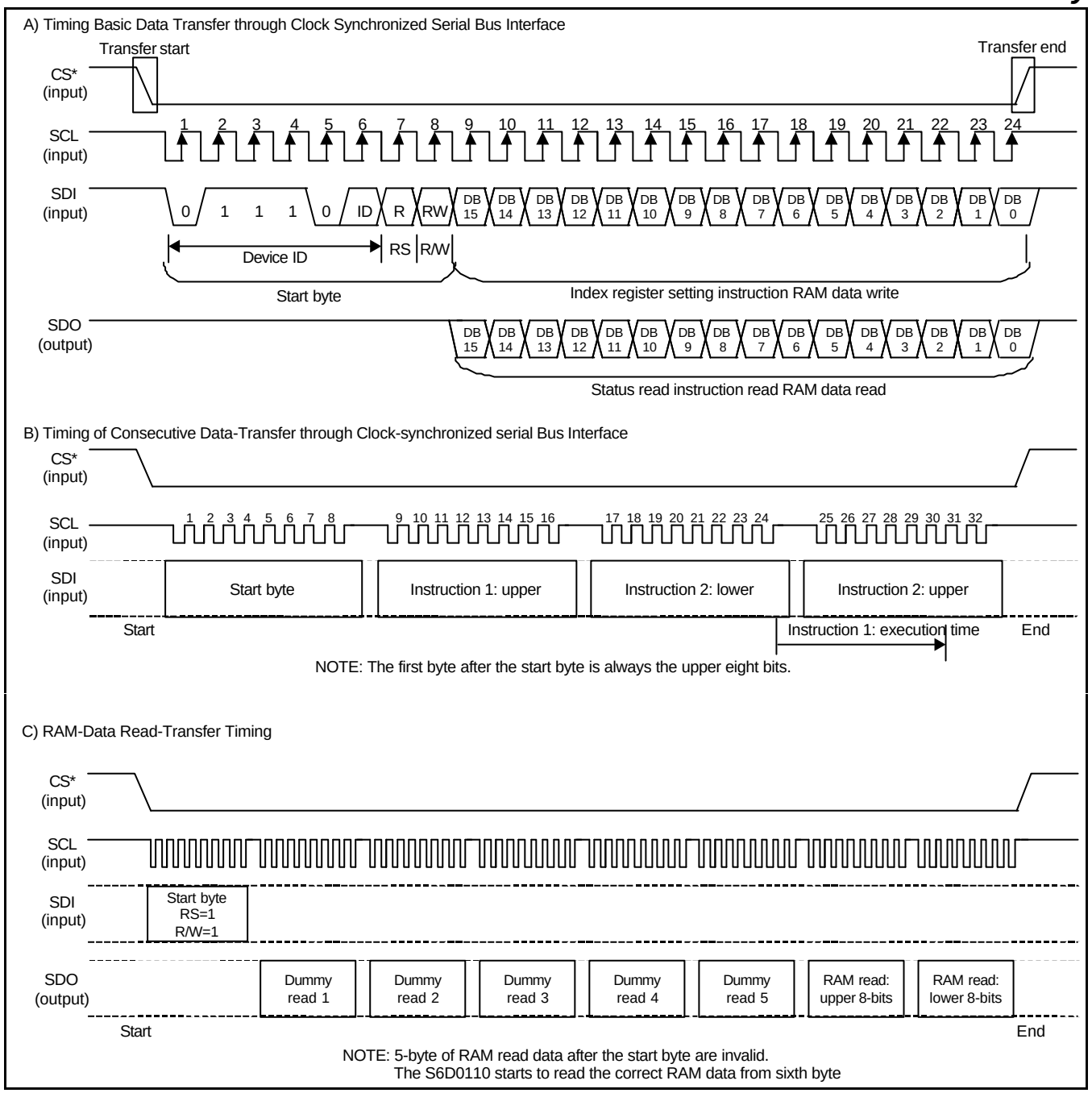

Figure 20. Procedure for transfer on clock synchronized serial bus interface

Preliminary

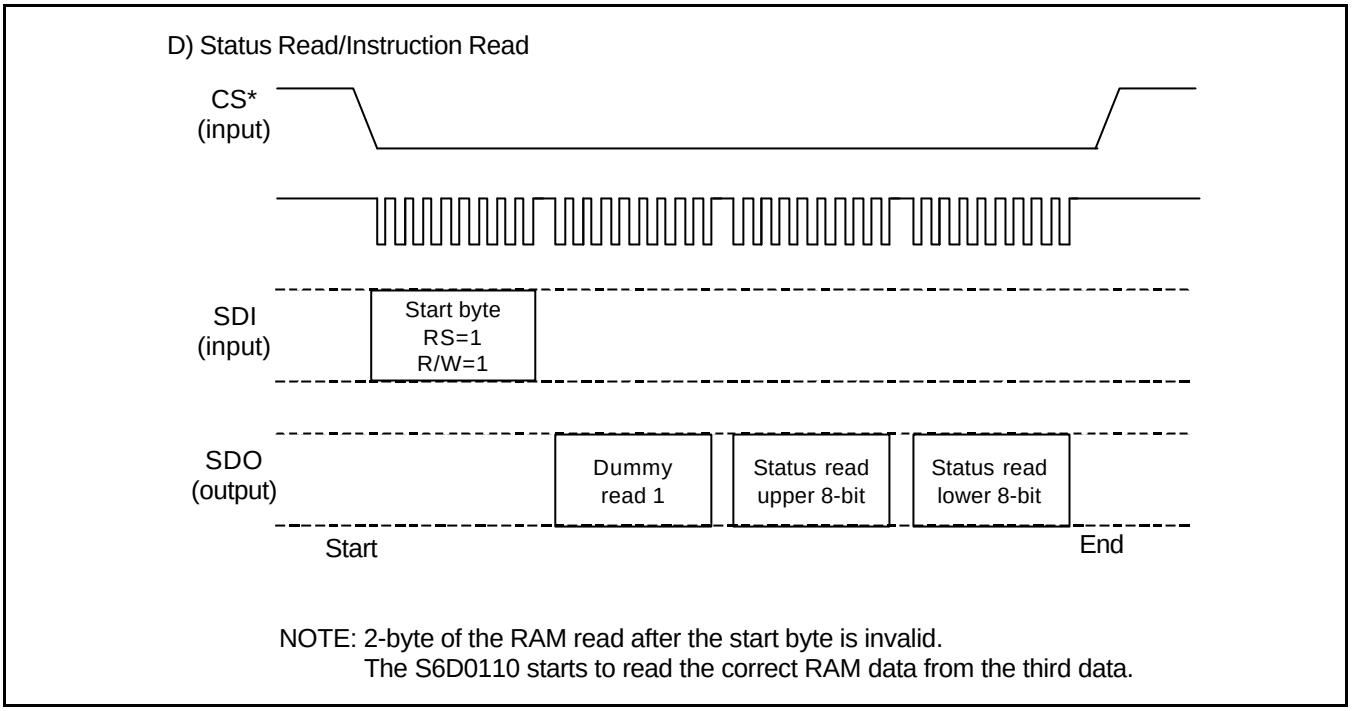

Figure 21. Procedure for transfer on clock synchronized serial bus interface (continued)

Preliminary

HIGH-SPEED BURST RAM WRITE FUNCTION

The S6D0110 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications that require the high-speed rewriting of the display data, for example, display of color animations, etc. When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the S6D0110 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

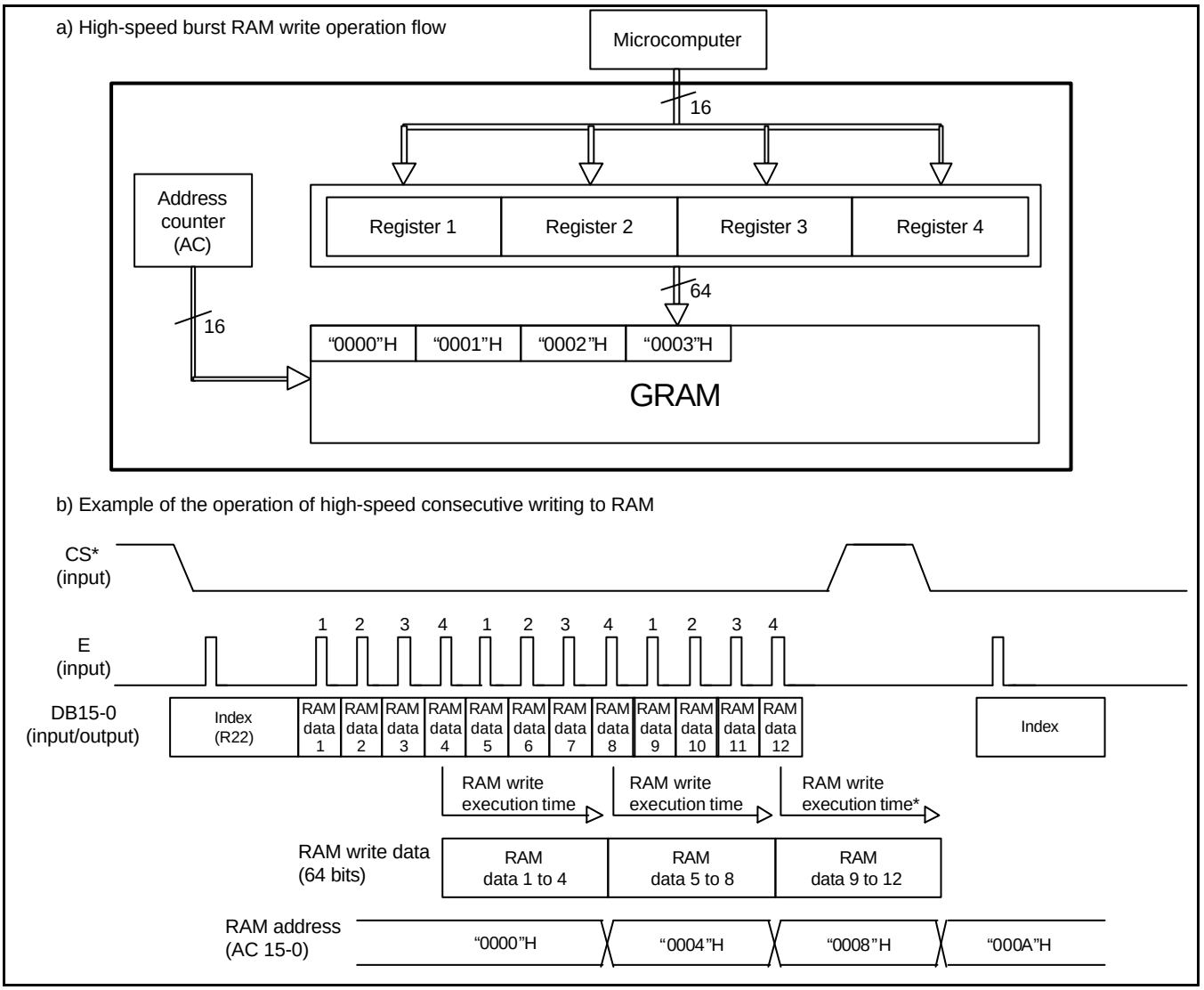

Figure 22. Example of the operation of high-speed consecutive writing to RAM

When high-speed write mode is used, note the following.

1. The logical and compare operations cannot be used.
2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.
*When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.
*When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.
3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
4. When the index register and RAM data write (R22h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.
5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 25. Comparison between Normal and High-speed RAM Write Operations

	Normal RAM Write (HWM=0)	High-speed RAM Write (HWM=1)
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Swap function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Can be set by word

NOTE: 1 word = 2 byte.

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HIGH-SPEED RAM WRITE IN THE WINDOW ADDRESS

When a window address range is specified, GRAM data that is in an optional window area can be updated quickly and continuously by use of dummy write operation. So that the number of RAM access become 4N as shown in the table below.
Dummy write operation must be inserted at the first or last of a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Numbers of dummy write operations of a row must be 4N.

Table 26. Number of Dummy Write Operations in High-Speed RAM Write (HSA bits)

HSA1	HSA0	Number of dummy write operations to be inserted at the start of a row
0	0	0
0	1	1
1	0	2
1	1	3

Table 27. Table 28. Number of Dummy Write Operations in High-Speed RAM Write (HEA bits)

HEA1	HEA0	Number of dummy write operations to be inserted at the end of a row
0	0	3
0	1	2
1	0	1
1	1	0

NOTE: Each row of access must consist of 4 X N operations, including the dummy writes.
Horizontal access count = first dummy write count + write data count + last dummy write count = 4 X N

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An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be accessed consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).

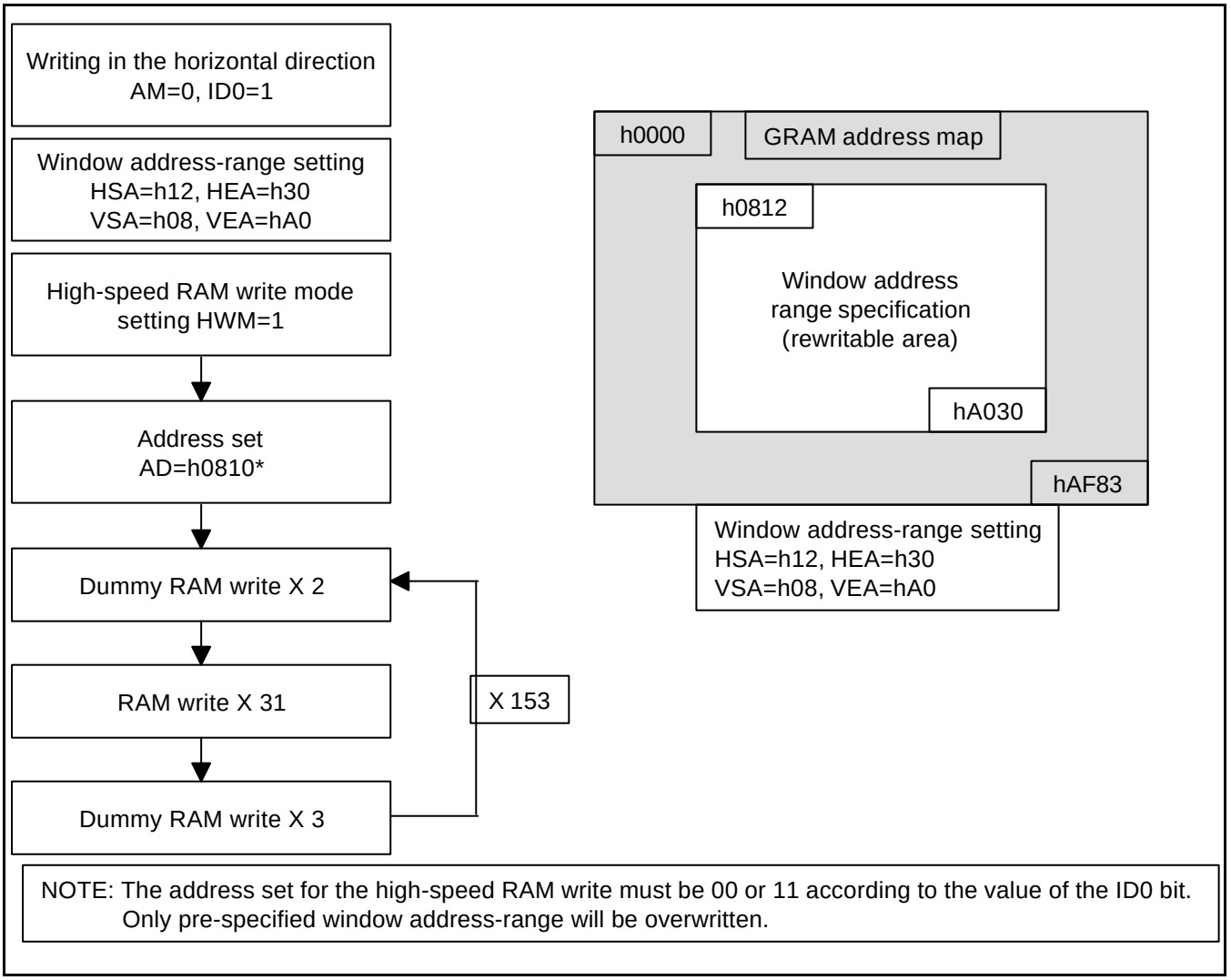


Figure 23. Example of High-speed RAM Write with a window address-range specification

Preliminary

WINDOW ADDRESS FUNCTION

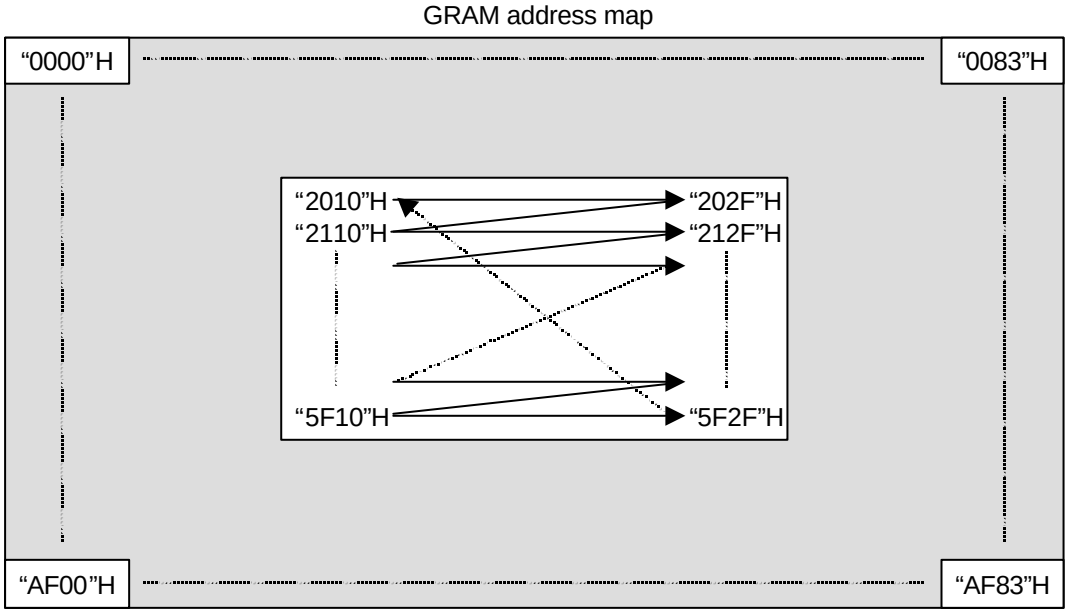
When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA 7-0) and vertical address register (start: VSA7-0, end: VEA7-0) can be updated consecutively.
Data is written to addresses in the direction specified by the AM and ID1-0 bit. When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.
The window must be specified to be within the GRAM address area described as following example. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) 00H ≤ HSA7-0 ≤ HEA7-0 ≤ 83H
(vertical direction) 00H ≤ VSA7-0 ≤ VEA7-0 ≤ AFH

[Restriction on address settings during the window address]
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0
VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.
ID0=0: The lower two bits of the address must be set to 11.
ID0=1: The lower two bits of the address must be set to 00.



Window address-range specification area
HSA7-0 = "10"H, HSE7-0 = "2F"H
VSA7-0 = "20"H, VEA7-0 = "5F"H

I/D = 1 (increment)
AM = 0 (horizontal writing)

Figure 24. Example of address operation in the window address specification

Preliminary

GRAPHICS OPERATION FUNCTION

The S6D0110 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten.
The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 29. Graphics Operation

Operation mode	Bit setting			Operation and usage
	I/D	AM	LG2-0	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

Preliminary

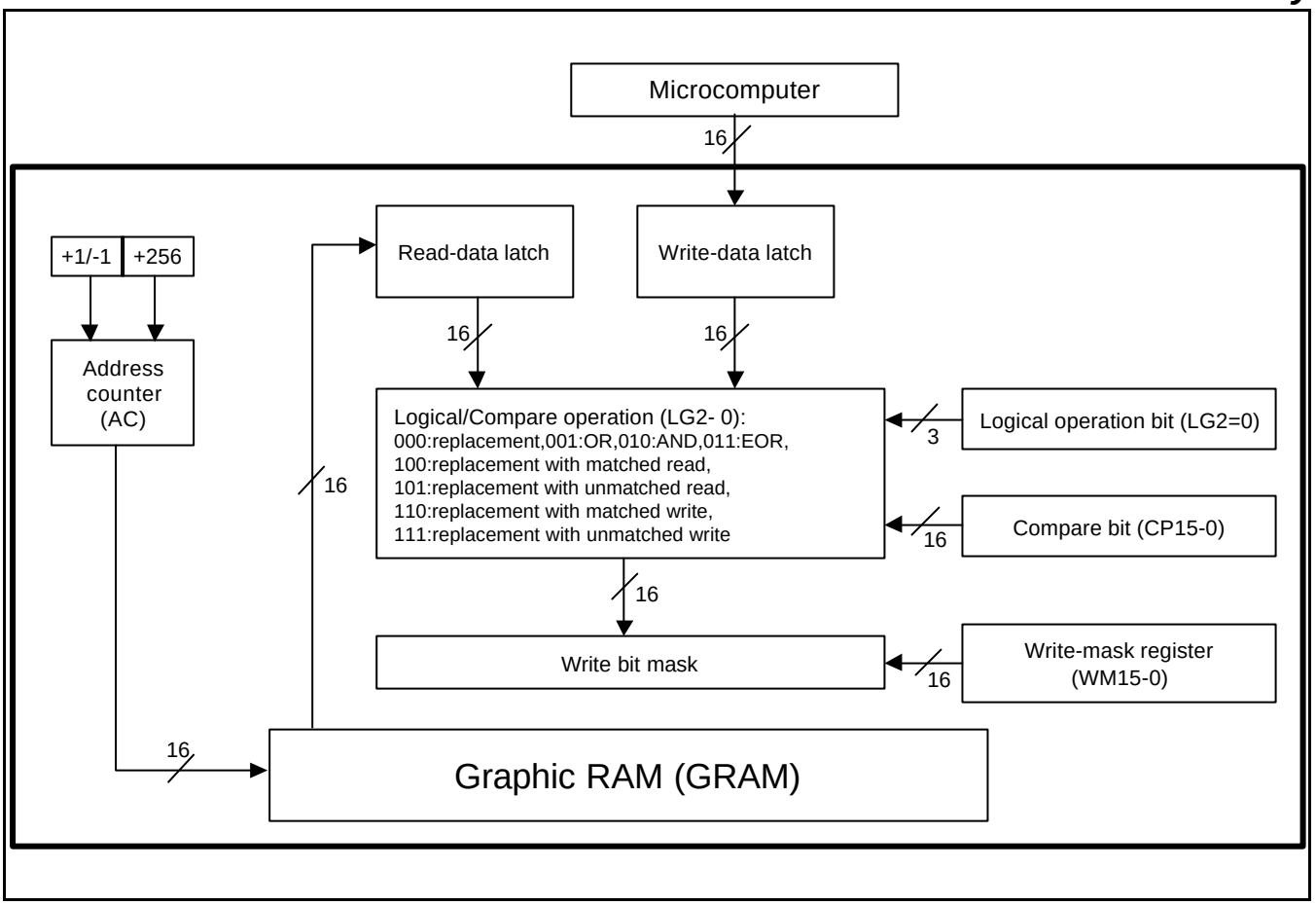


Figure 25. Data processing flow of graphic operation

Preliminary

WRITE-DATA MASK FUNCTION

The S6D0110 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is maintained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

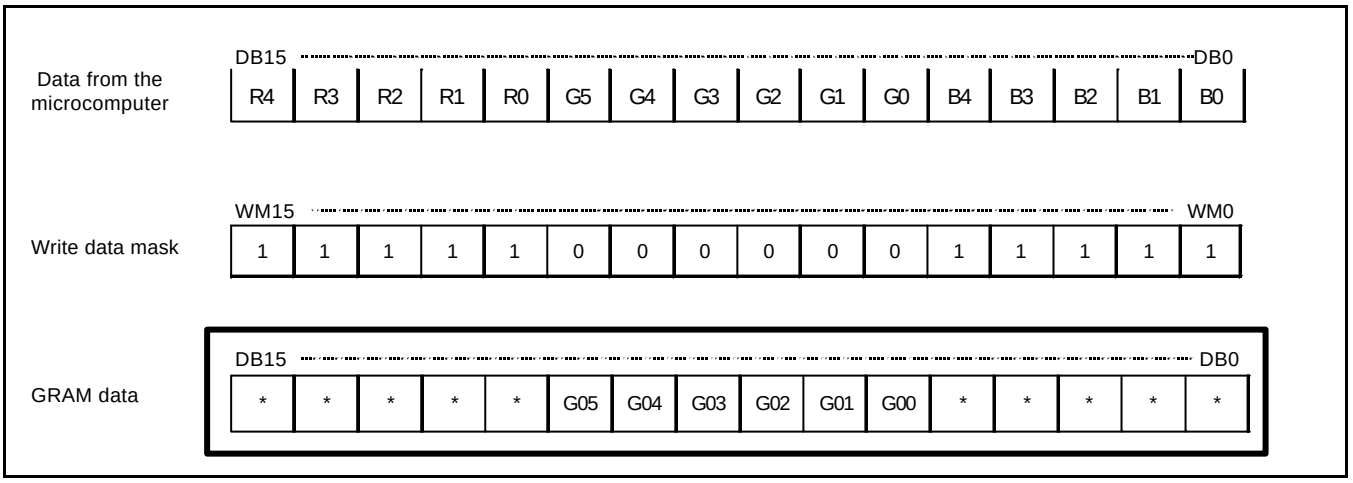


Figure 26. Example of write-data mask function operation

Preliminary

GRAPHICS OPERATION PROCESSING

1. Write mode 1: AM = 0, LG2–0 = 000

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

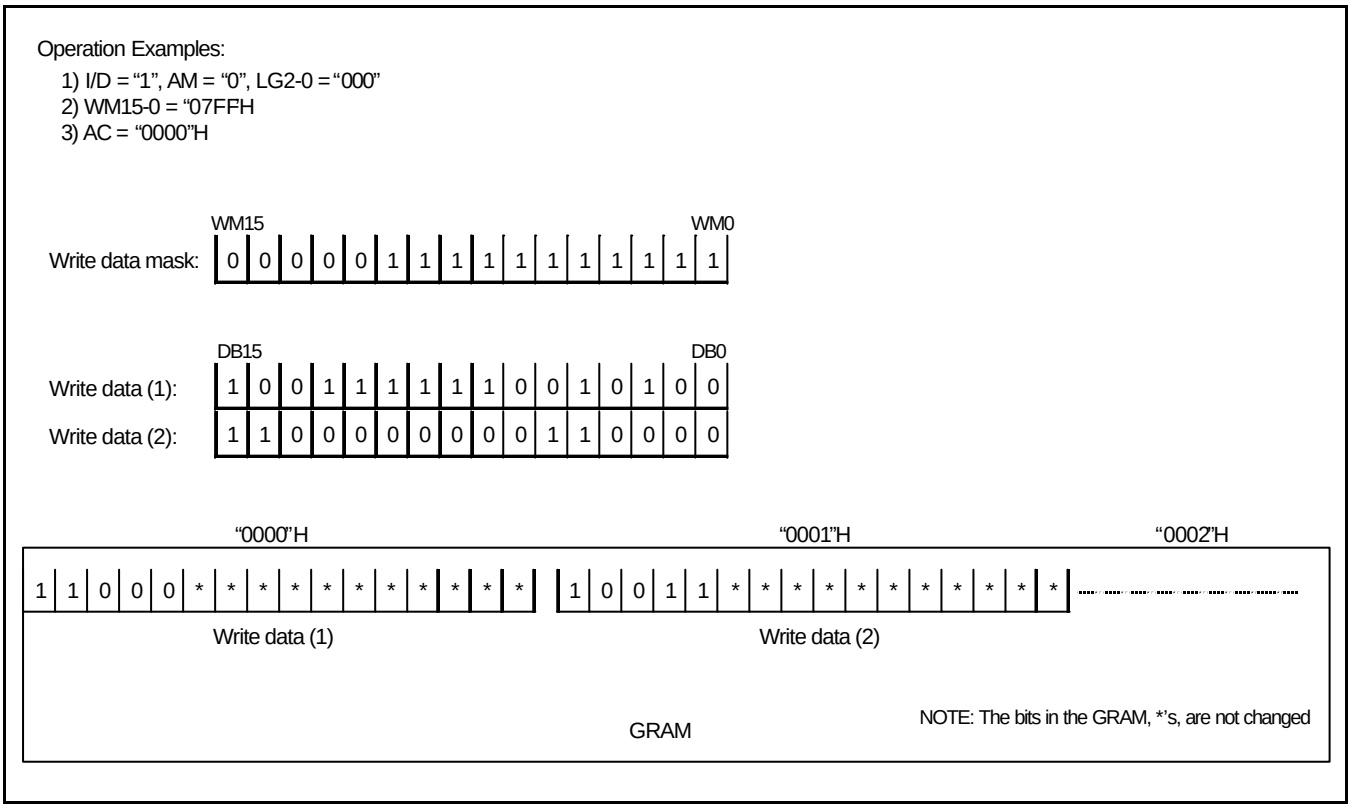


Figure 27. Writing operation of write mode 1

2. Write mode 2: AM = 1, LG2-0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

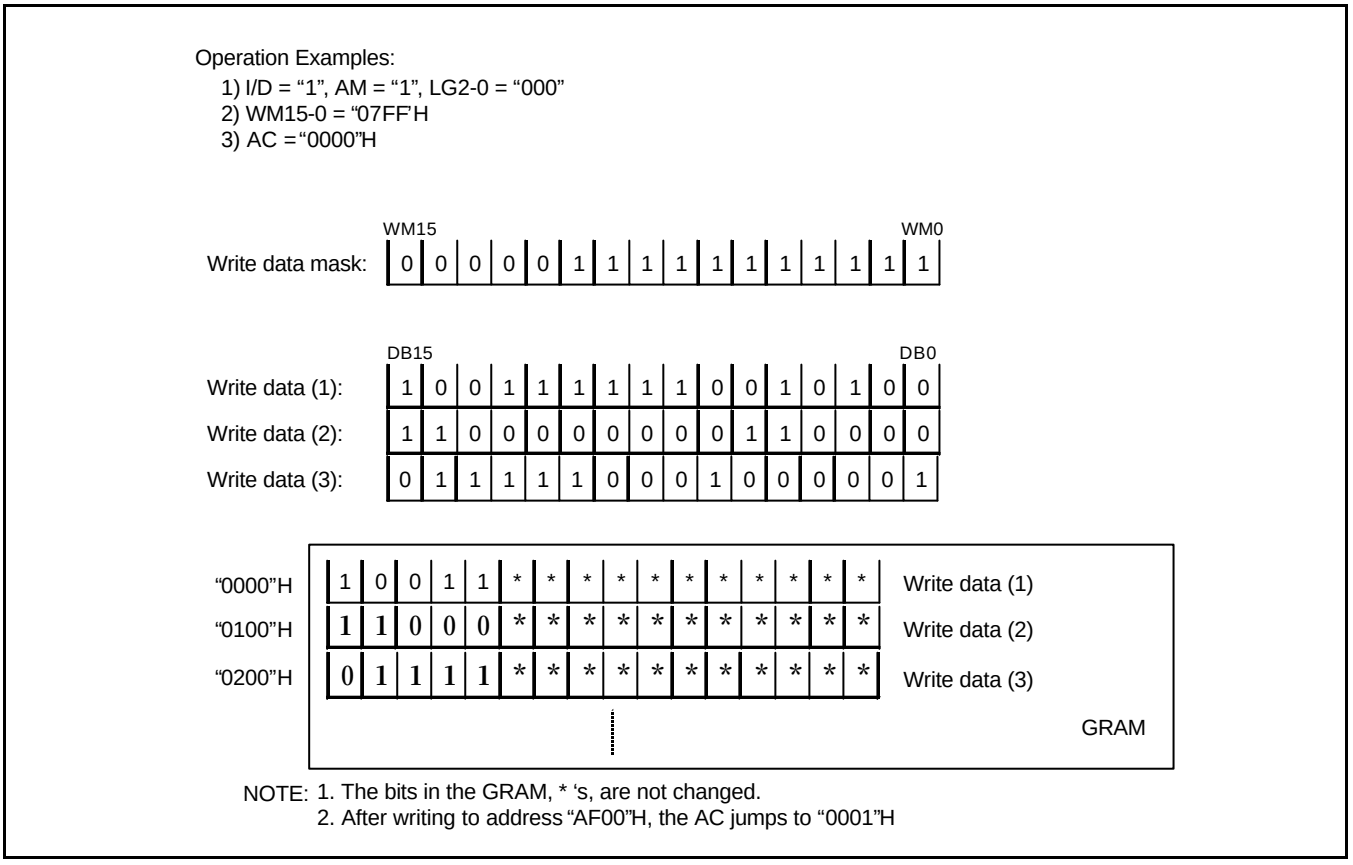


Figure 28. Writing operation of write mode 2

3. Write mode 3: AM = 0, LG2-0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP15–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

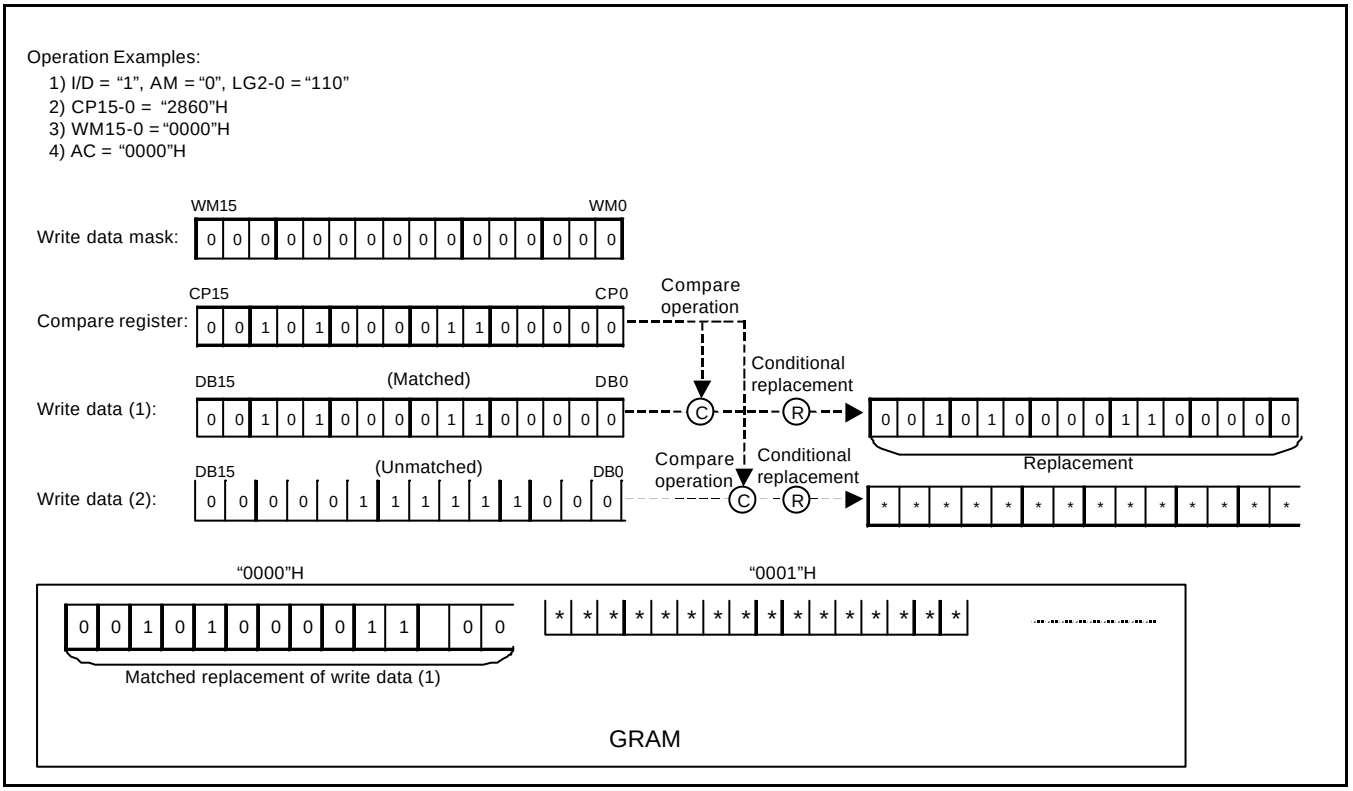


Figure 29. Writing operation write mode 3

Preliminary

4. Write mode 4: AM =1, LG2-0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP15–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) after it has reached the lower edge of the GRAM.

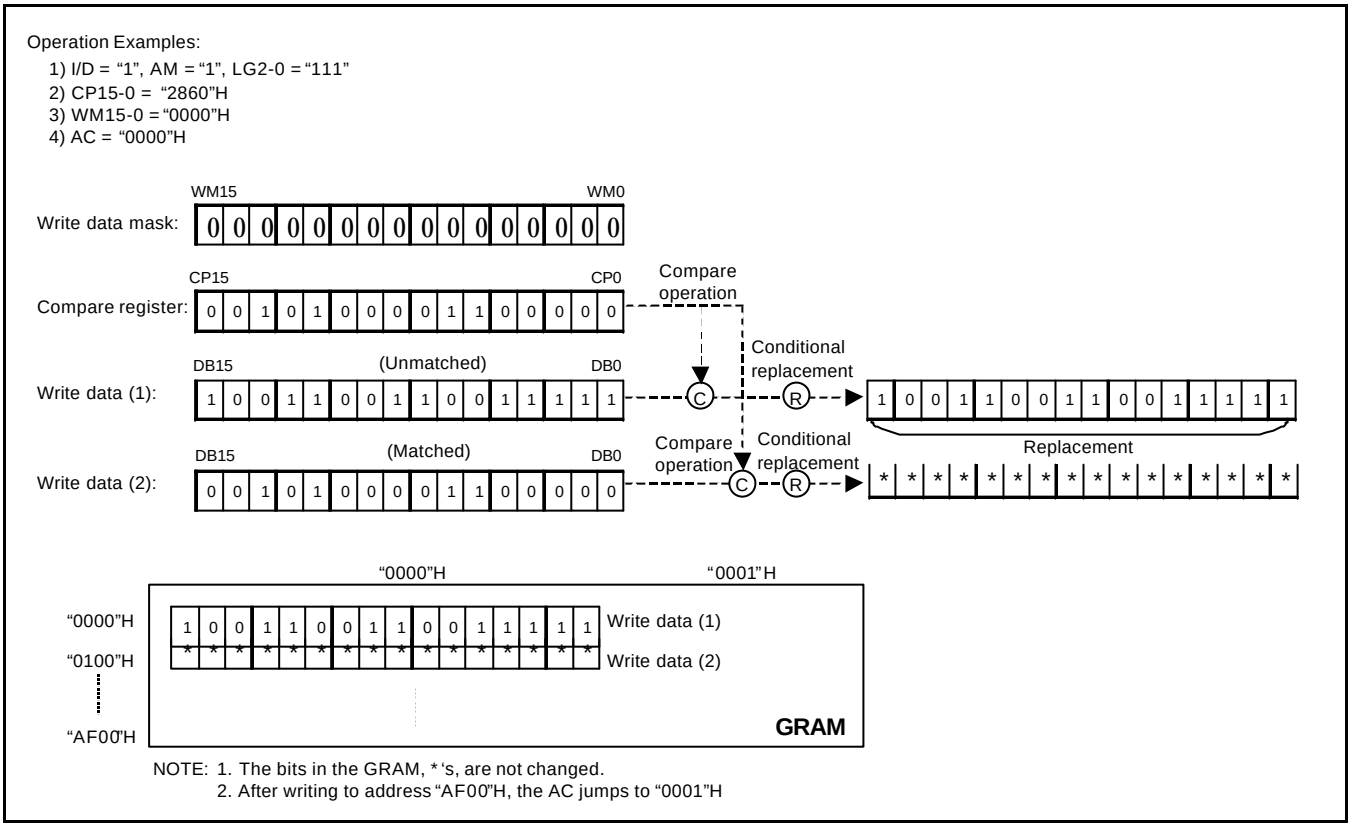


Figure 30. Writing operation of write mode 4

5. Read/Write mode 1: AM = 0, LG2-0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch.

However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

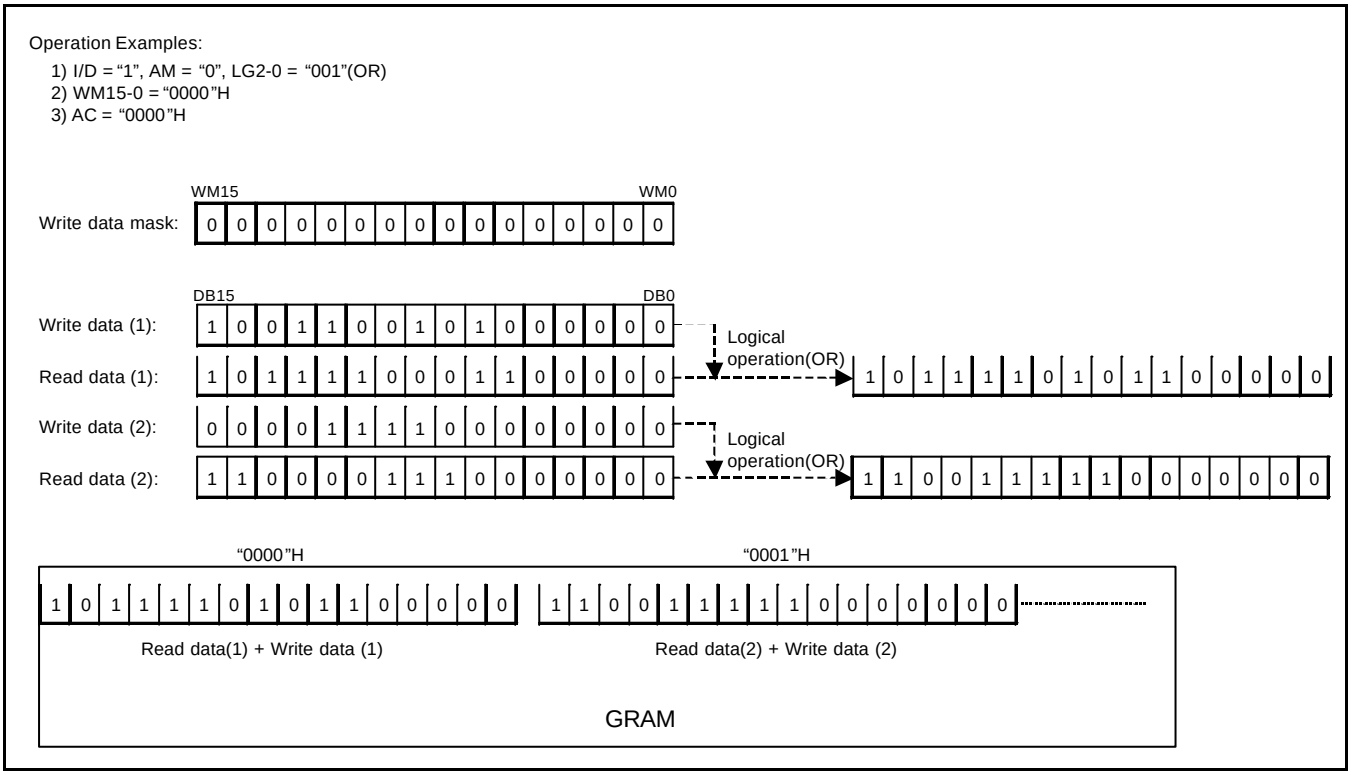


Figure 31. Writing operation of read/write mode 1

6. Read/Write mode 2: AM = 1, LG1-0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

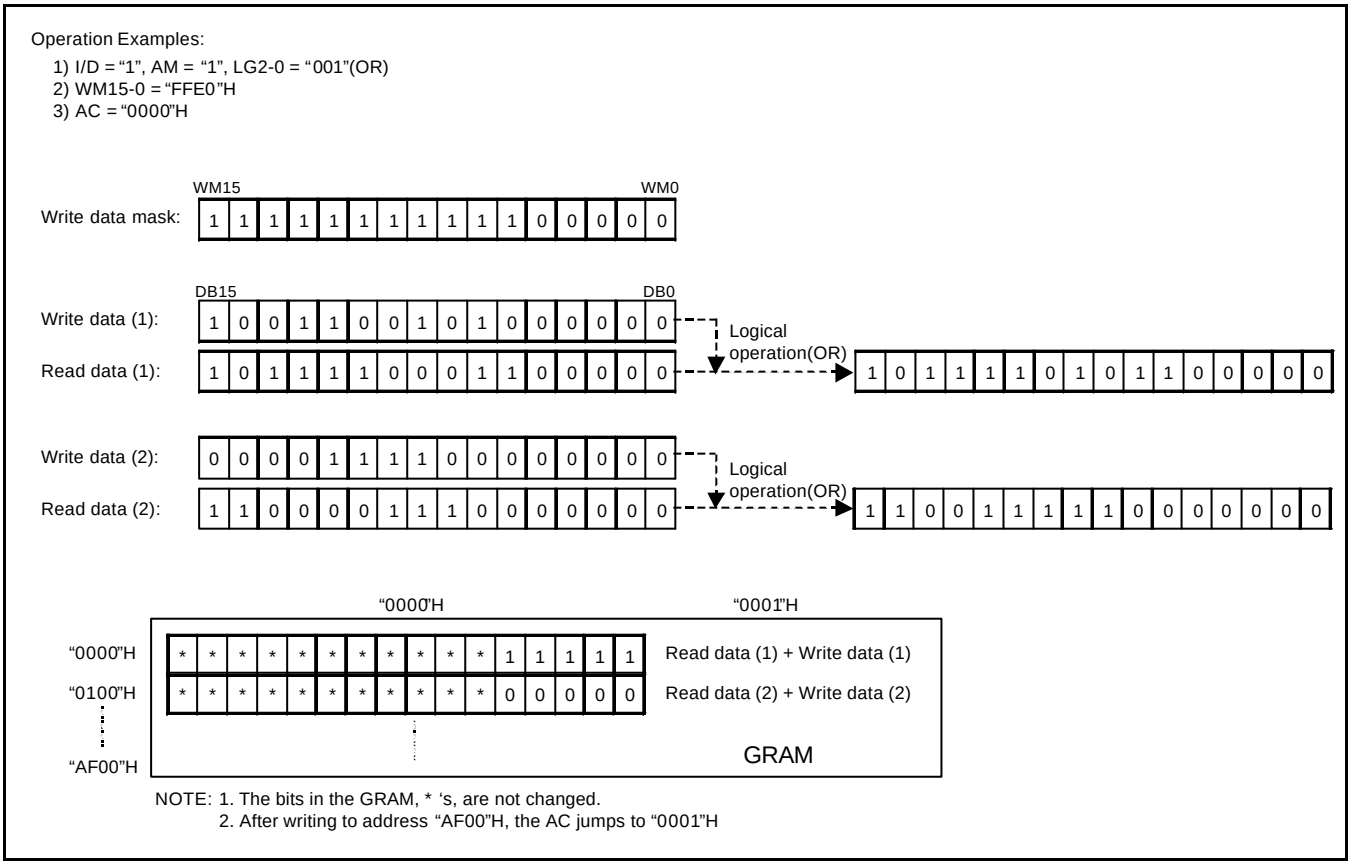


Figure 32. Writing operation of read/write mode 2

7. Read/Write mode 3: AM = 0, LG2-0 = 100/101

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

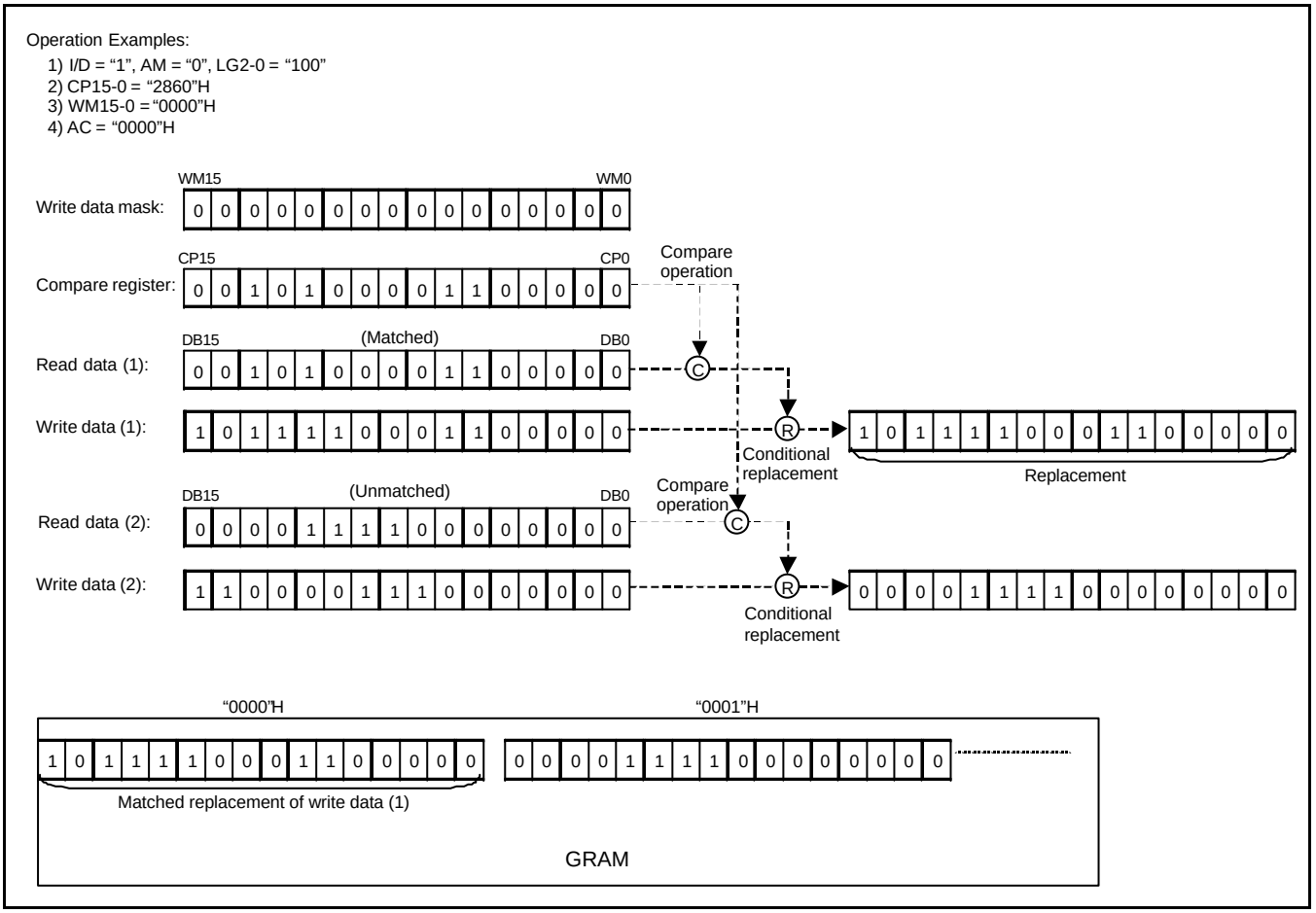


Figure 33. Writing operation of read/write mode 3

8. Read/Write mode 4: AM =1, LG2-0 = 100/101

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

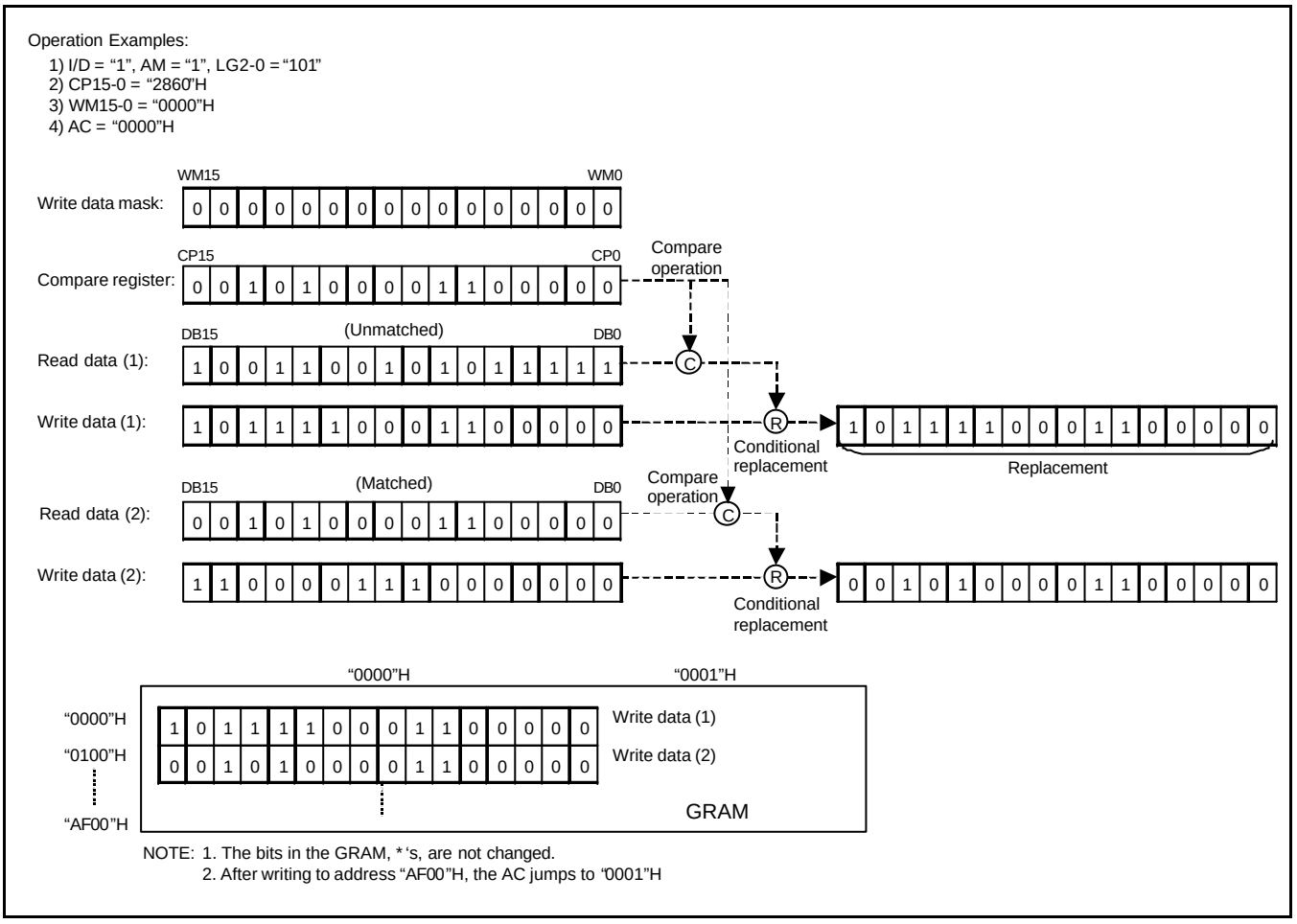


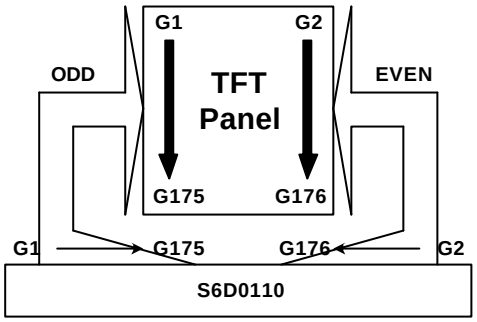
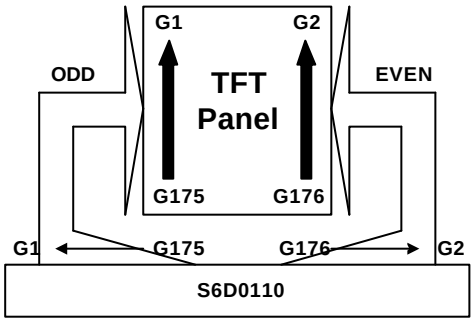
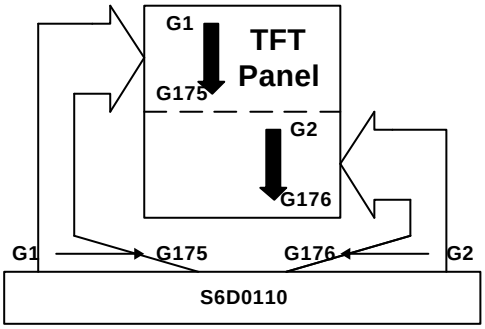
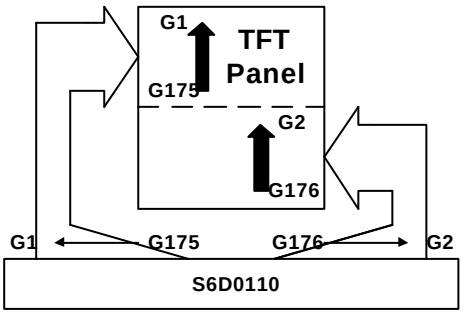
Figure 34. Writing operation of read/write mode 4

Preliminary

GATE DRIVER SCAN MODE SETTING

Gate scan mode of S6D0110 is set by SM and GS bit. GS bit determines the scan direction whether the gate driver scans forward or reverse direction. SM bit determines the method of display division (Even/Odd or Upper/Lower division drive). Using this function, various connections between S6D0110 and the liquid crystal panels can be accomplished

Figure 35. Scan mode setting

SM	GS	Scan Mode	
0	0		G1➔G2➔G3➔ G4➔····➔G173➔ G174➔G175➔G176
0	1		G174➔G175➔G176 G173➔····➔G4➔ G1➔G2➔G3➔
1	0		G1➔G3➔ G5➔····➔G173➔G175 G2➔G4➔ G6➔····➔G174➔G176
1	1		G176➔G174➔ G172➔····➔G4➔G2 G175➔G173➔ G171➔····➔G3➔G1

Preliminary

GAMMA ADJUSTMENT FUNCTION

The S6D0110 provides the gamma adjustment function to display 65,536 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

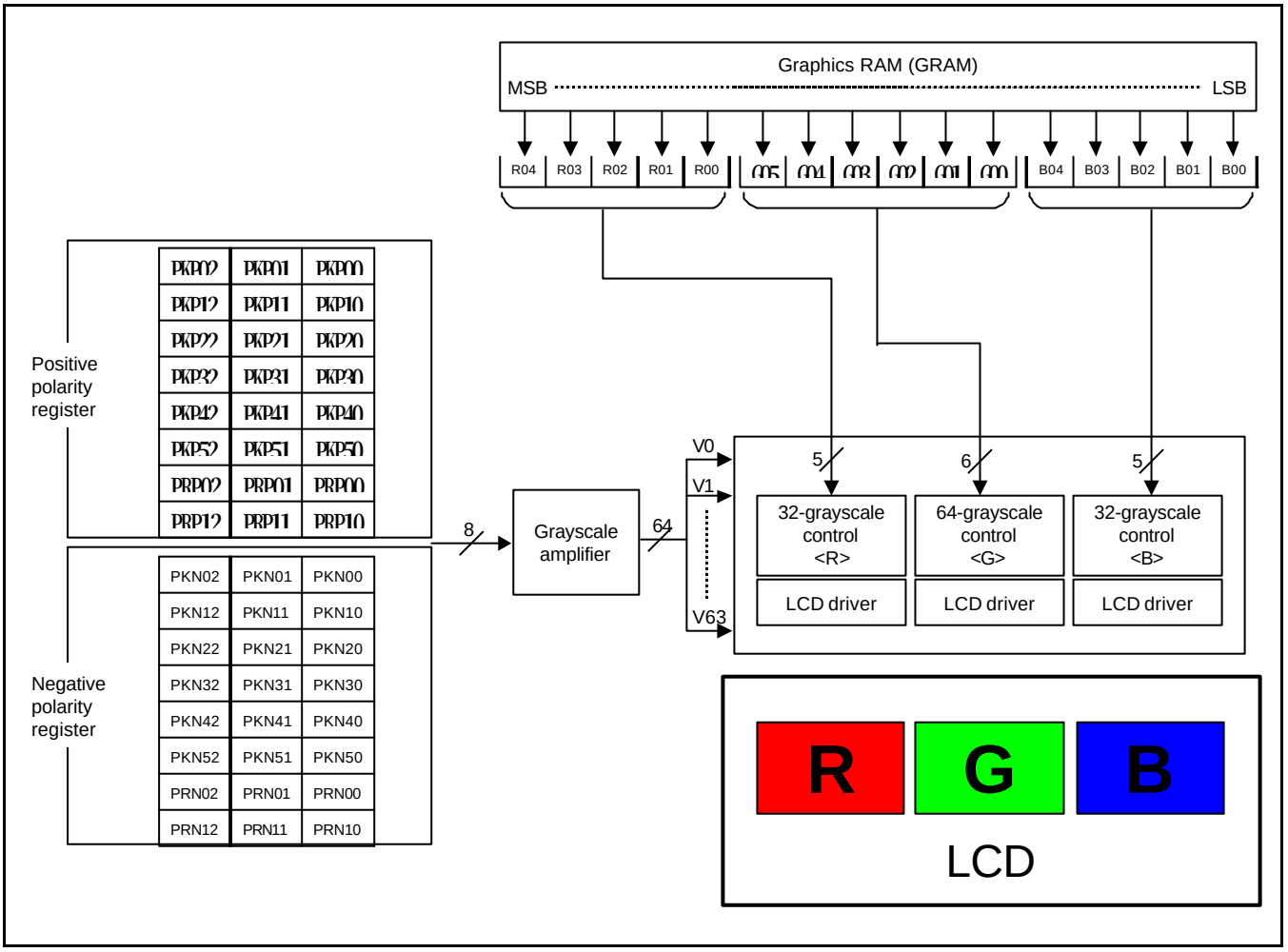


Figure 36. Grayscale control

Preliminary

STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of the grayscale amplifier is shown as below. Determine 8 level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, Period of each level is split by the internal ladder resistance and generates level between V0 to V63.

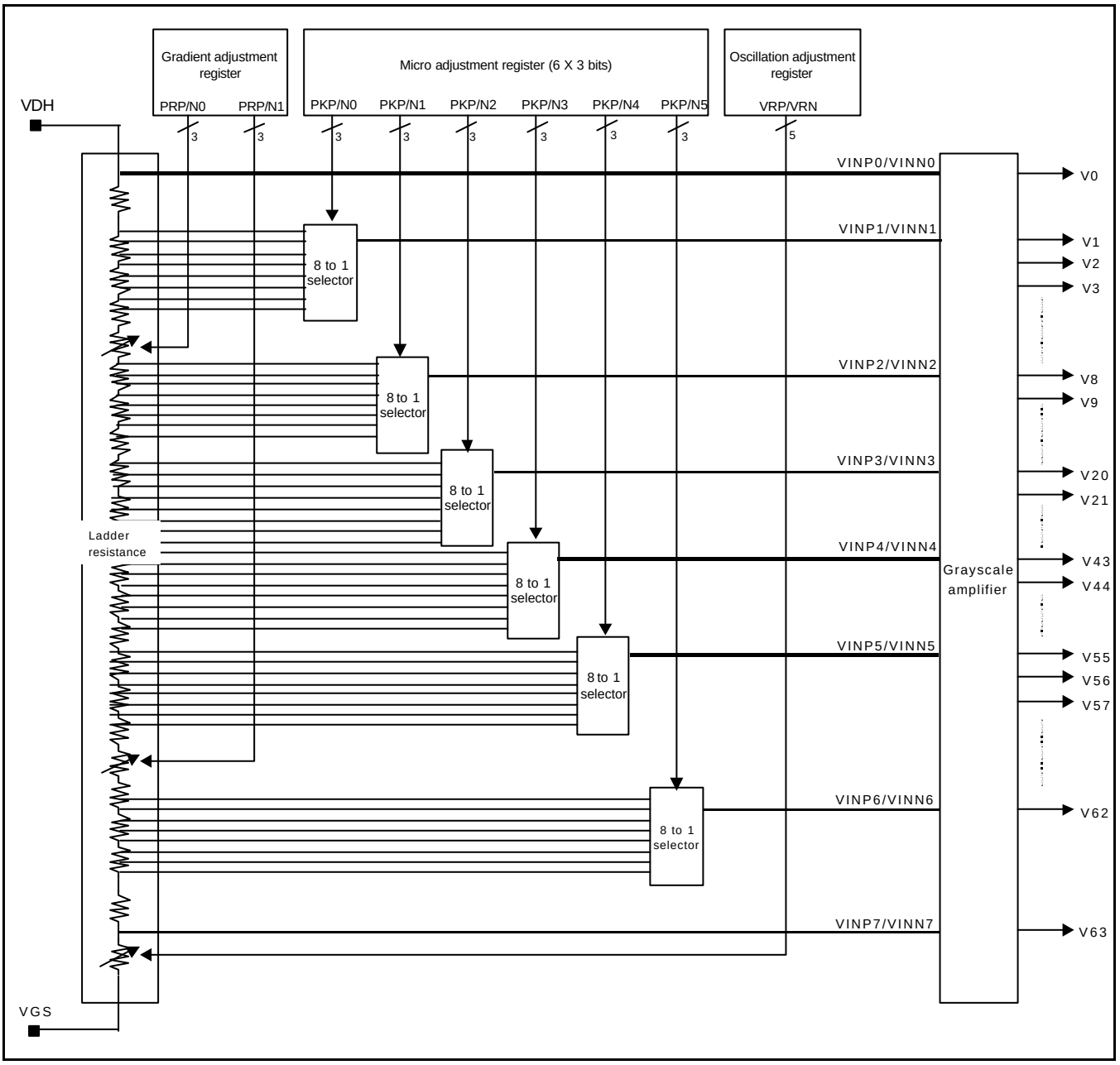


Figure 37. Structure of grayscale amplifier

Preliminary

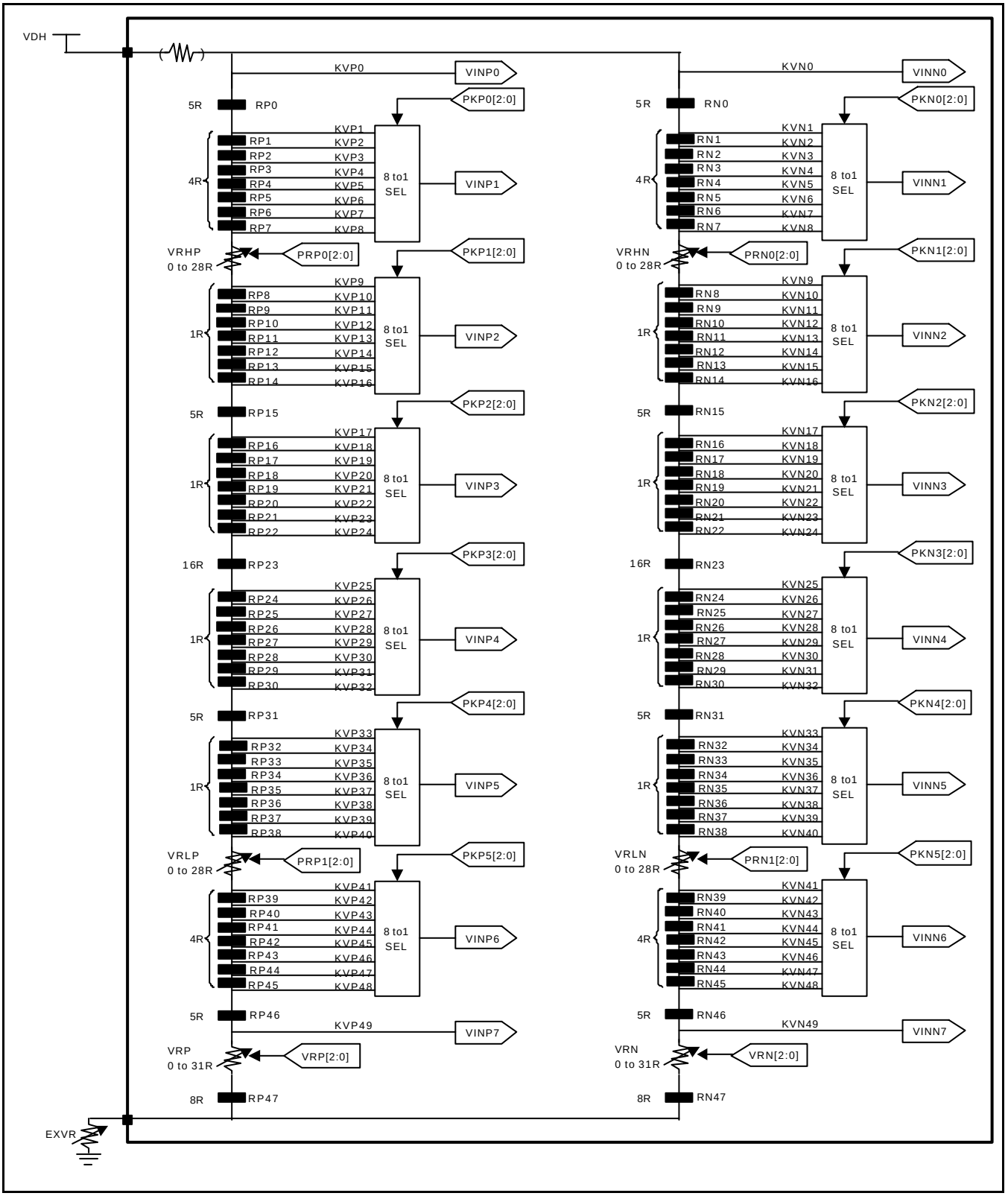


Figure 38. Structure of Ladder/8 to 1 selector

Preliminary

GAMMA ADJUSTMENT REGISTER

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are 3 types of register groups to adjust gradient and oscillation on number of the grayscale, characteristics of the grayscale voltage. (but, R.G.B. is commonness.) Following graphics indicates the operation of each adjusting register.

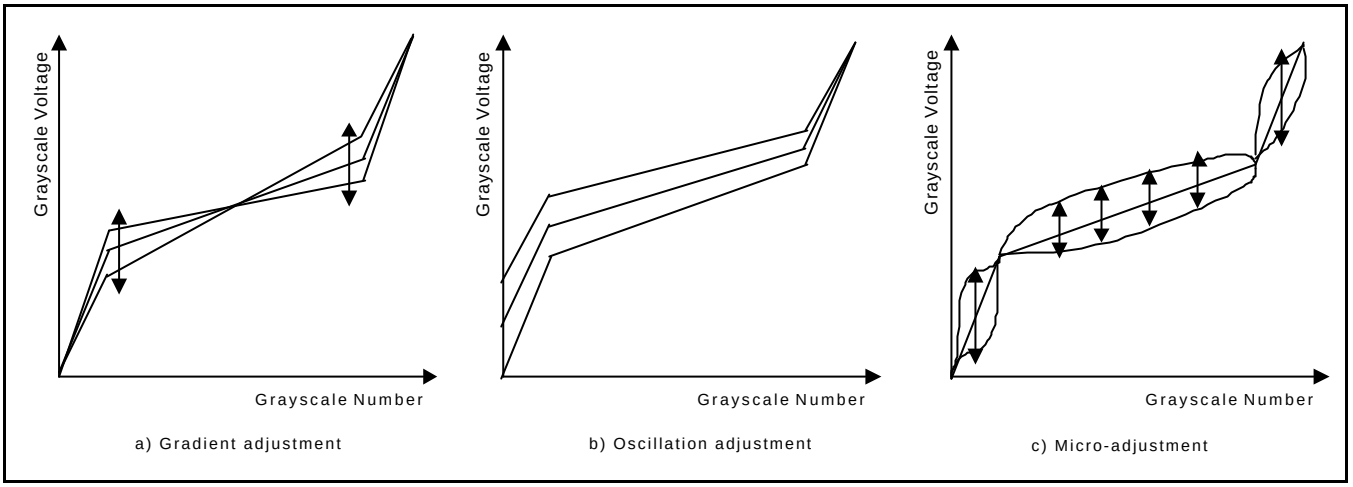


Figure 39. The operation of adjusting register

GRADIENT ADJUSTING RESISTOR

The gradient adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRL (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

OSCILLATION ADJUSTING RESISTOR

The oscillation-adjusting resistor is to adjust oscillation of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input GVDD level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient adjusting resistor.

MICRO-ADJUSTING RESISTOR

The micro-adjusting resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Preliminary

Table 30. Gamma adjusting register

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Oscillation adjustment	VRP[4:0]	VRN[4:0]	Variable resistor VRP(N)
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP6[2:0]	PKN6[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

Preliminary

LADDER RESISTOR/8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. And it allows to compensate the dispersion of length between one panel to another.

VARIABLE RESISTOR

There are 2 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)) and for the oscillation adjustment (VRP (N)). The resistance value is set by the gradient adjusting resistor and the oscillation adjusting resistor as below.

Table 31. Gradient Adjustment

Register value PRP(N) [2:0]	Resistance value PRP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 32. Oscillation Adjustment

Register value VRP(N) [2:0]	Resistance value VRP(N)
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

Preliminary

THE 8 TO 1 SELECTOR

In the 8 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. And output the voltage the six types of the reference voltage, the VIN1- to VIN6.
Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Table 33. Relationship between Micro-adjusting Register and Selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

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Table 34. Gamma Adjusting Voltage Formula (Positive polarity)

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD	-	VINP0
KVP1	GVDD-ΔV*5R/SUMRP	PKP02-00 = " 000"	VINP1
KVP2	GVDD-ΔV*9R/SUMRP	PKP02-00 = " 001"	
KVP3	GVDD-ΔV*13R/SUMRP	PKP02-00 = " 010"	
KVP4	GVDD-ΔV*17R/SUMRP	PKP02-00 = " 011"	
KVP5	GVDD-ΔV*21R/SUMRP	PKP02-00 = " 100"	
KVP6	GVDD-ΔV*25R/SUMRP	PKP02-00 = " 101"	
KVP7	GVDD-ΔV*29R/SUMRP	PKP02-00 = " 110"	
KVP8	GVDD-ΔV*33R/SUMRP	PKP02-00 = " 111"	
KVP9	GVDD-ΔV*(33R+VRHP)/SUMRP	PKP12-10 = " 000"	VINP2
KVP10	GVDD-ΔV*(34R+VRHP)/SUMRP	PKP12-10 = " 001"	
KVP11	GVDD-ΔV*(35R+VRHP)/SUMRP	PKP12-10 = " 010"	
KVP12	GVDD-ΔV*(36R+VRHP)/SUMRP	PKP12-10 = " 011"	
KVP13	GVDD-ΔV*(37R+VRHP)/SUMRP	PKP12-10 = " 100"	
KVP14	GVDD-ΔV*(38R+VRHP)/SUMRP	PKP12-10 = " 101"	
KVP15	GVDD-ΔV*(39R+VRHP)/SUMRP	PKP12-10 = " 110"	
KVP16	GVDD-ΔV*(40R+VRHP)/SUMRP	PKP12-10 = " 111"	
KVP17	GVDD-ΔV*(45R+VRHP)/SUMRP	PKP22-20 = " 000"	VINP3
KVP18	GVDD-ΔV*(46R+VRHP)/SUMRP	PKP22-20 = " 001"	
KVP19	GVDD-ΔV*(47R+VRHP)/SUMRP	PKP22-20 = " 010"	
KVP20	GVDD-ΔV*(48R+VRHP)/SUMRP	PKP22-20 = " 011"	
KVP21	GVDD-ΔV*(49R+VRHP)/SUMRP	PKP22-20 = " 100"	
KVP22	GVDD-ΔV*(50R+VRHP)/SUMRP	PKP22-20 = " 101"	
KVP23	GVDD-ΔV*(51R+VRHP)/SUMRP	PKP22-20 = " 110"	
KVP24	GVDD-ΔV*(52R+VRHP)/SUMRP	PKP22-20 = " 111"	
KVP25	GVDD-ΔV*(68R+VRHP)/SUMRP	PKP32-30 = " 000"	VINP4
KVP26	GVDD-ΔV*(69R+VRHP)/SUMRP	PKP32-30 = " 001"	
KVP27	GVDD-ΔV*(70R+VRHP)/SUMRP	PKP32-30 = " 010"	
KVP28	GVDD-ΔV*(71R+VRHP)/SUMRP	PKP32-30 = " 011"	
KVP29	GVDD-ΔV*(72R+VRHP)/SUMRP	PKP32-30 = " 100"	
KVP30	GVDD-ΔV*(73R+VRHP)/SUMRP	PKP32-30 = " 101"	
KVP31	GVDD-ΔV*(74R+VRHP)/SUMRP	PKP32-30 = " 110"	
KVP32	GVDD-ΔV*(75R+VRHP)/SUMRP	PKP32-30 = " 111"	
KVP33	GVDD-ΔV*(80R+VRHP)/SUMRP	PKP42-40 = " 000"	VINP5
KVP34	GVDD-ΔV*(81R+VRHP)/SUMRP	PKP42-40 = " 001"	
KVP35	GVDD-ΔV*(82R+VRHP)/SUMRP	PKP42-40 = " 010"	
KVP36	GVDD-ΔV*(83R+VRHP)/SUMRP	PKP42-40 = " 011"	
KVP37	GVDD-ΔV*(84R+VRHP)/SUMRP	PKP42-40 = " 100"	
KVP38	GVDD-ΔV*(85R+VRHP)/SUMRP	PKP42-40 = " 101"	
KVP39	GVDD-ΔV*(86R+VRHP)/SUMRP	PKP42-40 = " 110"	
KVP40	GVDD-ΔV*(87R+VRHP)/SUMRP	PKP42-40 = " 111"	
KVP41	GVDD-ΔV*(87R+VRHP+VRLP)/SUMRP	PKP52-50 = " 000"	VINP6
KVP42	GVDD-ΔV*(91R+VRHP+VRLP)/SUMRP	PKP52-50 = " 001"	
KVP43	GVDD-ΔV*(95R+VRHP+VRLP)/SUMRP	PKP52-50 = " 010"	
KVP44	GVDD-ΔV*(99R+VRHP+VRLP)/SUMRP	PKP52-50 = " 011"	
KVP45	GVDD-ΔV*(103R+VRHP+VRLP)/SUMRP	PKP52-50 = " 100"	
KVP46	GVDD-ΔV*(107R+VRHP+VRLP)/SUMRP	PKP52-50 = " 101"	
KVP47	GVDD-ΔV*(111R+VRHP+VRLP)/SUMRP	PKP52-50 = " 110"	
KVP48	GVDD-ΔV*(115R+VRHP+VRLP)/SUMRP	PKP52-50 = " 111"	
KVP49	GVDD-ΔV*(120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP
SUMRP: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN
ΔV: Potential difference between KV0 and KV49 = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 35. Gamma Voltage Formula (Positive Polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V43+(V20-V43)*(11/23)
V1	VINP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINP2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINP4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINP3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINP5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINP6
V31	V43+(V20-V43)*(12/23)	V63	VINP7

Table 36. Gamma Adjusting Voltage Formula (Negative polarity)

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD	-	VINN0
KVN1	GVDD-ΔV*5R/SUMRN	PKN02-00 = "000"	VINN1
KVN2	GVDD-ΔV*9R/SUMRN	PKN02-00 = "001"	
KVN3	GVDD-ΔV*13R/SUMRN	PKN02-00 = "010"	
KVN4	GVDD-ΔV*17R/SUMRN	PKN02-00 = "011"	
KVN5	GVDD-ΔV*21R/SUMRN	PKN02-00 = "100"	
KVN6	GVDD-ΔV*25R/SUMRN	PKN02-00 = "101"	
KVN7	GVDD-ΔV*29R/SUMRN	PKN02-00 = "110"	
KVN8	GVDD-ΔV*33R/SUMRN	PKN02-00 = "111"	
KVN9	GVDD-ΔV*(33R+VRHN)/SUMRN	PKN12-10 = "000"	VINN2
KVN10	GVDD-ΔV*(34R+VRHN)/SUMRN	PKN12-10 = "001"	
KVN11	GVDD-ΔV*(35R+VRHN)/SUMRN	PKN12-10 = "010"	
KVN12	GVDD-ΔV*(36R+VRHN)/SUMRN	PKN12-10 = "011"	
KVN13	GVDD-ΔV*(37R+VRHN)/SUMRN	PKN12-10 = "100"	
KVN14	GVDD-ΔV*(38R+VRHN)/SUMRN	PKN12-10 = "101"	
KVN15	GVDD-ΔV*(39R+VRHN)/SUMRN	PKN12-10 = "110"	
KVN16	GVDD-ΔV*(40R+VRHN)/SUMRN	PKN12-10 = "111"	
KVN17	GVDD-ΔV*(45R+VRHN)/SUMRN	PKN22-20 = "000"	VINN3
KVN18	GVDD-ΔV*(46R+VRHN)/SUMRN	PKN22-20 = "001"	
KVN19	GVDD-ΔV*(47R+VRHN)/SUMRN	PKN22-20 = "010"	
KVN20	GVDD-ΔV*(48R+VRHN)/SUMRN	PKN22-20 = "011"	
KVN21	GVDD-ΔV*(49R+VRHN)/SUMRN	PKN22-20 = "100"	
KVN22	GVDD-ΔV*(50R+VRHN)/SUMRN	PKN22-20 = "101"	
KVN23	GVDD-ΔV*(51R+VRHN)/SUMRN	PKN22-20 = "110"	
KVN24	GVDD-ΔV*(52R+VRHN)/SUMRN	PKN22-20 = "111"	
KVN25	GVDD-ΔV*(68R+VRHN)/SUMRN	PKN32-30 = "000"	VINN4
KVN26	GVDD-ΔV*(69R+VRHN)/SUMRN	PKN32-30 = "001"	
KVN27	GVDD-ΔV*(70R+VRHN)/SUMRN	PKN32-30 = "010"	
KVN28	GVDD-ΔV*(71R+VRHN)/SUMRN	PKN32-30 = "011"	
KVN29	GVDD-ΔV*(72R+VRHN)/SUMRN	PKN32-30 = "100"	
KVN30	GVDD-ΔV*(73R+VRHN)/SUMRN	PKN32-30 = "101"	
KVN31	GVDD-ΔV*(74R+VRHN)/SUMRN	PKN32-30 = "110"	
KVN32	GVDD-ΔV*(75R+VRHN)/SUMRN	PKN32-30 = "111"	
KVN33	GVDD-ΔV*(80R+VRHN)/SUMRN	PKN42-40 = "000"	VINN5
KVN34	GVDD-ΔV*(81R+VRHN)/SUMRN	PKN42-40 = "001"	
KVN35	GVDD-ΔV*(82R+VRHN)/SUMRN	PKN42-40 = "010"	
KVN36	GVDD-ΔV*(83R+VRHN)/SUMRN	PKN42-40 = "011"	
KVN37	GVDD-ΔV*(84R+VRHN)/SUMRN	PKN42-40 = "100"	
KVN38	GVDD-ΔV*(85R+VRHN)/SUMRN	PKN42-40 = "101"	
KVN39	GVDD-ΔV*(86R+VRHN)/SUMRN	PKN42-40 = "110"	
KVN40	GVDD-ΔV*(87R+VRHN)/SUMRN	PKN42-40 = "111"	
KVN41	GVDD-ΔV*(87R+VRHN+VRLN)/SUMRN	PKN52-50 = "000"	VINN6
KVN42	GVDD-ΔV*(91R+VRHN+VRLN)/SUMRN	PKN52-50 = "001"	
KVN43	GVDD-ΔV*(95R+VRHN+VRLN)/SUMRN	PKN52-50 = "010"	
KVN44	GVDD-ΔV*(99R+VRHN+VRLN)/SUMRN	PKN52-50 = "011"	
KVN45	GVDD-ΔV*(103R+VRHN+VRLN)/SUMRN	PKN52-50 = "100"	
KVN46	GVDD-ΔV*(107R+VRHN+VRLN)/SUMRN	PKN52-50 = "101"	
KVN47	GVDD-ΔV*(111R+VRHN+VRLN)/SUMRN	PKN52-50 = "110"	
KVN48	GVDD-ΔV*(115R+VRHN+VRLN)/SUMRN	PKN52-50 = "111"	
KVN49	GVDD-ΔV*(120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN

ΔV: Potential difference between KV0 and KV49 = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 37. Gamma Voltage Formula (Negative Polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7

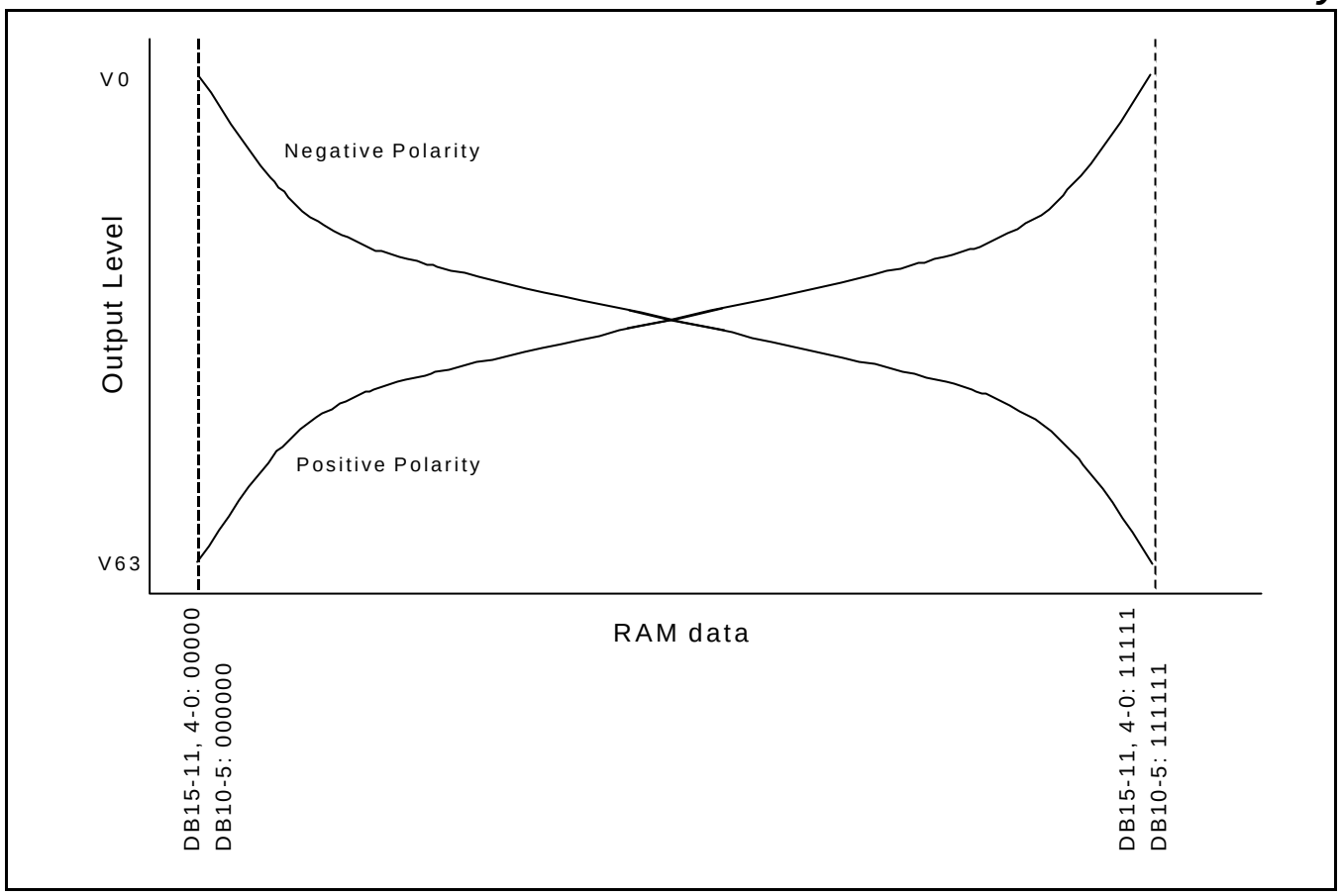

Figure 40. Relationship between RAM data and output voltage

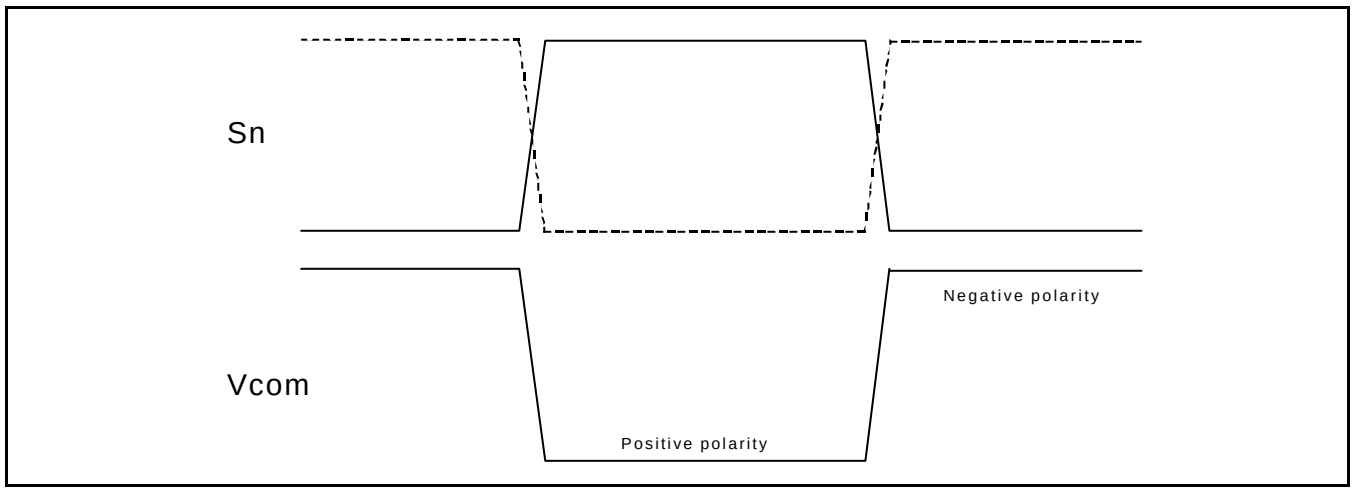

Figure 41. Relationship between source output and Vcom

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THE 8-COLOR DISPLAY MODE

The S6D0110 carries 8-color display mode. Using grayscale levels are V0 and V63 and all other level power supplies are halt. So that it attempts to lower power consumption. Also, during the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. Rewrite the data of GRAM R/B to 00000 or 11111, G to 000000 or 111111 before set the mode. The level power supply (V1-V62) is in OFF condition during the 8-color mode in order to select V0/V63.

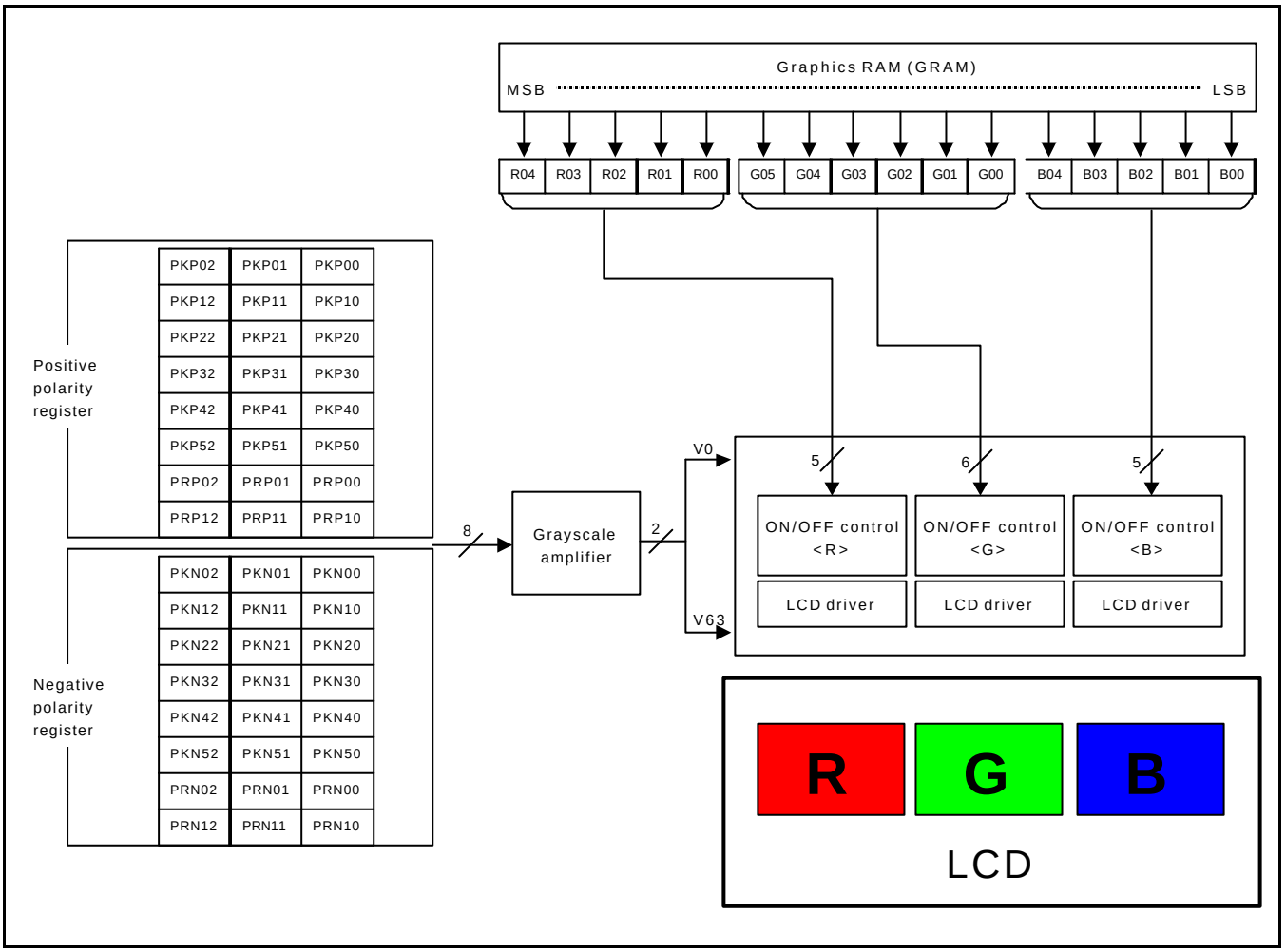

Figure 42. 8-color display control

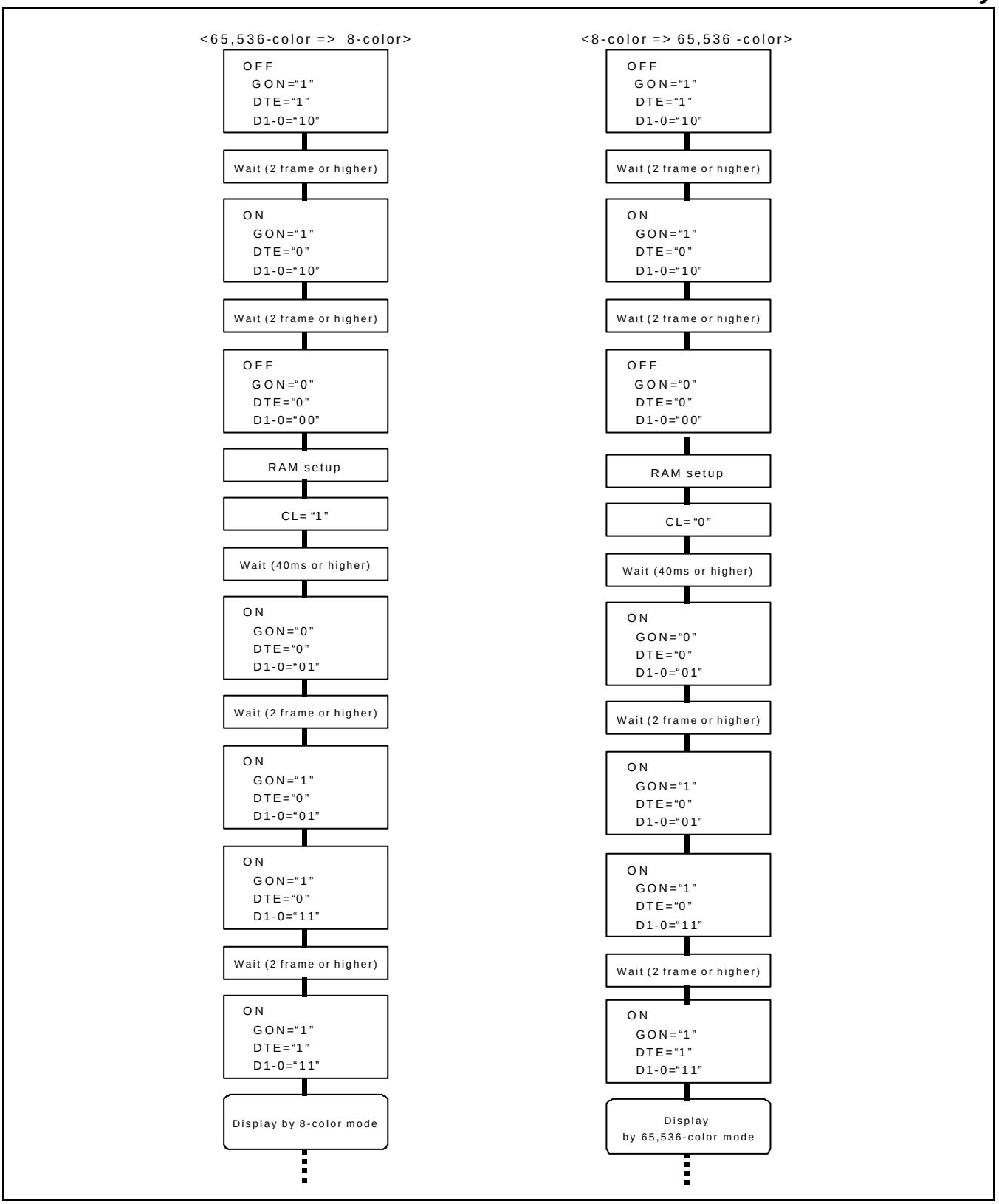

Figure 43. Set up procedure for the 8-color mode

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SYSTEM STRUCTURE EXAMPLE

Following diagram indicates the system structure, which composes the 132 (width) x 176 (length) dots TFT-LCD panel.

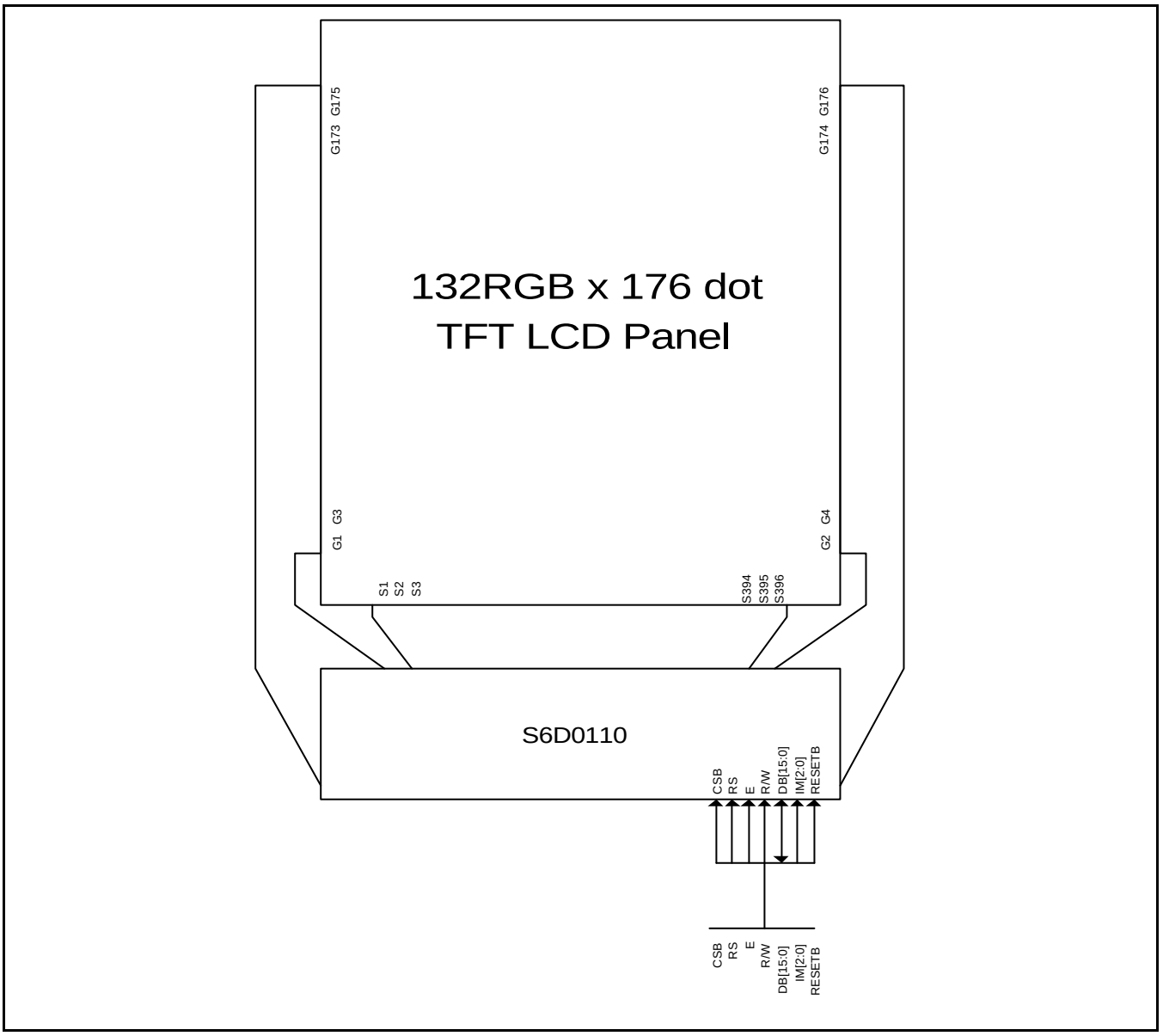

Figure 44. System structure

Instruction set up flow

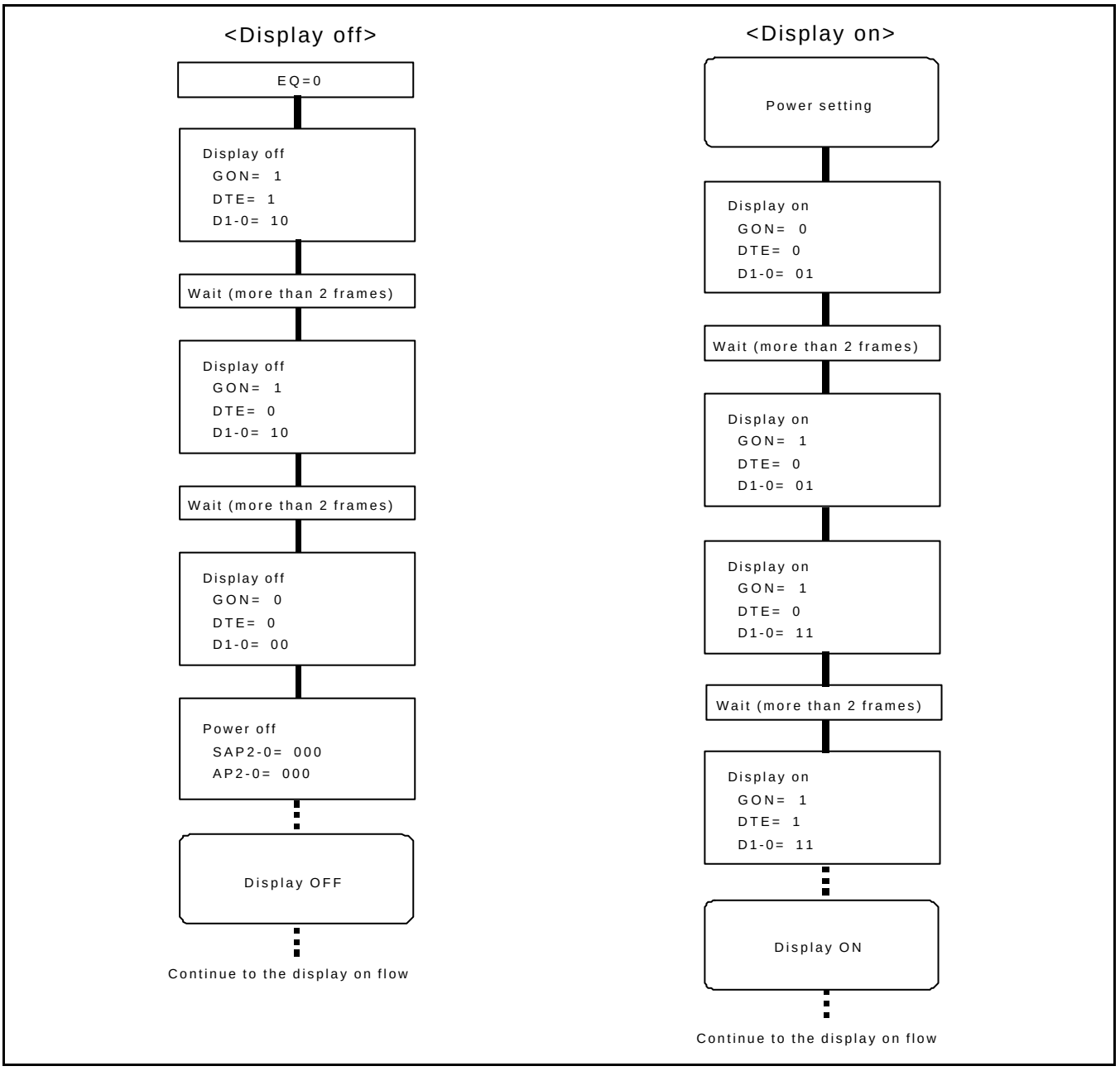

Figure 45. Instruction set up flow

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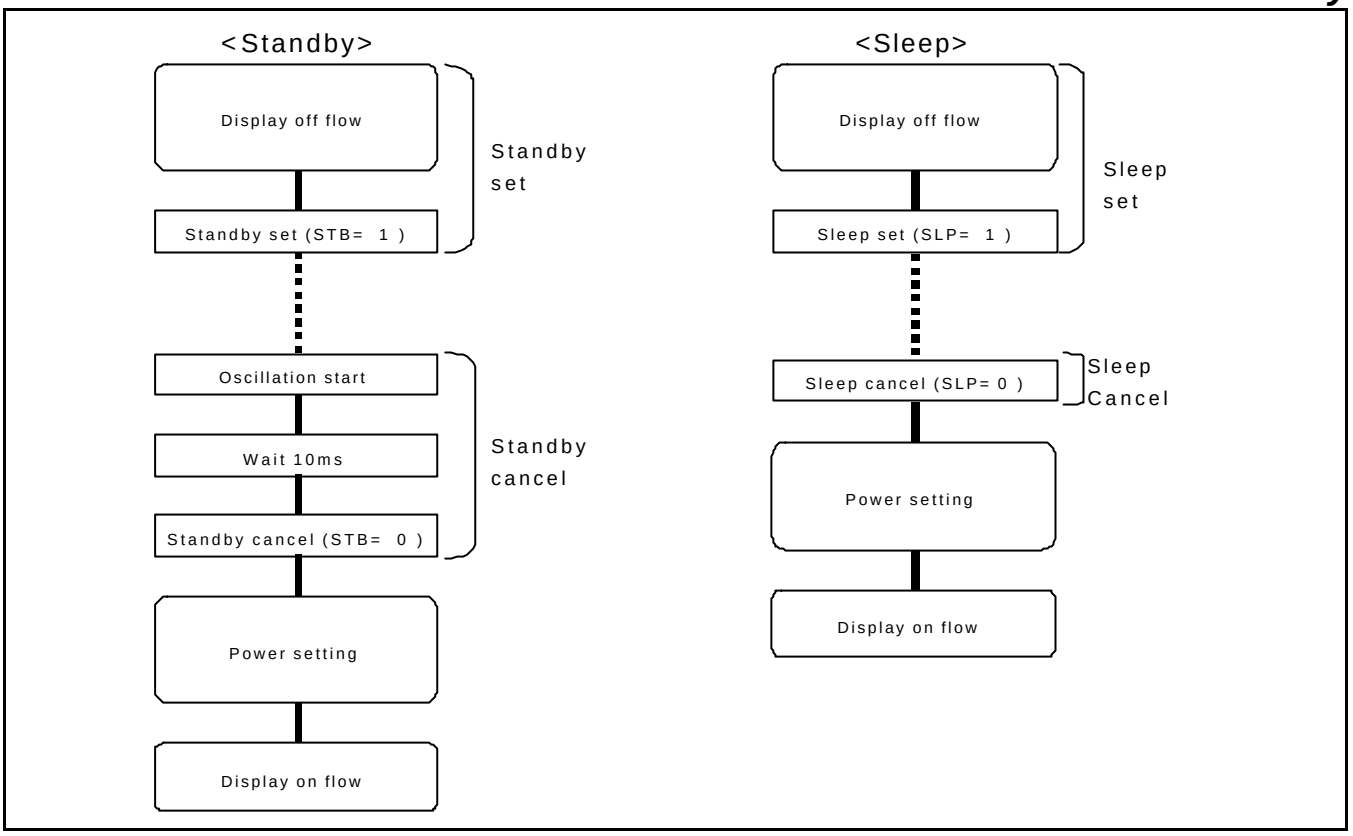

Figure 46. Instruction setup flow (continued)

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OSCILLATION CIRCUIT

The S6D0110 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

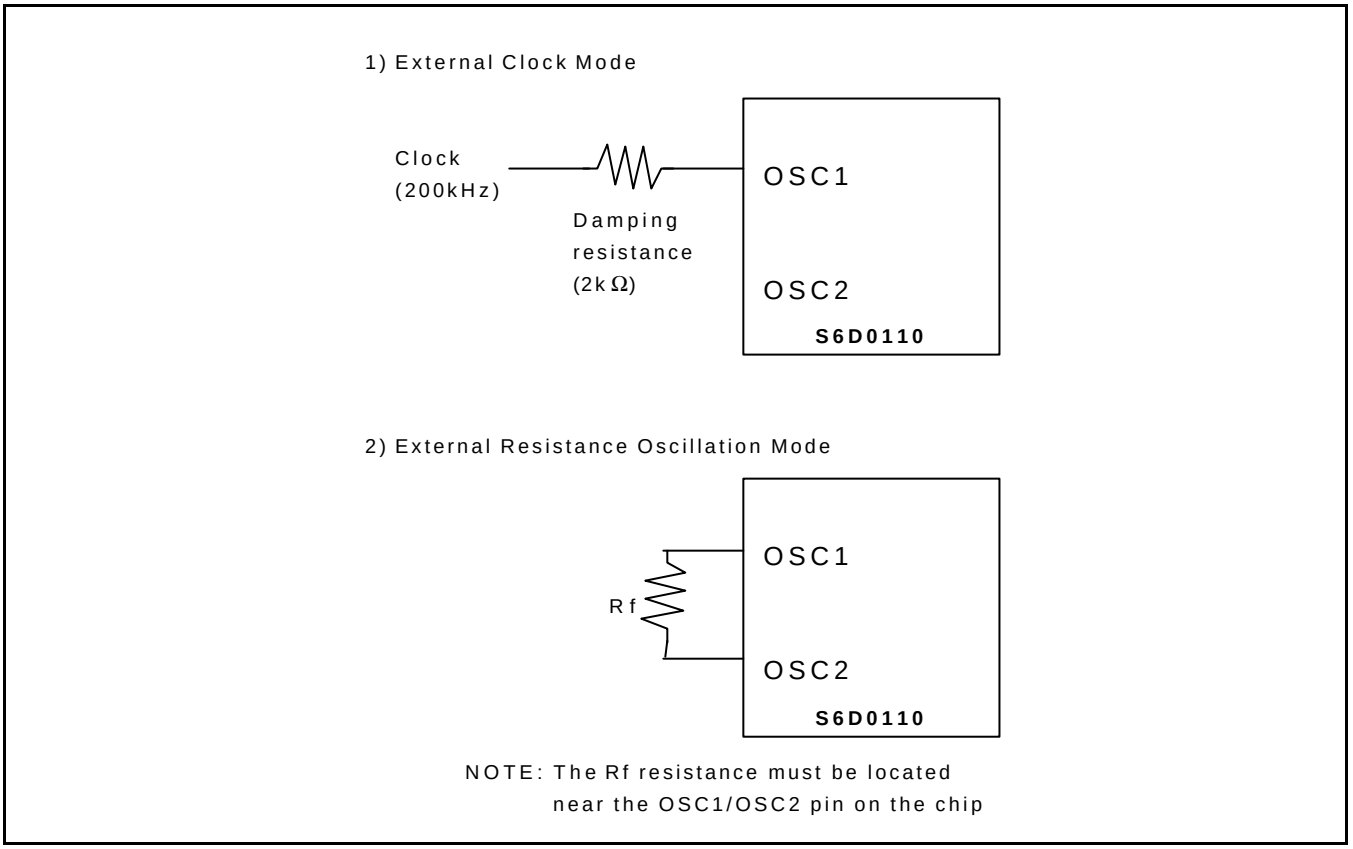

Figure 47. Oscillation Circuit

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N-RASTER-ROW REVERSED AC DRIVE

The S6D0110 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.
Determine the number of the raster-rows n (NW bit set value +1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

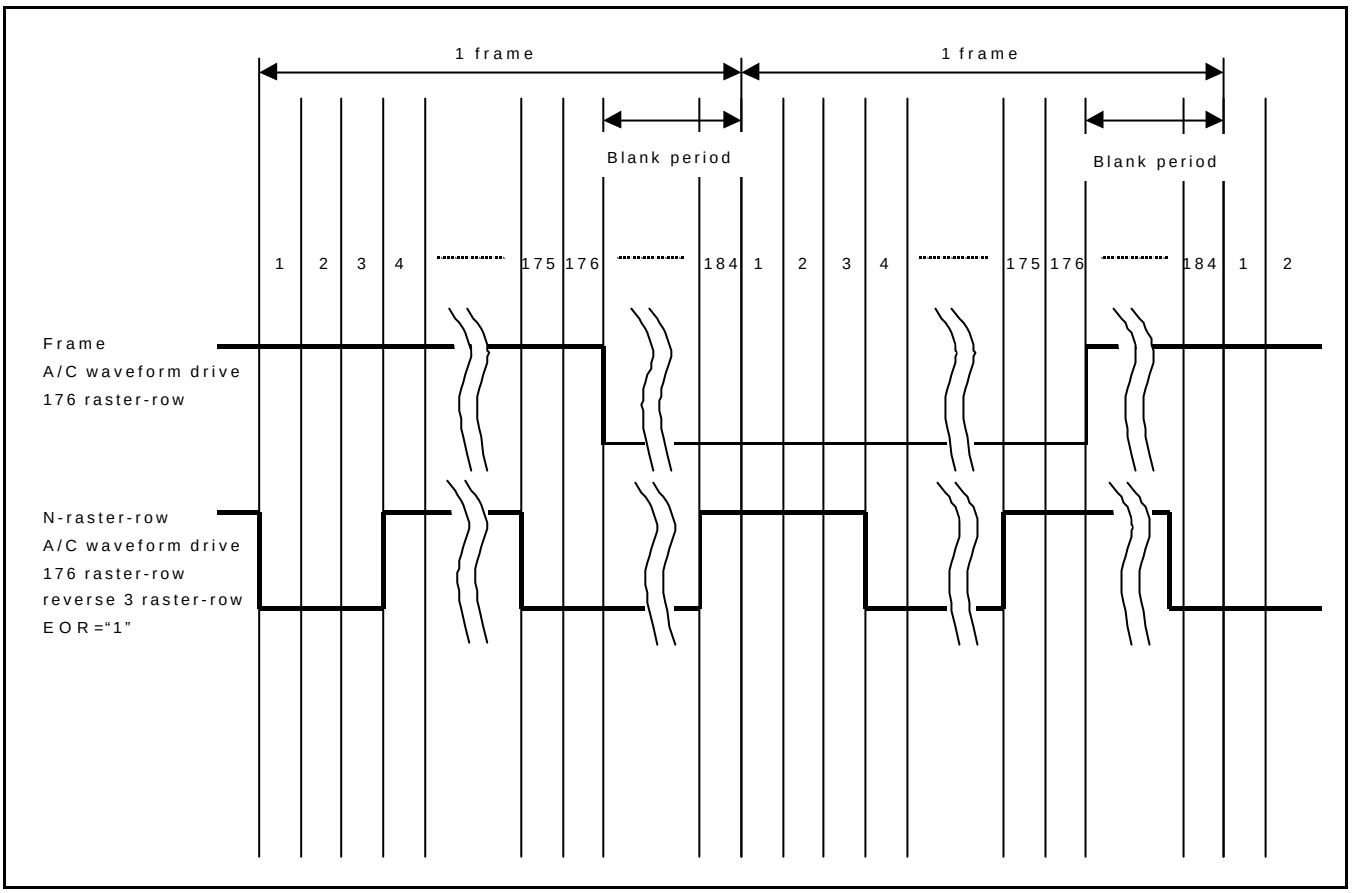

Figure 48. Example of an AC signal under n-raster-row reversed AC drive

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INTERLACE DRIVE

S6D0110 supports the interlace drive to protect from the flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display.
Following table indicates n fields: the gate selecting position when it is 1 or 3. and the diagram below indicates the output waveform when the field interlace drive is active.

GS="0"

FLD1-0 setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
⇓			⇓	
G173	O	O		
G174	O		O	
G175	O			O
G176	O	O		

GS="1"

FLD1-0 setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G176	O	O		
G175	O		O	
G174	O			O
G173	O	O		
G172	O		O	
G171	O			O
G170	O	O		
G169	O		O	
G168	O			O
⇓			⇓	
G4	O	O		
G3	O		O	
G2	O			O
G1	O	O		

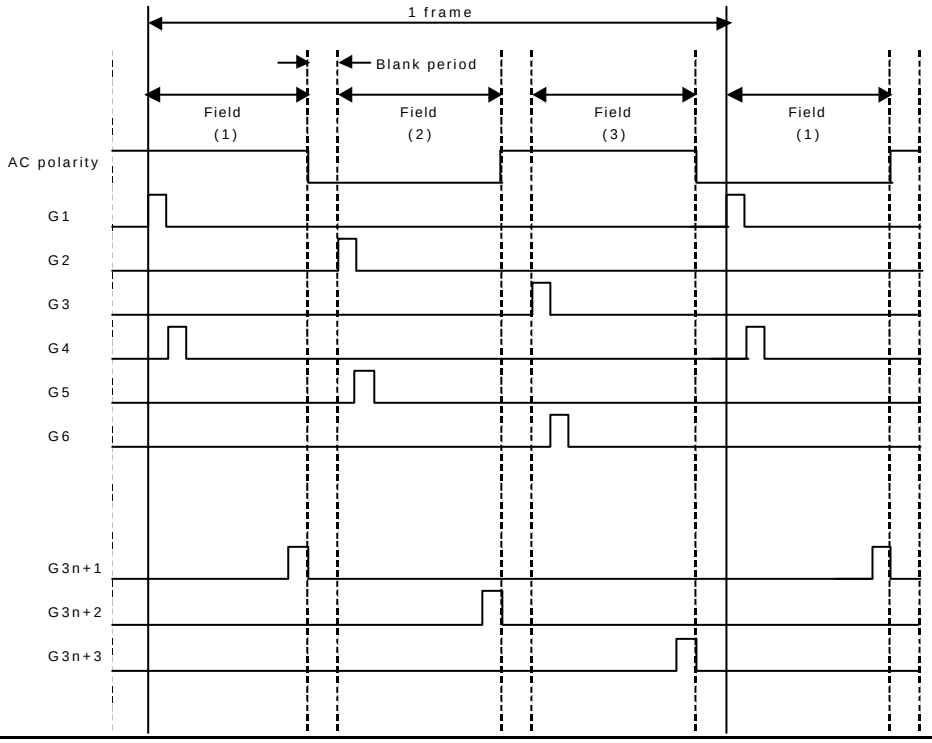

Figure 49. Interlace drive and output waveform

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A/C TIMING

Following diagram indicates the A/C timing on the each A/C drive method. After every 1 drawing, the A/C timing is occurred on the reversed frame AC drive. After the A/C timing, the blank (all gate output: Vgoff level) period described below is inserted. When it is on the interlace drive, blank period is inserted every A/C timing. When the reversed n-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h). In interlace drive mode, Blank period can be adjusted using BLP13-0 and BLP23-0 bit (R09h).

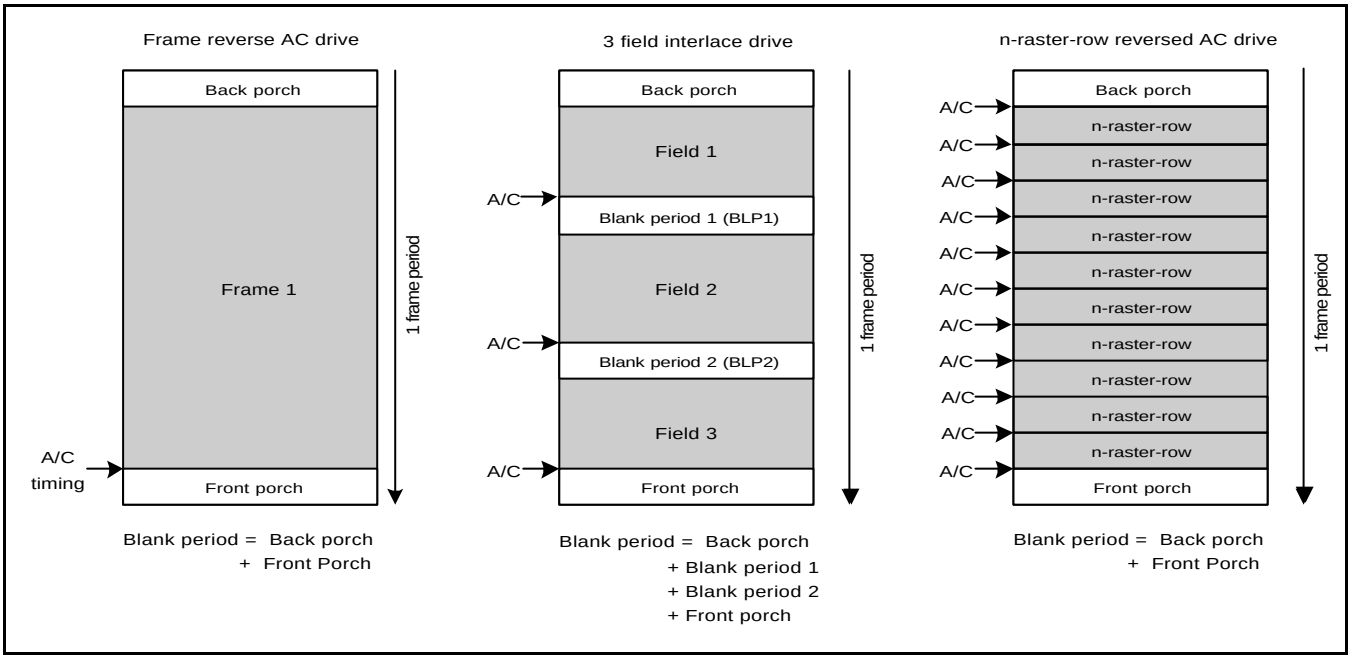

Figure 50. A/C timing

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FRAME FREQUENCY ADJUSTING FUNCTION

The S6D0110 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

RELATIONSHIP BETWEEN LCD DRIVE DUTY AND FRAME FREQUENCY

The relationships between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

$$\text{Frame Frequency} = \frac{f_{OSC}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{OSC}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 51. Formula for the frame frequency

Example calculation

Driver raster-row: 176
1H period: 16 clock (RTN3 to 0 = 0000)
Operation clock division ratio: 1division
B: Blank period (BP + FP): 8

fosc = 60Hz x (0+16) clock x 1 division x (176+B) lines = 177 [kHz]

In this case, the RC oscillation frequency becomes 177 kHz. The external resistance value of the RC oscillator must be adjusted to be 177 kHz.

Note: When FLD1-0=" 11" (interlace drive), B = BP + FP + BLP1 + BLP2

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SCREEN-DIVISION DRIVING FUNCTION

The S6D0110 can select and drive two screens at any position with the screen-driving position registers (R14 and R15). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17 to 10) and end line (SE17 to 10) are specified by the 1st screen-driving position register (R14). For the 2nd division screen, start line (SS27 to 20) and end line (SE27 to 20) are specified by the 2nd screen-driving position register (R15). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

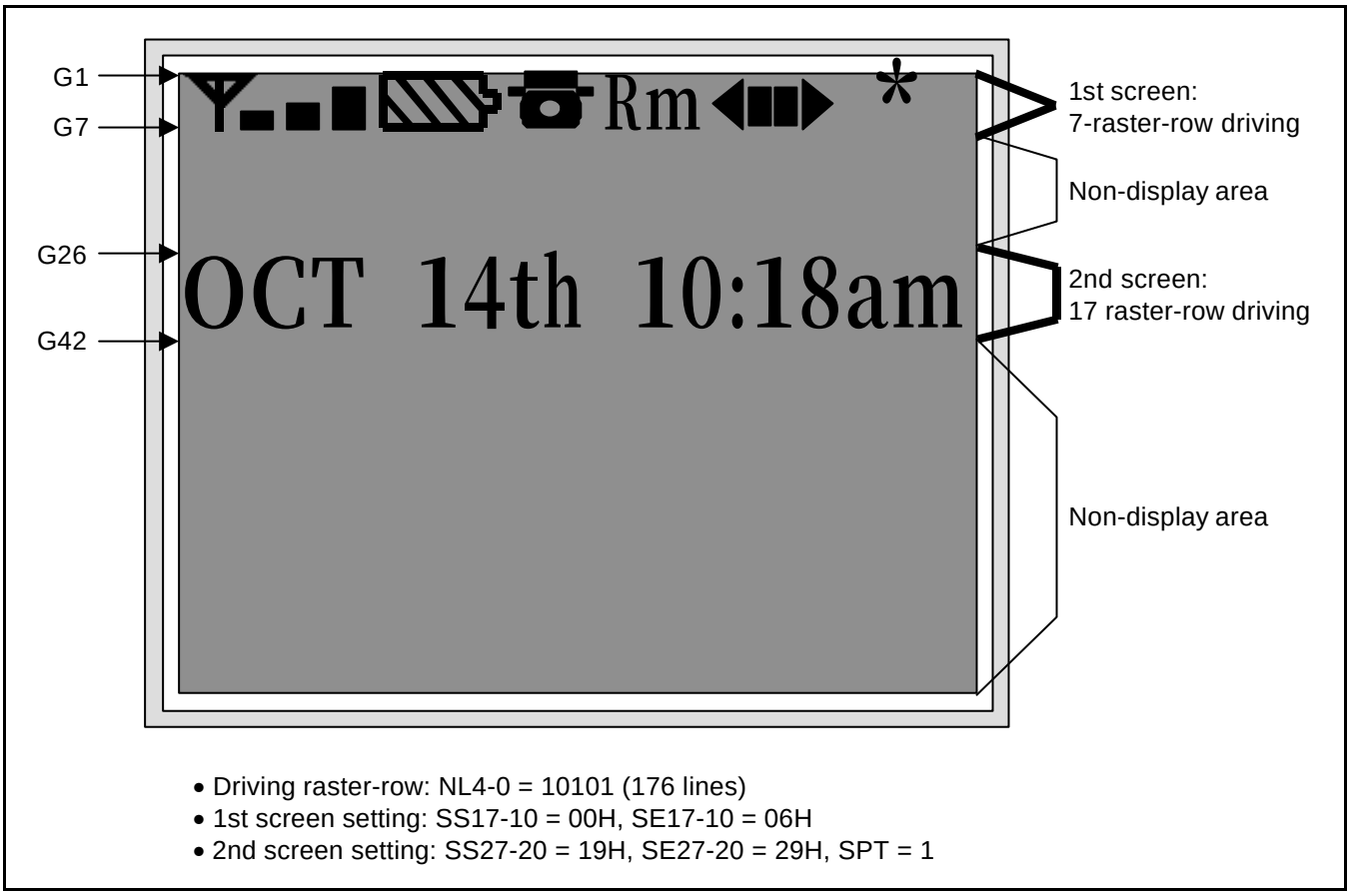

Figure 52. Driving on 2 screen

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RESTRICTION ON THE 1ST/2ND SCREEN DRIVING POSITION REGISTER SETTINGS

The following restrictions must be satisfied when setting the start line (SS17 to 10) and end line (SE17 to 10) of the 1st screen driving position register (R14) and the start line (SS27 to 20) and end line (SE27 to 20) of the 2nd screen driving position register (R15) for the S6D0110. Note that incorrect display may occur if the restrictions are not satisfied.

Table 38. Restrictions on the 1st/2nd Screen Driving Position Register Setting

1st Screen Driving (SPT=0)

Register setting	Display operation
(SE17 to 10) – (SS17 to 10) = NL	Full screen display Normally displays (SE17 to 10) to (SS17 to 10)
(SE17 to 10) – (SS17 to 10) < NL	Partial display Normally displays (SE17 to 10) to (SS17 to 10) White display for all other times (RAM data is not related at all)
(SE17 to 10) – (SS17 to 10) > NL	Setting disabled

NOTE 1: SS17 to 10 ≤ SE17 to 10 ≤ AFh
NOTE 2: Setting SE27 to 20 and SS27 to 20 are invalid

2nd Screen Driving (SPT=1)

Register setting	Display operation
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) = NL	Full screen display Normally displays (SE27 to 10) to (SS17 to 10)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) < NL	Partial display Normally displays (SE27 to 10) to (SS17 to 10) White display for all other times (RAM data is not related at all)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) > NL	Setting disabled

NOTE 1: SS17 to 10 ≤ SE17 to 10 < SS27 to 20 ≤ SE27 to 20 ≤ AFh
NOTE 2: (SE27 to 20) – (SS17 to 10) ≤ NL

The driver output can' t be set for non-display area during the partial display. Determine based on specification of the panels.

PT1	PT0	Source output in non-display area		Gate output in Non-display area
		Positive polarity	Negative polarity	
0	0	V63	V0	Normal drive
0	1	V63	V0	Vgoff
1	0	VSS	VSS	Vgoff
1	1	Hi-Z	Hi-Z	Vgoff

Refer to the following flow to set up the partial display.

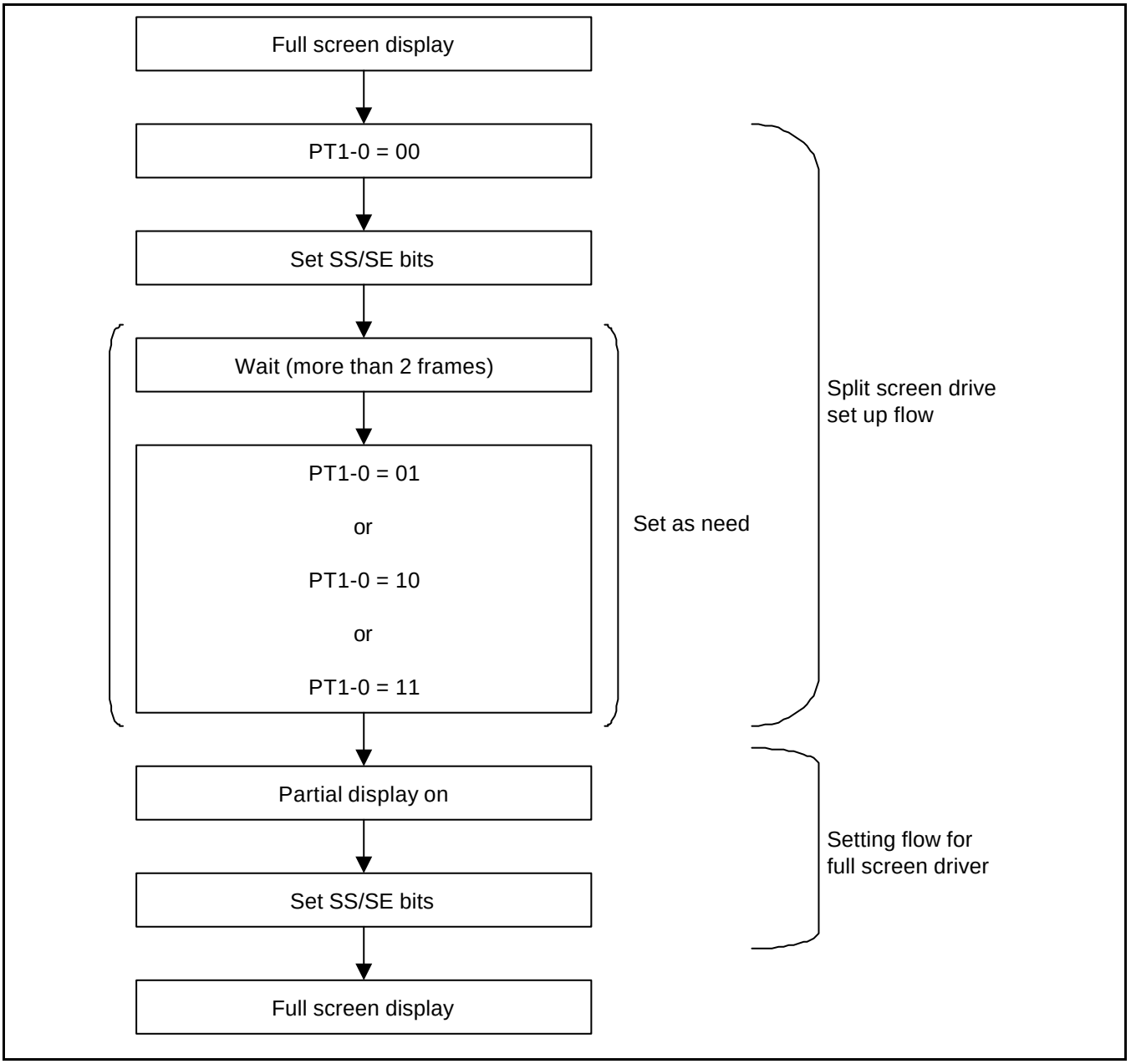

Figure 53. Partial display set up flow

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APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for S6D0110.

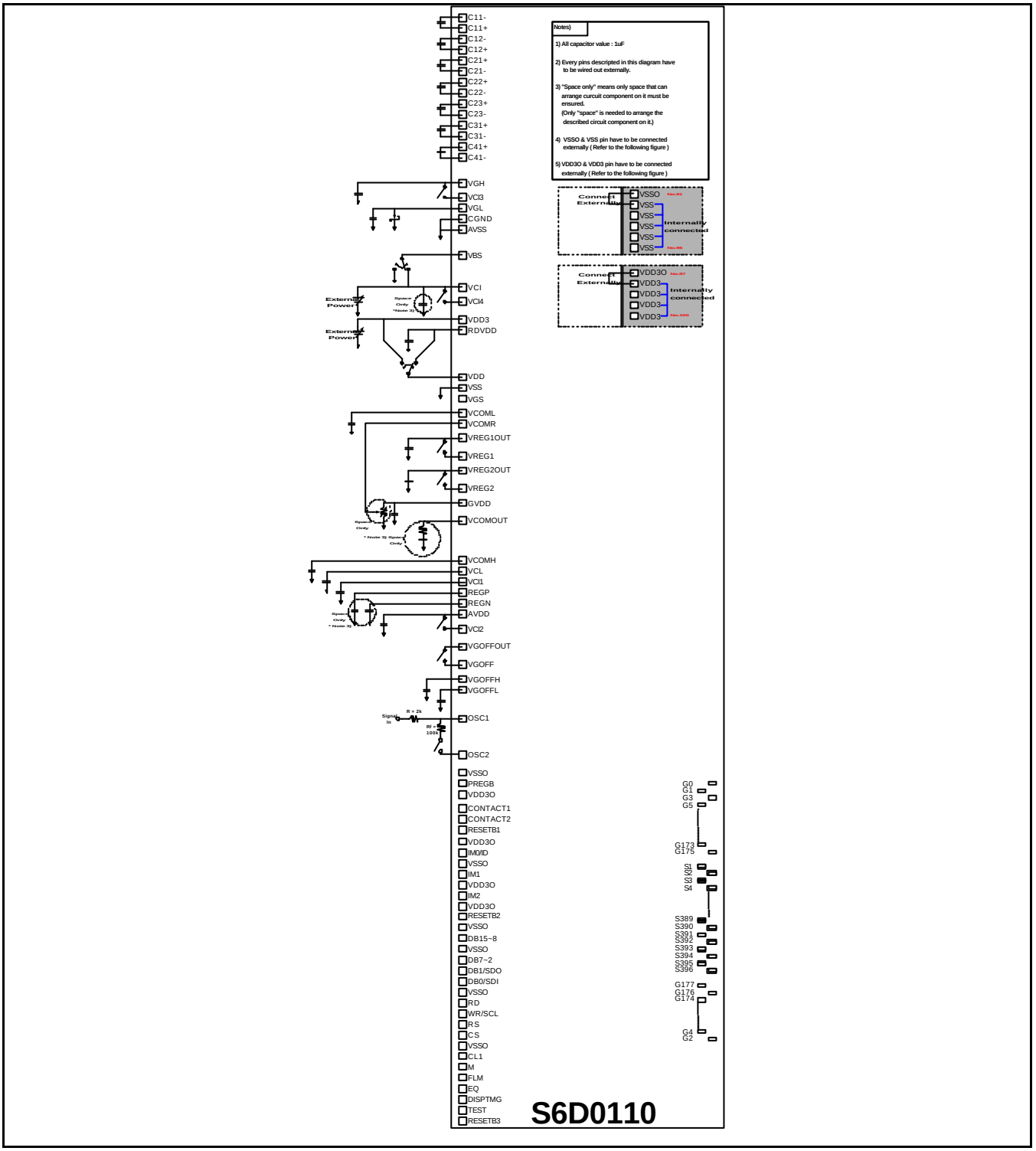

Figure 54. Application Circuit

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 39. Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage	VDD	- 0.3 ~ + 5.0	V
Supply voltage for step-up circuit	Vci	- 0.3 ~ + 5.0	V
LCD Supply Voltage range	|VGH – VGL|	30	V
Input Voltage range	Vin	- 0.3 to VDD +0.5	V
Operating temperature	T_{opr}	-40 ~ +85	°C
Storage temperature	T_{stg}	-55 ~ +110	°C

Notes:

1. Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations.
2. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
3. Absolute maximum rating is guaranteed when our company's package used.

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DC CHARACTERISTICS

Table 40. DC Characteristics

(VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD		1.8	-	2.5	V	*1
	VDD3		2.3	-	3.3	V	*1
LCD driving voltage	VGH		+7	-	20.0	V	
	VGL		-7	-	-15.0	V	
	VGOFF		-5	-	-15	V	
	AVDD		3.5		5.5	V	
	GVDD		3.0		5.0	V	
Input high voltage	V_{IH}		0.7VDD3	-	VDD3	V	*2
Input low voltage	V_{IL}		0	-	0.3VDD3	V	*2
Output high voltage	V_{OH}	I_{OH} = -2.0mA	VDD3-0.5		VDD3	V	*3
Output low voltage	V_{OL}	I_{OL} = 2.0mA	0.0	-	0.5	V	*3
Input leakage current	I_{IL}	VIN = VSS or VDD3	-1.0	-	1.0	μA	*2
Output leakage current	I_{OL}	VIN = VSS or VDD3	-3.0	-	3.0	μA	*3
Operating frequency	fosc	Frame freq. = 60 Hz Display line = 176	159	177	194	KHz	*4
Internal reference power supply voltage	VCI		2.5	-	3.3	V	
1st step-up input voltage	VCI1		1.7	-	2.75	V	
1st step-up output efficiency	AVDD	ILOAD = TBD mA	95	99	-	%	
2nd step-up input voltage	VCI2		3.4		5.5	V	
2nd step-up output efficiency	VGH	ILOAD = TBD mA	95	99	-	%	
3rd step-up input voltage	VCI3		6.8		15	V	
3rd step-up output efficiency	VGL	ILOAD = TBD mA	95	99	-	%	
4th step-up input voltage	VCI4		2.5		3.3	V	
4th step-up output efficiency	VCL	ILOAD = TBD mA	95	99	-	%	

Notes :

1. VSS = 0V.
2. Applied pins; IM2-1, CSB, E, R/W, RS, DB0 to DB15, PREGB, RESETB1,2,3.
3. Applied pins; DB0 to DB15, CL1, M, FLM, EQ, DISPTMG.
4. Target frame frequency = 60 Hz, Display line = 176, Back porch = 3, Front port = 5
   Internal RTN[3:0] register = "0000", Internal DIV[1:0] register = "00"

Table 41. DC Characteristics for LCD driver outputs

(VDD = 1.8V, VDD3 = 3.0V, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LCD gate driver output On resistance	Ron	VGH–VGOFF=30.0V, VGH=18V, VGOFF=-12V, Vgo = VGH – 0.5V	-	-	2	K	*5
LCD source driver high-level output current (Gradation output)	IHOG	Vso = 4.5V, Vsx = 3.5V	-	-	-50	A	*6
LCD source driver low-level output current (Gradation output)	ILOG	Vso = 0.5V, Vsx = 1.5V	50	-	-	A	*6
Output voltage deviation (Mean value)	ΔVo	4.2V ≤ Vso	-	±20	±30	MV	*6
		0.8V < Vso < 4.2V	-	±10	±20	MV	*6
		Vso ≤ 0.8V	-	±20	±30	MV	*6
LCD source driver output voltage range	Vso	-	GVDD+0.1	-	GVDD-0.1	V	
LCD source driver high-level output current (Binary output)	IHOB	Vso = 5.0V, Vsx = 4.0V	-	-	-100	A	*6
LCD source driver low-level output current (Binary output)	ILOB	Vso = 0.0V, Vsx = 1.0V	100	-	-	A	*6
LCD source driver delay	tSD	AVDD = 5.5V GVDD = 5.0V SAP = “001”	-	-	TBD	S	*9
Current consumption during standby mode	Istby	Standby mode, Ta = 25 °C	-	-	-	A	*7
Current consumption during normal operation	IVDD	No load, Ta = 25 °C	-	TBD	TBD	A	*8
	IVCI		-	TBD	TBD	A	*8

Notes :

5. Vgo is the output voltage of analog output pins G0 to G177.
6. Vsx is the voltage applied to analog output pins S1 to S396.
   Vso the output voltage of analog output pins S1 to S396
7. VDD3 = 3.0V, VDD = 2.0V, VCI = 2.7V, VBS = VSS and standby mode.
8. VDD3 = 3.0V, VDD = 2.0V, VCI = 2.7V, VBS = VSS,
   fosc = 177 kHz(176 display line), Internal register, NL[4:0] = “10101”, RTN[3:0] = “0000”, DIV[1:0] = “00”
   Internal power registers, VC[2:0] = “011”, BT[2:0] = “010”, VRH[3:0] = “1100”, VRL[3:0] = “0110”
   VCM[4:0] = “10110”, VDV[4:0] = “10000”

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AC CHARACTERISTICS

Table 42. Parallel Write Interface Characteristics (68 Mode, HWM = 0)

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic		Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
			Min.	Max.	Min.	Max.	
Cycle time	Write	t_{CYCW68}	600	-	250		ns
	Read	t_{CYCR68}	800		500		
Pulse rise / fall time		t_R, t_F	-	25		25	
E pulse width high	Write	t_{WHW68}	90	-	40		
	Read	t_{WHR68}	350		250		
E pulse width low	Write	t_{WLW68}	300	-	70		
	Read	t_{WLR68}	400		200		
RW, RS and CSB setup time		t_{AS68}	10	-	10		
RW, RS and CSB hold time		t_{AH68}	5	-	2		
Write data setup time		t_{WDS68}	60	-	60		
Write data hold time		t_{WDH68}	15	-	2		
Read data delay time		t_{RDD68}	-	200	-	200	
Read data hold time		t_{RDH68}	5		5		

Table 43. Parallel Write Interface Characteristics (68 Mode, HWM = 1)

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic		Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
			Min.	Max.	Min.	Max.	
Cycle time	Write	t_{CYCW68}	200	-	100		ns
	Read	t_{CYCR68}	800		500		
Pulse rise / fall time		t_R, t_F	-	25		25	
E pulse width high	Write	t_{WHW68}	90	-	40		
	Read	t_{WHR68}	350		250		
E pulse width low	Write	t_{WLW68}	90	-	40		
	Read	t_{WLR68}	400		200		
RW, RS and CSB setup time		t_{AS68}	10	-	10		
RW, RS and CSB hold time		t_{AH68}	5	-	2		
Write data setup time		t_{WDS68}	60	-	60		
Write data hold time		t_{WDH68}	15	-	2		
Read data delay time		t_{RDD68}		200		200	
Read data hold time		t_{RDH68}	5		5		

Table 44. Parallel Write Interface Characteristics (80 Mode, HWM = 0)

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic		Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
			Min.	Max.	Min.	Max.	
Cycle time	Write	t_{CYCW80}	600	-	250		ns
	Read	t_{CYCR80}	800		500		
Pulse rise / fall time		t_R, t_F	-	25		25	
Pulse width low	Write	t_{WLW80}	90	-	40		
	Read	t_{WLR80}	350		250		
Pulse width high	Write	t_{WHW80}	300	-	70		
	Read	t_{WHR80}	400		200		
RW, RS and CSB setup time		t_{AS80}	10	-	10		
RW, RS and CSB hold time		t_{AH80}	5	-	2		
Write data setup time		t_{WDS80}	60	-	60		
Write data hold time		t_{WDH80}	15	-	2		
Read data delay time		t_{RDD80}	-	200	-	200	
Read data hold time		t_{RDH80}	5		5		

Table 45. Parallel Write Interface Characteristics (80 Mode, HWM = 1)

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic		Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
			Min.	Max.	Min.	Max.	
Cycle time	Write	t_{CYCW80}	200	-	100		ns
	Read	t_{CYCR80}	800		500		
Pulse rise / fall time		t_R, t_F	-	25		25	
Pulse width low	Write	t_{WLW80}	90	-	40		
	Read	t_{WLR80}	350		250		
Pulse width high	Write	t_{WHW80}	90	-	40		
	Read	t_{WHR80}	400		200		
RW, RS and CSB setup time		t_{AS80}	10	-	10		
RW, RS and CSB hold time		t_{AH80}	5	-	2		
Write data setup time		t_{WDS80}	60	-	60		
Write data hold time		t_{WDH80}	15	-	2		
Read data delay time		t_{RDD80}		200		200	
Read data hold time		t_{RDH80}	5		5		

Table 46. Clock Synchronized Serial Write Mode Characteristics

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic	Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
		Min.	Max.	Min.	Max.	
Serial clock cycle time	tscyc	0.1	20	0.1	20	us
Serial clock rise / fall time	tR, tF	-	20		20	ns
Pulse width high for write	tSCHW	40	-	40	-	ns
Pulse width high for read	tSCHR	230	-	230	-	ns
Pulse width low for write	tSCLW	60	-	60	-	ns
Pulse width low for read	tSCLR	230	-	230	-	ns
Chip Select setup time	tCSS	20	-	20	-	ns
Chip Select hold time	tCSH	60	-	60	-	ns
Serial input data setup time	tSIDS	30	-	30	-	ns
Serial input data hold time	tSIDH	30	-	30	-	ns
Serial output data delay time	tSODD	-	200	-	130	ns
Serial output data hold time	tSODH	5	-	5	-	ns

Table 46. Reset Timing Characteristics

(VDD = 1.8V to 2.5V, T_A = -30 to +85 °C)

Characteristic	Symbol	VDD3 = 1.8V to 2.5V		VDD3 = 2.6V to 3.3V		Unit
		Min.	Max.	Min.	Max.	
Reset low pulse width	tRES	1	-	1	-	us