XFER eXtended FAXENGINE™ Device Set with Reduced Drive

Introduction

The Rockwell eXtended FAXENGINE™ Device Set consists of a Rockwell eXtended Facsimile Controller with reduced drive (XFCR) device and a Rockwell MONOFAX® Modem device. This family of eXtended FAXENGINE (XFER) devices provides upgradability via its hardware and software compatible controllers.

Starting with the basic eXtended Facsimile Controller (XFCR-B), combinations of voice (-V), page memory (-M), plain paper support (-P), and full-duplex speakerphone (-S) support can be added. Voice operation provides minutes (-V24) of digital telephone answering machine (DTAM) recording. Telephone line rates up to 9600 bps (R96) or 14400 bps (R144) are supported. The XFER Device Set models and the supported major functions are listed in Table 1.

Each eXtended FAXENGINE Device Set, including supplied firmware, comprises a complete facsimile machine controller–needing only a power supply, scanner, printer and paper path components to complete the machine.

The FAXENGINE Development System including the FAXENGINE Evaluation System (FEES-X) and the MC24 ROM Emulator (McFERE) provides an effective development environment.

FEATURES

- Microprocessor and Bus Interface
  - Enhanced MC24 central processing unit (CPU)
    - 10 MHz CPU clock speed
    - Memory efficient input/output bit manipulation
    - 24-bit internal address bus
    - 8-bit data bus
  - External Bus
    - Address, data, control, status, interrupt, and decoded chip select signals support connection to external ROM, RAM, and optional peripherals
    - 24-bit external address bus (XFER-B: 20-bit)
  - Chip selects
    - ROMCSn for ROM support
    - CS0n for SRAM
    - CS1n for external peripherals
    - MCSn for modem
    - Optional general purpose: CS2n, CS3n, CS4n and CS5n (CS5n is unavailable on the XFCR-B)
  - DRAM Controller (except XFCR-B, XFCR-P)
    - Supports external page memory
    - Battery-backed refresh with separate battery power
  - DMA Controller
    - Three to six dedicated internal channels for scanner, printer, and T.4/T.6 access of internal and/or external memory
    - External DMA channel (XFCR-P, XFCR-VP and XFCR-MVP only)
  - Internal RAM (1K X 8) for shading correction, line buffers and CPU (XFCR-MV, XFCR-MVP only)
  - External RAM up to 1 (XFER-B) or 14 (other) Mbytes
  - External ROM up to 1 (XFER-B) or 3 (other) Mbytes
- Interrupt controller
- T.4/T.6 Compression and Decompression in Hardware
  - MH/MR (except XFCR-B)
  - MH/MR/MMR (XFCR-MV, XFCR-MVP only)
  - Alternating compression/decompression (XFCR-MV, XFCR-MVP)
- Motor Control for Scanner, and Printer
  - Four outputs to external current drivers for the scanner motor and four for the printer motor
  - Motor outputs can be programmed as general purpose outputs (GPO) for application with a single motor or plain paper machines
- Scanner and Video Control
  - CCD and CIS scanners supported
  - Six programmable control signals:
    - Four programmable scanner control signals
    - Two video output control signals support external signal pre-processing
  - B4/A4 scanner support
  - 5 ms minimum line time
  - Line lengths to 4096 pixels
  - Scanner flash A/D Interface
    - Internal 6-bit flash A/D converter
    - A/D reference inputs enable external control
    - Video Processing
    - Per-pixel and per eight-pixel shading correction
    - Edge enhancement and dynamic background and contrast control
    - Up to 8x8 programmable dither table
    - Image data processing port allows access to scan data prior to video processing
  - Multi-level B4 to A4 size reduction (except XFCR-B)
- Programmable Resolution Conversion (see Table 1)
  - Two-dimensional bi-level resolution conversion provides expansion to 200%; reduction to 33%
  - Vertical line ORing
  - Scanner output bit order reversal

Table 1. Summary of XFER Family Characteristics

FAXENGINE Device Set	XFCR Fax Controller	MONOFAX Fax Modem	Page Memory	MH/MR/ MMR	DRAM Control	External DMA and Resolution Conversion	DTAM Recording Time (Minutes)[4]	Speakerphone
R96XFER-B	XFCR-B	R96DFXL		1				
R96XFER-M	XFCR-MV	R96DFXL	YES	3	YES			
R96XFER-P	XFCR-P	R96DFXL		2		YES		
R96XFER-MP	XFCR-MVP	R96DFXL	YES	3	YES	YES		
R144XFER-B	XFCR-B	R144EFXL		1				
R144XFER-M	XFCR-MV	R144EFXL	YES	3	YES			
R144XFER-P	XFCR-P	R144EFXL		2		YES		
R144XFER-MP	XFCR-MVP	R144EFXL	YES	3	YES	YES		
R96XFER-V24	XFCR-V	RFX96V24		2	YES		24	
R96XFER-V24S	XFCR-V	RFX96V24-S23		2	YES		24	YES
R96XFER-MV24	XFCR-MV	RFX96V24	YES	3	YES		24	
R96XFER-MV24S	XFCR-MV	RFX96V24-S23	YES	3	YES		24	YES
R96XFER-V24P	XFCR-VP	RFX96V24		2	YES	YES	24	
R96XFER-V24PS	XFCR-VP	RFX96V24-S23		2	YES	YES	24	YES
R96XFER-MV24P	XFCR-MVP	RFX96V24	YES	3	YES	YES	24	
R96XFER-MV24PS	XFCR-MVP	RFX96V24-S23	YES	3	YES	YES	24	YES
R144XFER-V24	XFCR-V	RFX144V24		2	YES		24	
R144XFER-V24S	XFCR-V	RFX144V24-S23		2	YES		24	YES
R144XFER-MV24	XFCR-MV	RFX144V24	YES	3	YES		24	
R144XFER-MV24S	XFCR-MV	RFX144V24-S23	YES	3	YES		24	YES
R144XFER-V24P	XFCR-VP	RFX144V24		2	YES	YES	24	
R144XFER-V24PS	XFCR-VP	RFX144V24-S23		2	YES	YES	24	YES
R144XFER-MV24P	XFCR-MVP	RFX144V24	YES	3	YES	YES	24	
R144XFER-MV24PS	XFCR-MVP	RFX144V24-S23	YES	3	YES	YES	24	YES

Notes: 1. MH in software.
2. MH/MR in hardware.
3. MH/MR/MMR and alternating compression/decompression in hardware.
4. DTAM recording time is shown for voice storage using 4 Mbits of memory.

FEATURES (CONT'D)

- Thermal Printer Interface
  - 1 to 4 programmable strobe signals
  - Traditional printers and latchless "split mode" printers
  - Line lengths up to 4096 pixels
  - Line times from 5 to 40 ms
  - A/D converter monitors printer head temperature
- Programmable Tone Generator
- Operator Interface
  - The XFCR can directly drive a 32-key keypad (XFCR-B: 20)
  - A 8x15 keyboard array is supportable with external circuitry (XFCR-B: 5x15)
  - Up to eight LEDs are driven directly (XFCR-B: 5)
  - Typical LCD display modules are supported
- Autobaud Interface
  - Automatically detects data rate for external UART support

Synchronous Asynchronous Receiver Transmitter (SART) Interface

  - Programmable baud rate generator to 9600 bps
  - Async mode: 1 start bit, 7/8 data bits, 1 stop bit, no parity
  - Sync mode: 8 data bits
  - Firmware controllable TXD and SCLK
- General Purpose Inputs and/or Outputs
  - Provides up to 20 GPIO (XFCR-B: 16) and 8 GPOs
- Real Time Clock
  - Battery backup
  - 32-year range with leap year compensation
- Watchdog Timer
- Compact Packages
  - XFCR: 144-pin TQFP
  - MONOFAX Modem: 100-pin PQFP
  - XIA: 28-pin PLCC
- FAXENGINE Development System (FEES-X, MC24 FERE)
  - Provides demonstration, prototype development, and evaluation capabilities to facsimile machine developers using the FAXENGINE Device Set
  - Connects to a host PC for software development

DESCRIPTION

FAXENGINE eXtended Facsimile Controller

The XFCR provides design flexibility by virtue of its built-in peripheral functions (e.g., scanner, printer, and operator interfaces) and programmable hardware registers.

The XFCR performs the primary facsimile machine control and monitoring functions, interfacing with all major fax machine components. The MC24™ embedded processor provides an 8-bit data bus, a 24-bit internal address bus and a direct external memory accessing capability of 16 Mbytes (2 Mbytes for the XFCR-B).

Scanner, printer, and keyboard interfaces, as well as motor control and the modem interface, are included. These programmable functions and interfaces support a wide range of peripherals. An integrated flash ADC, combined with Rockwell's Proprietary Image Correction System (RPICS™), provides state-of-the-art image processing performance on both bi-level and half-tone images.

MONOFAX Modems

Different MONOFAX modem models are available with selection depending upon the desired applications. The R144EFXL and R96DFXL support V.29 and V.17 fax machines, while the RFX modems add integrated fax/digital answering machine functionality by providing a voice codec that yields up to 12 (V12) or 24 (V24) minutes of voice storage per 4 Mbits of memory.

The RFX-S modems support the full range of features listed above and add DigiTalk full-duplex speakerphone features for “Natural” hand-free applications. An integrated Analog front-end (IA) is added to support full-duplex speakerphone operation.

FAXENGINE Firmware

The FAXENGINE firmware includes a complete software package–core code and application code–for the development of a customized facsimile machine. The following features are supported by the firmware:

- A real-time multitasking environment
- Modular software design
- T.30 protocol
- Call progress support for multiple countries
- T.4 MH compression and decompression (XFER-B)
- T.4 MH/MR & T.6 MMR control routines
- Alternating compression/decompression for MMR
- B4 to A4 reduction
- Fax transmit, receive and copy capabilities
- Polling, Broadcast and Delayed Transmission functions
- Page memory functions
- Digital Answering Machine functions
- Voice/Fax Discrimination

Core Code. The Core Code provides the functions with close functional proximity to the XFER hardware. The Core Code is provided in object code form ready for linking to developer-provided application program object code. The Core Code is highly structured for maximum application flexibility with minimum overhead.

Application Code. The Application Code “builds” an example fax machine using the XFER device set in the FEES-X environment. This code is provided in source code form and serves as basis for the developer’s application.

FAXENGINE Development System

The Rockwell FAXENGINE Evaluation System (FEES-X) and MC24 FERE ROM Emulator provides demonstration, prototype development, and evaluation capabilities to facsimile machine developers using the eXtended FAXENGINE Device Set. The FEES-X offers flexibility for visibility and access. It supplies the Modem Evaluation Board with Data Access Arrangement (DAA), sockets for programmable parts, and connectors for an emulator and all fax machine peripherals. The ROM Emulator (MC24 FERE) is a PC-based code development aid with breakpoint and trace capability for debugging firmware.

HARDWARE DESCRIPTION

The XFER system-level functional interface is shown in Figure 1. (**Note:** The suffix n indicates an active low signal.)

eXtended Facsimile Controller (XFCR)

The XFCR contains an internal 8-bit microprocessor with a 16-Mbyte (XFCR-B: 2-Mbyte) external address space and dedicated circuitry optimized for facsimile image processing, data compression/decompression and for facsimile machine control and monitoring.

Microprocessor

The microprocessor is an enhanced MC24 central processing unit (CPU). This CPU provides fast instruction (10 MHz clock speed) execution and memory efficient input/output bit manipulation. The CPU connects to other internal XFCR functions over a internal 24-bit address bus, 8-bit data bus, and dedicated control lines. The bus is routed outside the XFCR for external memory access. The external address bus is 24-bit except for the XFCR-B which provides a 20-bit external address bus.

External Bus Control

Address, data, control, status, interrupt, and decoded chip select signals support connection to external ROM, external RAM, and optional DRAM and peripheral devices. Dedicated internal DMA logic is included for scanner, printer and T.4 access of internal and/or external RAM.

Five (three for XFCR-B) internal DMA channels support scanner, printer and T.4 access of the external shading and line buffer RAM. A sixth DMA channel is available to support T.4/T.6 access to external page memory (“External DMA” column, Table 1) or to plain paper printer engines.

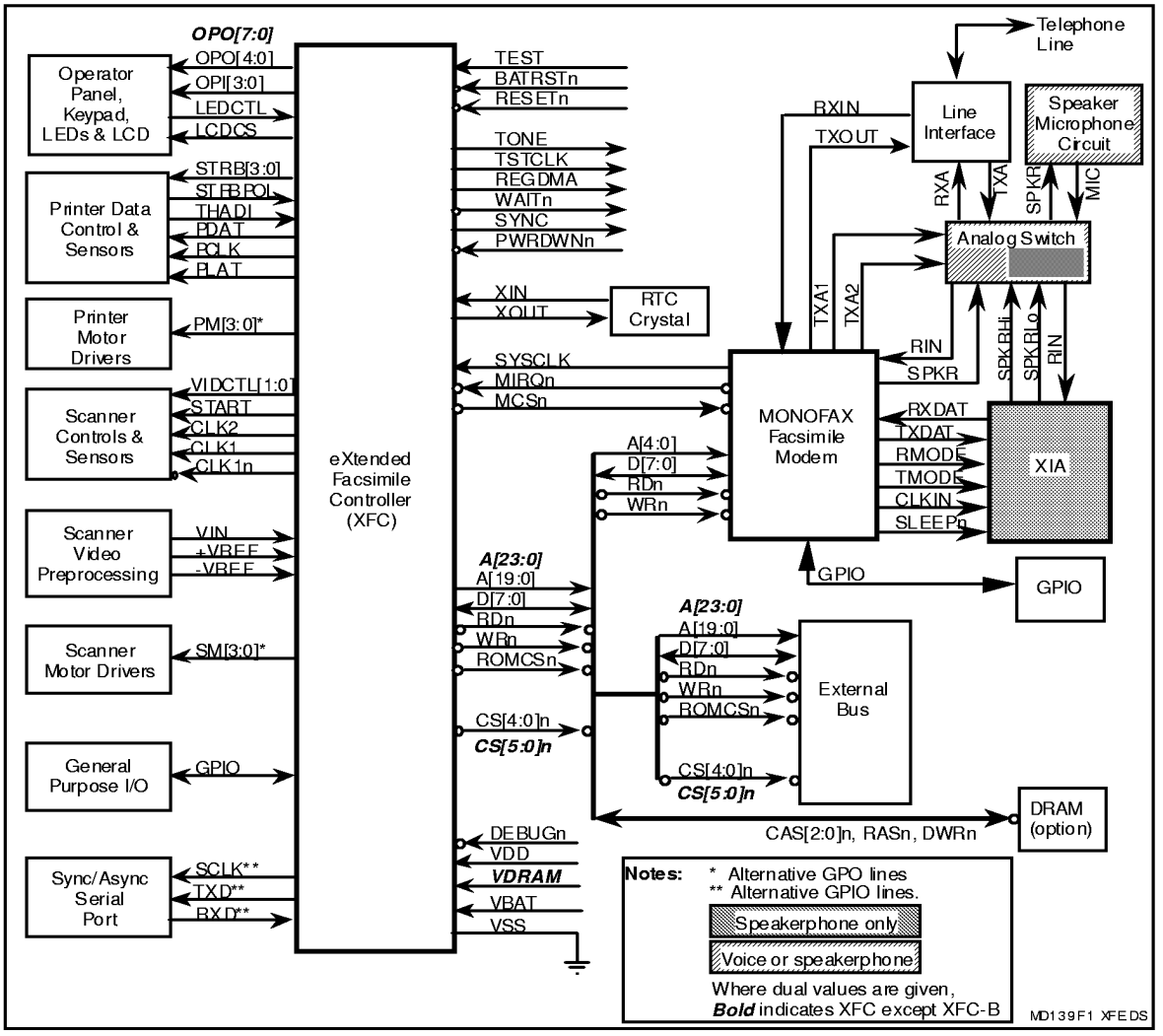


Figure 1. XFER Functional Interconnect Diagram

External RAM and ROM

Up to 1 Mbyte of RAM and up to 1 Mbyte of ROM can be connected to the XFCR-B as well as external peripherals. Other versions of the XFCR can use up to 3 Mbytes of ROM and up to 14 Mbytes of RAM. ROM stores all the FAXENGINE program object code and RAM is used by the FAXENGINE CPU, shading RAM and line buffer RAM.

Independently programmable RAM and ROM wait states from 0 to 3 are supported. RAM sizes may be 8k, 32k, 64k and 1M bytes.

Chip Selects

Various chip selects (CS) are provided by the XFCR such as ROMCSn, CS0n for SRAM, CS1n for external peripherals, MCSn for modem, and optional general purpose chip selects CS[4:2]n and CS5n (except XFCR-B).

Interrupt Signals

Up to four external interrupts are provided. IRQ8 (GPIO16) is an active high level sensitive interrupt; IRQ5n (GPIO17) and IRQ10n (GPIO18) (except XFCR-B) are active low level sensitive interrupts. MIRQn is dedicated to the modem.

Scanner and Printer Motor Control

Eight outputs are provided to external current drivers: four for the scanner motor and four for the printer motor. The printer and scanner motor outputs can be programmed as general purpose outputs (GPO) for applications using a single motor or plain paper printers.

T.4/T.6 Compressor/Decompressor (See Table 1)

The XFCRs (except XFCR-B) implement MH and MR data compression and decompression per ITU-T Recommendation T.4 in hardware. The XFCR-MV and -MVP also provide MMR data compression and decompression per ITU-T Recommendation T.6 in dedicated hardware. Compression and decompression can be alternated on a line-by-line basis in the XFCR-MV and -MVP as well.

DRAM Controller (See Table 1)

The DRAM controller supports memory devices of the sizes, number of bits and access speeds tabulated below. DRAM memory space is divided into three blocks thus, if 4M chips are used, a maximum of 12 Mbytes of DRAM is supported. Each block has a programmable size and starting address.

Addressing Size	4M, 1M, 512k, 256k
No. of Bits	8, 4, 1
Access Speed (ns)	60 to 150

The DRAM controller provides battery backed-up refresh using DRAM battery power (VDRAM).

Bi-Level Resolution Conversion (See Table 1)

Bi-level expansion (to 200%) and reduction (down to 33%) can be performed on either the scanner bi-level data (described herein), or the bi-level data output by the T4/T6 decompression hardware.

Thermal Printer Control

The thermal printer interface consists of programmable data, latch, clock, and up to four strobe signals. Programmable timing supports traditional thermal printers, as well as latchless and two-clock split mode printers, and line lengths up to 4096 pixels.

From one to four strobes are generated, with the length of the strobe cycle (line time) and strobe pulse width programmable. Line times from 5 to 40 ms are supported. A strap input to the XFCR sets the strobe polarity.

Three signals (PDAT, PCLK, and PLAT) control the transfer of data to the printer.

The XFCR includes a 6-bit A/D converter (conversion rate < 80 ms full scale) to monitor the head temperature of the thermal printer. Two external terminating resistors are determined by the specific printhead selected.

Scanner and Video Control

Six programmable control and timing signals support common CCD and CIS scanners. The video control function provides signals for controlling the scanner and for processing its video output. Four programmable control signals (START, CLK1, CLK1n, and CLK2) provide timing related to line and pixel timing. These are programmable with regard to start time, relative delay and pulse width.

Two video control output signals (VIDCTL[1:0]) provide digital control for external signal pre-processing circuitry. These signals provide a per pixel period, or per line period, timing with programmable positive-going and negative-going transitions for each signal.

Scanner Flash A/D Interface

An internal 6-bit flash A/D converter (FADC) and ADC clock are provided. The A/D reference inputs (Vref+ and Vref–) are available for control by external circuits. A programmable ADC sample position is provided and external video circuits can be tailored by the developer.

Video Processing

The XFCR supports two modes of correction for scanner data non-uniformities arising from uneven sensor output or uneven illumination. Correction may be provided to an 8-pixel group at a time or, separately to each pixel. Less than 1k bytes of RAM is required to support shading correction. Dynamic background and contrast control is provided for text images. Dithering with edge enhancement is performed for half-tone images. The XFCR includes a programmable 8x8 dither table, which is stored in internal RAM (8 bits per table entry). The table is arranged in a matrix of up to 8 rows by up to 8 columns. Multi-level horizontal B4 to A4 reduction is also provided (except XFCR-B) for the scanner data.

The XFCR includes an optional external image data processing port (multiplexed with GPIO) to allow the OEM developer to access scan data prior to video processing in order to perform proprietary processing.

VID0 - VID7 = parallel output port for multi-level FADC data or shading (or reduced shading) corrected data

VIDC0 - VIDC1 = control for synchronization with video port data

VIDC2 = bi-level data input for externally processed image data

Operator Interface

Operator interface functions are supported by the operator output bus OPO[7:0] (OPO[4:0] for the XFCR-B), the operator input bus OPI[3:0], and two control outputs (LEDCTL and LCDCS).

The XFCR can directly drive a 32-key keypad (20-key for the XFCR-B). External blocking diodes are required to isolate the keyboard strobe lines from the LEDs, as the LEDs and keyboard strobe signals use the same lines. An 8x15 keyboard array is supportable with external circuitry (5x15 for the XFCR-B).

Up to eight LEDs (five for the XFCR-B) can be driven directly by the XFCR. The keyboard strobes are shared with the LED drivers. An LED control signal is provided to disable the LEDs during keyboard strobing. The XFCR slightly offsets LED turn on/off times thereby preventing power supply overload when all indicators must be activated simultaneously. The LEDCTL signal can supply 12 mA.

Typical LCD display modules are driven by the XFCR. The XFCR drives the 4-bit bus (OPO[3:0]) and two separate control lines (OPO4 and LCDCS) for LCD support. (For example, the FAXENGINE Development System FEES-X uses a 2-line, 20 character per line, display.)

Synchronous Asynchronous Receiver Transmitter (SART)

The SART performs serial-to-parallel (S/P) conversion for data received from a peripheral device, and a parallel-to-serial (P/S) conversion of data for transmission to a peripheral device. The interface consists of three lines: TXD, RXD and clock (SCLK). The SART includes a programmable baud rate generator and produces an 8X clock for driving internal logic. Receive data is double-buffered to ease received timing restrictions.

SART status can be read at any time by the CPU. Status includes: IRQ source (TXD or RXD) and operation mode (sync or async). The CPU can also control and monitor TXD and SCLK: RXD can be monitored at any time.

Autobaud

The autobaud circuit with supporting firmware is used to analyze a serial data stream in order to determine the baud rate and data structure (parity and character length) to program an external UART.

A precision timer, shift register and edge detector are included to determine the width of the start bit, and to sample the serial data stream. Serial data rates up to 115.2 kbps are supported.

The serial transmitted data is connected to the precision timer and shift register inputs via the SERINP pin. The SEROUT pin is a gated version of the SERINP pin which can be enabled/disabled.

Real-Time Clock (RTC)

The XFCR includes a battery backed-up real-time clock. The RTC life is 32 years; its functions include leap year compensation. A 32.768 kHz watch crystal is required by the RTC.

General Purpose Inputs and/or Outputs

The XFCR provides up to 20 GPIO (16 for XFCR-B) and 8 GPO lines.

Programmable Tone Generator

A programmable tone generator provides single tone digital output, variable in frequency from 20 to 4000 Hz.

System Timing

The XFCR can derive its timing from the modem clock or from an external oscillator (max. frequency = 20 MHz). Two internal timer interrupts are provided:

- A 1 ms timer derived from the RTC oscillator timebase (exact period = 1.00708 ms).
- A programmable mechanical subsystem interrupt (MSINT) which serves as a source for motor stepping interrupts and/or scanner and printer interrupts. Independent, programmable, scan and print line times are supported.

Reset and Power Control

The BATRSTn input initializes the XFCR at power-on. An externally generated power-down input, PWRDWNn, controls switching between primary and battery power. The open drain RESETn I/O pin provides a reset output to external circuits, or can accept an externally generated reset. The external reset will not reset the RTC. Separate DRAM and RTC battery power inputs are provided for battery-backed up functions.

Documentation

Reference documentation for the XFER family of devices and MONOFAX modems is listed in Table 2.

Environmental and Power Requirements

Environmental requirements are listed in Table 3and power requirements are listed in Table 4.

XFCR Interface Signals

The XFCR hardware signal pin assignments are shown in Figure 2 (XFCR-B) and Figure 3 (all others), and are described in Table 5 and Table 6. Hardware signal characteristics are described in Table 5 through Table 7.

FACSIMILE MODEM INTERFACE SIGNALS

R96DFXL and R144EFXL pin assignments are shown in Figure 4 and described in Table 8. RFX modem hardware interface signals are shown in Figure 5 and described in Table 9. Pin assignments for the 28-pin XIA used with an RFX modem are shown in Figure 6 and are described in Table 10. Modem digital interface signal characteristics are listed in Table 11 and the analog interface characteristics are listed in Table 12.

Reference Documentation

Table 2. Reference Documentation

Document	Order No.
R96DFXL MONOFAX Modem Data Sheet	MD92
R144EFXL MONOFAX Modem Data Sheet	MD90
RFX144V24-S23 and RFX96V24-S23 MONOFAX Modems Data Sheet	MD141
9600 bps MONOFAX Modem Designer's Guide	820
9600 bps MONOFAX Modem Designer's Guide–Addendum for R96DFXL	820A
R144EFXL MONOFAX Modem Designer's Guide	895
RFX144V24-S and RFX96V24-S MONOFAX Modems Designer's Guide	1045
RFX144V24-S23 and RFX96V24-S23 MONOFAX Modems Designer's Guide	1070
MC24 Megacell CPU Programmer's Guide	415
eXtended Facsimile Controller (XFCR-B) Hardware Description	1039
eXtended Facsimile Controller (XFCR) Hardware Description (all except -B)	1065
eXtended FAXENGINE (XFER-B) Firmware Description	1040
FAXENGINE Evaluation System (FEES-X) User's Manual	1041
MC24 FAXENGINE ROM Emulator System (MC24 FERE) User's Manual	1016

Environmental Requirements

Table 3. Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32°F to 158°F)
Storage	-40°C to 80°C (-40°F to 176°F)
Relative Humidity	Up to 90% non-condensing, or a wet bulb temperature up to 35°C, whichever is less.

Power Requirements

Table 4. Power Requirements

Device	Voltage (Note 1)	Typical Current @25°C (Note 3)	Maximum Current @ 0°C (Note 3)
XFCR-B and XFCR			
Primary Power			
XFCR-B	+5 VDC +5%/-10%	60 mA	65 mA
XFCR	+5 VDC +5%/-10%	65 mA	70 mA
Battery Power and RTC (Note 2)			
	+5 VDC +3 VDC	18.5 µA 5.0 µA	21.0 µA 5.5 µA
MONOFAX Modems			
R96DFXL	+5 VDC ±5%	50 mA	55 mA
R144EFXL	+5 VDC ±5%	54 mA	60 mA
RFXV24 and RFXV24-S23-S	+5 VDC ±5% (Note 4)	124/2.15 mA	149/2.8 mA

Notes:
1. Input voltage ripple ²0.1 volts peak-to-peak. The amplitude of any frequency between 20 and 150 kHz must be less than 500 microvolts peak.
2. Real Time Clock (RTC) battery power measurements made with a 32.768 kHz crystal oscillator.
3. Normal/Standby current.
4. Modem and XIA combined.

HARDWARE INTERFACE SIGNALS

The XFCR hardware pin assignments are shown in Figure 2 (XFCR-B) and Figure 3 (all others); the signals are described by type in Table 5 and Table 6.

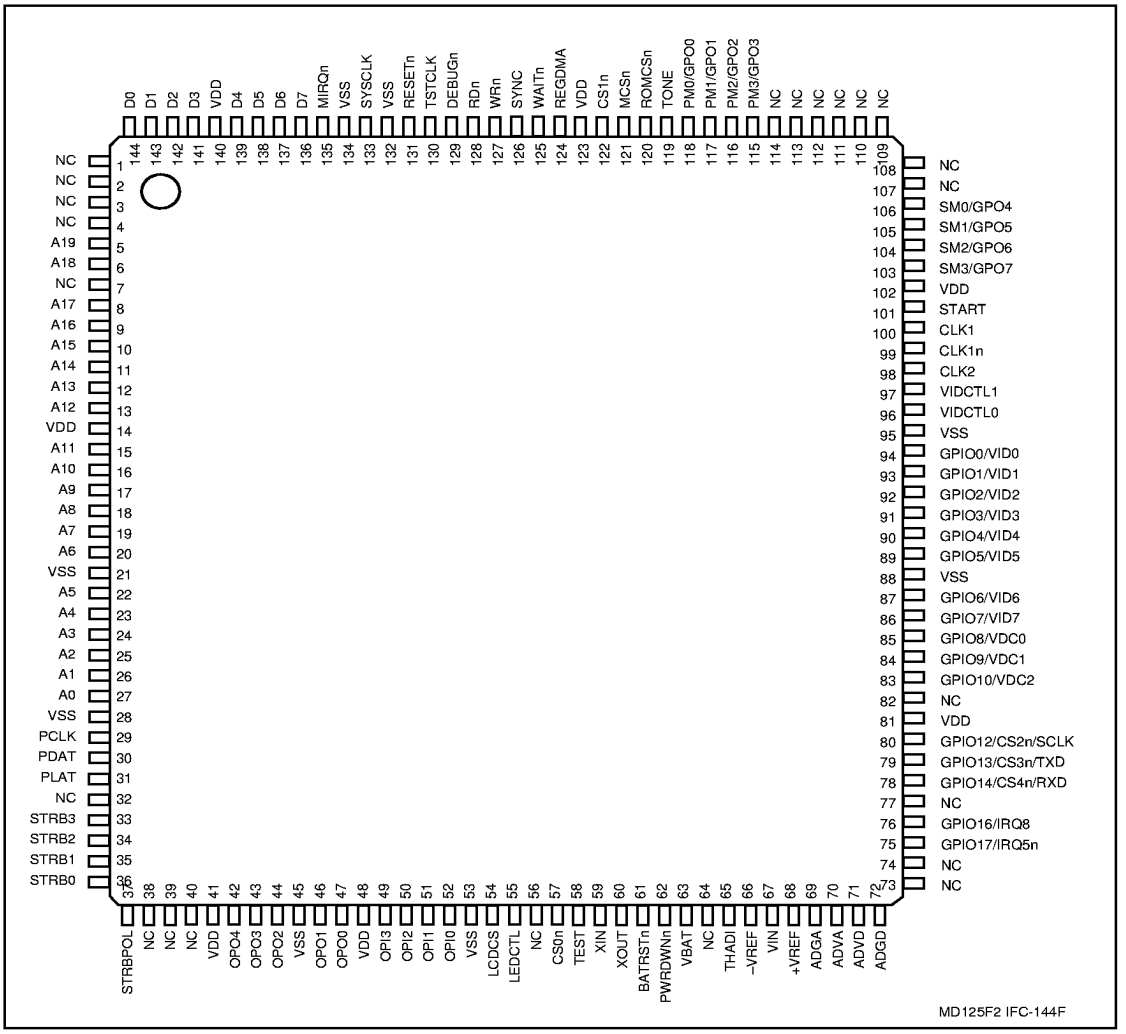


Figure 2. XFCR-B Pin Signals - 144-Pin TQFP

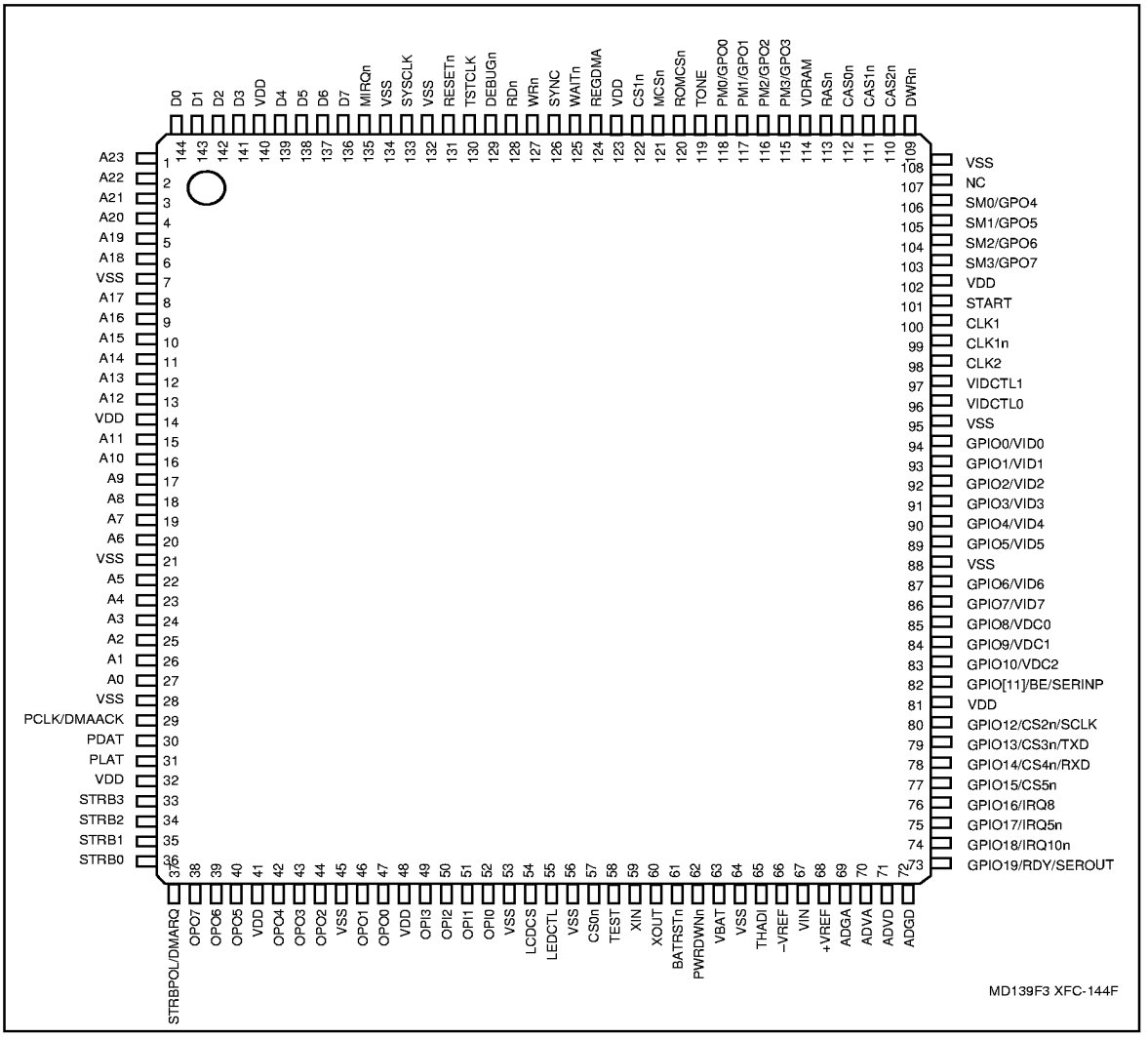


Figure 3. XFCR (Except -B) Pin Signals 144-Pin TQFP

Table 5. XFCR-B Pin Assignments

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description (Note: Active low signals have an "n" pin name ending.)
CPU Control Interface					
MIRQn	135	I	HU	--	Modem interrupt, active low. (Hysteresis In, Internal Pullup.)
SYSCLK	133	I	H	--	System clock. (Hysteresis In.)
TSTCLK	130	O	--	1XC	Test clock.
Bus Control Interface					
A[19:0]	[5:6][8:13] [15:20][22:27]	O	T	1XT	Address bus (20-bit).
D[7:0]	[136:139] [141:144]	I/O	T	1XT	Data bus (8-bit).
RDn	128	O	--	1XTT	Read strobe.
WRn	127	O	--	1XTT	Write strobe.
ROMCSn	120	O	--	1XT	ROM chip select.
CS1n	122	O	--	1XT	I/O chip select.
CS0n	57	O	--	1XTT	SRAM chip select. (Battery powered.)
MCSn	121	O	--	1XC	Modem chip select.
SYNC	126	O	--	1XC	Indicates CPU op code fetch cycle (active high).
REGDMA	124	O	--	1XC	Indicates REGSEL cycle and DMA cycle.
WAITn	125	O	--	1XC	Indicates current TSTCLK cycle is a wait state or a halt state.
Prime Power Reset Logic and Test					
DEBUGn	129	I	HU	--	External non-maskable input (NMI).
RESETn	131	I/O	HU	2XO	XFCR Reset.
TEST	58	I	C	--	Sets Test mode (battery powered).
Battery Power Control and Reset Logic					
XIN	59	I	OSC	--	Crystal oscillator input pin.
XOUT	60	O	--	OSC	Crystal oscillator output pin.
PWRDWNn	62	I	H	--	Indicates loss of prime power (results in NMI).
BATRSTn	61	I	H	--	Battery power reset input.
Scanner Interface					
START	101	O	--	2XS	Scanner shift gate control.
CLK1	100	O	--	2XS	Scanner clock.
CLK1n	99	O	--	2XS	Scanner clock-inverted.
CLK2	98	O	--	2XS	Scanner reset gate control (or clock for CIS scanner).
VIDCTL[1:0]	[97:96]	O	--	2XC	Control for video preprocessing circuits.
Printer Interface					
PCLK	29	O	--	3XC	Thermal Print Head (TPH) clock.
PDAT	30	O	--	2XP	Serial printing data (to TPH).
PLAT	31	O	--	3XP	TPH data latch.
STRB[3:0]	[33:36]	O	--	1XP	Strobe signals for the TPH.
STRBPOL	37	I	C	--	Sets strobe polarity, active high/low.

Table 5. XFCR-B Pin Assignments (Cont'd)

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description
Operator Panel Interface					
OPO[4:0]	[42:44][46:47]	O	--	2XL	Keyboard / LED strobe [4:0].
OPI[3:0]	[49:52]	I	HU	--	Keyboard return [3:0]. (Pullup, Hysteresis In.)
LEDCTL	55	O	--	4XC	Indicates outputs OPO[4:0] are for LEDs.
LCDCS	54	O	--	1XC	LCD chip select.
General Purpose I/O					
GPIO[7:0]/ VID[7:0]	[86:87][89:94]	I/O	H	2XC	Programmable: GPIO (8 lines) or video data bus.
GPIO[10:8]/ VDC[2:0]	[83:85]	I/O	H	2XC	Programmable: GPIO (3 lines) or video data control signals.
GPIO12/ CS2n/SCLK	80	I/O	H	2XC	Programmable: GPIO line, I/O chip select or SCLK (SART).
GPIO13/ CS3n/TXD	79	I/O	H	2XC	Programmable: GPIO line, I/O chip select or TXD (SART).
GPIO14/ CS4n/RXD	78	I/O	H	2XC	Programmable: GPIO line, I/O chip select or RXD (SART).
GPIO16/IRQ8	76	I/O	H	1XC	Programmable: GPIO line or active high interrupt.
GPIO17/ IRQ5n	75	I/O	H	1XC	Programmable: GPIO line or active low interrupt.
Miscellaneous					
SM[3:0] / GPO[7:4]	[103:106]	O	--	1XC	Programmable: scan motor control pins or GPO pins.
PM[3:0] / GPO[3:0]	[115:118]	O	--	1XC	Programmable: print motor control pins or GPO pins.
TONE	119	O	--	1XC	Tone output signal.
Power, Reference Voltages, Ground					
-Vref	66	I	–VR	--	Negative Reference Voltage for Video A/D.
+Vref	68	I	+VR	--	Positive Reference Voltage for Video A/D.
ADGA	69		VADG		A/D Analog Ground.
ADVA	70		VADV		A/D Analog Power.
ADGD	72		VADG		A/D Digital Ground.
ADVD	71		VADV		A/D Digital Power.
VIN	67	I	VA	--	Analog Video A/D input.
THADI	65	I	TA	--	Analog Thermal A/D input.
VSS(8)	134, 132, 95, 88, 53, 45 28, 21				Digital Ground.
VDD (7)	140, 123, 102, 81, 48, 41, 14				Digital Power.
VBAT	63				Battery Power.
No Connection					
NC	1, 2, 3, 4, 7, 32, 38, 39, 40, 56, 64, 73, 74, 77, 82, 107, 108, 109, 110, 111, 112, 113, 114				No connection.

Table 6. XFCR (Except -B) Pin Assignments

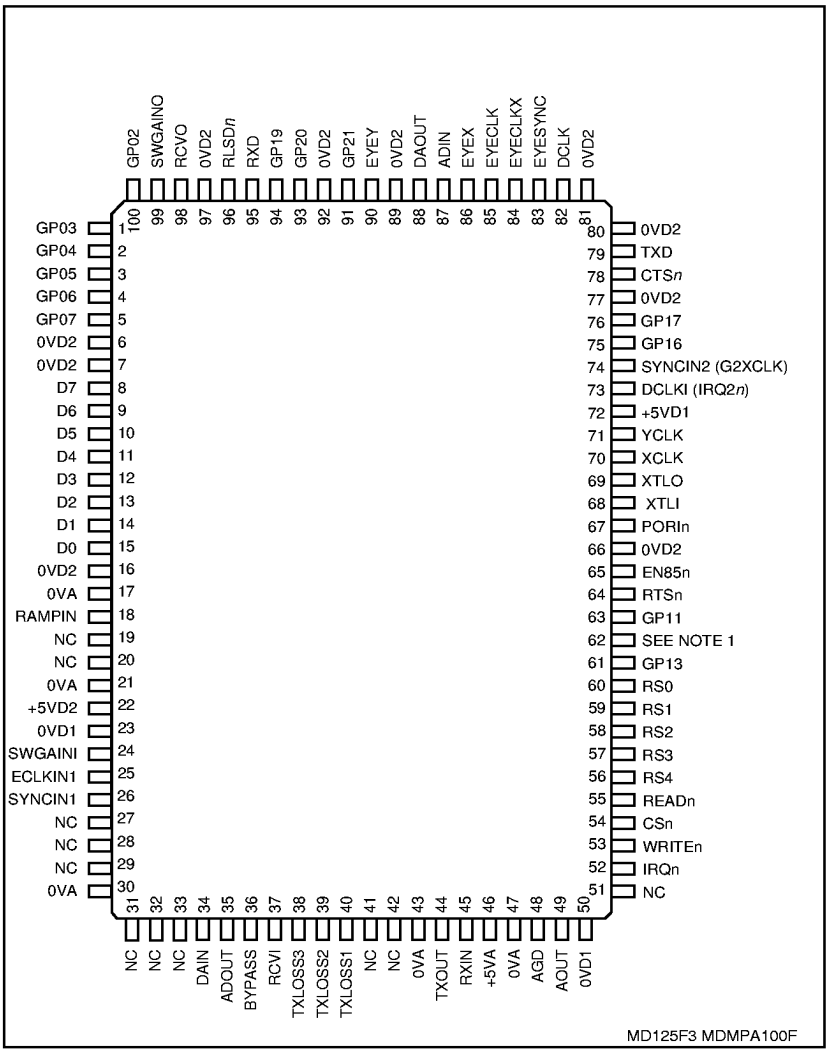
Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description (Note: Active low signals have an "n" pin name ending.)
CPU Control Interface					
MIRQn	135	I	HU	--	Modem interrupt, active low. (Hysteresis In, Internal Pullup.)
SYSCLK	133	I	H	--	System clock. (Hysteresis In.)
TSTCLK	130	O	--	1XC	Test clock.
Bus Control Interface					
A[23:0]	[1:6][8:13] [15:20][22:27]	O	T	1XT	Address bus (24-bit).
D[7:0]	[136:139] [141:144]	I/O	T	1XT	Data bus (8-bit).
RDn	128	O	--	1XTT	Read strobe.
WRn	127	O	--	1XTT	Write strobe.
ROMCSn	120	O	--	1XT	ROM chip select.
CS1n	122	O	--	1XT	I/O chip select.
CS0n	57	O	--	1XTT	SRAM chip select. (Battery powered.)
MCSn	121	O	--	1XC	Modem chip select.
SYNC	126	O	--	1XC	Indicates CPU op code fetch cycle (active high).
REGDMA	124	O	--	1XC	Indicates REGSEL cycle and DMA cycle.
WAITn	125	O	--	1XC	Indicates current TSTCLK cycle is a wait state or a halt state.
RASn	113	O	-	1XTT	DRAM row address select.
CAS[2:0]n	[110:112]	O	-	1XTT	DRAM column address select.
DWRn	109	O	-	1XTT	DRAM write.
Prime Power Reset Logic and Test					
DEBUGn	129	I	HU	--	External non-maskable input (NMI).
RESETn	131	I/O	HU	2XO	XFCR Reset.
TEST	58	I	C	--	Sets Test mode (battery powered).
Battery Power Control and Reset Logic					
XIN	59	I	OSC	--	Crystal oscillator input pin.
XOUT	60	O	--	OSC	Crystal oscillator output pin.
PWRDWNn	62	I	H	--	Indicates loss of prime power (results in NMI).
BATRSTn	61	I	H	--	Battery power reset input.
Scanner Interface					
START	101	O	--	2XS	Scanner shift gate control.
CLK1	100	O	--	2XS	Scanner clock.
CLK1n	99	O	--	2XS	Scanner clock-inverted.
CLK2	98	O	--	2XS	Scanner reset gate control (or clock for CIS scanner).
VIDCTL[1:0]	[97:96]	O	--	2XC	Control for video preprocessing circuits.
Printer Interface					
PCLK/DMAACK	29	O	--	3XC	Thermal Print Head (TPH) clock or external DMAACK.
PDAT	30	O	--	2XP	Serial printing data (to TPH).
PLAT	31	O	--	3XP	TPH data latch.
STRB[3:0]	[33:36]	O	--	1XP	Strobe signals for the TPH.
STRBPOL/ DMARQ	37	I	C	--	Sets strobe polarity, active high/low., or external DMAREQ.

Table 6. XFCR (Except -B) Pin Assignments (Cont'd)

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description
Operator Panel Interface					
OPO[7:0]	[38:40][42:44] [46:47]	O	--	2XL	Keyboard / LED strobe [7:0].
OPI[3:0]	[49:52]	I	HU	--	Keyboard return [3:0]. (Pullup, Hysteresis In.)
LEDCTL	55	O	--	4XC	Indicates outputs OPO[7:0] are for LEDs.
LCDCS	54	O	--	1XC	LCD chip select.
General Purpose I/O					
GPIO[7:0]/ VID[7:0]	[86:87][89:94]	I/O	H	2XC	Programmable: GPIO (8 lines) or video data bus.
GPIO[10:8]/ VDC[2:0]	[83:85]	I/O	H	2XC	Programmable: GPIO (3 lines) or video data control signals.
GPIO11/BE/ SERINP	82	I/O	H	1XC	Programmable: GPIO line, Bus Enable, serial data input (Autobaud).
GPIO12/ CS2n/SCLK	80	I/O	H	2XC	Programmable: GPIO line, I/O chip select or SCLK (SART).
GPIO13/ CS3n/TXD	79	I/O	H	2XC	Programmable: GPIO line, I/O chip select or TXD (SART).
GPIO14/ CS4n/RXD	78	I/O	H	2XC	Programmable: GPIO line, I/O chip select or RXD (SART).
GPIO15/CS5n	77	I/O	H	2XC	Programmable: GPIO line or I/O chip select.
GPIO16/IRQ8	76	I/O	H	1XC	Programmable: GPIO line or active high interrupt.
GPIO17/ IRQ5n	75	I/O	H	1XC	Programmable: GPIO line or active low interrupt.
GPIO18/IRQ10n	74	I/O	H	1XC	Programmable: GPIO line or active low interrupt.
GPIO[19]/RDY/ SEROUT	73	I/O	H	1XC	Programmable: GPIO line, Ready or Serial out (Autobaud).
Miscellaneous					
SM[3:0] / GPO[7:4]	[103:106]	O	--	1XC	Programmable: scan motor control pins or GPO pins.
PM[3:0] / GPO[3:0]	[115:118]	O	--	1XC	Programmable: print motor control pins or GPO pins.
TONE	119	O	--	1XC	Tone output signal.
Power, Reference Voltages, Ground					
-Vref	66	I	–VR	--	Negative Reference Voltage for Video A/D.
+Vref	68	I	+VR	--	Positive Reference Voltage for Video A/D.
ADGA	69		VADG		A/D Analog Ground.
ADVA	70		VADV		A/D Analog Power.
ADGD	72		VADG		A/D Digital Ground.
ADVD	71		VADV		A/D Digital Power.
VIN	67	I	VA	--	Analog Video A/D input.
THADI	65	I	TA	--	Analog Thermal A/D input.
VSS(12)	134, 132, 108, 95, 88, 64, 56, 53, 45 28, 21, 7				Digital Ground.
VDD (8)	140, 123, 102, 81, 48, 41, 32, 14				Digital Power.
VDRAM	114				Battery power for DRAM refresh.
VBAT	63				Battery Power for RTC and SRAM.
No Connection					
NC	107,				No connection.

Table 7. XFCR Input and Output Signal Characteristics

Input Signal Characteristics						
Input Type	**Description**	**VIL (V max)**	**VIH (V min)**	**Hysteresis (V min)**	**Pullup Resistance (K ohm)**	
C	CMOS Input	0.3*VDD	0.7*VDD	--	--	
H	Hysteresis	0.3*VDD	0.6*VDD	1.0	--	
HU	Hysteresis/Pullup	0.3*VDD	0.6*VDD	1.0	35–150	
T	TTL Input	0.8	2.0	--	--	
TU	TTL/Pullup	0.8	2.0	--	35-150	
OSC	CMOS Input	0.3*VDD	0.7*VDD	--	--	
Absolute Input Range = 0.5 to VDD+0.5						
Input Type	**Description**	**Operating (V min)**	**Operating (V max)**	**Abs. Max. (V min)**	**Abs. Max. (V max)**	
TA	Thermal Head Analog Input	0.2*VDD	0.8*VDD	–0.5	VDD+0.5	
VA	Video Analog In	-VR	+VR	-0.5	VADV + 0.5	
+VR	Video A/D +Vref	0.8	3.3	-0.5	VADV + 0.5	
-VR	Video A/D -Vref	-0.2	2.0	-0.5	VADV + 0.5	
VADV	Video A/D Power	VDD-0.1	VDD + 0.1	-0.5	7.0	
VADG	Video A/D GND	-0.1	0.1	-0.5	0.5	
VDD	Digital Power	4.5	5.25	–0.5	7.0	
GND	Digital Ground	0	0	0	0	
VDRAM	Battery Power for DRAM	2.25	5.25	–0.5	7.0	
VBAT	Battery Power for RTC/SRAM	2.25	5.25	–0.5	7.0	
Output Signal Characteristics						
Output Type	**Description**	**VOL (V max)**	**IOL (mA max)**	**VOH (V min)**	**IOH (mA max)**	**CL (pF max)**
1XC	CMOS Output (1X)	0.4	1.6	VDD–1.5	1.6	50
1XP, 2XP	High Capacitance Driver	0.4	1.6	VDD–1.5	1.6	200
2XC	CMOS Output (2X)	0.4	3.5	VDD–1.5	3.5	50
1XT	TTL Output (1X)	0.4	1.6	2.4	1.6	50
2XS	CMOS Output (2X)	0.4	3.5	VDD–1.5 1.5	3.5 15	50 50
2XL	LED Driver	0.7	10	VDD–1.5	3.5	100
2XO	CMOS Output, Open Drain	0.4	3.5	N/A	N/A	50
3XC	CMOS Output (3X)	0.4	6	VDD–1.5	6	50
3XP	High Capacitance Driver (3X)	0.4	6	VDD–1.5	6	700
4XC	CMOS Output (4X)	0.4	12	VDD–1.0	12	50
1XTT	1X Tristate TTL Output	0.4	1.6	2.4	1.6	50



Notes:
1. For R96DFXL, pin 62 is connected to +5VD1 or leave, open (nc);
   For R144EFXL, pin 62 is connected to +5VD1.
2. Names in parentheses apply to R144EFXL only.

Figure 4. R96DFXL and R144EFXL Facsimile Modem Pin Assignments

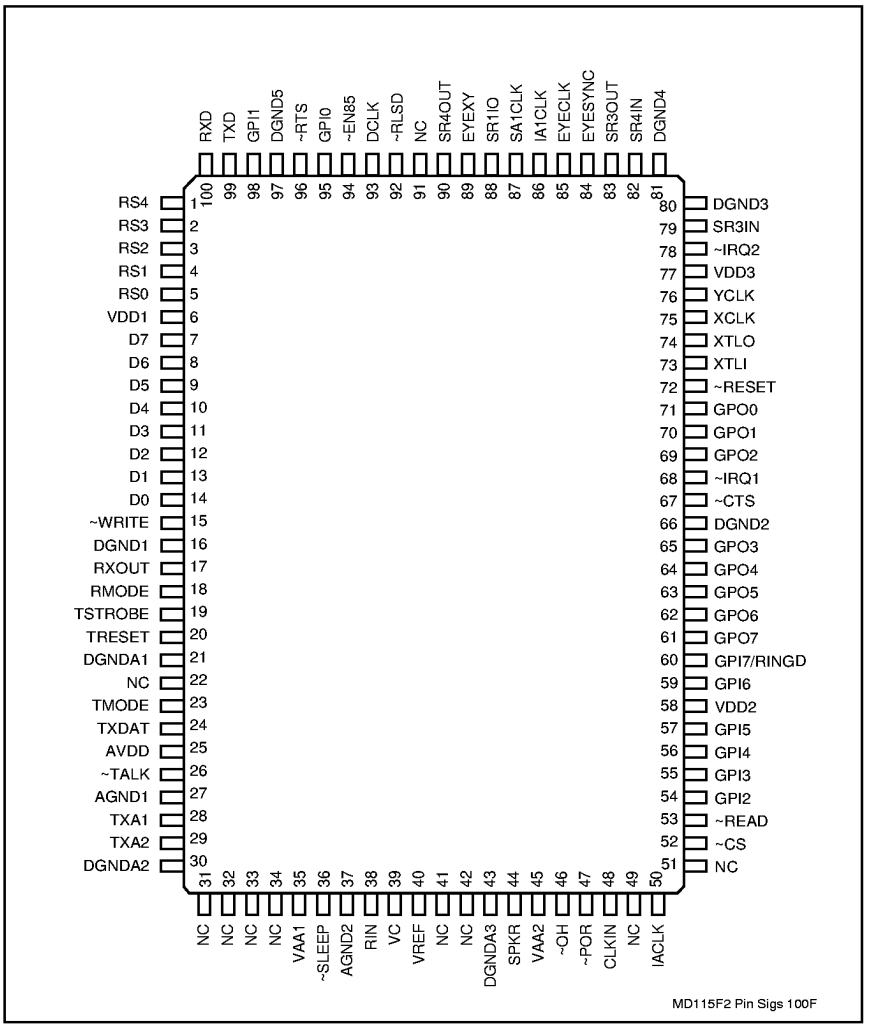


Figure 5. RFX96V24(-S23) and RFX144V24(-S23) Facsimile Modem Pin Assignments

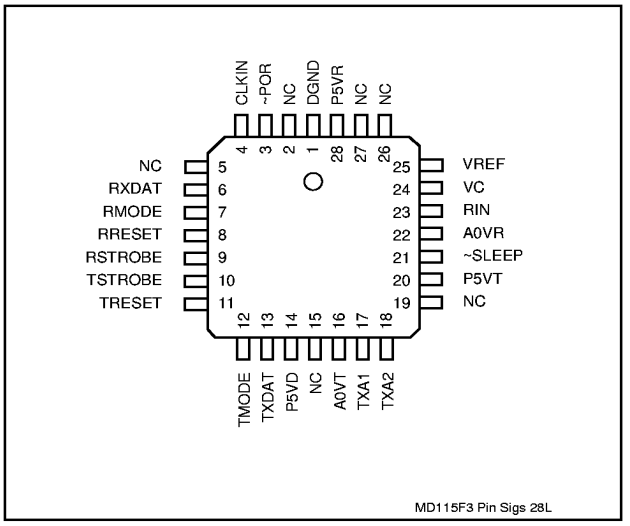


Figure 6. 28-Pin XIA Pin Signals

Table 8. R96DFXL and R144EFXL Modem Pin Assignments

Pin No.	Signal Name	I/O Type	Pin No.	Signal Name	I/O Type
1	GP03	IA/OB	51	NC	
2	GP04	IA/OB	52	IRQn, (IRQ1n)	OC (Note 4)
3	GP05	IA/OB	53	WRITEn, R/Wn	IA
4	GP06	IA/OB	54	CSn	IA
5	GP07	IA/OB	55	READn-f2	IA
6	0VD2	GND	56	RS4	IA
7	0VD2	GND	57	RS3	IA
8	D7	IA/OB	58	RS2	IA
9	D6	IA/OB	59	RS1	IA
10	D5	IA/OB	60	RS0	IA
11	D4	IA/OB	61	GP13	IA/OB
12	D3	IA/OB	62	NC (+5VD1)	(Note 4)
13	D2	IA/OB	63	GP11	IA/OB
14	D1	IA/OB	64	RTSn	IA
15	D0	IA/OB	65	EN85n	R
16	0VD2	GND	66	0VD2	GND
17	0VA	GND	67	PORIn	ID
18	RAMPIN	R	68	XTLI	R
19	NC		69	XTLO	R
20	NC		70	XCLK	OD
21	0VA	GND	71	YCLK	OD
22	+5VD2	PWR	72	+5VD1	PWR
23	0VD1	GND	73	DCLKI, (IRQ2n)	R
24	SWGAINI	R	74	SYNCIN2 (G2xCLK)	R (Note 4)
25	ECLKIN1	R	75	GP16	IA/OB
26	SYNCIN1	R	76	GP17	IA/OB
27	NC		77	0VD2	GND
28	NC		78	CTSn	OA
29	NC		79	TXD	IA
30	0VA	GND	80	0VD2	GND
31	NC		81	0VD2	GND
32	NC		82	DCLK	OA
33	NC		83	EYESYNC	OA
34	DAIN	R	84	EYECLKX	OA
35	ADOUT	R	85	EYECLK	OA
36	BYPASS	IC	86	EYEX	OA
37	RCVI	R	87	ADIN	R
38	TXLOSS3	IC	88	DAOUT	R
39	TXLOSS2	IC	89	0VD2	GND
40	TXLOSS1	IC	90	EYEY	OA
41	NC		91	GP21	IA/OB
42	NC		92	0VD2	GND
43	0VA	GND	93	GP20	IA/OB
44	TXOUT	AA	94	GP19	IA/OB
45	RXIN	AB	95	RXD	OA
46	+5VA	PWR	96	RLSDn	OA
47	0VA	GND	97	0VD2	GND
48	AGD	R	98	RCVO	R
49	AOUT	R	99	SWGAINO	R
50	0VD1	GND	100	GP02	IA/OB

Notes:
1. NC = No connection; leave pin open.
2. I/O Type (See Table 11 and Table 12).
3. R = Required modem interconnection; no connection to host equipment.
4. The name in parentheses applies to the R144EFXL only.

Table 9. RFX(-S) Modem Pin Assignments

Pin No.	Signal Name	I/O Type	Pin No.	Signal Name	I/O Type
1	RS4	IA	51	NC	
2	RS3	IA	52	CSn	IA
3	RS2	IA	53	READn	IA
4	RS1	IA	54	GPI2	IA
5	RS0	IA	55	GPI3	IA
6	VDD1	PWR	56	GPI4	IA
7	D7	IA/OB	57	GPI5	IA
8	D6	IA/OB	58	VDD2	PWR
9	D5	IA/OB	59	GPI6	IA
10	D4	IA/OB	60	GPI7/RINGD	IA
11	D3	IA/OB	61	GPO7	OB
12	D2	IA/OB	62	GPO6	OB
13	D1	IA/OB	63	GPO5	OB
14	D0	IA/OB	64	GPO4	OB
15	WRITEn	IA	65	GPO3	OB
16	DGND1	GND	66	DGND2	GND
17	RXOUT	MI	67	CTSn	OA
18	RMODE	MI	68	IRQ1n	OC
19	TSTROBE	MI	69	GPO2	OB
20	TRESET	MI	70	GPO1	OB
21	DGNDA1	GND	71	GPO0	OB
22	NC		72	RESETn	OA
23	TMODE	MI	73	XTLI	I
24	TXDAT	MI	74	XTLO	O
25	AVDD	PWR	75	XCLK	OD
26	TALKn	OD	76	YCLK	OD
27	AGND1	GND	77	VDD3	PWR
28	TXA1	O(DD)	78	IRQ2n	OC
29	TXA2	O(DD)	79	SR3IN	MI
30	DGNDA2	GND	80	DGND3	GND
31	NC		81	DGND4	GND
32	NC		82	SR4IN	MI
33	NC		83	SR3OUT	MI
34	NC		84	EYESYNC	OA
35	VAA1	PWR	85	EYECLK	OA
36	SLEEPn	MI	86	IA1CLK	MI
37	AGND2	GND	87	SA1CLK	MI
38	RIN	I(DA)	88	SR1IO	MI
39	VC	MI	89	EYEXY	OA
40	VREF	MI	90	SR4OUT	MI
41	NC		91	NC	
42	NC		92	RLSDn	OA
43	DGNDA3	GND	93	DCLK	OA
44	SPKR	O(DF)	94	EN85n	IA
45	VAA2	PWR	95	GPI0	IA
46	OHn	OD	96	RTSn	IA
47	PORn	MI	97	DGND5	GND
48	CLKIN	MI	98	GPI1	IA
49	NC		99	TXD	IA
50	IACLK	MI	100	RXD	OA

Notes:
1. NC = No connection; leave pin open.
2. I/O Type (See Table 11 and Table 12).

Table 10. XIA Pin Signals - 28-Pin PLCC

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	DGND	GND	AGND	15	NC		NC
2	NC		NC	16	A0VT	GND	AGND
3	~POR	MI	MDP: ~POR (47)	17	SPKHI (TXA1)	O(DD)	Analog Switch/Line Interface (SPKHI)
4	CLKIN	MI	MDP: IACLK (50)	18	SPKLO (TXA2)	O(DD)	Analog Switch/Line Interface (SPKLO)
5	NC		NC	19	NC		NC
6	RXDAT	MI	MDP: SR4IN (82)	20	P5VT	PWR	To P5VD (14) & P5VR (28) & to VCC through a power decoupling filter
7	RMODE	MI	MDP: RMODE (18); XIA: TMODE (12)	21	~SLEEP	MI	MDP: ~SLEEP (36)
8	RRESET		NC	22	A0VR	GND	AGND
9	RSTROBE		NC	23	RIN (MICIN)	I(DA)	Analog Switch/Line Interface (MICOUT)
10	TSTROBE		NC	24	VC	MI	AGND through capacitors
11	TRESET		NC	25	VREF	MI	VC through capacitors
12	TMODE	MI	XIA: RMODE (7)	26	NC		NC
13	TXDAT	MI	MDP: SR3OUT (83)	27	NC		NC
14	P5VD	PWR	To P5VT (20) & P5VR (28) & to VCC through a power decoupling filter	28	P5VR	PWR	To P5VD (14) & P5VT (20) & to VCC through a power decoupling filter

Notes:
1. NC = No connection; leave pin open.
2. NC = No external connection allowed.
3. MI = Modem interconnect.

Table 11. Modem Digital Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA and IB		2.0	–	VCC		
Type IC and ID		0.8 VCC	–	VCC		
Input High Current	I_{IH}				µA	VCC = 5.25 V, VIN = 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}				VDC	
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (VCC)		
Input Low Current	I_{IL}				µA	VCC = 5.25 V
Type IB and IC		–	–	–400		
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	VIN = 0 to +5V, VCC =5.25V
Types IA and ID						
Output High Voltage	V_{OH}		–	–	VDC	
Type OA and OB		3.5	–	VCC		ILOAD = – 100 µA
Type OD						ILOAD = – 40 µA
Output Low Voltage	V_{OL}				VDC	
Type OA and OC		–	–	0.4		ILOAD = 1.6 mA
Type OB		–	–	0.4		ILOAD = 0.8 mA
Type OD		–	–	0.75		ILOAD = 0.4 mA
Output Leakage Current	I_{LO}			±10	µADC	VIN = 0.4 to VCC-1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID			–	10		
Type IB			–	20		
Capacitive Drive	C_D				pF	
Types OA, OB, OC			–	10		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Clock driver

Table 12. Modem Analog Electrical Characteristics

Name	Type	Characteristic	Value
RFX96V24-S23 (-S) and RFX144V12 (-S)			
RIN	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 70K ½ 1.7 VP-P +2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 ½ 0.01 µF 10 ½ 1.2 VP-P @9600 Hz sample rate 2.7 VP-P @8000 Hz sample rate +2.5 VDC ± 200 mV
SPKR	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 ½ 0.01 µF 10 ½ 2.0 VP-P +2.5 VDC ± 20 mV
R96DFXL and R144EFXL			
TXOUT	AA	Maximum Output Minimum load	2.5 ± 1.015 volts 10K ½
RXIN	AB	Input impedance	1M ½
XIA (-S only)			
RIN	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 70K ½ 1.7 VP-P +2.5 VDC
TXA1 (SPKHI), TXA2 (SPKLO)	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 ½ 0.01 µF 10 ½ 2.7 VP-P +2.5 VDC ± 200 mV
* Reference voltage provided internal to the device.			

SOFTWARE INTERFACE

Memory Map and Chip Select

Memory Maps

XFCR-B

Although the MC24 processor can directly access 16M bytes, the XFCR-B can access only 2MB of this memory by means of the 20-bit external address bus (A0-A19), and the chip selects. Figure 7 shows the XFCR-B memory map. Chip select allocation, is shown in Table 12.

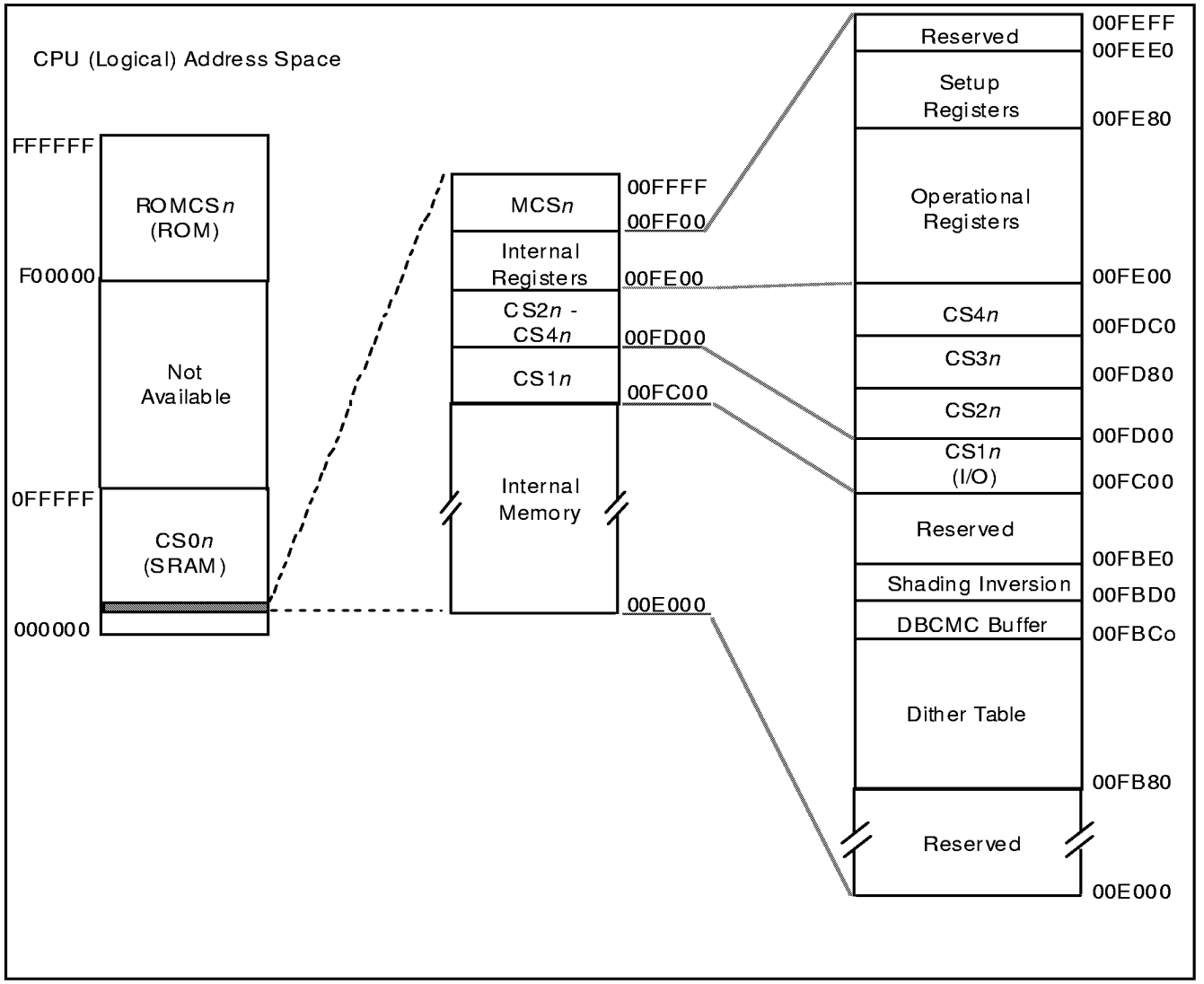


Figure 7. XFCR-B Memory Map

XFCR - All Others

The XFCR types for all other XFERs have the full 24-bit address bus available externally, and therefor can address 16 Mbytes of memory. The XFCR memory map is shown in Figure 8.

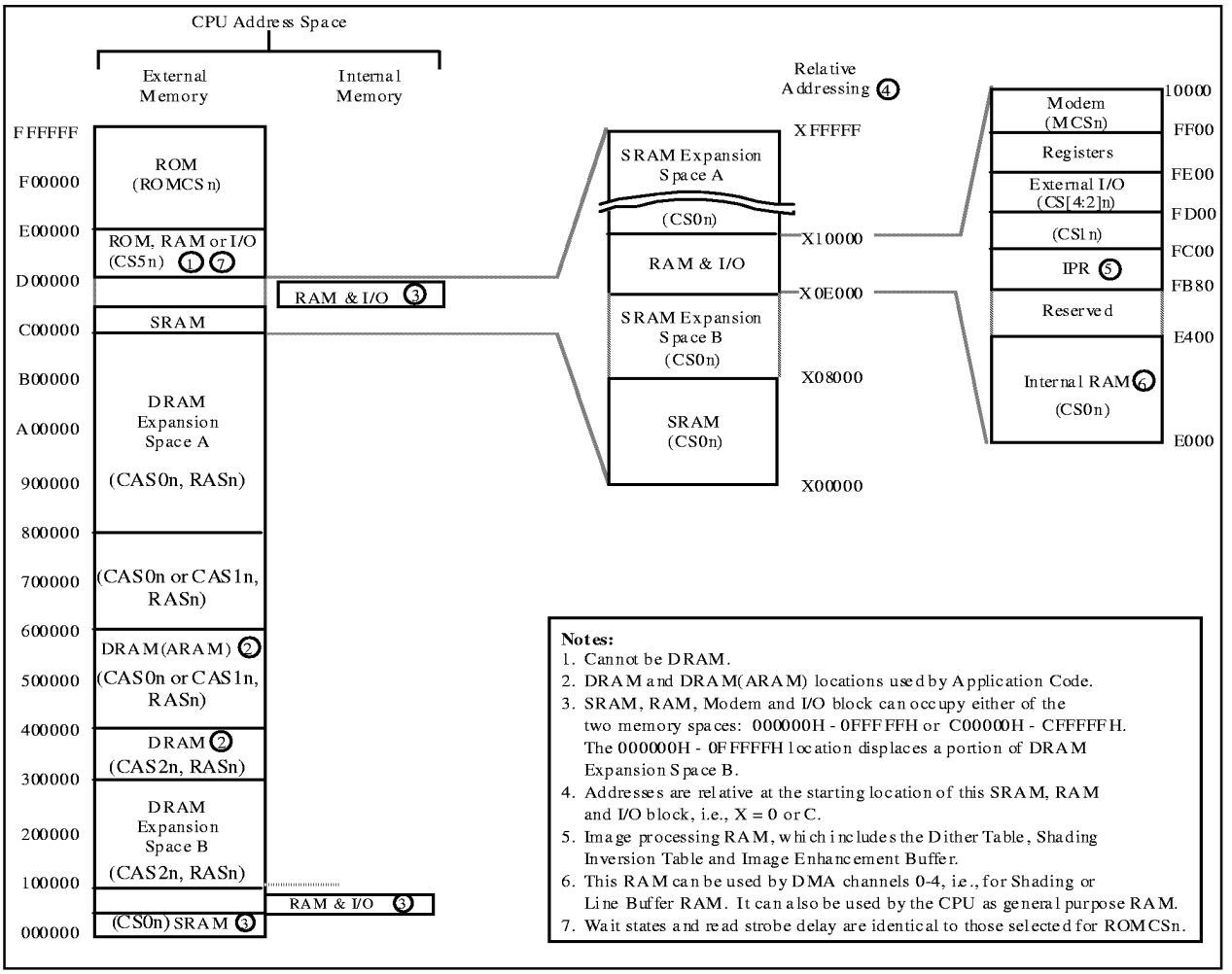


Figure 8. XFCR (Except XFCR-B) Memory Map

External Memory Space

XFCR-B

The external memory space (up to 2048k bytes) consists of ROM, SRAM, modem and variable use spaces with assigned chip selects. Most external chip selects have programmable wait states, and read and write strobe timing. The SRAM chip select has programmable size and can be battery backed up.

Table 13. XFCR-B Memory Allocation

Item (See notes below)	CPU (Logical) Address Range	External (Physical) Address Range
ROMCSn: ROM	F00000 - FFFFFF	00000 - FFFFF
CS0n: SRAM or general	000000 - 0FFFFF	00000 - FFFFF
MCSn: Modem	00FF00 - 00FFFF	0FF00 - 0FFFF
CS1: I/O	00FC00 - 00FCFF	0FC00 - 0FCFF
CS2n - CS4n: optional, general	00FD00 - 00FDFF	0FD00 - 0FDFF

Notes:

1. ROMCSn is a read/write, fixed location and size, chip select. CS0n is intended primarily for external SRAM, but may be used for other purposes, and can be programmed to one of four sizes (from 8k bytes to 1M bytes). MCS is for the FAXENGINE Modem Device, and CS1n selects a variable use 256-byte memory space. Optional chip selects CS2n through CS4n are multiplexed with the GPIO12-GPIO14 signals. CS3n is generated only on write accesses, and CS4n is generated only on read accesses.
2. The ROMCSn and CS0n occupy the same (24-bit) physical address range, but are selected by different (24-bit) logical addresses via the appropriate chip selects.
3. Portions of the CS0n memory space are displaced by other chip selects (e.g., internal memory, modem, and CS1n - CS4n).

XFCR - All Others

The XFCR provides pre-defined chip selects and control signals to define various areas of the memory as ROM, SRAM, DRAM, internal I/O, external I/O. Table 14 and its notes indicate the possible memory configurations.

Table 14. XFCR (Except -B) Memory Allocation

Item (See notes below)	CPU Address Range	
ROMCSn: ROM	E00000 - FFFFFF	
CS5n: ROM or I/O	D00000 - DFFFFF	
CS0n: SRAM or general	C00000 - CFFFFF or 000000 - 0FFFFF	
MCSn: Modem	00FF00 - 00FFFF	Relative addresses, see XFER memory map, Figure 8.
CS1: External I/O	00FC00 - 00FCFF	
CS2n - CS4n: External I/O	00FD00 - 00FDFF	
CAS0, RASn: DRAM Expansion A	800000 - BFFFFF	
CAS0n or CAS1n, RASn: DRAM Expansion A	400000 - 7FFFFF	
CAS2n, RASn: DRAM	300000 - 3FFFFF	
CAS2n, RASn: DRAM Expansion B	100000 - 2FFFFF	

Notes:

1. ROMCSn is a read/write, fixed location and size (2 Mbytes) chip select. For a third Mbyte of ROM, CS5n is used. CS0n is intended primarily for external SRAM, but may be used for other purposes, and can be programmed to one of four sizes (from 8k bytes to 1M bytes). MCS is for the FAXENGINE Modem Device, and CS1n selects a variable use 256-byte memory space. Optional chip selects CS2n through CS4n are multiplexed with the GPIO12-GPIO14 signals. CS3n is generated only on write accesses, and CS4n is generated only on read accesses.
2. Portions of the CS0n memory space are displaced by other chip selects (e.g., internal memory, modem, and CS1n - CS4n).

Supplied Firmware

FAXENGINE firmware supplied with the XFER consists of Core Code and Application Code. The Application Code, in conjunction with Core Code and XFCR when connected to scanner and printer peripherals, provides a complete working facsimile machine.

The Core Code (subdivided as Macro and Primitive functions) is supplied as object code, whereas the Application Code (to complete a fax machine) is supplied as assembly-level source code.

Core Code

The Core Code includes proprietary primitives and macros in object code form located in ROM at the top of the FAXENGINE processor address space (see Figure 7). These Core Code primitives and macros provide the following functions:

- Modem control
- T.30 framing and control
- T.4 MH Compression & Decompression (XFCR-B)
- T.4 MH, MR and MMR control for XFCR compression/decompression hardware. Line times of 5 ms per line are supported.
- Send and receive a page
- Real-time multitasking executive for scheduling high priority (interrupt-driven) tasks and servicing low priority (background) tasks

The Core Code subroutines are organized with a modular layered structure which allows for the replacement of any of these subroutines by original equipment manufacturer (OEM)-written custom subroutines.

Core Code routines are organized in a library and the Core Code linkage routine optimizes ROM space code by preventing code duplication when Core Code routines are unused or replaced by Developer routines.

Application Code

The Application Code provides the Developer with the source assembly code for a complete facsimile machine application. The Application Code links to the Core Code functions to control the FAXENGINE peripheral functions. The Application Code performs all the functions that can be customized to give enough flexibility to the Developer, such as:

- Scanner and printer control
- Operator panel control (Keypad, LED, LCD, Beeper)
- Scan document handling (e.g., pull-in and eject)
- Printer paper handling (e.g., eject and cut)
- Copy page
- Setup controls for the facsimile machine (e.g., date and time, header, transmit level, etc.)
- Call progress controls with parameter tables to allow modification for PTT requirements in different countries
- T.30 control by generating frame content and sequence used during a T.30 negotiation
- Fax/Voice discrimination with external answering machine interface

Conditional Assembly

Other supported functions, which are included in the final object code only when the appropriate conditional assembly switches are enabled, are:

- Error Correction Mode (ECM)
- Page Memory support that includes broadcast/delayed capabilities and receiving to memory
- Resolution conversion
  - Multi-level and bi-level B4 to A4 reduction
- Digital answering machine support

The supplied firmware also allows conditional inclusion of the following items, some of which automatically add other options, as noted:

- XFCR type (T.4 implementation for XFER-B vs. others; MMR and ACD option.)
- Modem type
- ECM RAM (and size of Comm Buffer)
- Speakerphone
- UART interface for debug
- Scan image processing enabled/disabled
- Line ORing enabled/disabled
- Call progress country
- Language for operator interface
- Fax mechanism (Specifies parameter ranges for scanning and printing timing, scanner and printer width, shading correction and edge enhancement threshold value.)

FEES-X OPERATOR PANEL AND USER INTERFACE

The FEES-X operator panel consists of a 12-key TAM control keypad, a 20-key dialing keypad, a 20-character by 2-line liquid crystal display, eight indicator LEDs, a beeper, and a speaker.

FEES-X Initialization

When the FEES-X power is applied, or the RESET switch is pressed, all the LEDs turn on for 3 seconds, the beeper sounds, and a sign-on message is displayed on the LCD. When initialization is complete, the FEES-X will enter idle mode and display the clock on the second line of the LCD.

Program Operation

Several operational parameters can be set by the user. These parameters are separated into the Fax Menu, Phone Menu, System Menu, and Service Menu.

FAX Menu

The Fax menu includes:

- Enabling Receive-By-Polling
- Programming a Delayed Broadcast
- Programming Delayed Receive-By-Polling
- Storing a Transmit-By-Polling Document
- Printing And Deleting Documents From Page Memory
- Setting the Local ID
- Setting the Text Header
- Setting the Fax/Voice Silence Time
- Setting the Fax/Voice Timeout

Voice Menu

The Voice menu includes:

- Record OGM
- Play OGM
- Fax/Voice Silence
- TAM Toll Saver
- Announce Only
- Remote Access Enable
- Message Time Limit
- Security Code
- Phone Menu

The Phone menu includes:

- Setting Speed Dial Numbers
- Setting the Number of Rings to Answer On
- Setting the Dial Mode
- Enabling Blind Dialing

System Menu

The System menu includes:

- Setting the Clock
- Setting the Speaker Control
- Setting the Darkness Level
- Printing User Settings
- Resetting To Factory Defaults

Service Menu

The Service Menu includes:

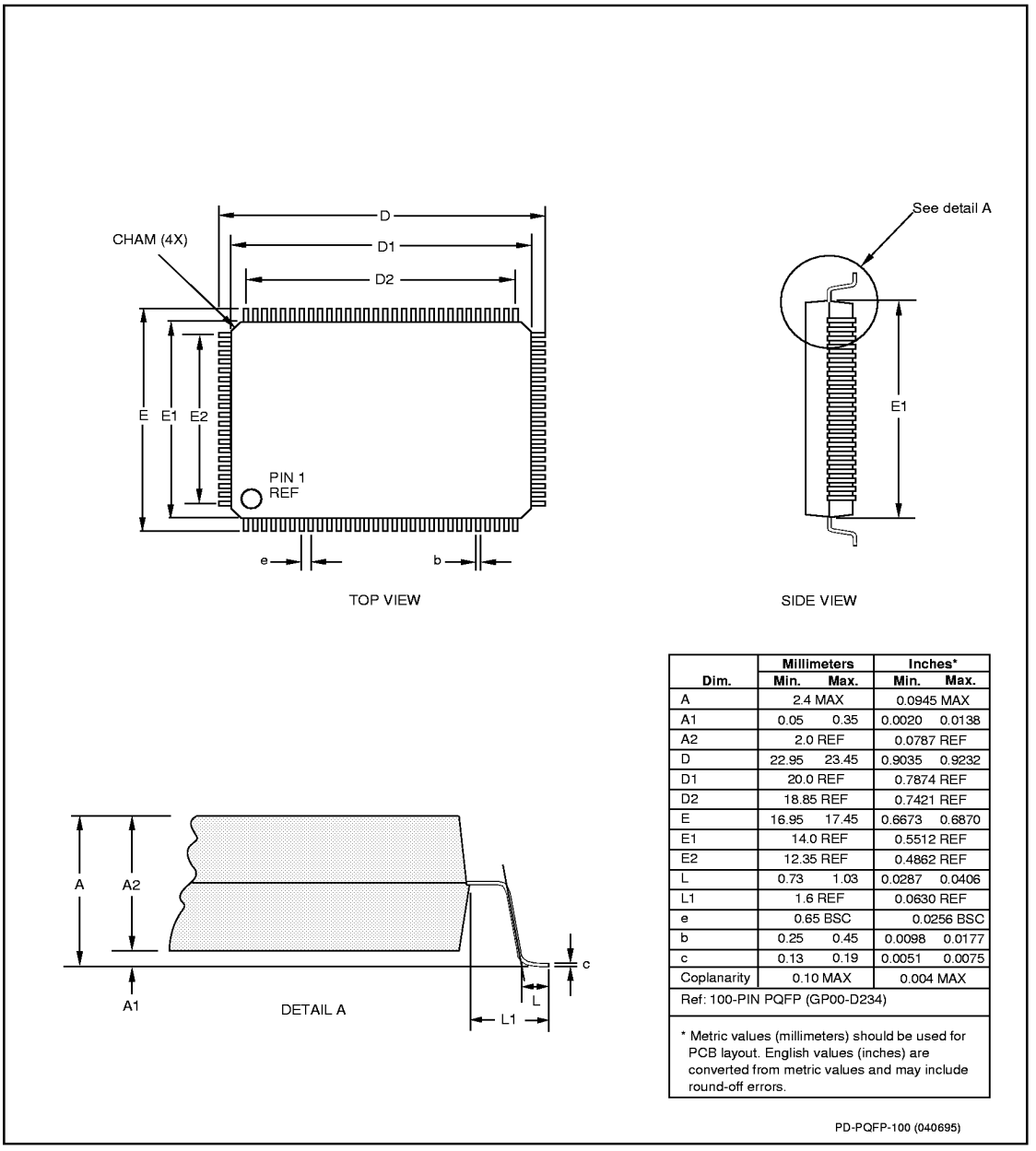
- Setting FAX Options
- Setting The Starting Speed
- Setting the Transmitter Attenuation
- Setting the Fax Equalizer
- Reference Voltage Test

Fax Operation

The Operation menu includes:

- Setting Auto-Answer
- Setting Image Resolution and Halftone
- Copying a Document
- Transmitting a Document Using Manual Dialing
- Transmitting a Document Using Automatic Dialing
- Transmitting a Document by Polling
- Receiving a Document Manually
- Receiving a Document Automatically
- Receiving a Document to Page Memory
- Receiving by Polling
- Initiating a Voice Request
- Responding to a Voice Request

PACKAGE DIMENSIONS

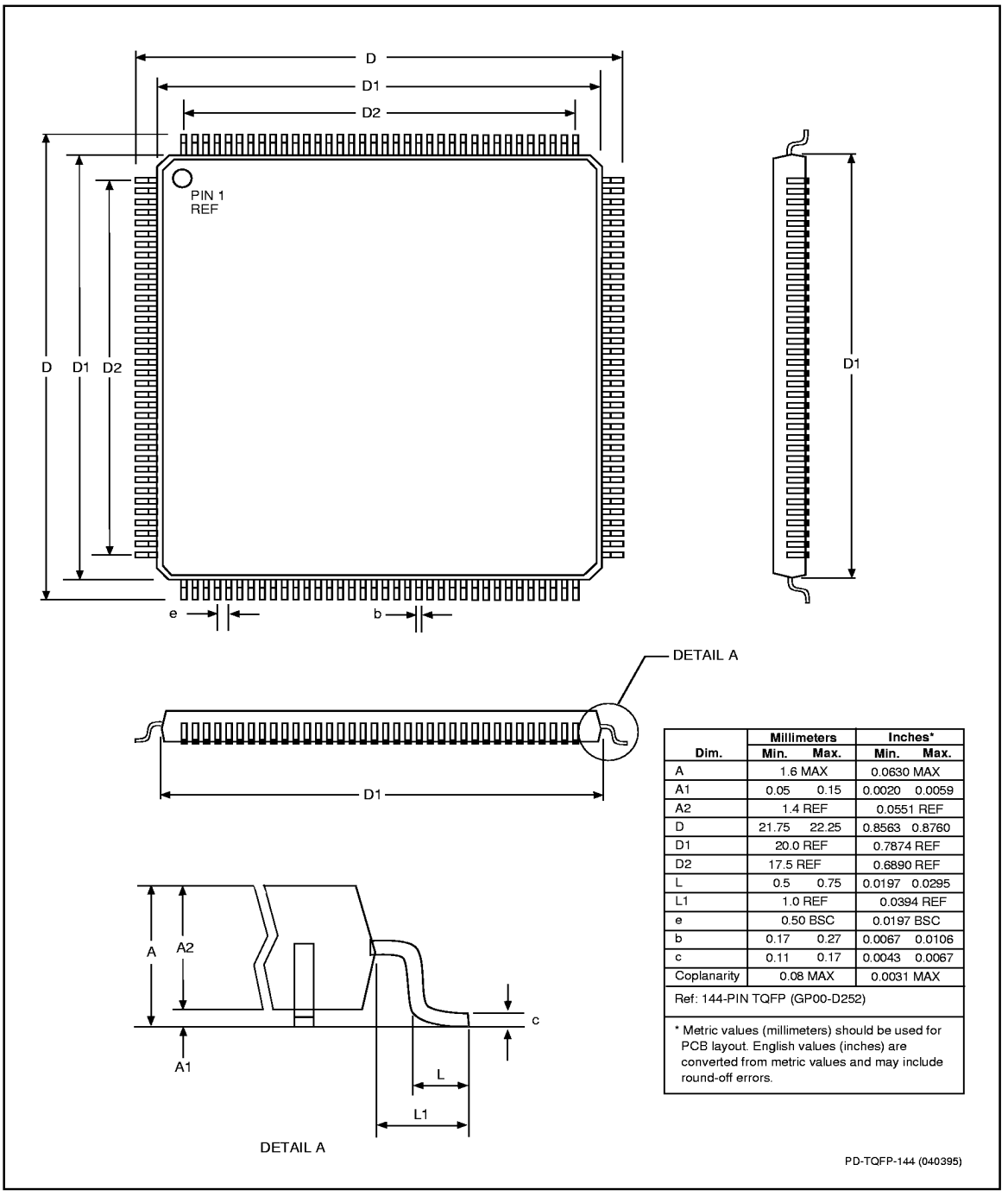


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		2.4 MAX		0.0945 MAX
A1	0.05	0.35	0.0020	0.0138
A2		2.0 REF		0.0787 REF
D	22.95	23.45	0.9035	0.9232
D1		20.0 REF		0.7874 REF
D2		18.85 REF		0.7421 REF
E	16.95	17.45	0.6673	0.6870
E1		14.0 REF		0.5512 REF
E2		12.35 REF		0.4862 REF
L	0.73	1.03	0.0287	0.0406
L1		1.6 REF		0.0630 REF
e		0.65 BSC		0.0256 BSC
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX
Ref: 100-PIN PQFP (GP00-D234)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-PQFP-100 (040695)

Figure 9. 100-Pin PQFP Dimensions

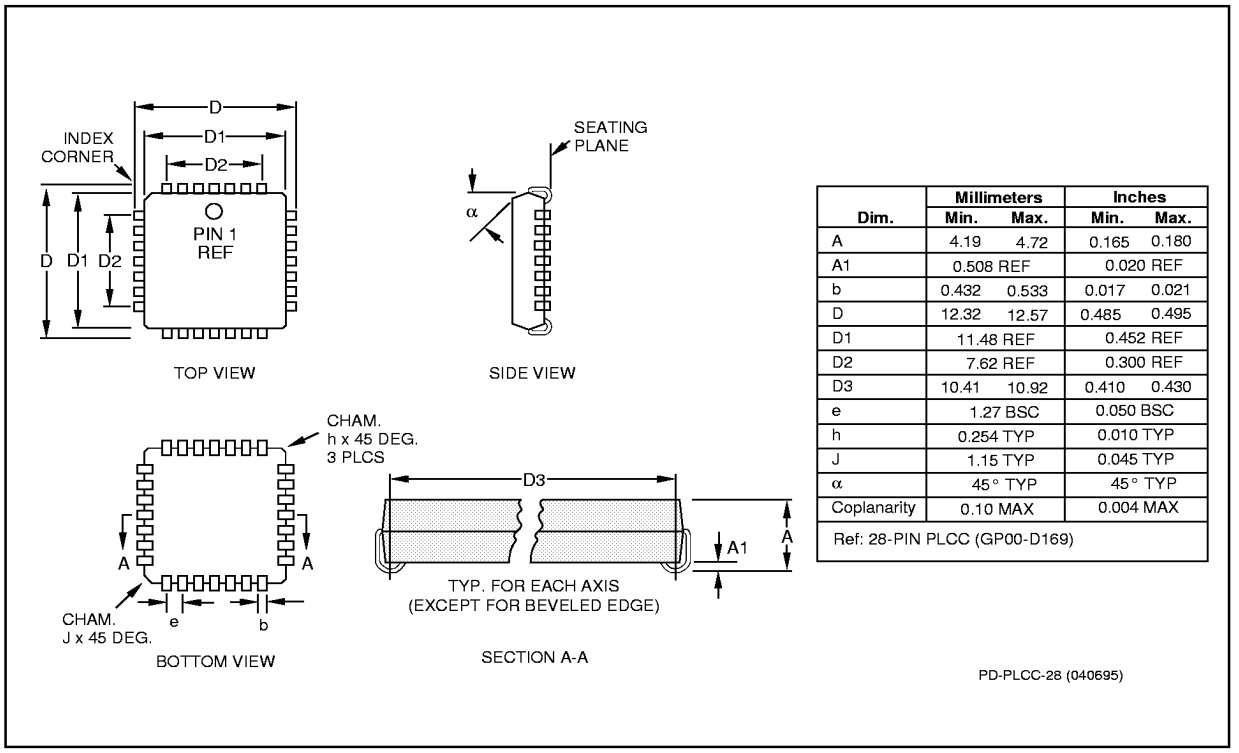


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		17.5 REF		0.6890 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 10. 144-Pin TQFP Dimensions



Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.19	4.72	0.165	0.180
A1	0.508 REF		0.020 REF	
b	0.432	0.533	0.017	0.021
D	12.32	12.57	0.485	0.495
D1	11.48 REF		0.452 REF	
D2	7.62 REF		0.300 REF	
D3	10.41	10.92	0.410	0.430
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
Coplanarity	0.10 MAX		0.004 MAX	
Ref: 28-PIN PLCC (GP00-D169)				

Figure 11. 28-Pin PLCC Dimensions