INTERNATIONAL CMOS TECHNOLOGY, INC.

T-46-19-07

PEEL™18CV8
CMOS Programmable Electrically Erasable Logic Device

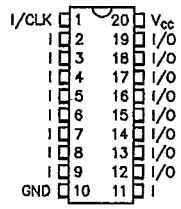
Features

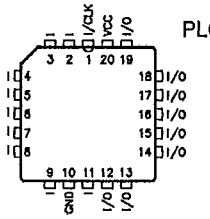
- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 20mA standby + 0.7mA/MHz max
- **High Performance**
  - t_{PD} = 25ns max, fmax=33.3MHz
- **EE Instant Reprogrammability**
  - 100% factory tested
  - Cost-effective windowless package
  - Erases and programs in seconds
  - Adds convenience, reduces field retrofit and development costs
- **Foolproof Design Security**
  - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  - 74 product term x 36 input array
  - Up to 18 inputs and 8 I/O pins
  - Independent configurable I/O macro cells
  - Synchronous preset, asynchronous clear
  - Independent output enables
- **Application Versatility**
  - Replaces SSI/MSI logic
  - Emulates bipolar PAL* devices, GAL* devices, and EPLDs
  - Simplifies inventory control
  - Allows new design possibilities
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PEEL Development System and Software

General Description

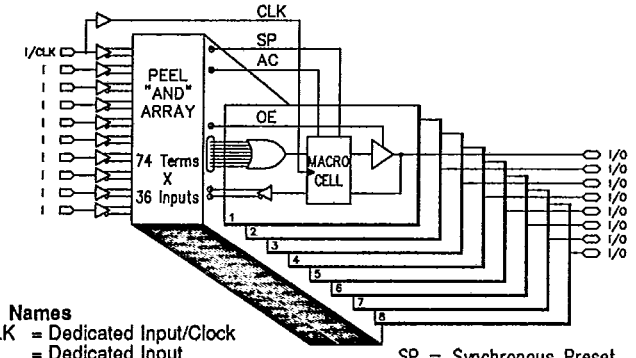
The ICT PEEL18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. ICT also offers a free design software package and a low-cost development system.

Pin Configuration (Figure 1)





Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

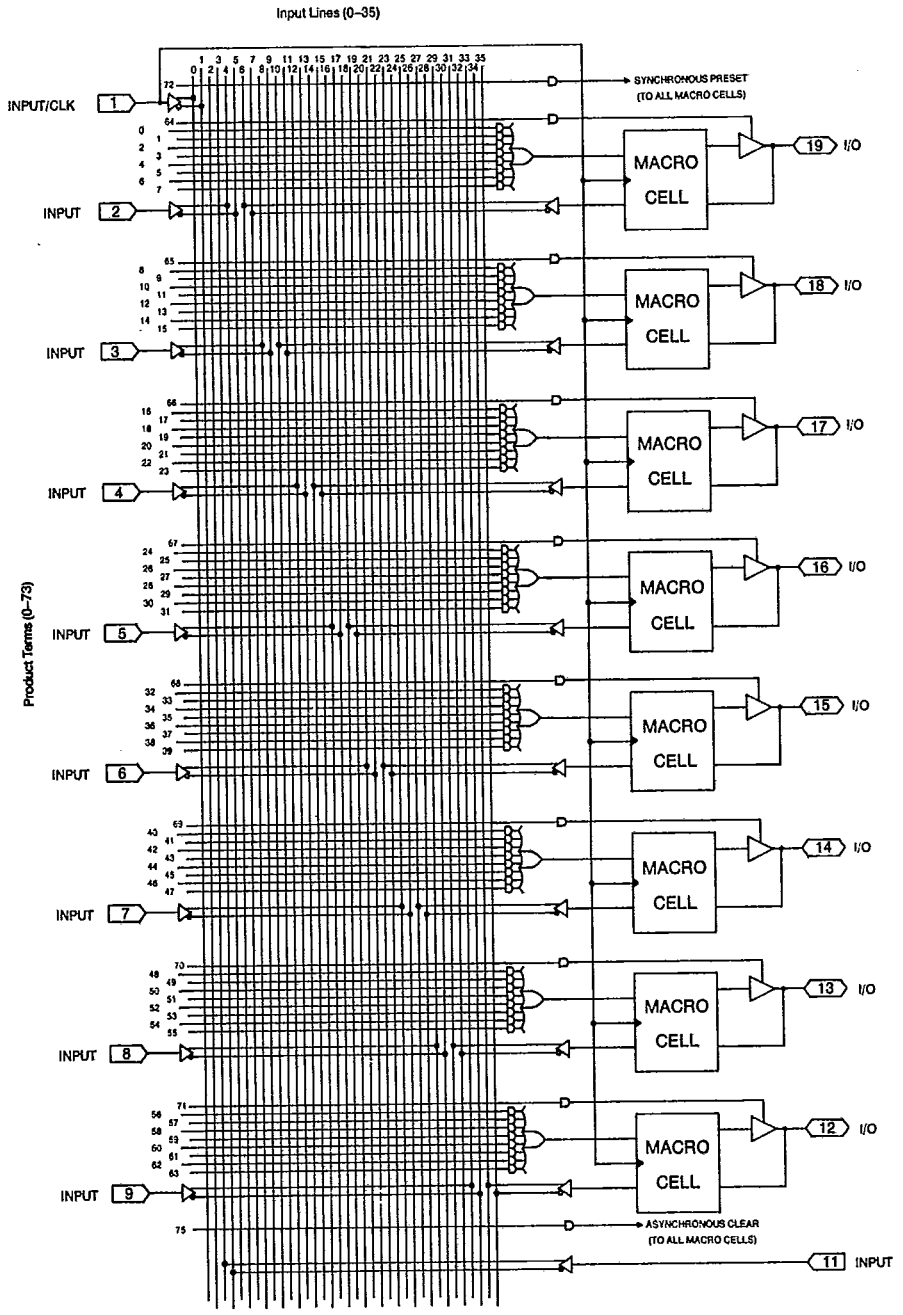


Figure 3. PEEL18CV8 Logic Array Diagram

Function Description
The PEEL18CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview
The PEEL18CV8 architecture is illustrated in the block diagram of figure 2. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL18CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array
The programmable AND array of the PEEL18CV8 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

36 Input Lines:

- 20 input lines carry the true and compliment of the signals applied to the 10 input pins
- 16 additional lines carry the true and compliment values of feedback or input signals from the 8 I/Os

74 product terms:

- 64 product terms (arranged in groups of 8) used to form sum of product functions
- 8 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL18CV8, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell
The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL18CV8 to the precise requirements of their designs.

Macrocell Architecture
Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Refer to table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type
The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL18CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gate, bypassing the output buffer, regardless of whether the output function is registerd or combinatorial. This feature allows the creation of asynchronous latches,

5

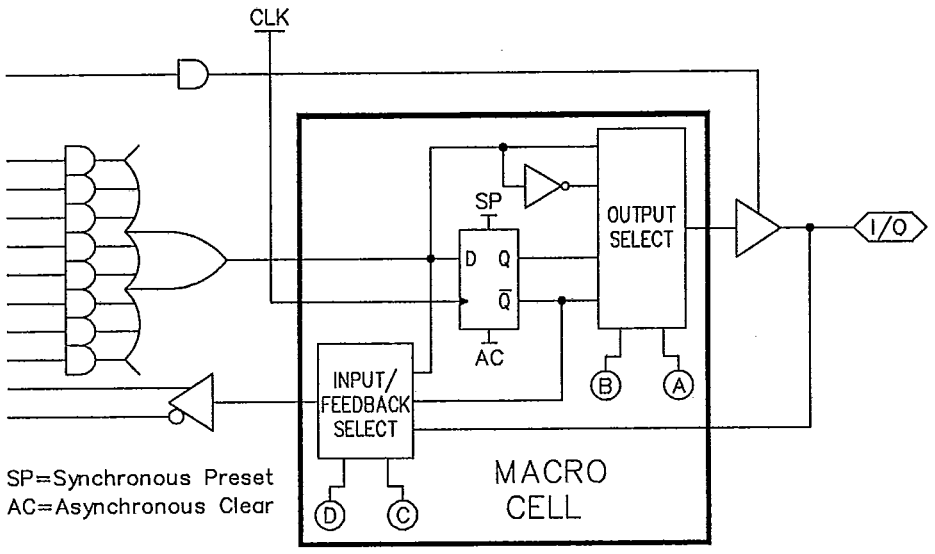


Figure 4. Block Diagram of the PEEL18CV8 I/O Macrocell

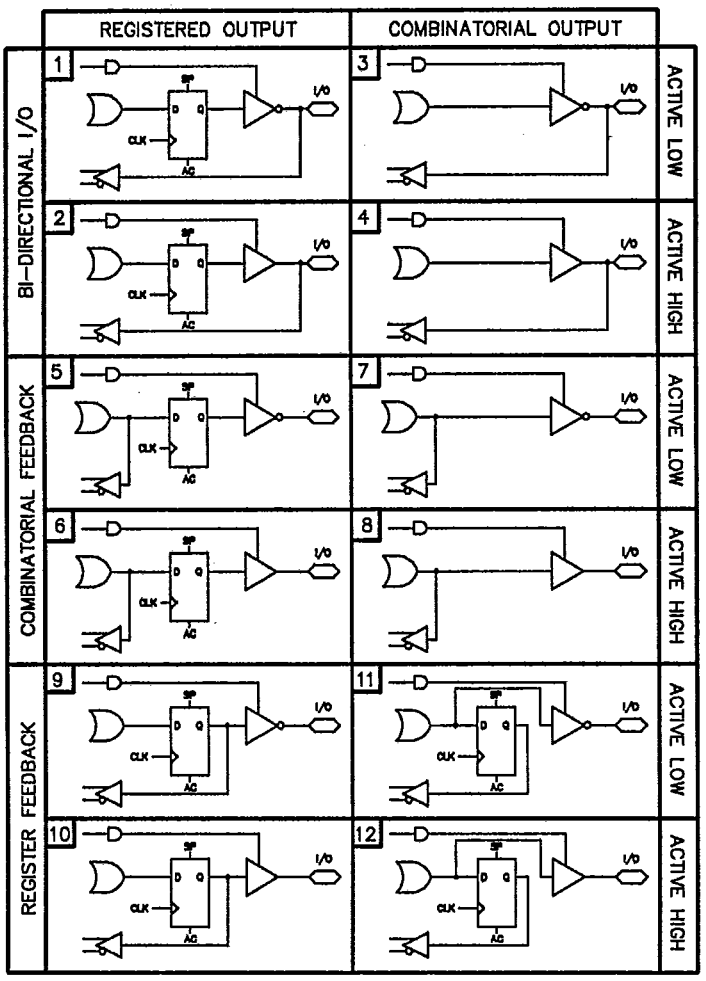


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL18CV8 I/0 Macrocell.

Configuration #	A B C D	Input/Feedback Select	Output Select	
1	1 1 1 1	Bi-Directional I/O	Register	Active Low
2	0 1 1 1	"	"	Active High
3	1 0 1 1	"	Combinatorial	Active Low
4	0 0 1 1	"	"	Active High
5	1 1 1 0	Combinatorial Feedback	Register	Active Low
6	0 1 1 0	"	"	Active High
7	1 0 1 0	"	Combinatorial	Active Low
8	0 0 1 0	"	"	Active High
9	1 1 0 0	Register Feedback	Regisiter	Active Low
10	1 1 0 0	"	"	Active High
11	1 0 0 0	"	Combinatorial	Active Low
12	0 0 0 0	"	"	Active High

Table 1. PEEL18CV8 Macrocell Configuration Bits

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gate, bypassing the output buffer, regardless of whether the output function is registerd or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback
Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security
The PEEL18CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

INTERNATIONAL CMOS TECHNOLOGY, INC.

PEEL™18CV8

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [6]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

T-46-19-07

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T_A	Ambient Temperature	Commercial	0	+ 70	°C
		Industrial	− 40	+ 85	°C
T_R	Clock Rise Time	See note 4		250	ns
T_F	Clock Fall Time	See note 4		250	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

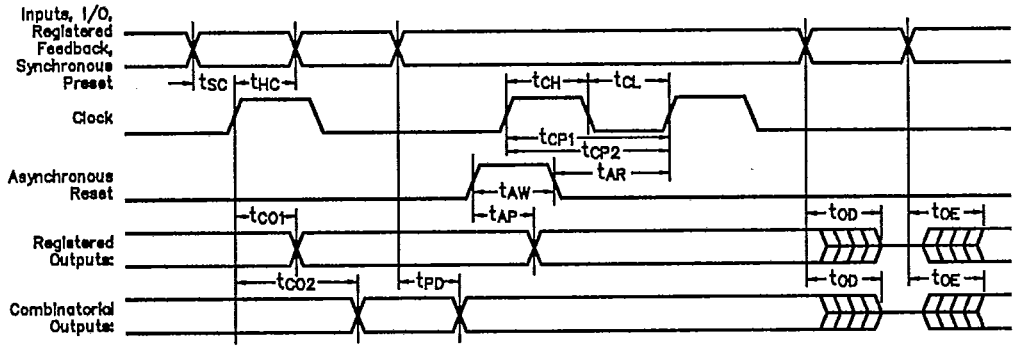
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.45	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 100	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [5]		20 (30)*	mA
I_{CCAC}[1]	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND, All outputs open. [5,11]		I_{CCSC} + 0.7mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		25 (35)*	mA
I_{CCAT}[1]	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH}, All outputs open. [5]		I_{CCST} + 0.7mA/MHz	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

* Numbers in parenthesis specify parameters for industrial temperature range.

A.C. Electrical Characteristics Over the Operating Range[3,12]

Symbol	Parameter	18CV8-25		18CV8-30		18CV8-35		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input[4] or feedback to non-registered output		25		30		35	nS
t_{OE}	Input[4] to output enable[6]		25		30		35	nS
t_{OD}	Input[4] to output disable[6]		25		30		35	nS
t_{CO1}	Clock to output		15		20		20	nS
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35		45		50	nS
t_{SC}	Input[4] or feedback setup to clock	20		25		30		nS
t_{HC}	Input[4] hold after clock	0		0		0		nS
t_{CL},t_{CH}	Clock width - clk low time, clk high time [5]	15		15		15		nS
t_{CP1}	Clock period (register feedback to registered output via internal path)	30		40		45		nS
f_{max1}	Maximum clock frequency ($1/t_{CP1}$)	33.3		25		22.2		MHz
t_{CP2}	Clock period ($t_{SC} + t_{CO1}$)	35		45		50		nS
f_{max2}	Maximum clock frequency ($1/t_{CP2}$)	28.5		22.2		20		MHz
t_{AW}	Asynchronous clear pulse width	25		30		35		nS
t_{AP}	Input[4] to asynchronous clear		30		35		40	nS
t_{AR}	Asynchronous Reset Recovery Time		20		35		30	nS
t_{RESET}	Power-on reset time for registers in clear state		5		5		5	µS

Switching Waveforms



1. Minimum DC input is -0,5V, however inputs may undershoot to -2.0V for periods less than 20ns
2. Contact ICT for other operating ranges. (Industrial, Mil-temp.)
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are open (no load).
6. "Input" refers to input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitance are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration less than 1 second.
11. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit counter.
12. PEEL Device test loads are specified at the end of this section.