INTERNATIONAL CMOS TECHNOLOGY, INC.

Preliminary Data

T-46-19-07

PA7024 PEEL™ Array
CMOS Programmable Electrically Erasable Logic Array

Features

User-Configurable High Density Logic Array
- Create multi-level I/O-buried logic circuits
- Over 80 sum-of-products functions
- 20 I/Os, 2 Input/system-clocks
- 24 pin DIP, 28 pin PLCC packaging

CMOS EE-Technology
- Low power, ICC=100mA+0.5mA/MHz
- Reprogrammable in plastic package
- Low risk inventory, superior factory testing

High Performance
- Wide-gate functions in single level delays
- tpd = 13ns/20ns (internal/external)
- fmax = from 41.6MHz to 58.8MHz

Flexible Architecture
- Input registers and latches
- I/O buried D, T and JK registers with independent clock, preset and reset
- Separate output enables per I/O

Logic Integration and Customization of:
- PLDs, SSI/MSI, random logic, decoders, encoders, muxs, comparators, shifters, counters, state machines, etc.

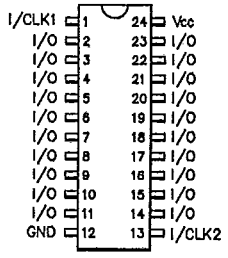
Simplified Development Methodology
- Predictable symmetrical timing, no routing
- Design support with PLACE™ Software and PEEL Development System from ICT

General Description

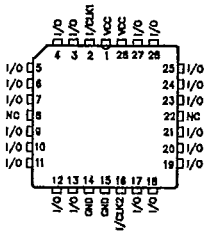
The PA7024 is a user-configurable high-density Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. Designed in ICTs advanced 1-micron CMOS EE-technology, the PA7024 offers low power consumption, high speed performance, and reprogrammability in a plastic package allowing superior factory testing and a low risk re-usable inventory. The PA7024s wide-gate architecture can implement complex combinatorial and sequential functions with-in single-level delays as fast as 13nS (internal) and at clock rates greater than 50MHz.

Its flexible architecture offers; input reg/latches per I/O, buried D, T, or JK registers with independent clock, preset and reset, and separate output enables. This versatility makes the PA7024 ideal for integrating SSI/MSI, multiple PLDs and customizing random logic, decoders, muxs, comparators, shifters, counters, state machines, etc.. Extensive signal interconnectivity makes all timing paths symmetrical, simplifying design with predictable performance and the elimination of gate-array-like routing. Complete development and programming support is provided by ICTs PLACE Software and PEEL Development System.

Pin Configuration



DIP

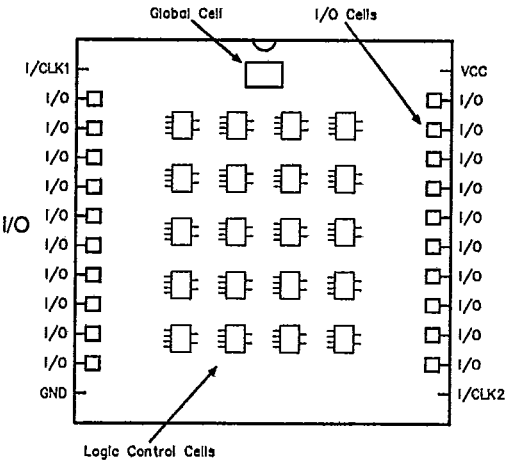


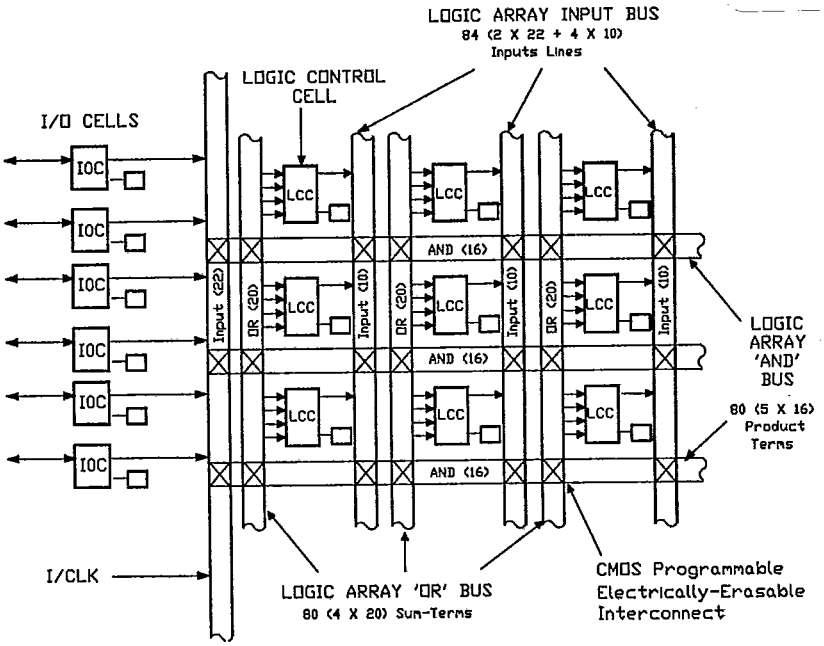
PLCC

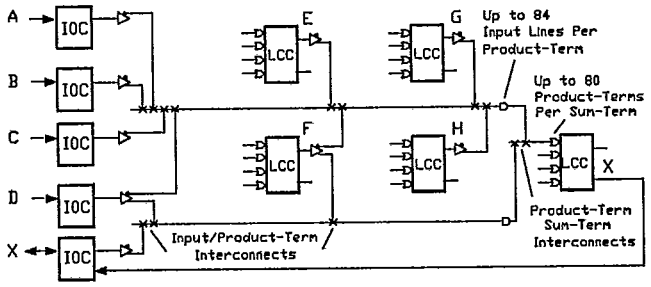
Pin Names:

I/CLK = Input and/or System Clock
I/O = Bi-directional I/O
GND = Ground
Vcc = Power Supply

Block Diagram







$$X = (\overline{A} * B * \overline{C} * \overline{D} * E * \overline{F} * G * H) + (X * D * F)$$

Figure 3. Distributed logic array matrix (partial view) and illustration of a sum-of-products logic equation interconnected in the array

PA7024 Functional Description

The PA7024 is a user-configurable high-density CMOS Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. As illustrated by figures 1 and 2 shown on the previous page (pin configuration and block diagram), the PA7024 has 20 I/O pins and 2 Input/System-Clock pins and is available in both 24-pin 300-mil DIP or 28-pin PLCC packages. The internal architecture of the PA7024 consists of 20 Logic Control Cells (LCCs), 20 I/O Cells (IOCs) and a Global Cell all of which are interconnected and controlled via a distributed programmable logic array matrix.

Logic Control Cell (LCC) Inputs and Outputs

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the distributed logic array matrix. Each of the twenty PA7024 LCCs have four primary inputs and two primary outputs. The inputs to each LCC are complete sum-of-product logic functions from the array matrix. The PA7024 has a total of 80 sum-of-product functions for controlling; LCC registers, IOC output enables, and combinatorial and sequential logic functions.

The two outputs of each LCC can function with complete independence from one another. This makes it possible with the PA7024 to have up to 40 independent output functions for internal and external use. (To put this in perspective, the popular 22V10 PLD architecture provides a total of 10 output logic functions.) Of the two LCC outputs, one can be connected to any I/O Cell (IOC) and associated I/O pin, the other is "buried" for use within the logic array matrix. The PA7024 allows up to 20 levels of I/O buried logic making it possible to implement , for example, a 20-bit high speed binary counter, without sacrificing any I/O pins for input or output use.

Distributed Logic Array Matrix

To better understand how sum-of-products logic functions are created and how the interconnects between LCCs and IOCs work, figure 3 illustrates the distributed logic array matrix. The logic array matrix is made up of multiple busses of input lines (Input bus), product terms (AND bus) and sum terms (OR bus). One output of each LCC can be connected to any IOC, the other is connected to the internal Input bus. The four inputs to each LCC are actually complete sum-of-product functions from the OR bus.

At the intersection of each Input/AND bus and AND/OR bus reside programmable CMOS EEPROM memory cells for controlling interconnectivity between input lines and product terms, and product terms and sum terms. When selectively programmed, complete sum-of-product logic functions can be created similar to that of a PLA structure. The end result allows each sum-term feeding into an LCC to share up to 80 product-terms and each product-term to share up to 84 input lines (the true and compliments of the 22 input pins and the 20 LCC buried outputs). This extensive sharing means product-term resources can be used where they are needed and not left un-utilized as with traditional programmable-AND fixed-OR PLDs.

Eliminating Complex Routing and Timing Issues

Because of the extensive interconectivity in the PA7024s distributed logic array structure, the complex routing and timing issues that are often associated with Field Programmable Gate Arrays (FPGAs) are eliminated. This makes it possible to predict performance and utilization results before actually implementing the design. With few exceptions, all signals route automatically, as expressed in equation form, provided that the maximum number of product terms are not exceeded. Also, all timing delays are completely symmetrical between I/O pins, IOCs or LCCs. For instance, the internal combinatorial delay from the output of any LCC, through the array, to the input of another LCC, is a maximum of one tPDI (13nS with a PA7024-1). External delay, from any I/O pin, through any LCC, to any I/O pin, is tPDX (20nS). Clock signals are also symmetrical avoiding any problems of clock skew.

Inside the Logic Control Cell (LCC)

Each PA7024 LCC includes: three signal routing and control multiplexers, a versatile register with synchronous or asynchronous D, T or JK flip-flops, and several EEPROM memory cells for programming a desired configuration. The key elements of the LCC are illustrated in the LCC block diagram, figure 4. The diagram shows how the four LCC inputs (SUM terms A, B, C and D) are distributed into the cell and how each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

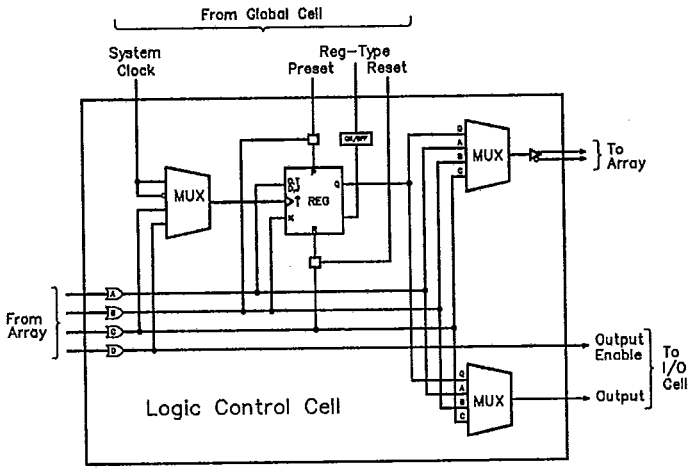


Figure 4. PA7024 Logic Control Cell (LCC)

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input or the preset to the register, or a combinatorial path. SUM-C can be the clock or the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, or the output enable for the connected I/O cell . It is important to note that unlike many PLDs, the PA7024 has complete sum-of-product (not just product term) control of clocks, resets, presets and output enables. The two primary outputs of the LCC can independently select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be combinatorial while the other is registered.

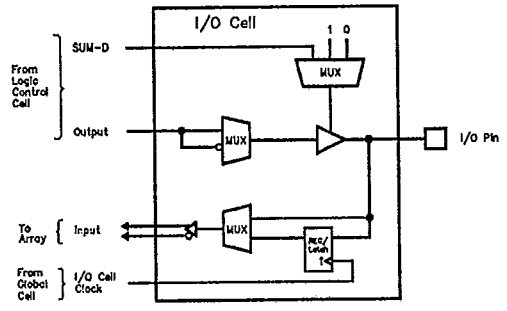


Figure 5. PA7024 I/O Cell (IOC)

Besides the SUM inputs, several inputs from the Global Cell are provided for control. The Global Cell inputs are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that allows dynamic switching of register selection. This last feature is useful for implementing loadable counters and state machines by dynamically switching from D to T for instance.

The I/O Cell (IOC)

The block diagram for the PA7024 I/O Cell (IOC) is shown in figure 5. The input to the IOC can be provided from any one of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The reg/latch can be clocked from a variety of sources determined in the Global Cell. It can also be bypassed for a non-registered input.

The Global Cell

The PA7024s Global Cell, shown in figure 6, is used primarily to control the allocation of the system clock signals to the LCCs and the IOCs. The global cell also contains several global product and sum control terms for LCC functions such as reset, preset, register type and IOC clock. If additional partitioning of global cell clocks and control terms is needed, a second global cell can be selected that allows the

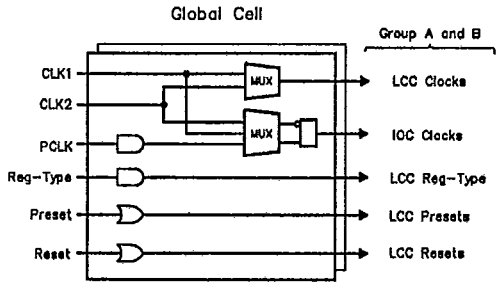


Figure 6. PA7024 Global Cell

LCCs to be divided into two groups, A and B. That is, half of the LCCs can be controlled by Global Cell A and half with Global Cell B. Global Cell A controls the LCCs connected to IOCs 2-11, and Global Cell B, the LCCs connected IOCs 14-23. This allows, for instance, two high speed clocks to be used among the LCCs in the same PA7024. Unless the second global cell is selected all LCCs and IOCs will be controlled by Global Cell A.

PA7024 Applications

The unique combination of wide gate performance and logic cell flexibility, allows the PA7024 to address a multitude of logic functions ranging from random logic to high-speed state machines. The PA7024 is ideal for implementing wide-path applications at high speeds such as fast binary counters, clock dividers, state machines, address decoders, encoders, comparators, adders and look-ahead carry. Yet, its LCC flexibility makes possible standard random logic functions such as a D flip-flops (74LS74) with independent clock reset and preset, SR latches and gated latches. Additionally, the number of registers and latches available for data storage as well as three-state I/Os, open up many possibilities for bus interfaced sub-systems.

Design Security

The PA7024 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PA7024 can not be accessed until the entire chip has been electrically erased.

Development Support

Development support for the PA7024 is provided by the PLACE Development Software and PEEL Development System from ICT. The PLACE (PEEL Architectural Compiler and Editor) software creates a software design environment that combines the attributes of logic equation and schematic entry. The mouse driven PLACE editor graphically illustrates and controls the PA7024s architecture making the overall design easy to understand, while allowing the effectiveness of boolean logic equations or state machine design entry.

The PLACE compiler performs logic transformation and logic reduction making it possible to specify equations in almost any fashion and to get the maximum logic into every design. PLACE also provides a multi-level logic simulator that allows the external and internal signals to be fully simulated and analyzed via a waveform display. Programming is supported with direct interface to the ICT PEEL Development System programmer (PDS-1) as well with a down-load capability to other popular programmers. System requirements for PLACE are: IBM XT/AT or compatible, 640K memory, EGA or VGA graphics and mouse.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permenant damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		250	ns
T_F	Clock Fall Time	(Note 3)		250	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [5]	− 30	− 120	mA
I_{CCSC}	V_{CC} Current, Standby, CMOS	V_{IN} = V_{CC} or GND [4]		110	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN} = V_{CC} or GND [4,12]		I_{CCSC} + 0.5mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH} [4]		140	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH} [4,12]		I_{CCST} + 0.5mA/MHz	mA
C_{IN}	Input Capacitance [6]	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

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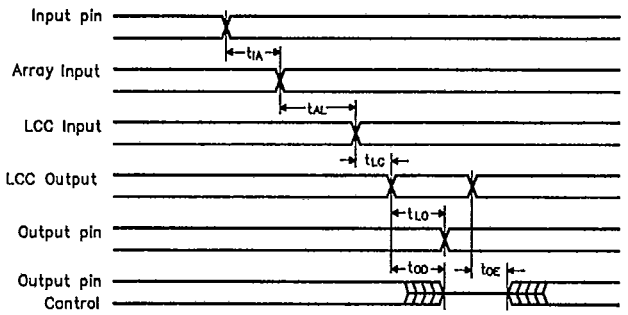
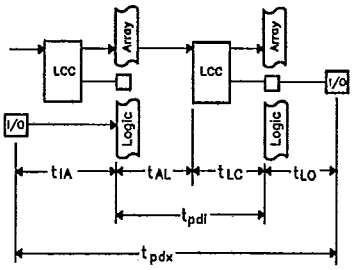
PA7024

T-46-19-07

Combinatorial Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

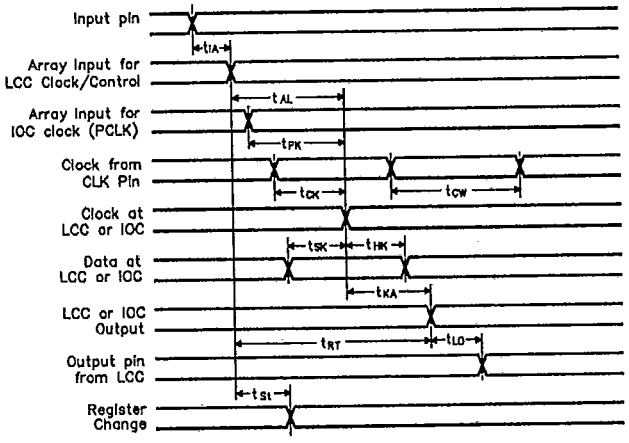
Over operating conditions

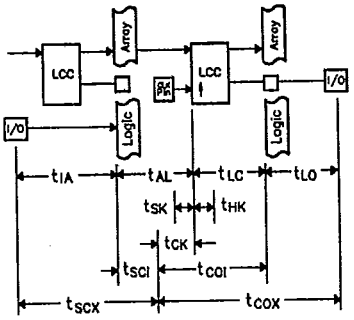
Symbol	Parameters [7, 13]	PA7024-1		PA7024-2		Units
		Min	Max	Min	Max	
tPDI	Propagation delay Internal (tAL+ tLC)		13		17	nS
tPDX	Propagation delay External (tIA+ tAL+ tLC+ tLO)		20		25	nS
tIA	Input or I/O pin to input of Array		2		2	nS
tAL	Input of Array to LCC		12		16	nS
tLC	LCC input to LCC output [11]		1		1	nS
tLO	LCC output to output pin		5		6	nS
tOD, tOE	Output Disable, Enable from LCC output [8]		5		6	nS
tOX	Output Disable, Enable from input pin[8]		20		25	nS

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges (Industrial, Mil-Temp)
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins open (no load).
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads at end of section 5 for V_{REF} value). t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$..
9. "System-clock" refers to pin 1 or pin 13 high speed clocks
10. For T or JK registers in toggle (divide by 2) operation only
11. For combinatorial and async-clock to LCC output delay
12. ICC for a typical application: This parameter is tested with the device programmed as a 20-bit Counter.
13. Test loads are specified at the end of section 5 in this data book.

Sequential Timing - Waveforms and Block Diagram





A.C. Electrical Characteristics (preliminary)

Over operating conditions

Symbol	Parameters [7, 13]	PA7024-1		PA7024-2		Units
		Min	Max	Min	Max	
tSCI	Set-up to system-clock [9] Int.(tAL+ tSK+ tLC - tCK)	10		15		nS
tSCX	Set-up to system-clock Ext.(tIA+ tSCI)	12		17		nS
tCOI	System-clock to Array Int.(tCK+ tLC)		7		8	nS
tCOX	System-clock to Output Ext.(tCOI+ tLO)		12		13	nS
tCK	System-clock delay to LCC/IOC		6		7	nS
tSK	LCC\IOC input data set-up time to async. clock	3		4		nS
tHK	LCC\IOC input data hold time to async. clock	4		4		nS
fMAX1	Max system-clock frequency Int/Int 1/(tSCI + tCOI)		58.8		43.5	MHz
fMAX2	Max system-clock frequency Ext/Int 1/(tSCX + tCOI)		52.6		40.0	MHz
fMAX3	Max system-clock frequency Int/Ext 1/(tSCI + tCOX)		45.7		35.7	MHz
fMAX4	Max system-clock frequency Ext/Ext 1/(tSCX+ tCOX)		41.6		33.3	MHz
fTGL	Max system-clock toggle frequency 1/(tCW + tCW) [10]		71.4		62.5	MHz
tCW	System-clock low or high pulse width	7		8		nS
tST	Array input to Global Cell preset/reset		17		23	nS
tRT, tPK	Array input to Global Cell: reg-type change, PCLK		9		11	nS
tHX	Input hold time from system clock	0		0		nS
tPR	LCC preset/reset to LCC output		5		6	nS