T-50-09

PLESSEY
Semiconductors

NJ8822, NJ8822B

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ8822 is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 950MHz operation.

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >i10MHz Input Frequency

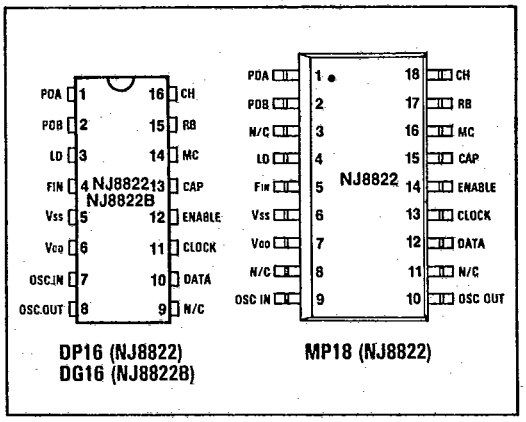


Fig.1 Pin connections - top view, not to scale

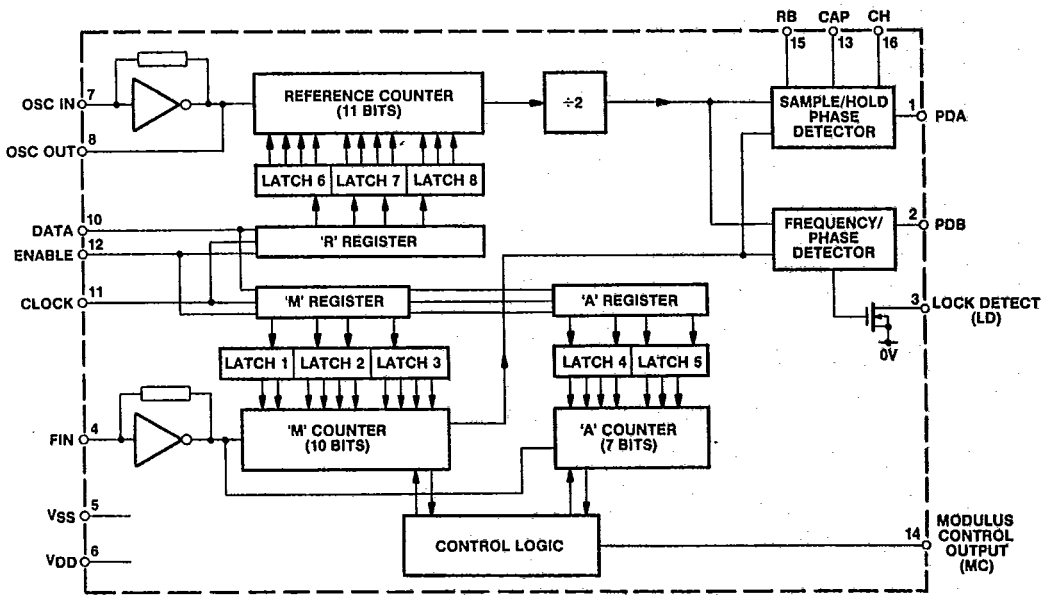


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range: NJ8822 -30°C to +70°C, NJ8822B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current			5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
			1.5	mA	FOSC, FIN = 1MHz } 0 to 5V square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T +	3			V	Note 1
Negative going threshold, V_T-			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}) -0.5V to 7V
Input voltage
Open drain O/P (pin 3 (DG) pin 4 (MP)) 7V
All other pins V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature -55°C to +125°C (DP and MP packages, NJ8822)
Storage temperature -65°C to +150°C (DG package, NJ8822B)

PIN DESIGNATION

T-50-09

Pin No. DG,DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD}-V_{SS})/2 when the system is in lock.**
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8822, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to Vss).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M $\geq$ A. Where every possible channel is required, the minimum division ratio should be $N^2 - N$.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and Vss.
16	18	CH	An external hold capacitor should be connected between this pin and Vss.

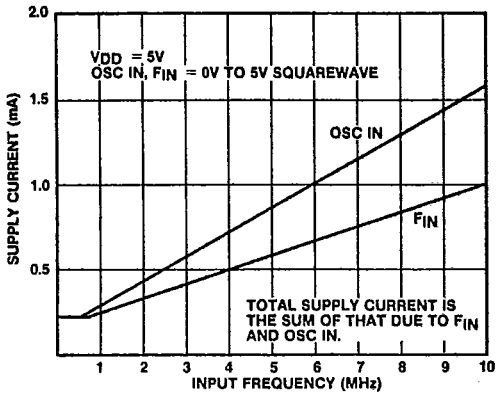


Fig.3 Typical supply current v. input frequency

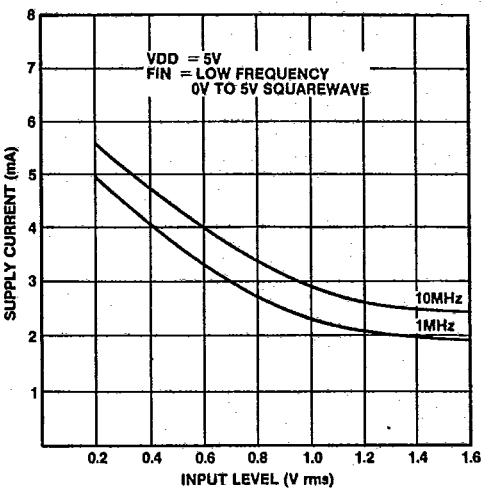


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N+1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \text{ therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non resettable version NJ8824 should be considered.

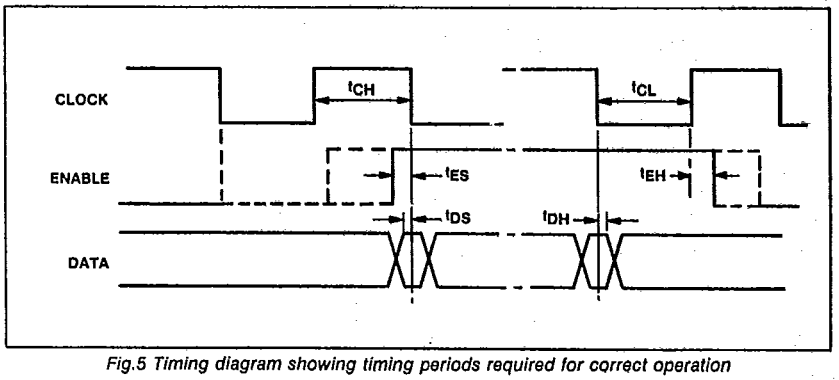


Fig.5 Timing diagram showing timing periods required for correct operation

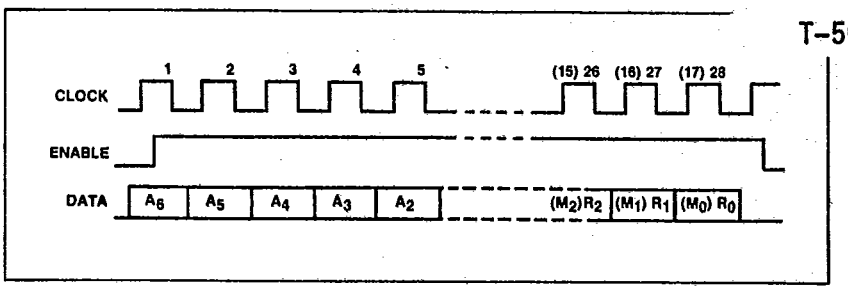


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ8822 has both a high gain and uses a double sampling technique to reduce spurious ouputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/4})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

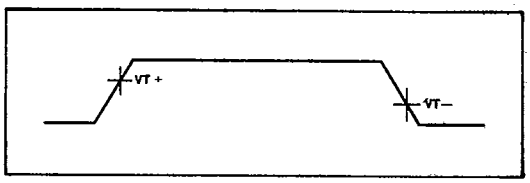


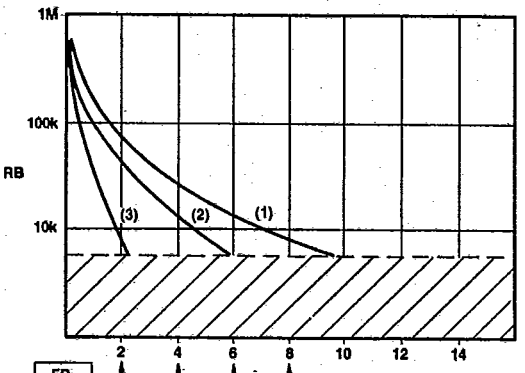
Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320
	K_Φ IN VOLTS/RAD.			

Fig.8 RB v. gain and reference frequency