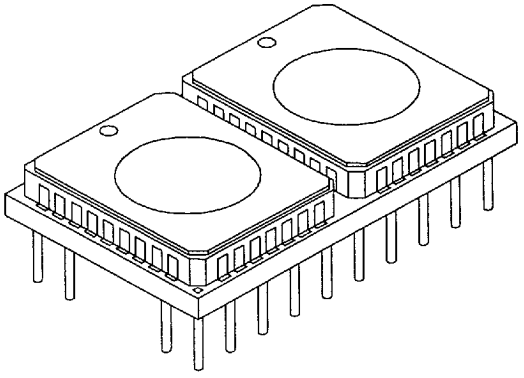
2 Megabit UVEPROM

DPV128X16A

DESCRIPTION:

The DPV128X16A is a 40-pin Pin Grid Array (PGA) consisting of two 128K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a pattern resulting in the smallest possible module outline.

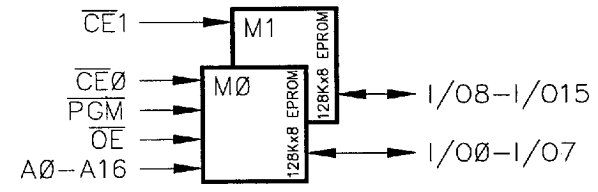
The pins have been arranged around a central 0.3" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing two 0.1µf decoupling capacitors.



FEATURES:

- Organizations Available:
  128K X 16 or 256K X 8
- Access Times:
  120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 13.0 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (100µs Pulses Typ.)
- Common Data Inputs and Outputs
- Power Consumption:
  11mW (Standby)
  0.55W (Active)
- TTL-compatible Inputs and Outputs
- 40-Pin PGA (Pin Grid Array) Package

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CE0}$, $\overline{CE1}$	Chip Enables
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
V_{DD}	Power (+ 5V)
V_{SS}	Ground
V_{PP}	Programming Voltage
N.C.	No Connect

PIN-OUT DIAGRAM

(TOP VIEW)

$\overline{CE}$Ø	1	I/O7	11	1	11	21	31	21	I/O3	31	VDD
A13	2	I/O6	12	2	12	22	32	22	I/O2	32	AØ
A1Ø	3	I/O5	13	3	13	23	33	23	I/O1	33	A1
A8	4	I/Ø4	14	4	14	24	34	24	I/OØ	34	A3
A15	5	$\overline{OE}$	15	5	15	25	35	25	A4	35	A5
A9	6	$\overline{PGM}$	16	6	16	26	36	26	VPP	36	A6
A16	7	I/O15	17	7	17	27	37	27	I/O11	37	A7
A2	8	I/O14	18	8	18	28	38	28	I/O1Ø	38	A12
A11	9	I/O13	19	9	19	29	39	29	I/O9	39	A14
VSS	1Ø	I/O12	2Ø	1Ø	2Ø	3Ø	4Ø	3Ø	I/O8	4Ø	$\overline{CE}$1

ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [2]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to +7.0	V
V_{PP}	Programming Voltage [2]	-0.5 to 14.0	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

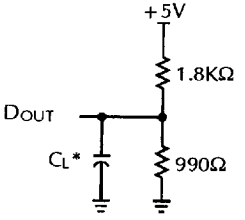
RECOMMENDED OPERATING RANGE [2]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage [4]		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+1.0	V
V_{IL}	Input LOW Voltage		-0.2		0.8	V
V_{PP}	V_{PP} Supply Voltage [5]		12.75	13.0	13.25	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100pF	except t_{DF} and t_{DFP}
2	5pF	t_{DF} and t_{DFP}

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	15	pF	V_{IN} = 0V
C_{ADR}	Address Input	35		
C_{OE}	Output Enable	35		
$C_{I/O}$	Data Input/Output	25		
C_P	Program Enable	35		

Figure 1. Output Load

* Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	X8		X16		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD}	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{DD} or V_{SS}	-20	+20	-10	+10	µA
I_{CC}	V_{DD} Operating Current, Read	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA Cycle=min., Duty=100%		50		100	mA
I_{SB1}	V_{DD} Standby Current (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}		2		2	mA
I_{SB2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = V_{DD} ± 0.3V, I_{OUT} = 0mA V_{IN} ≥ V_{DD} -0.3V or V_{IN} ≤ +0.3V		200		200	mA
I_{PP1}	V_{PP} Supply Current Programming	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, T_A = +25°C		20		40	mA
I_{PP3}	V_{PP} Supply Current Read [4]	$\overline{CE}$, $\overline{OE}$ = V_{IL}, I_{OUT} > 0mA		20		20	µA
V_{OL}	Output LOW Voltage	I_{OUT} = 2.1mA		0.45		0.45	V
V_{OH}	Output HIGH Voltage	I_{OUT} = -400µA	2.4		2.4		V

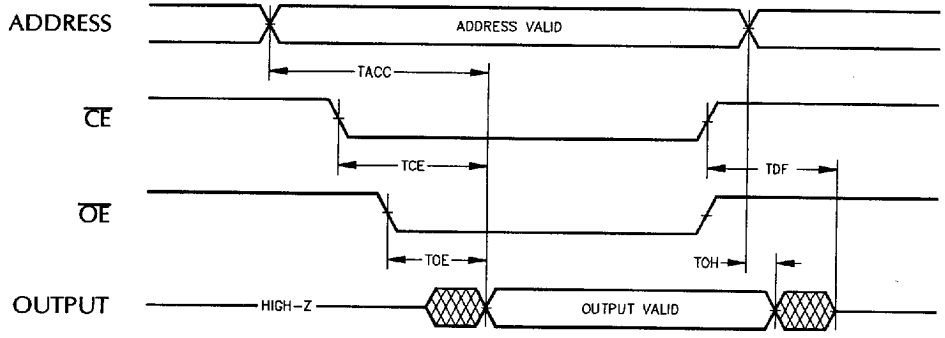
FUNCTIONS AND PIN CONNECTIONS							
Mode / Function		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{DD}	I/O0 - I/O15
Read Operations	Read	L	L	X	5.0V	5.0V	Data Out
	Output Deselect	L	H	X			High Impedance
	Standby	H	X	X			High Impedance
Program Operations (T_A = +25 ± 5°C)	Program	L	H	L	13.0V	6.5V	Data In
	Program Inhibit	H	X	X			High Impedance
	Program Verify	L	L	H			Data Out

L = LOW, H = HIGH and X = Don't Care

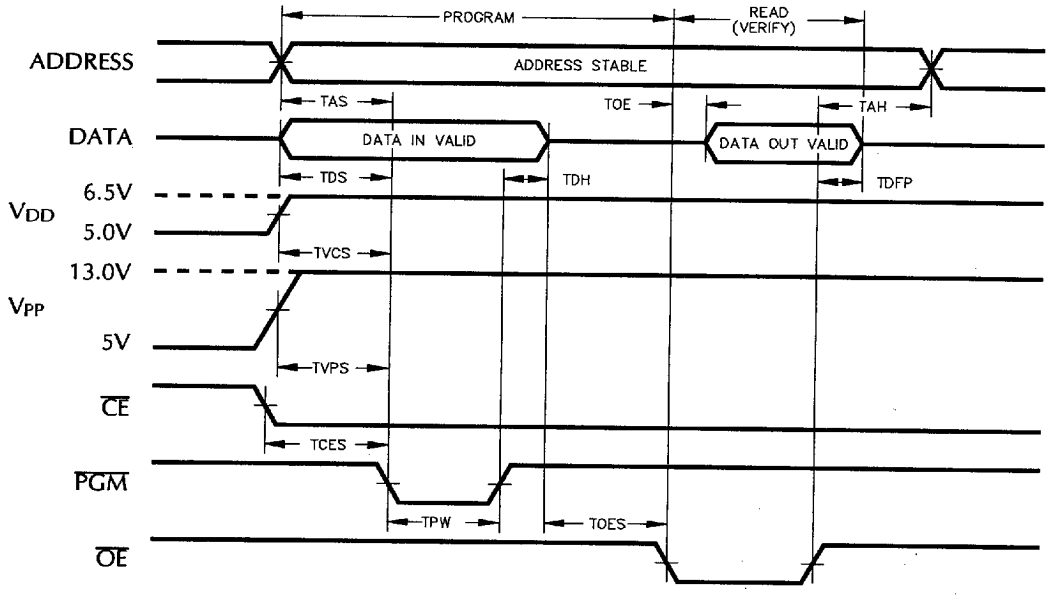
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	120ns		150ns		170ns		200ns		250ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time [8]		120		150		170		200		250	ns
2	t_{CE}	Chip Enable to Output Valid [7]		120		150		170		200		250	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		40		40		65		75		100	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]	0	35	0	40	0	50	0	60	0	60	ns
5	t_{OH}	Output Hold from Address Change	0		0		0		0		0		ns

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Set-up Time	2		µs
7	t_{CES}	Chip Enable Set-up Time	2		µs
8	t_{OES}	Output Enable Set-up Time	2		µs
9	t_{DS}	Data Set-up Time	2		µs
10	t_{VCS}	V_{DD} Set-up Time [5]	2		µs
11	t_{VPS}	V_{PP} Set-up Time [5]	2		µs
12	t_{AH}	Address Hold Time	0		µs
13	t_{DH}	Data Hold Time	2		µs
14	t_{DFP}	Output Enable HIGH Output Float Delay [3]	0	130	ns
15	t_{PW}	Programming Pulse Width [10]	95	105	µs
16	t_{OE}	Data Valid from Output Enable		150	ns

READ TIMING



PROGRAMMING TIMING [4]



PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure *(See Erasure section)*, the DPV128X16A contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV128X16A through the procedure of programming. A 0.1µF capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.5V and +13.0V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode, $\overline{OE}$ is set at V_{IH}, V_{DD} is set at +6.5V, and then V_{PP} is set at +13.0V followed by $\overline{CE}$ being set to V_{IL}. After the applied address and input data signals are stable, programming is accomplished by a 100µs V_{IL} pulse on the $\overline{PGM}$ pin *(refer to the Programming Timing Diagram)*.

First program each address with a 100µs pulse on the $\overline{PGM}$ without verification. Then return to first address and start a verification loop verifying each address. If an address location fails verification, apply up to 10 consecutive 100µs $\overline{PGM}$ pulses with a verification after each pulse.

If the device fails to program after 10 attempts, the programming is considered failed. After the byte is verified, continue the algorithm through all the required addresses. Lower V_{PP} to +5.0V and then lower V_{DD} to 5.0V and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

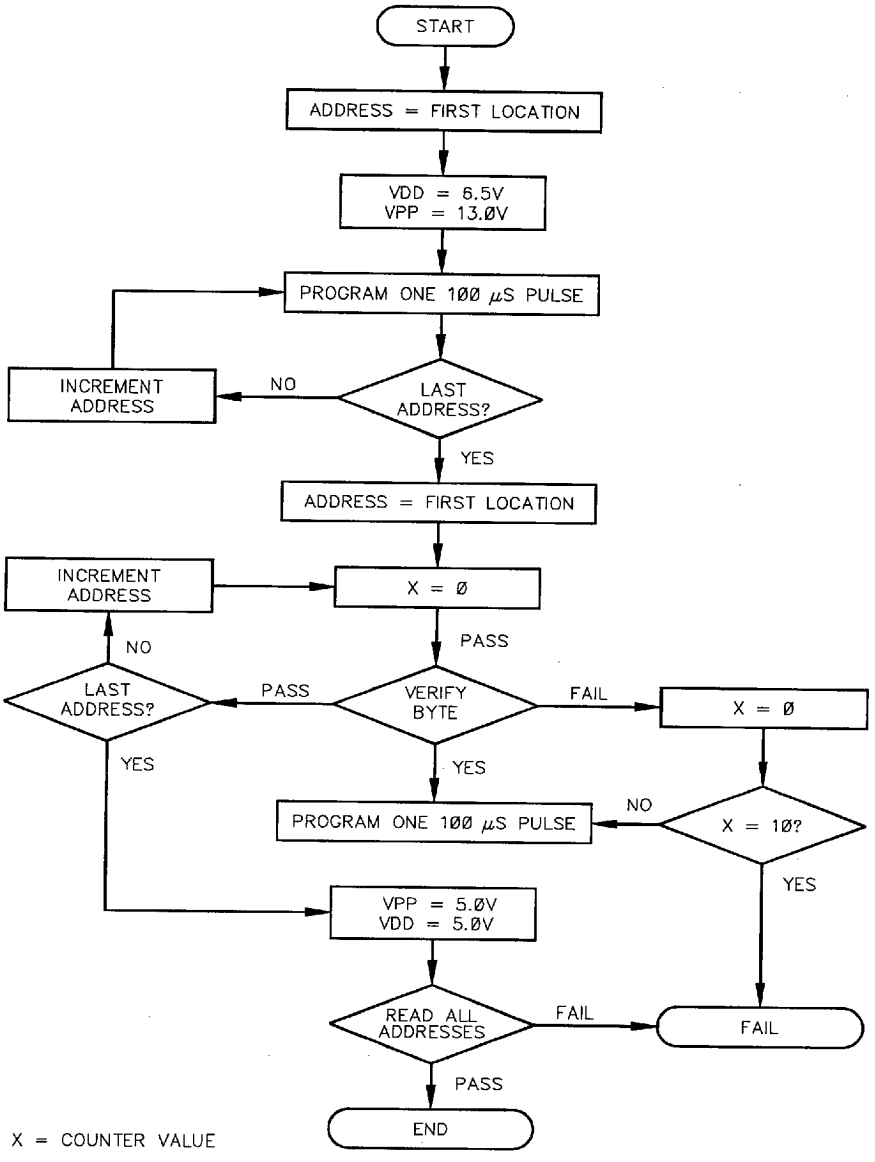
To clear all locations of their programmed contents it is necessary to expose the DPV128X16A to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase a DPV128X16A. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000µW/cm^2] for 20 minutes.

The DPV128X16A and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV128X16A. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.
5. V_{PP} must not be greater than 14.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 13.0V. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. t_A = -55°C to +125°C, V_{DD} = 5.0V ± 0.5V, and V_{PP} = V_{DD} reading. t_A = +25°C ± 5°C, V_{DD} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V programming.
7. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the following edge of $\overline{CE}$ without impact on t_{CE}.
8. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the following Address is valid without impact on t_{ACC}.
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Program Pulse Width Tolerance is 100µs ± 5%.

Figure 2. Programming Flow Chart



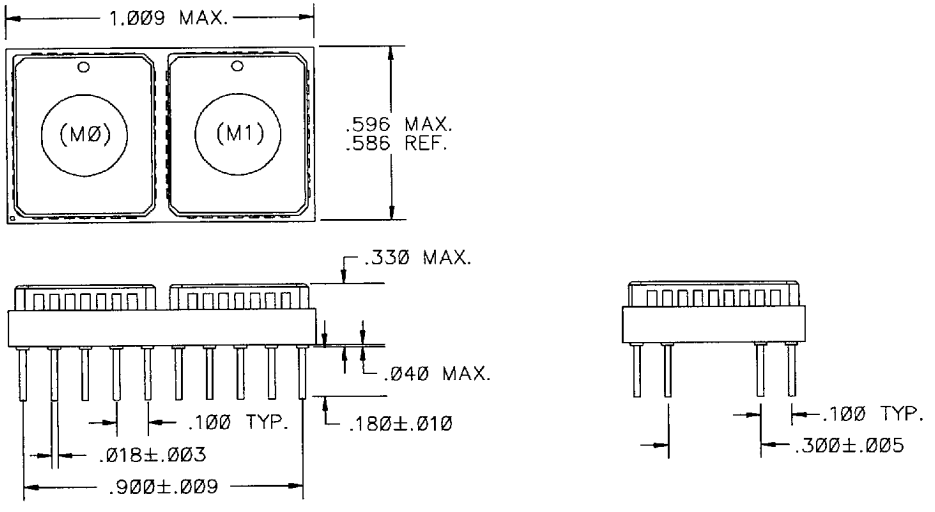
ORDERING INFORMATION

DP V 128 X 16 A – XX X

PREFIX		
TYPE	V	UVEPROM
MEMORY DEPTH	128	
DESIG	X	MODULE WITHOUT SUPPORT LOGIC
MEMORY WIDTH	16	
PACKAGE	A	40-PIN PGA MODULE
SPEED	12	120ns
	15	150ns
	17	170ns
	20	200ns
	25	250ns
GRADE	C	COMMERCIAL 0°C to +70°C
	I	INDUSTRIAL −40°C to +85°C
	M	MILITARY −55°C to +125°C
	B*	MIL-PROCESSED −55°C to +125°C

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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