HARRIS SEMICONDUCTOR

CMM5104

Radiation Hardened, High Reliability, CMOS/SOS 4096 Word by 1 Bit LSI Static RAM

December 1992

T-46-23-05

Features

- Radiation Hardened to 100KRAD(Si)
- Cosmic Ray Upset Immunity Typically 2 x 10^{-9} Errors/Bit Day
- Latch Up Free Under Transient Radiation
- Transient Upset > 10^{10} RADS/s, 20ns Pulse
- Fully Static Operation
- Single Power Supply 4.5V to 6.5V
- All Inputs and Outputs TTL Compatible
- Tri-State Outputs
- Industry Standard 18 Pin Configuration
- Fast Access Time tAVQV = 200ns
- Low Standby and Operating Power

Description

The CMM5104 is a high reliability 4096 word by 1 bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable.

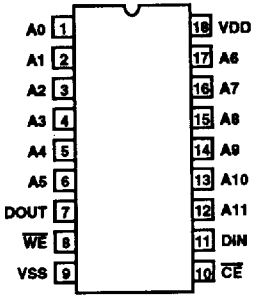
CMOS/SOS technology permits operation in high radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single event upset caused by cosmic rays or heavy ions.

TTL compatibility on all input and output terminals permits easy system integration. The data out signal has the same polarity as the input data. A separate data input and a separate tri-state output are used.

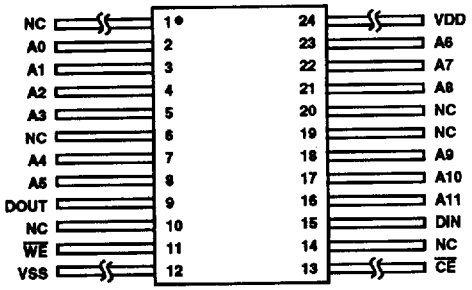
The CMM5104 is supplied in 18 lead dual-in-line sidebrazed ceramic package (D suffix). The part is also available in a 24 lead flatpack ceramic package (K suffix).

Pinout

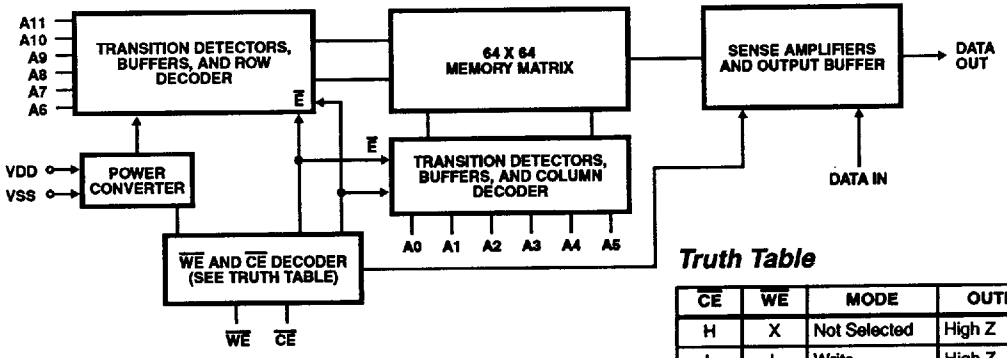
18 PIN CERAMIC DIP
CASE OUTLINE D6, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
INTERNAL PACKAGE CODE "H9L"
TOP VIEW



Functional Diagram



Truth Table

CE	WE	MODE	OUTPUT
H	X	Not Selected	High Z
L	L	Write	High Z
L	H	Read	Data Out

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3406

Specifications CMM5104

Absolute Maximum Ratings

Supply Voltage (VDD),
All voltage values referenced to VSS terminal ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5 to VDD +0.5V
Input Current, Any One Input ..... ±10mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C
Typical Derating Factor ..... 3.0 mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Maximum Package Power Dissipation
For T_A = -55°C to +100°C 100mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
Power Dissipation per Output Transistor
For T_A = Full Package Temperature Range 100mW
Gate Count ..... 5400 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +6.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD/2 to VDD
Data Retention Supply Voltage 2.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	0.1	-	1.0	mA
Operating Device Current (Note 1)	IOPER	Cycle Time = 1µs	-	4.5	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs	-	0.1	-	1.0	mA
Output Low Drive (Sink) Current	IDN	VOUT = 0.4V	4.0	-	2.5	-	mA
Output High Drive (Source) Current	IDP	VOUT = VDD - 0.4V	3	-	2	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±2	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VDD	-	±5	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR		-	40	-	400	µA

NOTES:

1. Operating current measured using 1MHz cycle and CL = 50pF.
2. Measured using 1MHz cycle.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
READ CYCLE TIMES						
Read Cycle	tAVAV	200	-	250	-	ns
Access from Address	tAVQV	-	200	-	250	ns
Access from $\overline{CE}$	tELQV	-	220	-	280	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	200	-	250	-	ns
Write Pulse Width (Note 1)	tWLWH	125	-	145	-	ns
Address Set Up to Beginning of Write	tAVWL	0	-	0	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5% **(Continued)**

PARAMETER	SYMBOL	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Address Set Up to End of Write	tAVWH	160	-	205	-	ns
Address Hold Time	tWHAV	40	-	45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	160	-	205	-	ns
$\overline{CE}$ Pulse Width (Note 1)	tELEH	180	-	220	-	ns
Data to Write Set Up Time	tDVWH	100	-	120	-	ns
Data Hold From Write	tWHDX	5	-	10	-	ns

NOTE:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

PARAMETER	SYMBOL	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Output Voltage Low Level	VOL	-	0.1	-	0.1	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.1	-	V
Input Capacitance (Note 2)	CIN	-	5	-	5	pF
Output Capacitance (Note 2)	COUT	-	7	-	7	pF
Output Hold From Address	tAVQZ	-	80	-	100	ns
Output Hold From $\overline{CE}$	tEHQZ	-	80	-	100	ns

NOTE:

1. Parameters in this table are not directly 100% tested, but are characterized at initial design and after design or processing changes affating these parameters.
2. Capacitance measurements are made with no bias applied.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C MIN	LIMITS POST RADIATION +25°C MAX	UNITS
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	1.0	mA
Operating Device Current (Note 1)	IOPER	Cycle Time = 1µs	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs	-	1.0	mA
Output Low Drive Current (Sink)	IDN	VOUT = 0.4V	2.5	-	mA
Output High Drive Current (Source)	IDP	VOUT = VDD - 0.4V	2.0	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2.5	V
Data Retention Quiescent Current	IDDDR		-	400	µA
Read Cycle	tAVAV		250	-	ns
Access from Address	tAVQV		-	250	ns
Access from $\overline{CE}$	tELQV		-	280	ns

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C		UNITS
			MIN	MAX	
Write Cycle	tAVAV		250	-	ns
Write Pulse Width (Note 3)	tWLWH		145	-	ns
Address Set Up to Beginning of Write	tAVWL		0	-	ns
Address Set Up to End of Write	tAVWH		205	-	ns
Address Hold Time	tWHAV		45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH		205	-	ns
$\overline{CE}$ Pulse Width (Note 3)	tELEH		220		ns
Data to Write Set Up Time	tDVWH		120	-	ns
Data Hold From Write	tWHDX		10	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Measured using 1MHz cycle.
3. Operating current measured using 1MHz cycle and CL = 50pF.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

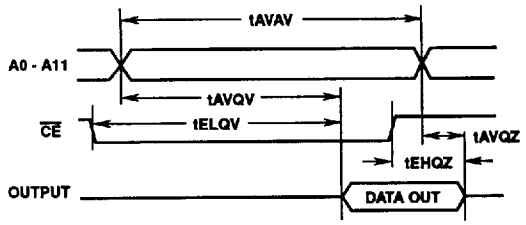
PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IDN	-15% of 0 hr. value
Output High Drive Current (Source)	IDP	-15% of 0 hr. value
Tri-State Output Leakage Current	IOZ	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-IRZ SUBGROUPS	3Z SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A	N/A
PDA		100%/5004	1, 7, Δ	1, 7	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A	N/A
	Others	Samples/5005	1, 7	N/A	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9	N/A

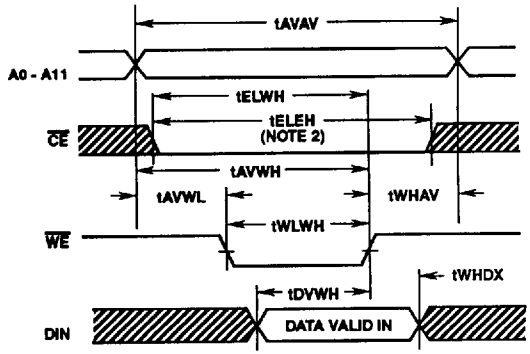
Timing Waveforms

READ CYCLE



NOTE: Timing measurement is referenced to VDD/2.

WRITE CYCLE

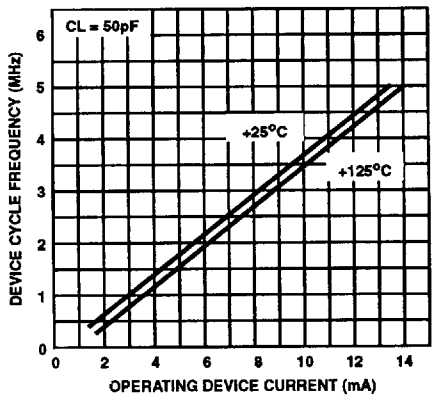


NOTES:

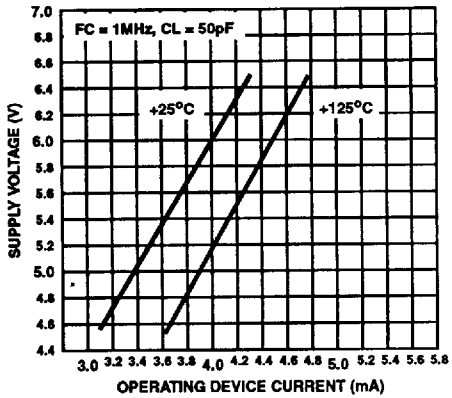
1. Timing measurement is referenced to VDD/2.
2. $\overline{CE}$ and $\overline{WE}$ must overlap for at least TWLWH minimum value, tDVWH minimum value must occur during this overlap.

Typical Performance Curves

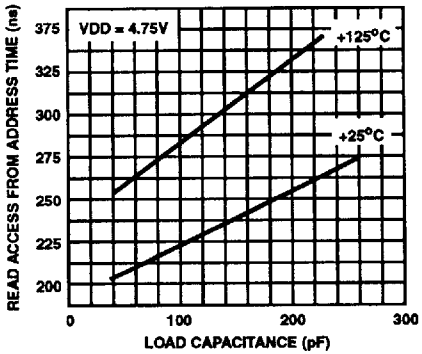
TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF CYCLE FREQUENCY



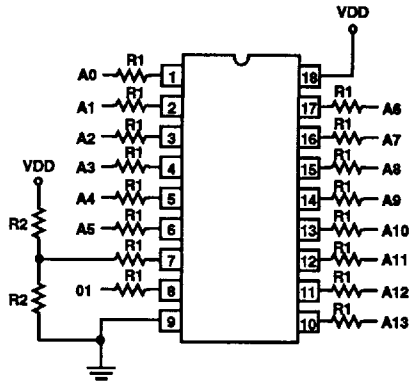
TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF SUPPLY VOLTAGE



READ ACCESS FROM ADDRESS TIME (tAVQV) AS A FUNCTION OF LOAD CAPACITANCE. (TIME MEASUREMENTS MADE AT 50% VDD POINT)

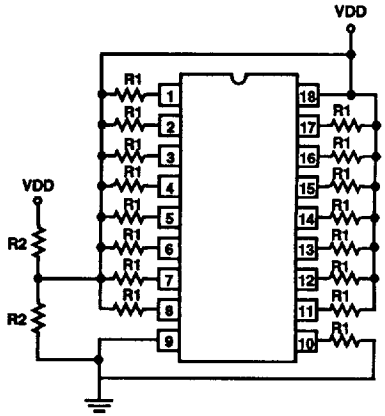


Burn-In Circuits



DYNAMIC CONFIGURATION

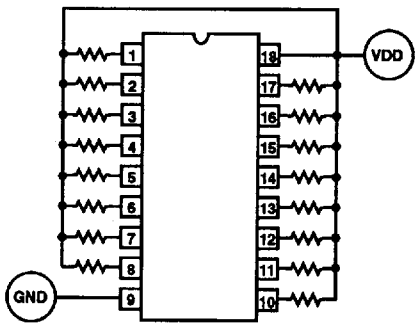
NOTES:
R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kW ± 5%
VDD = 5.5V (Min)
VIN = 0V, VDD
Frequency: A0 = 100kHz ± 5%; A1 = A0/2 . . . . A13 = A12/2
01 = 200kHz ± 5%, 0.6µs Low, 4.4µs High



STATIC CONFIGURATION

NOTES:
R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kΩ ± 5%
VDD = 5.5V (Min)
Static Burn-In 1 memory array pre-initialized with all Highs at VDD, VIN = VDD
Static Burn-In 2 memory array pre-initalized with all Lows at VSS, VIN = VSS

Irradiation Circuit



NOTES:
VDD = +5V, +5%
GND = 0V
All Resistors are 47kΩ ± 5%

Harris - IRZ Product Flow

Wafer Lot Acceptance Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 100K RADS(Si) Total Dose 2 Samples/Wafer, 0 Reject

Nondestructive Bond Pull Method 2023

Internal Visual (100%) Method 2010 (See "Visual Inspection")

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs Min., +150°C Min

Temperature Cycling (100%) Method 1010, Condition C, -65°C to +150°C

Constant Acceleration (100%) Method 2001, Condition E, Y1 (30,000g)

Particle Impact Noise Detection Method 2020, Condition A, 20g Peak at 60Hz

Visual Inspection (100%)

Serialization (100%)

Initial Electrical Tests (100%)

High Temperature Stress (100%) 48 Hrs, +125°C

Interim 1 Electrical Tests (100%), PDA 10% All Tests

Static Burn-In I (100%) 24 Hrs, +125°C

Interim 2 Electrical Tests (100%) (Note 1)

Static Burn-In 2 (100%) 24 Hrs, +125°C

Interim 3 Electrical Tests (100%) (Note 1)

Dynamic Burn-In (100%) 240 Hrs, +125°C

Interim 4 Electrical Tests (100%) PDA 5% All Tests, PDA 3% Functional

Fine and Gross Seal (100%) Method 1014

Final Electrical Tests (100%)

Radiographic (100%) Method 2012 (1 View)

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class S)
- Group B (Optional) Method 5005 (Class S)
- Group D (Optional) Method 5005 (Class S)

CSI and/or GSI (Optional)

NOTES:

1. Failures from Interim Electrical Tests 2 and 3 are combined for determining PDA (PDA = 5% All Tests, 3% Functional)

Visual Inspection

Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A **except** as follows:

Use:

3.2.1.1 - Metallization Scratches

3.2.1.2 - Metallization Voids

3.2.1.6 - Metallization Bridging

3.2.1.7 - Metallization Alignment

3.2.3 - Scribing and Die Defects. In addition, semicircular cracks that point away from the active circuit area are acceptable

3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line

3.1.7b - Lifting or Peeling of Glassivation, add Note of 3.2.7b to 3.1.7b

NOTES:

1. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.
2. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.
3. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.
4. SOS Technology Devices
   - Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
   - The 1 mil wire clearance criteria is not applicable
   - Passivation faults are not applicable when a second free flow oxide is used prior to metallization
   - Oxide gate bridge inspection is not applicable
   - Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

Harris - 3Z Product Flow

Radiation Verification (Each Wafer) Method 1019, 100KRADS(Si) Total Dose 2 Samples/Wafer, 0 Reject (3Z Product Flow continues below)

Harris - 3 Product Flow (Without Radiation Verifications)

Internal Visual (100%) Method 2010, Condition B (Modified) (See "Internal Visual Inspection Modified for LSI")

Pre-Seal Bake (100%)

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs, +25°C , No End Point Measurements Required

Temperature Cycling (100%) Method 1010, Condition C

Constant Acceleration (100%) Method 2001, Condition E, Y1, Direction, Centrifuge

Seal:
- Fine (100%) Method 1014, Condition A or B
- Gross (100%) Method 1014, Condition C

Initial Electrical Tests (100%) Per Applicable Device Specification, +25°C

High Temperature Stress (100%) 48 Hrs, +125°C

Interim Electrical Tests 1 (100%) Per Applicable Device Specifications, +25°C PDA 10%, All Tests

Static Burn-In (100%) 160 Hrs, +125°C

Interim Electrical Tests 2 (100%) Per Applicable Device Specifications, +25°C PDA 5%, All Tests, PDA 3% Functional

Final Electrical Tests (100%) Per Applicable Device Specifications, +25°C

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class B)
- Group B (Optional) Method 5005 (Class B)
- Group C (Optional) Method 5005 (Class B)
- Group D (Optional) Method 5005 (Class B)

Internal Visual Inspection Modified for LSI

Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High Magnification Inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required

B. **Metallization Voids** (3.2.1.2) Criteria 3.2.1.1a Metallization Scratches and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed

C. **Metallization Alignment** (3.2.1.7) Diffusion and Passivation Layer(s) Faults (3.2.0)

High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view

D. **Scribing and Die Defects** (3.2.3) in addition:

A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line to be unacceptable

Semicircular cracks that point away from the active circuit area are acceptable

E. **SOS Technology Devices:**

- Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
- The 1 mil wire clearance criteria is not applicable
- Passivation faults are not applicable when a second free flow oxide is used prior to metallization
- Oxide gate bridge inspection is not applicable
- Semicircular cracks not in an active area which start and end at the pellet edge are acceptable