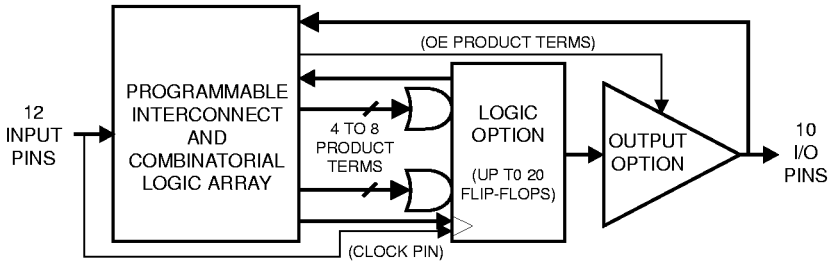
Features

- 3.0V to 3.6V Operating Range
- Advanced, High-speed, Electrically-erasable Programmable Logic Device
  - Superset of 22V10
  - Enhanced Logic Flexibility
  - Architecturally Compatible with ATV750B/BL and ATV750/L Software and Hardware
- Low-power – Edge-sensing "L" Option with 1 mA Standby Current
- Pin-controlled Power-down Features (ATF750LVC)
- D- or T-type Flip-flop
- Product Term or Direct Input Pin Clocking
- 15 ns Maximum Pin-to-pin Delay with 3V Operation
- Highest Density Programmable Logic Available in 24-pin Package
  - Advanced Electrically-erasable Technology
  - Reprogrammable
  - 100% Tested
- Increased Logic Flexibility
  - 42 Array Inputs, 20 Sum Terms and 20 Flip-flops
- Enhanced Output Logic Flexibility
  - All 20 Flip-flops Feed Back Internally
  - 10 Flip-flops are also Available as Outputs
- Programmable Pin-keeper Circuits
- Dual-in-line and Surface Mount Package in Standard Pinouts
- Commercial and Industrial Temperature Ranges
- 20-year Data Retention
- 2000V ESD Protection
- 1000 Erase/Write Cycles

Block Diagram



Description

The ATF750LVC(L)'s are twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations

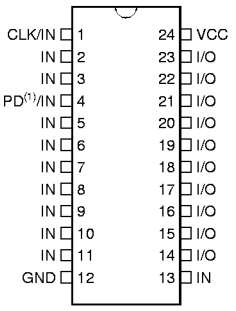
(continued)

Pin Configurations

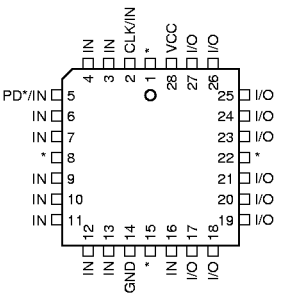
Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	3V Supply
PD(1)	Power-down (active high)

Note: 1. Not available for ATF750LVCL Devices.

DIP/SOIC/TSSOP



PLCC/LCC



Note: 1. Not available for ATF750LVCL devices.

High-speed Complex Programmable Logic Device

ATF750LVC
ATF750LVCL

Advance Information

Rev. 1447A–08/99

translate into more usable gates. High-speed logic and uniform, predictable delays guarantee fast in-system performance. The ATF750LVC(L) is a high-performance CMOS (electrically-erasable) Complex Programmable Logic Device (CPLD) which utilizes Atmel's proven electrically-erasable technology.

Each of the ATF750LVC(L)'s 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. There are two sum terms per output, providing added flexibility. A variable format is used to assign between four to eight product terms per sum term. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

The ATF750LVC(L) is a low-power device with speeds as fast as 20 ns. The ATF750LVC(L) provides the optimum low-power CPLD solution. This device significantly reduces total system power, thereby allowing battery-powered operations.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

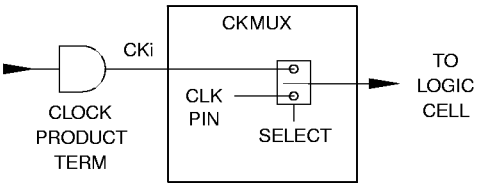
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

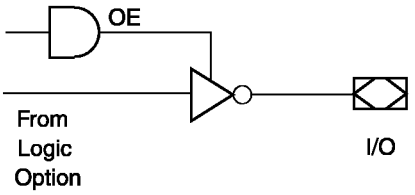
DC and AC Operating Conditions

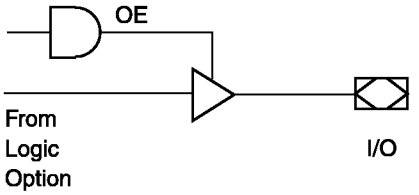
5V Operation	Commercial -7.5, -10, -15	Industrial -10, -15
Operating Temperature	0°C - 70°C (Ambient)	-40°C - +85°C (Ambient)
V_{CC} Power Supply	3.0V ± 3.6V%	3.0V ± 3.6V%

Clock MUX



Output Options





Bus Friendly Pin-keeper Input and I/O's

All Input and I/O pins on the ATF750LVC(L) have programmable "pin-keeper" circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

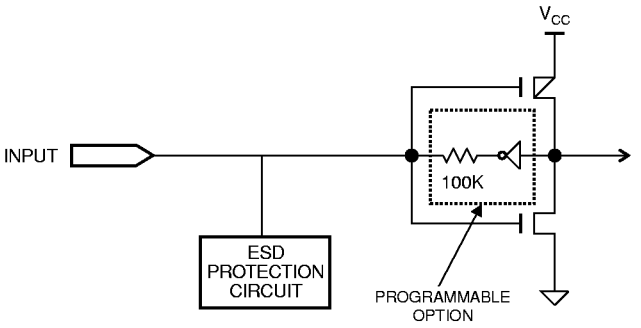
This circuitry prevents unused Input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the software compiler table for more details. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

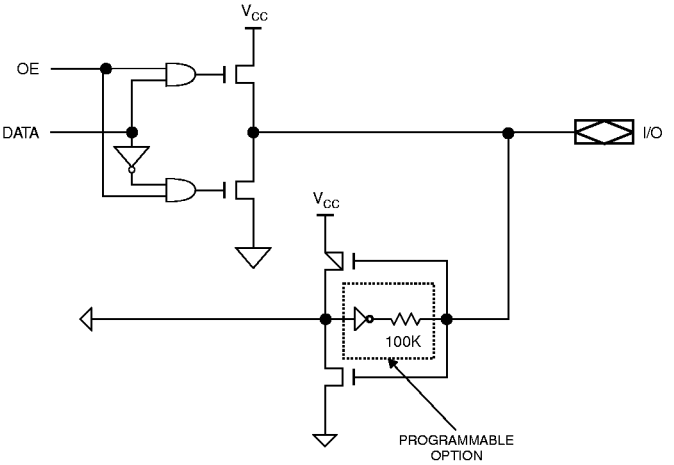
Table 1. Software Compiler Mode Selection

Synario	Wincupl	Pin-keeper Circuit
ATF750LVC	V750C	Disabled
ATF750LVC (PPK)	V750CPPK	Enabled

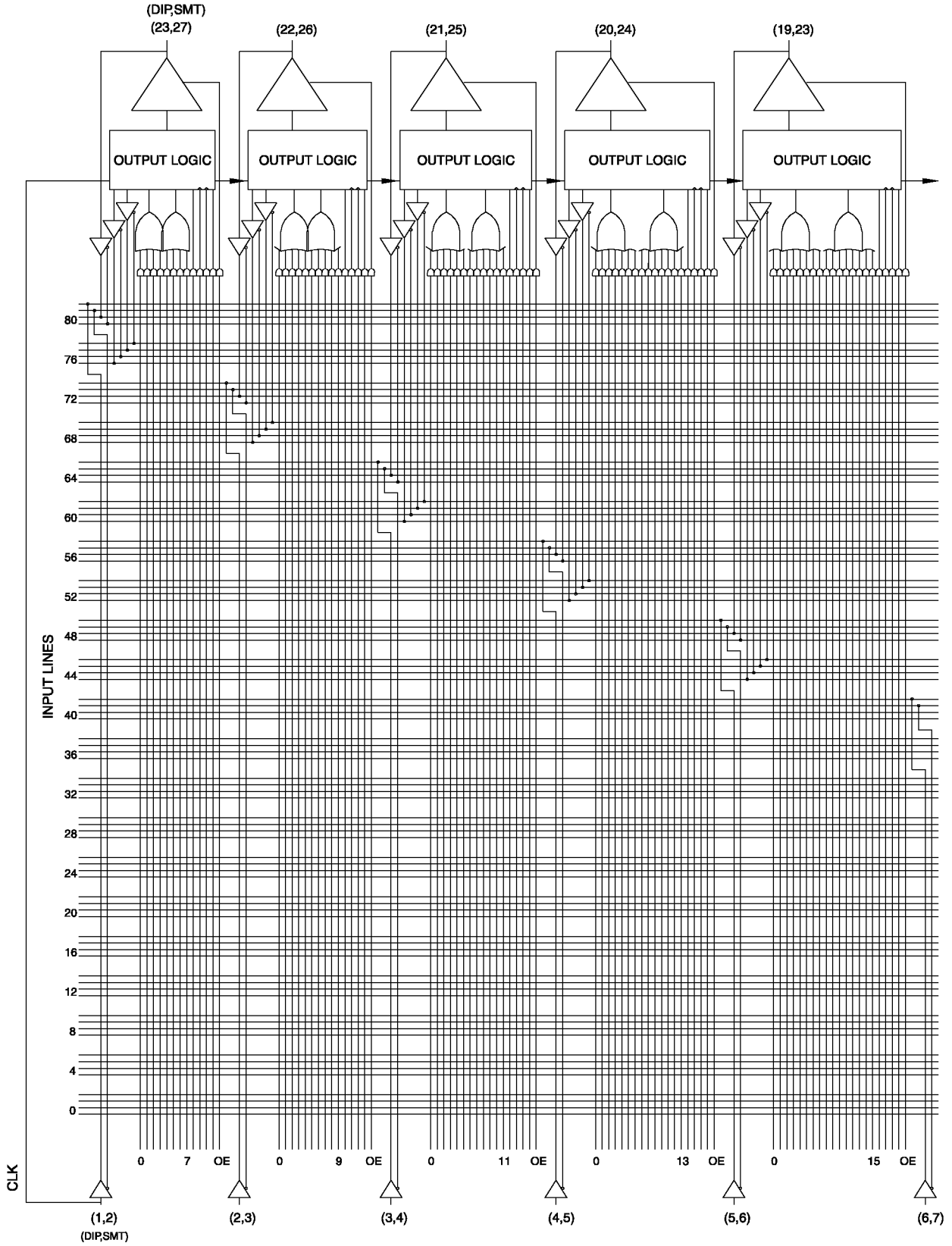
Input Diagram



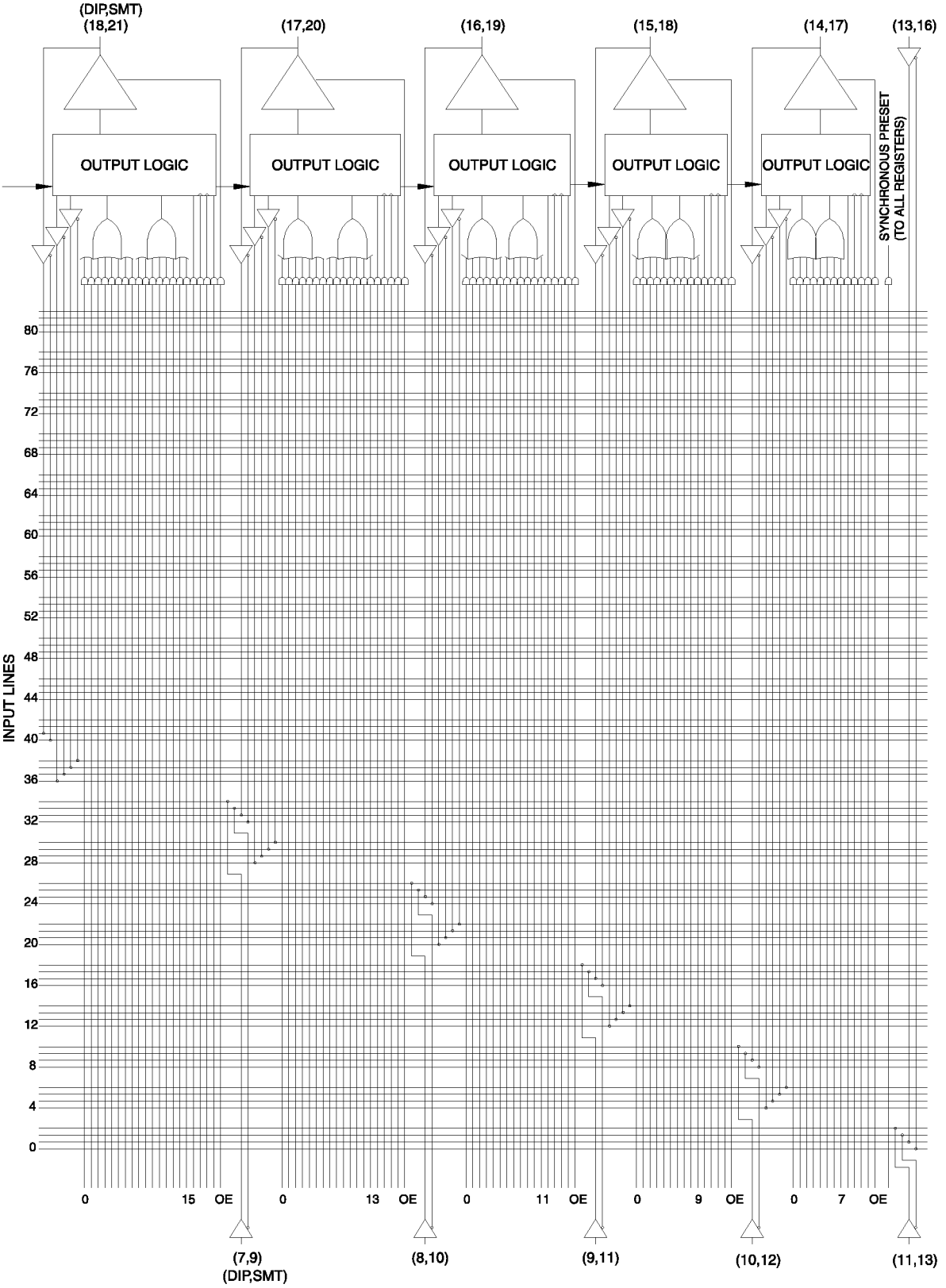
I/O Diagram



Functional Logic Diagram ATF750LVC, Upper Half



Functional Logic Diagram ATF750LVC, Lower Half



Using the ATF750LVC's Many Advanced Features

The ATF750LVC(L)'s advanced flexibility packs more usable gates into 24-pins than any other logic device. The ATF750LVC/L's start with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-type Registers** – Each ATF750LVC(L) flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Selectable Asynchronous Clocks** – Each of the ATF750LVC(L)'s flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Full Bank of Ten More Registers** – The ATF750LVC(L) provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.
- **Independent I/O Pin and Feedback Paths** – Each I/O pin on the ATF750LVC(L) has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

Superset Features

The ATF750LVC(L) support enhanced features not available on the ATV750/L and ATV750B/L devices. These are:

- Programmable pin-keeper circuits. Each input and I/O pin on this ATF150C has pin-keeper circuits. These circuits are weak which hold the state of pin before it is tri-stated. Pin-keeper circuits can easily be overdriven by an input or by the output pins on the device. The ATF750LVC(L) has a user-programmable option to enable or disable these circuits.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATF750LVC(L). The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF750LVC(L) fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

ATF750LVC Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	10	55	ATF750LVC-15JC	28J	Commercial
			ATF750LVC-15PC	24P3	(0°C to 70°C)
			ATF750LVC-15SC	24S	
			ATF750LVC-15XC	24X	
			ATF750LVC-15JI	28J	Industrial
			ATF750LVC-15PI	24P3	(-40°C to 85°C)
			ATF750LVC-15SI	24S	

Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP)

ATFV750CL Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	10	44	ATF750LVCL-20JC ATF750LVCL-20PC ATF750LVCL-20SC ATF750LVCL-20XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF750LVCL-20JI ATF750LVCL-20PI ATF750LVCL-20SI	28J 24P3 24S	Industrial (-40°C to 85°C)

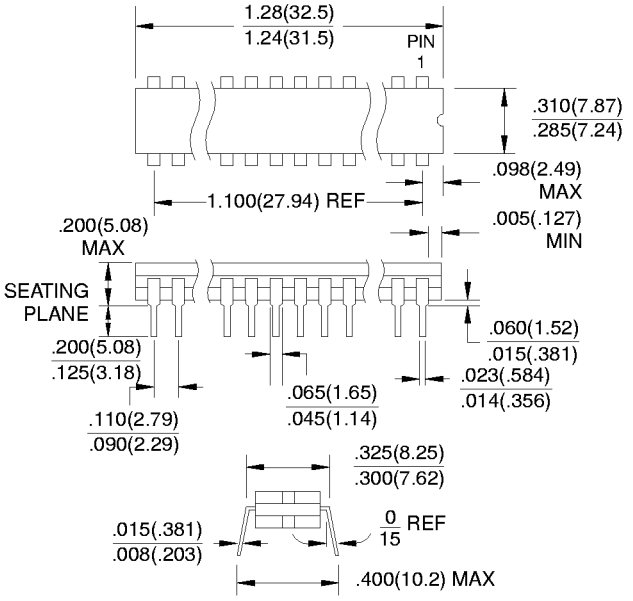
Using “C” Product for Industrial

To use commercial product for industrial ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

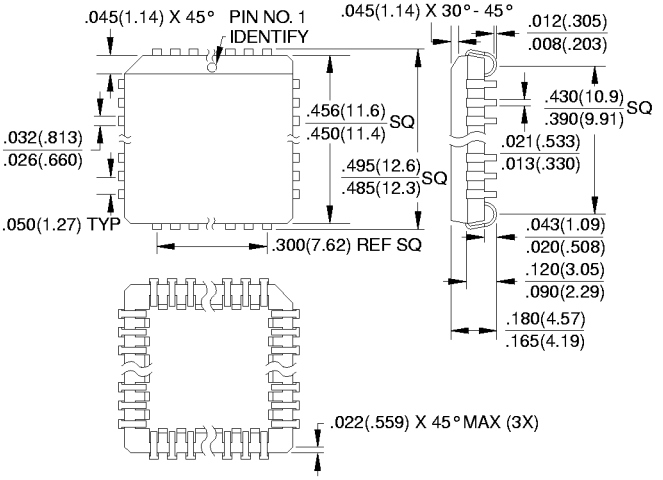
Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP)

Packaging Information

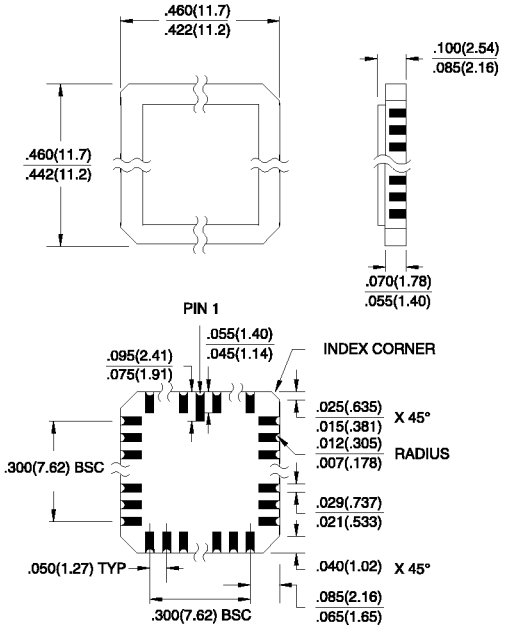
24D3, 24-lead, 0.300" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A



28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB

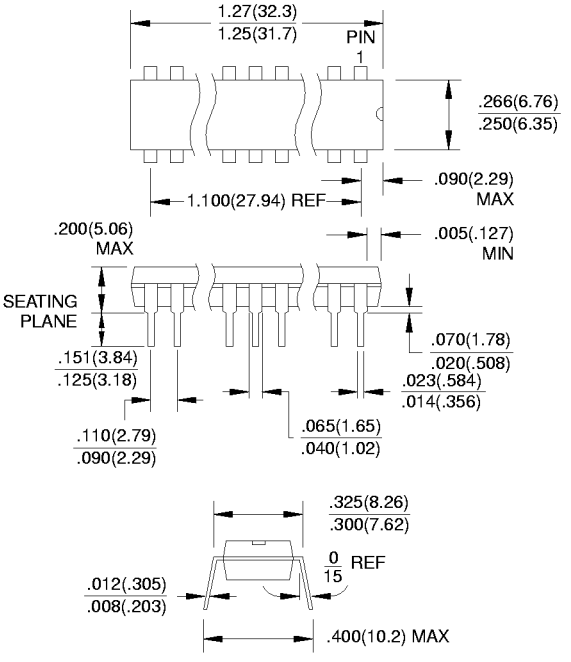


28L, 28-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



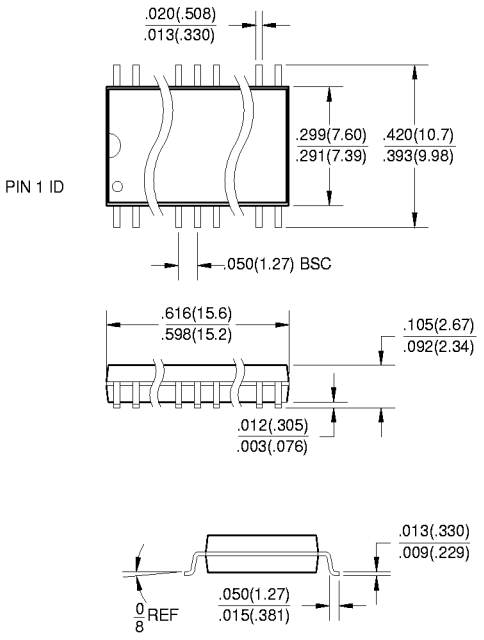
*Ceramic lid standard unless specified.

24P3, 24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF

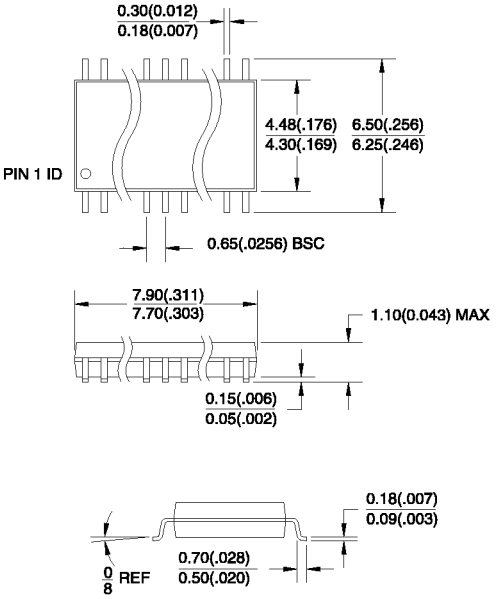


Packaging Information

24S, 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



24X, 24-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

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