1

Features

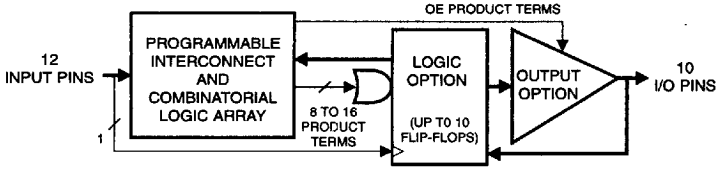
- **Low Voltage Programmable Logic Device**
  - **Wide Power Supply Range - 3.0 V to 5.5 V**
  - **Ideal for Battery Powered Systems**
- **High Speed Operation**
  - **20 ns max Propagation Delay at V_{CC} = 3.0 V**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Familiar 22V10 Logic Architecture**
- **Low Power 3-Volt CMOS Operation**

	AT22LV10L	AT22LV10	
Temp	Com./Mil.	Com./Mil.	
I_{CC} (mA)	4 / 5	35 / 45	V_{CC} = 3.6 V

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Dual-In-Line and Surface Mount Packages**

Low Voltage UV Erasable Programmable Logic Device

Logic Diagram



Description

The AT22LV10 and AT22LV10L are low voltage compatible CMOS high performance Programmable Logic Devices (PLDs). Speeds down to 20 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0 V to 5.5 V range. All pins offer a low ±10 µA leakage.

The AT22LV10L provides the optimum low power CMOS PLD solution, with low DC power (1 mA typical at V_{CC} = 3.3 V) and full CMOS output levels. The AT22LV10L significantly reduces total system power, allowing battery powered operation.

Full CMOS output levels help reduce power in many other system components.

The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

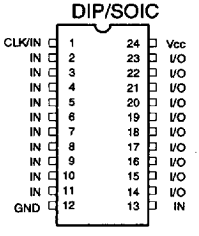
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

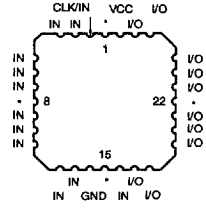
Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
•	No Internal Connection
VCC	3.0 V to 5.5 V Supply

DIP/SOIC



PLCC



0190B

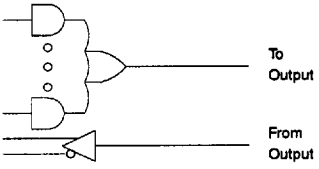
Absolute Maximum Ratings*

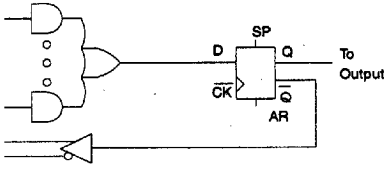
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

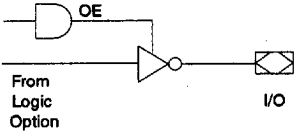
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum pin voltage is V_{CC}+0.75 V dc which may overshoot to V_{CC} +2.0 V for pulses of less than 20 ns.

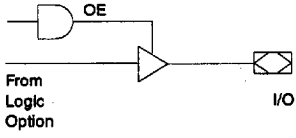
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22LV10/L -20, -25, -30	Industrial AT22LV10/L -20, -25, -30	Military AT22LV10/L -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = 3.6 V / 5.5 V, V_{IN} = GND, Outputs Open	AT22LV10	Com.		20/50	35/90	mA
				Ind., Mil.		20/50	45/100	mA
			AT22LV10L(2)	Com.		1/2	4/12	mA
				Ind., Mil.		1/2	5/15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open	AT22LV10L(2)	Com.		1.0		mA/MHz
				Ind., Mil.		1.0		mA/MHz
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V			-0.6		0.8	V
V_{IL2}	Input Low Voltage	3.0 V ≤ V_{CC} < 4.5 V			-0.6		0.6	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage V_{IN} = V_{IH} or V_{IL}	V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 8 mA / 6 mA			0.5	V
		V_{CC} = 4.5 V	Com.,Ind./Mil.	I_{OL} = 16 mA / 12 mA			0.5	V
		V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 6 mA / 4 mA			0.35	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 3.0 V / 4.5 V	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -0.4 mA / -4.0 mA		2.4			V

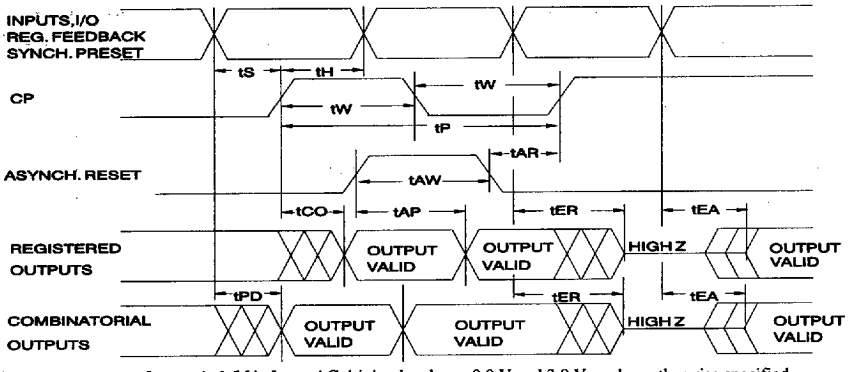
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics for the AT22LV10

		AT22LV10-20			AT22LV10-25			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		12	20		15	25	ns
t_{EA}	Input to Output Enable			20		15	25	ns
t_{ER}	Input to Output Disable			20		15	25	ns
t_{CF}	Clock to Feedback	0	4	9	0	5	9	ns
t_{CO}	Clock to Output	0	8	14	0	10	17	ns
t_S	Input or Feedback Setup Time	10	6		12	7		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	10			12			ns
t_W	Clock Width	5			6			ns
F_{MAX}	External Feedback 1/(t_S+t_{CO})			41.6			34.5	MHz
	Internal Feedback 1/(t_S + t_{CF})			52.6			47.6	MHz
	No Feedback 1/(t_P)			100.0			83.3	MHz
t_{AW}	Asynchronous Reset Width	20	12		25	15		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	20	12		25	15		ns

A.C. Waveforms [1]

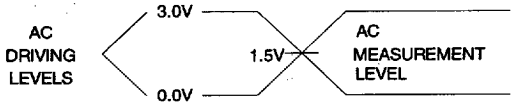


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics for the AT22LV10L

Symbol	Parameter	AT22LV10L-25			AT22LV10L-30			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		15	25		20	30	ns
t_{EA}	Input to Output Enable		15	25		20	30	ns
t_{ER}	Input to Output Disable		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	5	9	0	6	10	ns
t_{CO}	Clock to Output	0	10	14	0	12	17	ns
t_{SF}	Feedback Setup Time	12	7		15	10		ns
t_S	Input Setup Time	17	15		20	15		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	12			14			ns
t_W	Clock Width	6			7			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			32.2			27.0	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$			47.6			40.0	MHz
	No Feedback $1/(t_P)$			83.3			71.4	MHz
t_{AW}	Asynchronous Reset Width	25	15		30	18		ns
t_{AR}	Asynchronous Reset Recovery Time	25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		18	28		20	30	ns

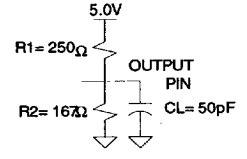
Input Test Waveforms and Measurement Levels



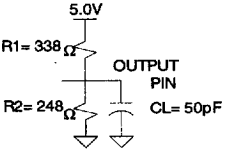
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

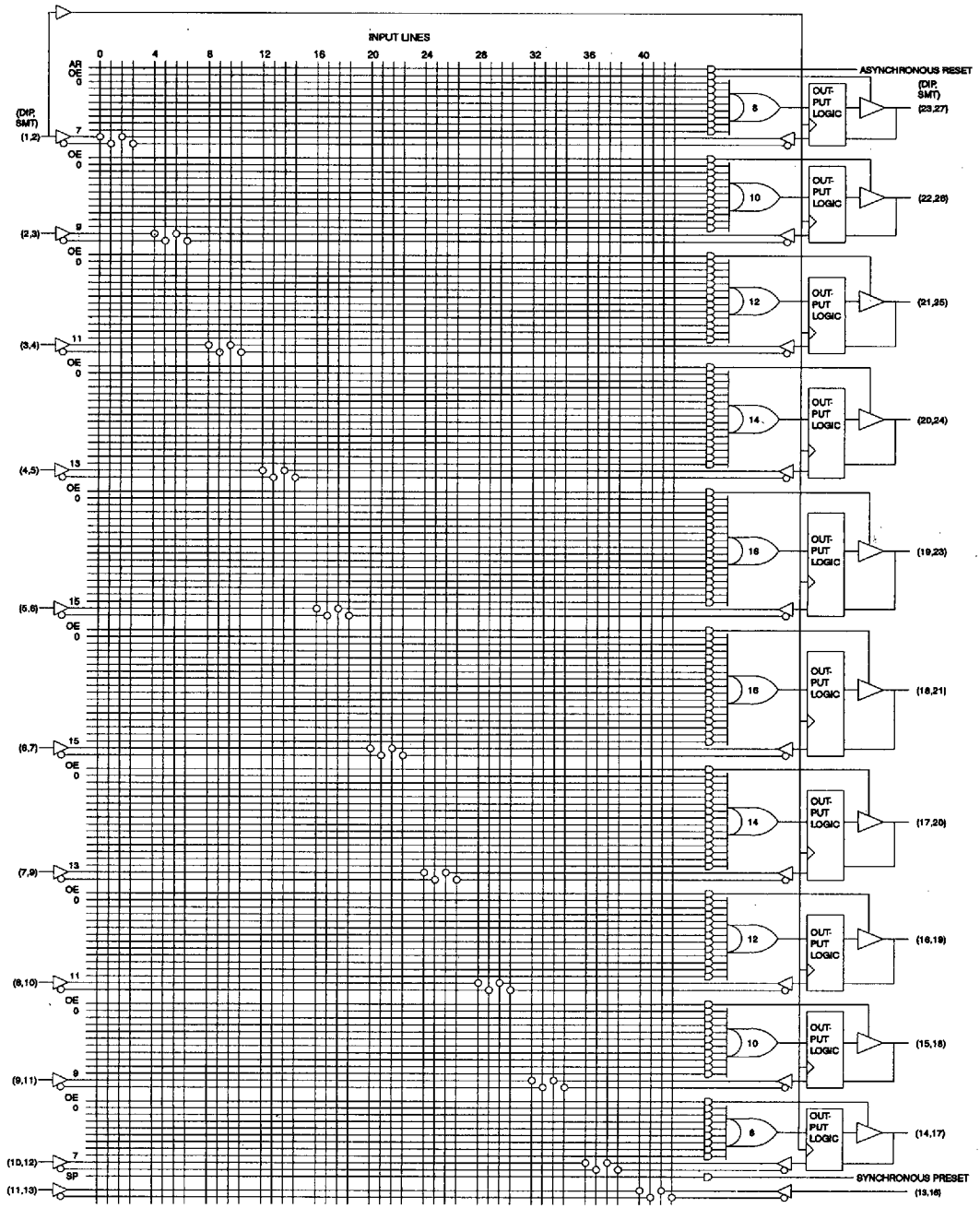
Commercial



Military



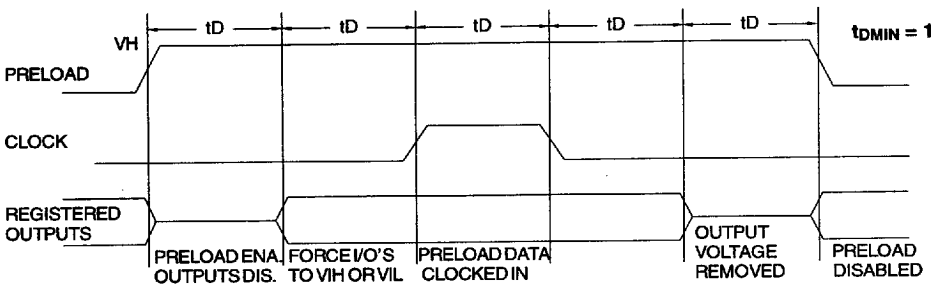
Functional Logic Diagram AT22LV10/L



Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5-V to 13-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during preload cycle	Register state after cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

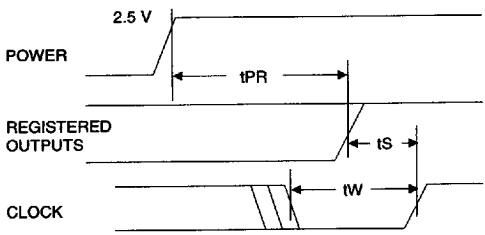
The registers in the AT22LV10 and AT22LV10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 2.5 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

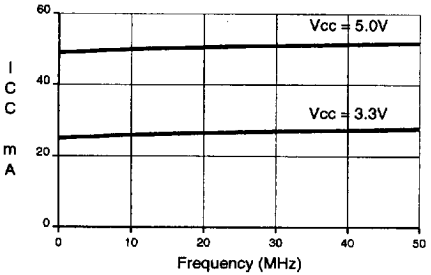
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

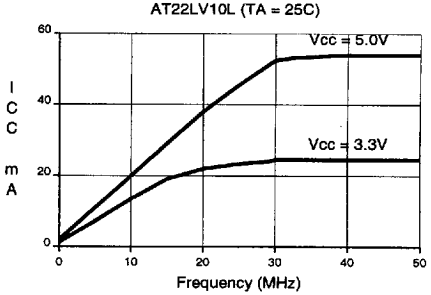
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10 (TA = 25C)

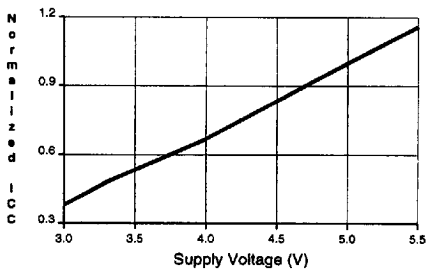


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10L (TA = 25C)

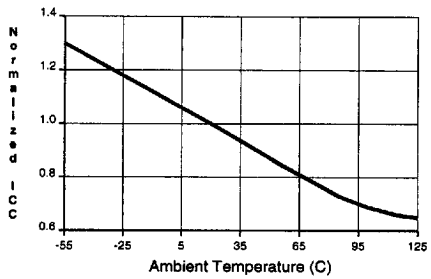


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



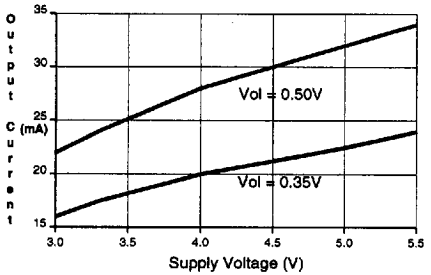
NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz



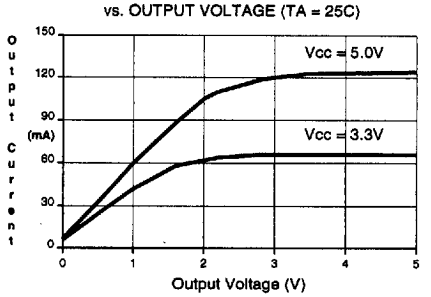
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



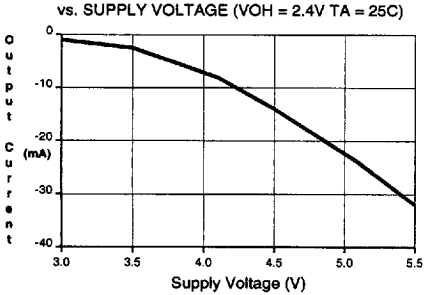
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C)



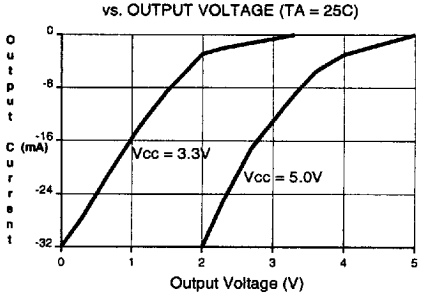
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V TA = 25C)

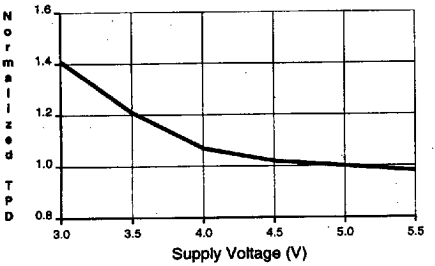


OUTPUT SOURCE CURRENT

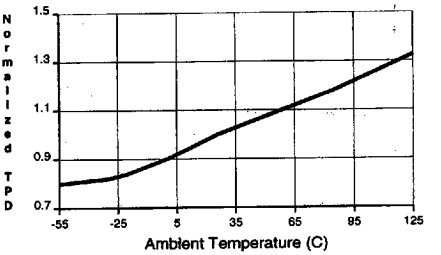
vs. OUTPUT VOLTAGE (TA = 25C)



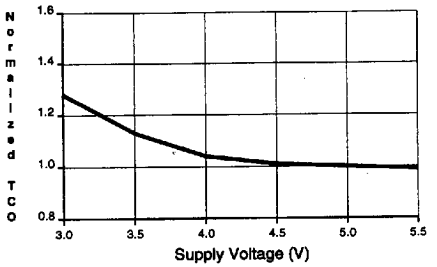
NORMALIZED TPD vs. SUPPLY VOLTAGE



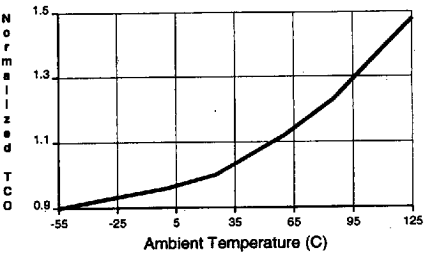
NORMALIZED TPD vs. TEMPERATURE



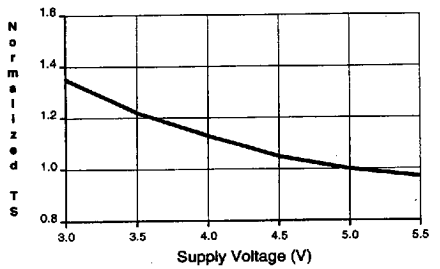
NORMALIZED TCO vs. SUPPLY VOLTAGE



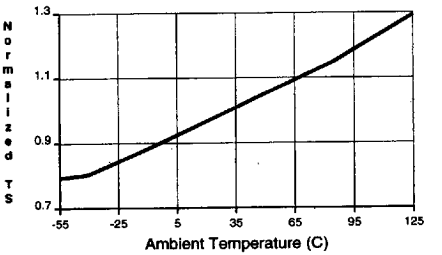
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

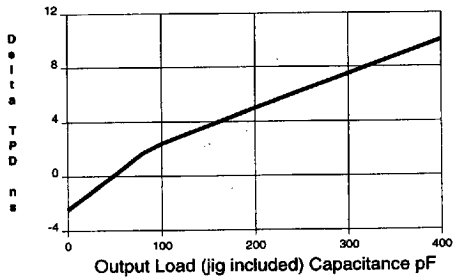


NORMALIZED TS vs. TEMPERATURE



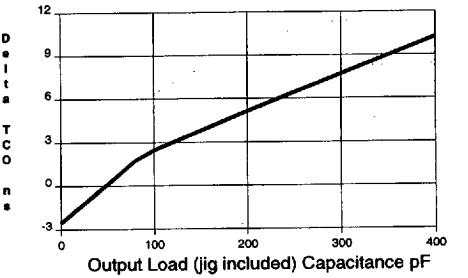
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	10	14	AT22LV10-20DC AT22LV10-20GC AT22LV10-20JC AT22LV10-20PC AT22LV10-20SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-20DI AT22LV10-20GI AT22LV10-20JI AT22LV10-20PI AT22LV10-20SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	12	17	AT22LV10-25DC AT22LV10-25GC AT22LV10-25JC AT22LV10-25PC AT22LV10-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-25DI AT22LV10-25GI AT22LV10-25JI AT22LV10-25PI AT22LV10-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22LV10-25DM AT22LV10-25GM AT22LV10-25LM AT22LV10-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22LV10-25DM/883 AT22LV10-25GM/883 AT22LV10-25LM/883 AT22LV10-25NM/883	24DW3 24D3 28LW 28L	Military/883D (-55°C to 125°C) Class B, Fully Compliant
25	12	17	5962-93245 01M LA 5962-93245 01M 3X	24DW3 28LW	Military/883D (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	17	14	AT22LV10L-25DC AT22LV10L-25GC AT22LV10L-25JC AT22LV10L-25PC AT22LV10L-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-25DI AT22LV10L-25GI AT22LV10L-25JI AT22LV10L-25PI AT22LV10L-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
30	20	17	AT22LV10L-30DC AT22LV10L-30GC AT22LV10L-30JC AT22LV10L-30PC AT22LV10L-30SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-30DI AT22LV10L-30GI AT22LV10L-30JI AT22LV10L-30PI AT22LV10L-30SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22LV10L-30DM AT22LV10L-30GM AT22LV10L-30LM AT22LV10L-30NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22LV10L-30DM/883 AT22LV10L-30GM/883 AT22LV10L-30LM/883 AT22LV10L-30NM/883	24DW3 24D3 28LW 28L	Military/883D (-55°C to 125°C) Class B, Fully Compliant
30	20	17	5962-93245 03M LA 5962-93245 03M LX	24DW3 28LW	Military/883D (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

	Package Type
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)