010511

Am9341-Am54/74181

Four Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics:

- Provides 16 arithmetic operations including add, subtract, double and compare.
- Provides ALL 16 possible logic operations of two variables in typically 19 ns.
- Typical add time for 4 bits of only 19 ns, and typical carry time of 12 ns.
- Full look-ahead for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

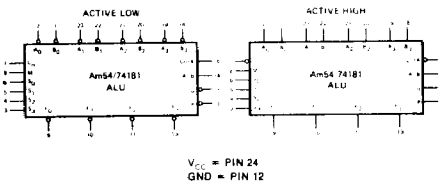
The Am54/74181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

An open collector A = B output is provided so that equivalence of two parallel words can be made by connecting A = B outputs of several ALU's together.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate (P) and carry generate (G) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am54/74181 ALU's and one Am 54/74182 look-ahead generator is only 31 ns.

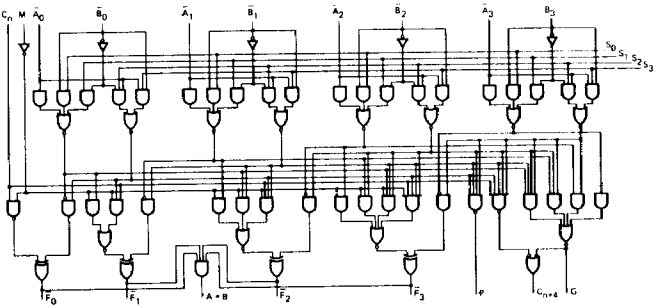
For systems where ultra high-speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple-block arithmetic operations. The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode. The interconnection patterns are identical for both cases.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

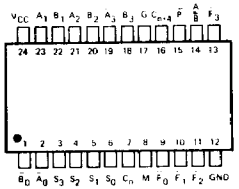


Am54/74181-Am9341 ORDERING INFORMATION

Package Type	Temperature Range	54/74181 Order Number	9341 Order Number
Molded DIP	0°C to +75°C	SN74181N	Am9341C
Hermetic DIP	0°C to +75°C	SN74181J	U6N934159X
Hermetic DIP	−55°C to +125°C	SN54181J	U6N934151X
Hermetic Flat Pak	−55°C to +125°C	SN54181W	U4M934151X
Dice		SN54181D	UXX9341XXD

NOTE: The DICE supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RA **S** (Above which the useful life may be impaired)

Storage Temper...	
Temperature (Amb...) Under Bias	−65°C to +150°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−55°C to +125°C
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +7 V
DC Input Voltage	−0.5 V to +V_{CC} max.
Output Current, Into Outputs	−0.5 V to +5.5 V
DC Input Current	30 mA
	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am74181 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54181 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Except A=B Output)		V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{OH}	Output HIGH Current for A=B Output		V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	μA
I_{IL} (Note 3)	Input LOW Current	M	V_{CC} = MAX., V_{IN} = 0.5V				−1.6	mA
		$\overline{A}_i$ or $\overline{B}_i$					−4.8	
		S_i					−6.4	
		C_n					−8	
I_{IH} (Note 3)	Input HIGH Current	M	V_{CC} = MAX., V_{IN} = 2.7V				40	μA
		$\overline{A}_i$ or $\overline{B}_i$					120	
		S_i					160	
		C_n					200	
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4) (Except A=B Output)		V_{CC} = MAX.	Am54	−20		−55	mA
				Am74	−18		−57	
I_{CC}	Power Supply Current		V_{CC} = MAX.	Note 5 A Am54		88	127	mA
				Am74		88	140	
				Note 5 B Am54		94	135	
				Am74		94	150	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured under two conditions.
   A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open
   B. S_i, M at 4.5V; all other inputs grounded; outputs open.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{A}_i$ Active LOW Data A inputs i = 0, 1, 2, 3.

A = B Open collector output. This output can be 'AND tied' to other A = B outputs to form equivalence over complete word length.

$\overline{B}_i$ Active LOW Data B inputs i = 0, 1, 2, 3.

C_n Active HIGH Carry in to nth ALU bit.

C_{n+4} Active HIGH Carry Out of n+4th ALU bit.

$\overline{F}_i$ Active LOW Data Outputs of ALU i = 0, 1, 2, 3.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{G}$ Active LOW carry generate output for use in multi-level look-ahead schemes.

M Mode input controls whether arithmetic or logic operation.

$\overline{P}$ Active LOW carry propagate output for use in multi-level look ahead schemes.

S_i Control inputs determine the arithmetic or logic function obeyed i = 0, 1, 2, 3.

Unit Load One T^2L gate input load. In the HIGH state it is equal 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 3.

V_{IL} Maximum logic LOW input voltage. Refer to figure 3.

V_{OH} Minimum logic HIGH output voltage with output HIGH curr I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW curr I_{OL} into output.

TEST TABLES

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_3 = S_2 = 4.5\ V$, $S_0 = S_1 = M = 0\ V$

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$F_i\ (i \geq 1)$	1
t_{pd-}							
t_{pd+}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$F_i\ (i \geq 1)$	2
t_{pd-}							
t_{pd+}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	1
t_{pd-}							
t_{pd+}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	2
t_{pd-}							
t_{pd+}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd-}							
t_{pd+}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{pd-}							
t_{pd+}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{pd-}							
t_{pd+}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{pd-}							
t_{pd+}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$	1
t_{pd-}							
t_{pd+}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$	2
t_{pd-}							
t_{pd+}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{pd-}							
t_{pd+}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{pd-}							
t_{pd+}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}	1
t_{pd-}							

Table 1

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_3 = S_2 = 4.5\ V$, $S_0 = S_1 = M = 0\ V$

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+}	A	B	None	Remaining A and B	C	$F_i\ (i \geq 1)$	1
t_{pd-}							
t_{pd+}	B	A	None	Remaining A and B	C	$F_i\ (i \geq 1)$	1
t_{pd-}							
t_{pd+}	$\overline{A}$	$\overline{B}$	None	C	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	1
t_{pd-}							
t_{pd+}	$\overline{B}$	$\overline{A}$	None	C	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	1
t_{pd-}							
t_{pd+}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C	$\overline{P}$	1
t_{pd-}							
t_{pd+}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C	$\overline{P}$	1
t_{pd-}							
t_{pd+}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C	$\overline{G}$	1
t_{pd-}							
t_{pd+}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C	$\overline{G}$	1
t_{pd-}							
t_{pd+}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C	C_{i+1}	2
t_{pd-}							
t_{pd+}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C	C_{i+1}	2
t_{pd-}							
t_{pd+}	C	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{i+1}	1
t_{pd-}							

Table 2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S = S_3 = M = 4.5\ V$, $S_2 = S_1 = 0\ V$

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C	$\overline{F}$	1
t_{pd-}							
t_{pd+}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C	$\overline{F}$	1
t_{pd-}							

Table 3

SWITCHING CHARACTERISTICS $V_{CC} = 5\ V$, $T_A = 25°C$, $N = 10$ ($C_L = 15\ pF$, $R_1 = 400\ \Omega$)

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions (See also Tables 1, 2, 3)	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}	1 and 2	M = 0 V (SUM or DIFF mode)	12	18		ns
t_{pd-}					13	19		
t_{pd+}	C_n	$\overline{F}_i$			13	19		ns
t_{pd-}					12	18		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		M = 0 V, $S_0 = S_1 = 4.5$ V, $S_2 = S_3 = 0$ V (SUM mode)	13	19		ns
t_{pd-}					13	19		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		M = 0 V, $S_0 = S_2 = 0$ V, $S_1 = S_3 = 4.5$ V (DIFF mode)	17	25		ns
t_{pd-}					17	25		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		M = 0 V, $S_0 = S_1 = 4.5$ V $S_2 = S_3 = 0$ V (SUM mode)	13	19		ns
t_{pd-}					15	22		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		M = 0 V, $S_0 = S_1 = 0$ V, $S_2 = S_3 = 4.5$ V (DIFF mode)	17	25		ns
t_{pd-}					17	25		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i\ (i \geq 1)$		M = 0 V, $S_0 = S_1 = 4.5$ V $S_2 = S_3 = 0$ V (SUM mode)	18	27		ns
t_{pd-}					12	18		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i\ (i \geq 1)$		M = 0 V, $S_0 = S_2 = 0$ V, $S_1 = S_3 = 4.5$ V (DIFF mode)	20	30		ns
t_{pd-}					16	24		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		M = 0 V, $S_0 = S_1 = 4.5$ V, $S_2 = S_3 = 0$ V (SUM mode)	19	29		ns
t_{pd-}					20	30		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		M = 0 V, $S_0 = S_2 = 0$ V, $S_1 = S_3 = 4.5$ V (DIFF mode)	24	36		ns
t_{pd-}					21	32		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$		M = 4.5 V (LOGIC mode)	19	29		ns
t_{pd-}					19	29		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		M = 0 V, $S_0 = S_1 = 4.5$ V, $S_2 = S_3 = 0$ V (SUM moue)	17	25		ns
t_{pd-}					20	30		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		M = 0 V, $S_0 = S_2 = 0$ V, $S_1 = S_3 = 4.5$ V (DIFF mode)	21	32		ns
t_{pd-}					20	30		
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	A = B		M = 0 V, $S_0 = S_1 = 0$ V, $S_2 = S_3 = 4.5$ V (DIFF mode)	25	37		ns
t_{pd-}					21	32		

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

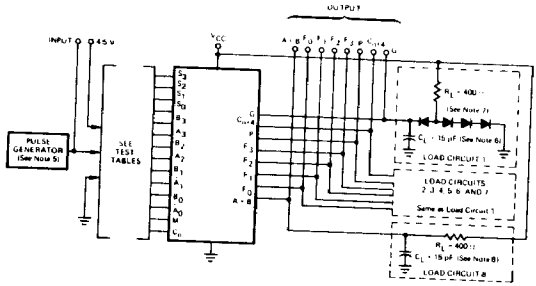


Figure 1

Note 5. The pulse generator has the following characteristics: frequency = 1 MHz, $Z_{out} \approx 50\ \Omega$.
6. C_L includes probe and jig capacitance.
7. All diodes are 1N3064.

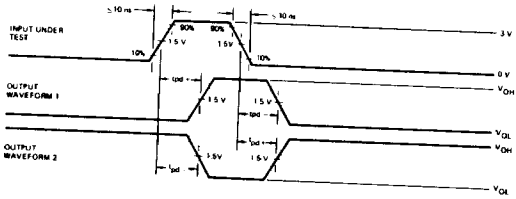
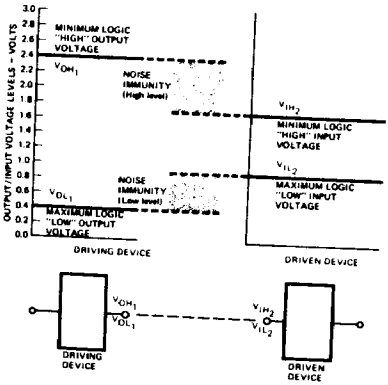


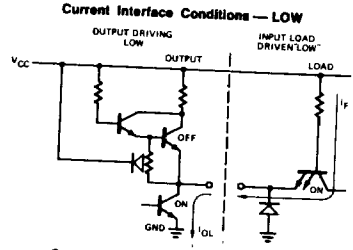
Figure 2

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

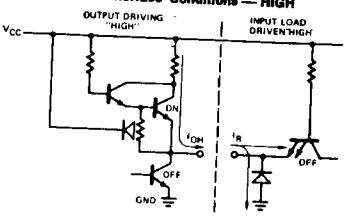


Figure 3

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table 4

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement arithmetic requires an end around carry.
4. Subtraction in 2's complement arithmetic requires a carry in (C_n = HIGH) active LOW case, ($\overline{C}_n$ = LOW) active HIGH case.

Am54/74181 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive Output HIGH	Output LOW
$\overline{B}_0$	1	3	—	—
$\overline{A}_0$	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
$\overline{F}_0$	9	—	20	10
$\overline{F}_1$	10	—	20	10
$\overline{F}_2$	11	—	20	10
GND	12	—	—	—
$\overline{F}_3$	13	—	20	10
A = B	14	—	O/C	10
$\overline{P}$	15	—	20	10
C_{n+4}	16	—	20	10
$\overline{G}$	17	—	20	10
$\overline{B}_3$	18	3	—	—
$\overline{A}_3$	19	3	—	—
$\overline{B}_2$	20	3	—	—
$\overline{A}_2$	21	3	—	—
$\overline{B}_1$	22	3	—	—
$\overline{A}_1$	23	3	—	—
V_{CC}	24	—	—	—

O/C = Open Collector

A unit load is defined as 40μA at 2.4V and 1.6mA at 0.4V.

Table 5

OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0 S_1 S_2 S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L L L L	A minus 1	$\overline{A}$	A	$\overline{A}$
H L L L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L H L L	$A\overline{B}$ minus 1	$\overline{A}+B$	$A+\overline{B}$	$\overline{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus [A + $\overline{B}$]	$\overline{A+B}$	A plus $A\overline{B}$	$\overline{A\overline{B}}$
H L H L	AB plus [A + $\overline{B}$]	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L H H L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$
H H H L	A + $\overline{B}$	$A+\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L L L H	A plus [A + B]	$\overline{AB}$	A plus AB	$\overline{A}+B$
H L L H	A plus B	$A \oplus B$	A plus B	$\overline{A \oplus B}$
L H L H	$A\overline{B}$ plus [A + B]	B	AB plus [A + $\overline{B}$]	B
H H L H	A + B	A + B	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus $A\overline{B}$	$A\overline{B}$	A plus [A + B]	$A+\overline{B}$
L H H H	A plus $A\overline{B}$	AB	A plus [A + $\overline{B}$]	A + B
H H H H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

Table 6

Am54/74181 APPLICATIONS

16-Bit ALU Ripple Carry

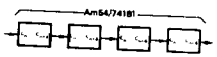


Figure 4

32-Bit ALU Two-Level Look-Ahead Over 16-Bit Groups

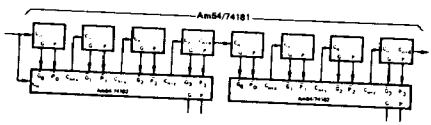


Figure 5

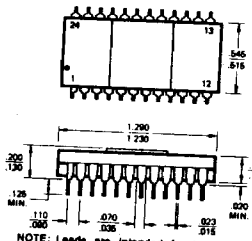
Typical addition times for various configurations are given in the table below. Subtraction times are approximately 5 ns longer.

TYPICAL ADDITION TIMES

No. of Bits	Total Addition Time (ns)	Add Time Per Bit (ns)	Package Count	
			Am 54/74181	Am 54/74182
4	19	4.8	1	
8	31	3.9	2	
12	43	3.6	3	
12	31	2.6	3	1
16	55	3.5	4	
16	31	2.0	4	1
32	103	3.2	8	
32	79	2.5	8	1
32	56	1.8	8	2
48	151	3.2	12	
48	127	2.6	12	1
48	104	2.2	12	2
48	81	1.7	12	3
48	57	1.2	12	4
64	199	3.1	16	
64	152	2.4	16	2
64	129	2.0	16	3
64	106	1.7	16	4
64	57	0.9	16	5

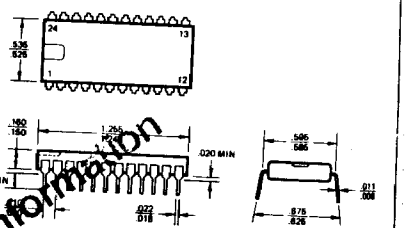
Table 7

PHYSICAL DIMENSIONS
Hermetic Dual-In-Line

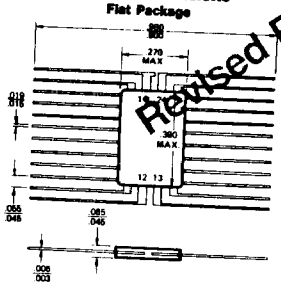


NOTE: Leads are intended for insertion in hole rows on .600" centers and are misaligned to facilitate insertion.

PHYSICAL DIMENSIONS
Molded Dual-In-Line

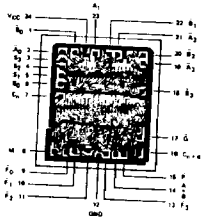


PHYSICAL DIMENSIONS
Flat Package



NOTE: Leads are gold plated kovar.

Metallization and Pad Layout
90 x 102 Mils



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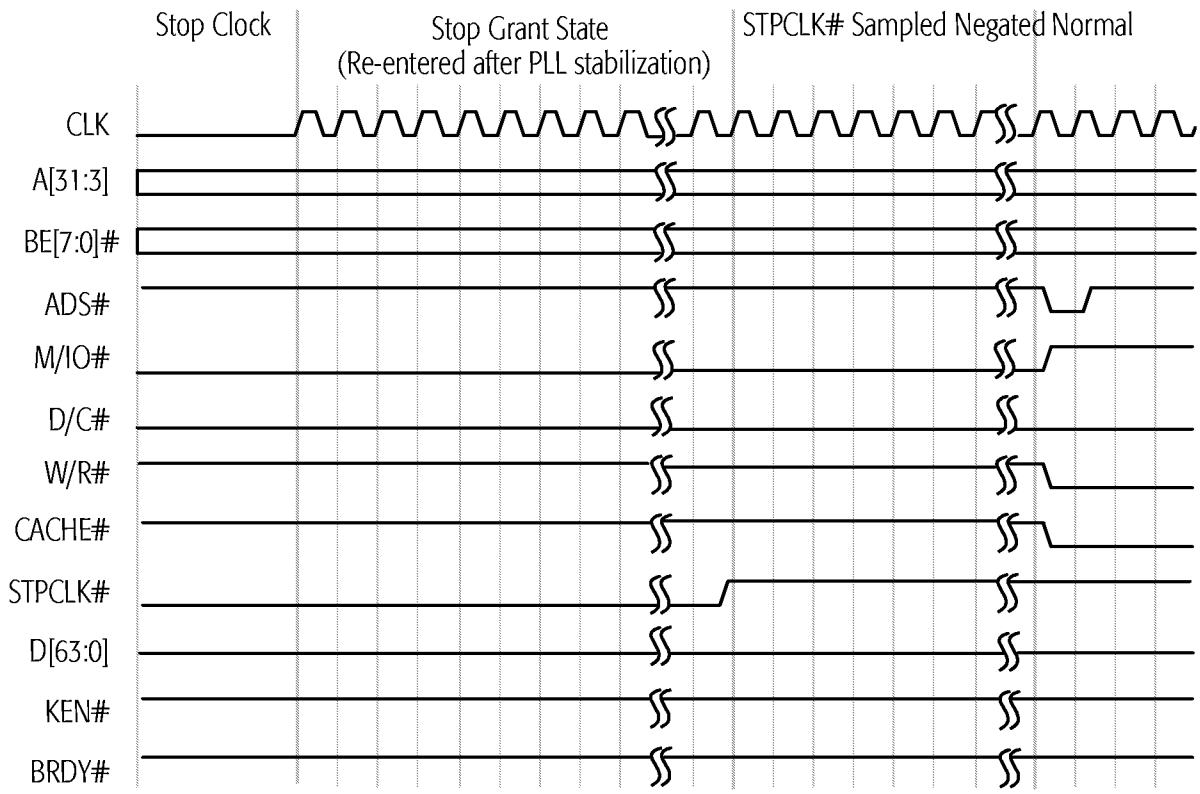

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

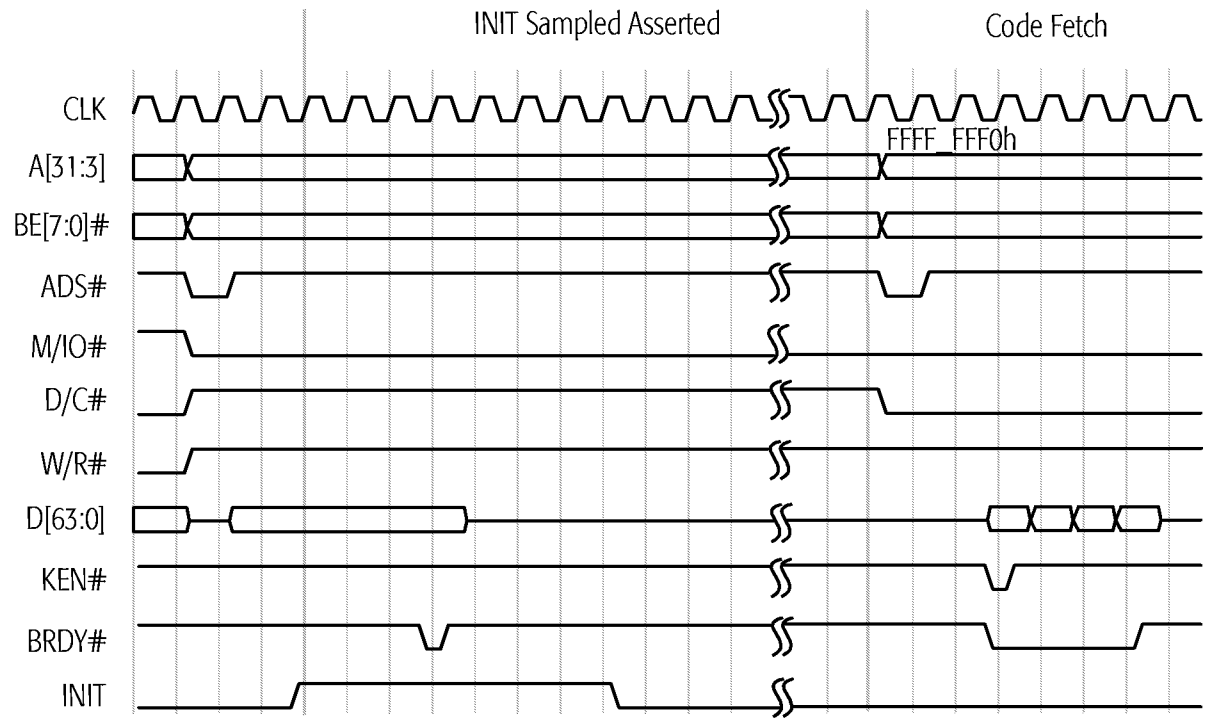

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.