TMS320C6713
FLOATING-POINT DIGITAL SIGNAL PROCESSOR

SPRS186E − DECEMBER 2001 − REVISED JULY 2003

- **Highest-Performance Floating-Point Digital Signal Processor (DSP): TMS320C6713**
  - **Eight 32-Bit Instructions/Cycle**
  - **32/64-Bit Data Word**
  - **225-, 200-MHz (GDP), and 200-, 167-MHz (PYP) Clock Rates**
  - **4.4-, 5-, 6-Instruction Cycle Times**
  - **1800 /1350 , 1600 /1200 , and 1336 /1000 MIPS /MFLOPS**
  - **Rich Peripheral Set, Optimized for Audio**
  - **Highly Optimized C/C++ Compiler**
- **VelociTI™ Advanced Very Long Instruction Word (VLIW) TMS320C67x™ DSP Core**
  - **Eight Independent Functional Units:**
    - **Two ALUs (Fixed-Point)**
    - **Four ALUs (Floating- and Fixed-Point)**
    - **Two Multipliers (Floating- and Fixed-Point)**
  - **Load-Store Architecture With 32 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Native Instructions for IEEE 754**
    - **Single- and Double-Precision**
  - **Byte-Addressable (8-, 16-, 32-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Saturation; Bit-Field Extract, Set, Clear; Bit-Counting; Normalization**
- **L1/L2 Memory Architecture**
  - **4K-Byte L1P Program Cache (Direct-Mapped)**
  - **4K-Byte L1D Data Cache (2-Way)**
  - **256K-Byte L2 Memory Total: 64K-Byte L2 Unified Cache/Mapped RAM, and 192K-Byte Additional L2 Mapped RAM**
- **Device Configuration**
  - **Boot Mode: HPI, 8-, 16-, 32-Bit ROM Boot**
  - **Endianness: Little Endian, Big Endian**
- **32-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to SRAM, EPROM, Flash, SBSRAM, and SDRAM**
  - **512M-Byte Total Addressable External Memory Space**
- **Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)**
- **16-Bit Host-Port Interface (HPI)**
- **Two Multichannel Audio Serial Ports (McASPs)**
  - **Two Independent Clock Zones Each (1 TX and 1 RX)**
  - **Eight Serial Data Pins Per Port: Individually Assignable to any of the Clock Zones**
  - **Each Clock Zone Includes:**
    - **Programmable Clock Generator**
    - **Programmable Frame Sync Generator**
    - **TDM Streams From 2-32 Time Slots**
    - **Support for Slot Size: 8, 12, 16, 20, 24, 28, 32 Bits**
    - **Data Formatter for Bit Manipulation**
  - **Wide Variety of I2S and Similar Bit Stream Formats**
  - **Integrated Digital Audio Interface Transmitter (DIT) Supports:**
    - **S/PDIF, IEC60958-1, AES-3, CP-430 Formats**
    - **Up to 16 transmit pins**
    - **Enhanced Channel Status/User Data**
  - **Extensive Error Checking and Recovery**
- **Two Inter-Integrated Circuit Bus (I^2C Bus™) Multi-Master and Slave Interfaces**
- **Two Multichannel Buffered Serial Ports:**
  - **Serial-Peripheral-Interface (SPI)**
  - **High-Speed TDM Interface**
  - **AC97 Interface**
- **Two 32-Bit General-Purpose Timers**
- **Dedicated GPIO Module With 16 pins (External Interrupt Capable)**
- **Flexible Phase-Locked-Loop (PLL) Based Clock Generator Module**
- **IEEE-1149.1 (JTAG[†]) Boundary-Scan-Compatible**
- **Package Options:**
  - **208-Pin PowerPAD™ Plastic (Low-Profile) Quad Flatpack (PYP)**
  - **272-Ball, Ball Grid Array Package (GDP)**
- **0.13-µm/6-Level Copper Metal Process**
  - **CMOS Technology**
- **3.3-V I/Os, 1.2-V Internal (PYP)**
- **3.3-V I/Os, 1.26-V Internal (GDP)**

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[†] IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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GDP 272-Ball BGA package (bottom view)

Y	V_{SS}	V_{SS}	ED18	$\overline{\text{BE2}}$	ARDY	EA2	DV_{DD}	EA7	EA9	ECLKOUT	ECLKIN	CLKOUT2/GP[2]	V_{SS}	EA14	EA16	EA18	DV_{DD}	EA20	V_{SS}	V_{SS}
W	V_{SS}	CV_{DD}	DV_{DD}	ED17	V_{SS}	$\overline{\text{CE2}}$	EA4	EA6	DV_{DD}	$\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/SSOE	V_{SS}	DV_{DD}	EA11	EA13	EA15	V_{SS}	EA19	$\overline{\text{CE1}}$	CV_{DD}	V_{SS}
V	ED20	ED19	CV_{DD}	ED16	$\overline{\text{BE3}}$	$\overline{\text{CE3}}$	EA3	EA5	EA8	EA10	$\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/SSADS	$\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/SSWE	DV_{DD}	EA12	DV_{DD}	EA17	$\overline{\text{CE0}}$	CV_{DD}	DV_{DD}	$\overline{\text{BE0}}$
U	ED22	ED21	ED23	V_{SS}	DV_{DD}	CV_{DD}	DV_{DD}	V_{SS}	V_{SS}	CV_{DD}	CV_{DD}	DV_{DD}	V_{SS}	CV_{DD}	CV_{DD}	DV_{DD}	V_{SS}	EA21	$\overline{\text{BE1}}$	V_{SS}
T	ED24	ED25	DV_{DD}	V_{SS}													V_{SS}	ED13	ED15	ED14
R	DV_{DD}	ED27	ED26	CV_{DD}													CV_{DD}	DV_{DD}	ED11	ED12
P	ED28	ED29	ED30	V_{SS}													V_{SS}	ED9	V_{SS}	ED10
N	SCL0	SDA0	ED31	V_{SS}													V_{SS}	ED6	ED7	ED8
M	CLKR1/AXR0[6]	DR1/SDA1	FSR1/AXR0[7]	V_{SS}					V_{SS}	V_{SS}	V_{SS}	V_{SS}					V_{SS}	DV_{DD}	ED4	ED5
L	FSX1	DX1/AXR0[5]	CLKX1/AMUTE0	CV_{DD}					V_{SS}	V_{SS}	V_{SS}	V_{SS}					CV_{DD}	ED2	ED3	CV_{DD}
K	CV_{DD}	V_{SS}	CLKS0/AHCLKR0	CV_{DD}					V_{SS}	V_{SS}	V_{SS}	V_{SS}					CV_{DD}	ED0	ED1	V_{SS}
J	DR0/AXR0[0]	DV_{DD}	FSR0/AFSR0	V_{SS}					V_{SS}	V_{SS}	V_{SS}	V_{SS}					$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$	BUS REQ	$\overline{\text{HINT}}$/GP[1]
H	FSX0/AFSX0	DX0/AXR0[1]	CLKR0/ACLKR0	V_{SS}													V_{SS}	DV_{DD}	$\overline{\text{HRDY}}$/ACLKR1	HHWIL/AFSR1
G	TOUT0/AXR0[2]	TINP0/AXR0[3]	CLKX0/ACLKX0	V_{SS}													V_{SS}	HCNTL0/AXR1[3]	HCNTL1/AXR1[1]	HR/$\overline{\text{W}}$/AXR1[0]
F	TOUT1/AXR0[4]	TINP1/AHCLKX0	DV_{DD}	CV_{DD}													CV_{DD}	$\overline{\text{HDS2}}$/AXR1[5]	V_{SS}	$\overline{\text{HCS}}$/AXR1[2]
E	CLKS1/SCL1	V_{SS}	GP[7] (EXT_INT7)	V_{SS}													V_{SS}	$\overline{\text{HAS}}$/ACLKX1	$\overline{\text{HDS1}}$/AXR1[6]	HD0/AXR1[4]
D	DV_{DD}	GP[6] (EXT_INT6)	EMU2	V_{SS}	CV_{DD}	CV_{DD}	RSV	V_{SS}	EMU0	CLKOUT3	CV_{DD}	RSV	V_{SS}	CV_{DD}	CV_{DD}	DV_{DD}	V_{SS}	HD2/AFSX1	DV_{DD}	HD1/AXR1[7]
C	GP[5] (EXT_INT5)/AMUTEIN0	GP[4] (EXT_INT4)/AMUTEIN1	CV_{DD}	CLK MODE0	PLLHV	V_{SS}	CV_{DD}	V_{SS}	V_{SS}	DV_{DD}	EMU4	RSV	NMI	HD14/GP[14]	HD12/GP[12]	HD9/GP[9]	HD6/AHCLKR1	CV_{DD}	HD4/GP[0]	HD3/AMUTE1
B	V_{SS}	CV_{DD}	DV_{DD}	V_{SS}	RSV	$\overline{\text{TRST}}$	TMS	DV_{DD}	EMU1	EMU3	RSV	EMU5	DV_{DD}	HD15/GP[15]	V_{SS}	HD10/GP[10]	HD8/GP[8]	HD5/AHCLKX1	CV_{DD}	V_{SS}
A	V_{SS}	V_{SS}	CLKIN	CV_{DD}	RSV	TCK	TDI	TDO	CV_{DD}	CV_{DD}	V_{SS}	RSV	$\overline{\text{RESET}}$	V_{SS}	HD13/GP[13]	HD11/GP[11]	DV_{DD}	HD7/GP[3]	V_{SS}	V_{SS}
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

▨ Shading denotes the GDP package pin functions that drop out on the PYP package.

GDP 272-Ball BGA package (bottom view) (continued)

Table 1. Terminal Assignments for the 272-Ball GDP Package (in Order of Ball No.)

BALL NO.	SIGNAL NAME	BALL NO.	SIGNAL NAME
A1	V_{SS}	C1	GP[5](EXT_INT5)/AMUTEIN0
A2	V_{SS}	C2	GP[4](EXT_INT4)/AMUTEIN1
A3	CLKIN	C3	CV_{DD}
A4	CV_{DD}	C4	CLKMODE0
A5	RSV	C5	PLLHV
A6	TCK	C6	V_{SS}
A7	TDI	C7	CV_{DD}
A8	TDO	C8	V_{SS}
A9	CV_{DD}	C9	V_{SS}
A10	CV_{DD}	C10	DV_{DD}
A11	V_{SS}	C11	EMU4
A12	RSV	C12	RSV
A13	$\overline{\text{RESET}}$	C13	NMI
A14	V_{SS}	C14	HD14/GP[14]
A15	HD13/GP[13]	C15	HD12/GP[12]
A16	HD11/GP[11]	C16	HD9/GP[9]
A17	DV_{DD}	C17	HD6/AHCLKR1
A18	HD7/GP[3]	C18	CV_{DD}
A19	V_{SS}	C19	HD4/GP[0]
A20	V_{SS}	C20	HD3/AMUTE1
B1	V_{SS}	D1	DV_{DD}
B2	CV_{DD}	D2	GP[6](EXT_INT6)
B3	DV_{DD}	D3	EMU2
B4	V_{SS}	D4	V_{SS}
B5	RSV	D5	CV_{DD}
B6	$\overline{\text{TRST}}$	D6	CV_{DD}
B7	TMS	D7	RSV
B8	DV_{DD}	D8	V_{SS}
B9	EMU1	D9	EMU0
B10	EMU3	D10	CLKOUT3
B11	RSV	D11	CV_{DD}
B12	EMU5	D12	RSV
B13	DV_{DD}	D13	V_{SS}
B14	HD15/GP[15]	D14	CV_{DD}
B15	V_{SS}	D15	CV_{DD}
B16	HD10/GP[10]	D16	DV_{DD}
B17	HD8/GP[8]	D17	V_{SS}
B18	HD5/AHCLKX1	D18	HD2/AFSX1
B19	CV_{DD}	D19	DV_{DD}
B20	V_{SS}	D20	HD1/AXR1[7]

▨ Shading denotes the GDP package pin functions that drop out on the PYP package.

Table 1. Terminal Assignments for the 272-Ball GDP Package (in Order of Ball No.) (Continued)

BALL NO.	SIGNAL NAME	BALL NO.	SIGNAL NAME
E1	CLKS1/SCL1	J17	$\overline{\text{HOLD}}$
E2	V_{SS}	J18	$\overline{\text{HOLDA}}$
E3	GP[7](EXT_INT7)	J19	BUSREQ
E4	V_{SS}	J20	$\overline{\text{HINT}}$/GP[1]
E17	V_{SS}	K1	CV_{DD}
E18	$\overline{\text{HAS}}$/ACLKX1	K2	V_{SS}
E19	$\overline{\text{HDS1}}$/AXR1[6]	K3	CLKS0/AHCLKR0
E20	HD0/AXR1[4]	K4	CV_{DD}
F1	TOUT1/AXR0[4]	K9	V_{SS}
F2	TINP1/AHCLKX0	K10	V_{SS}
F3	DV_{DD}	K11	V_{SS}
F4	CV_{DD}	K12	V_{SS}
F17	CV_{DD}	K17	CV_{DD}
F18	$\overline{\text{HDS2}}$/AXR1[5]	K18	ED0
F19	V_{SS}	K19	ED1
F20	$\overline{\text{HCS}}$/AXR1[2]	K20	V_{SS}
G1	TOUT0/AXR0[2]	L1	FSX1
G2	TINP0/AXR0[3]	L2	DX1/AXR0[5]
G3	CLKX0/ACLKX0	L3	CLKX1/AMUTE0
G4	V_{SS}	L4	CV_{DD}
G17	V_{SS}	L9	V_{SS}
G18	HCNTL0/AXR1[3]	L10	V_{SS}
G19	HCNTL1/AXR1[1]	L11	V_{SS}
G20	HR/$\overline{\text{W}}$/AXR1[0]	L12	V_{SS}
H1	FSX0/AFSX0	L17	CV_{DD}
H2	DX0/AXR0[1]	L18	ED2
H3	CLKR0/ACLKR0	L19	ED3
H4	V_{SS}	L20	CV_{DD}
H17	V_{SS}	M1	CLKR1/AXR0[6]
H18	DV_{DD}	M2	DR1/SDA1
H19	$\overline{\text{HRDY}}$/ACLKR1	M3	FSR1/AXR0[7]
H20	HHWIL/AFSR1	M4	V_{SS}
J1	DR0/AXR0[0]	M9	V_{SS}
J2	DV_{DD}	M10	V_{SS}
J3	FSR0/AFSR0	M11	V_{SS}
J4	V_{SS}	M12	V_{SS}
J9	V_{SS}	M17	V_{SS}
J10	V_{SS}	M18	DV_{DD}
J11	V_{SS}	M19	ED4
J12	V_{SS}	M20	ED5

▨ Shading denotes the GDP package pin functions that drop out on the PYP package.

Table 1. Terminal Assignments for the 272-Ball GDP Package (in Order of Ball No.) (Continued)

BALL NO.	SIGNAL NAME	BALL NO.	SIGNAL NAME
N1	SCL0	U9	V_{SS}
N2	SDA0	U10	CV_{DD}
N3	ED31	U11	CV_{DD}
N4	V_{SS}	U12	DV_{DD}
N17	V_{SS}	U13	V_{SS}
N18	ED6	U14	CV_{DD}
N19	ED7	U15	CV_{DD}
N20	ED8	U16	DV_{DD}
P1	ED28	U17	V_{SS}
P2	ED29	U18	EA21
P3	ED30	U19	$\overline{\text{BE1}}$
P4	V_{SS}	U20	V_{SS}
P17	V_{SS}	V1	ED20
P18	ED9	V2	ED19
P19	V_{SS}	V3	CV_{DD}
P20	ED10	V4	ED16
R1	DV_{DD}	V5	$\overline{\text{BE3}}$
R2	ED27	V6	$\overline{\text{CE3}}$
R3	ED26	V7	EA3
R4	CV_{DD}	V8	EA5
R17	CV_{DD}	V9	EA8
R18	DV_{DD}	V10	EA10
R19	ED11	V11	$\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$
R20	ED12	V12	$\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$
T1	ED24	V13	DV_{DD}
T2	ED25	V14	EA12
T3	DV_{DD}	V15	DV_{DD}
T4	V_{SS}	V16	EA17
T17	V_{SS}	V17	$\overline{\text{CE0}}$
T18	ED13	V18	CV_{DD}
T19	ED15	V19	DV_{DD}
T20	ED14	V20	$\overline{\text{BE0}}$
U1	ED22	W1	V_{SS}
U2	ED21	W2	CV_{DD}
U3	ED23	W3	DV_{DD}
U4	V_{SS}	W4	ED17
U5	DV_{DD}	W5	V_{SS}
U6	CV_{DD}	W6	$\overline{\text{CE2}}$
U7	DV_{DD}	W7	EA4
U8	V_{SS}	W8	EA6

░ Shading denotes the GDP package pin functions that drop out on the PYP package.

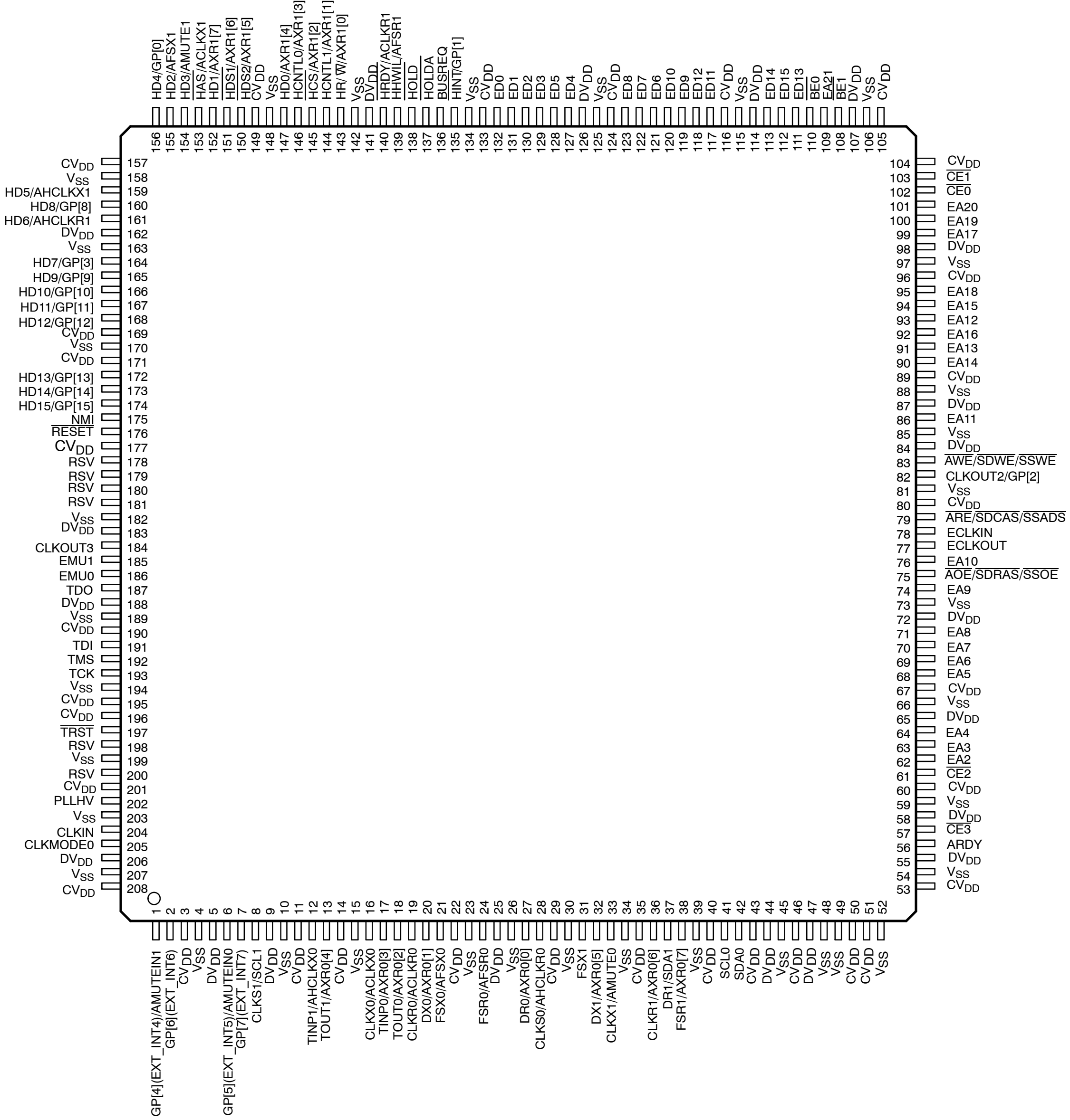
Table 1. Terminal Assignments for the 272-Ball GDP Package (in Order of Ball No.) (Continued)

BALL NO.	SIGNAL NAME	BALL NO.	SIGNAL NAME
W9	DV_{DD}	Y5	ARDY
W10	$\overline{AOE}$/$\overline{SDRAS}$/$\overline{SSOE}$	Y6	EA2
W11	V_{SS}	Y7	DV_{DD}
W12	DV_{DD}	Y8	EA7
W13	EA11	Y9	EA9
W14	EA13	Y10	ECLKOUT
W15	EA15	Y11	ECLKIN
W16	V_{SS}	Y12	CLKOUT2/GP[2]
W17	EA19	Y13	V_{SS}
W18	$\overline{CE1}$	Y14	EA14
W19	CV_{DD}	Y15	EA16
W20	V_{SS}	Y16	EA18
Y1	V_{SS}	Y17	DV_{DD}
Y2	V_{SS}	Y18	EA20
Y3	ED18	Y19	V_{SS}
Y4	$\overline{BE2}$	Y20	V_{SS}

▨ Shading denotes the GDP package pin functions that drop out on the PYP package.

PYP PowerPAD™ QFP package (top view)

PYP 208-PIN PowerPAD™ PLASTIC QUAD FLATPACK (PQFP)
(TOP VIEW)



description

The TMS320C67x™ DSPs (including the TMS320C6713 device) compose the floating−point DSP generation in the TMS320C6000™ DSP platform. The TMS320C6713 (C6713) device is based on the high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making this DSP an excellent choice for multichannel and multifunction applications.

Operating at 225 MHz, the C6713 delivers up to 1350 million floating-point operations per second (MFLOPS), 1800 million instructions per second (MIPS), and with dual fixed-/floating-point multipliers up to 450 million multiply-accumulate operations per second (MMACS).

The C6713 uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 4K-Byte direct-mapped cache and the Level 1 data cache (L1D) is a 4K-Byte 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 256K-Byte memory space that is shared between program and data space. 64K Bytes of the 256K Bytes in L2 memory can be configured as mapped memory, cache, or combinations of the two. The remaining 192K Bytes in L2 serves as mapped SRAM.

The C6713 has a rich peripheral set that includes two Multichannel Audio Serial Ports (McASPs), two Multichannel Buffered Serial Ports (McBSPs), two Inter-Integrated Circuit (I2C) buses, one dedicated General-Purpose Input/Output (GPIO) module, two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM, and asynchronous peripherals.

The two McASP interface modules each support one transmit and one receive clock zone. Each of the McASP has eight serial data pins which can be individually allocated to any of the two zones. The serial port supports time-division multiplexing on each pin from 2 to 32 time slots. The C6713 has sufficient bandwidth to support all 16 serial data pins transmitting a 192 kHz stereo signal. Serial data in each zone may be transmitted and received on multiple serial data pins simultaneously and formatted in a multitude of variations on the Philips Inter-IC Sound (I2S) format.

In addition, the McASP transmitter may be programmed to output multiple S/PDIF, IEC60958, AES-3, CP-430 encoded data channels simultaneously, with a single RAM containing the full implementation of user data and channel status fields.

The McASP also provides extensive error-checking and recovery features, such as the bad clock detection circuit for each high-frequency master clock which verifies that the master clock is within a programmed frequency range.

The two I2C ports on the TMS320C6713 allow the DSP to easily control peripheral devices and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI) mode peripheral devices.

The TMS320C6713 device has two bootmodes: from the HPI or from external asynchronous ROM. For more detailed information, see the *bootmode* section of this data sheet.

The TMS320C67x DSP generation is supported by the TI eXpressDSP™ set of industry benchmark development tools, including a highly optimizing C/C++ Compiler, the Code Composer Studio™ Integrated Development Environment (IDE), JTAG-based emulation and real-time debugging, and the DSP/BIOS™ kernel.

TMS320C6000, eXpressDSP, Code Composer Studio, and DSP/BIOS are trademarks of Texas Instruments.

device characteristics

Table 2 provides an overview of the C6713 DSP. The table shows significant features of the C6713 device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count. For more details on the C67x™ DSP device part numbers and part numbering, see Table 24 and Figure 12.

Table 2. Characteristics of the C6713 Processor

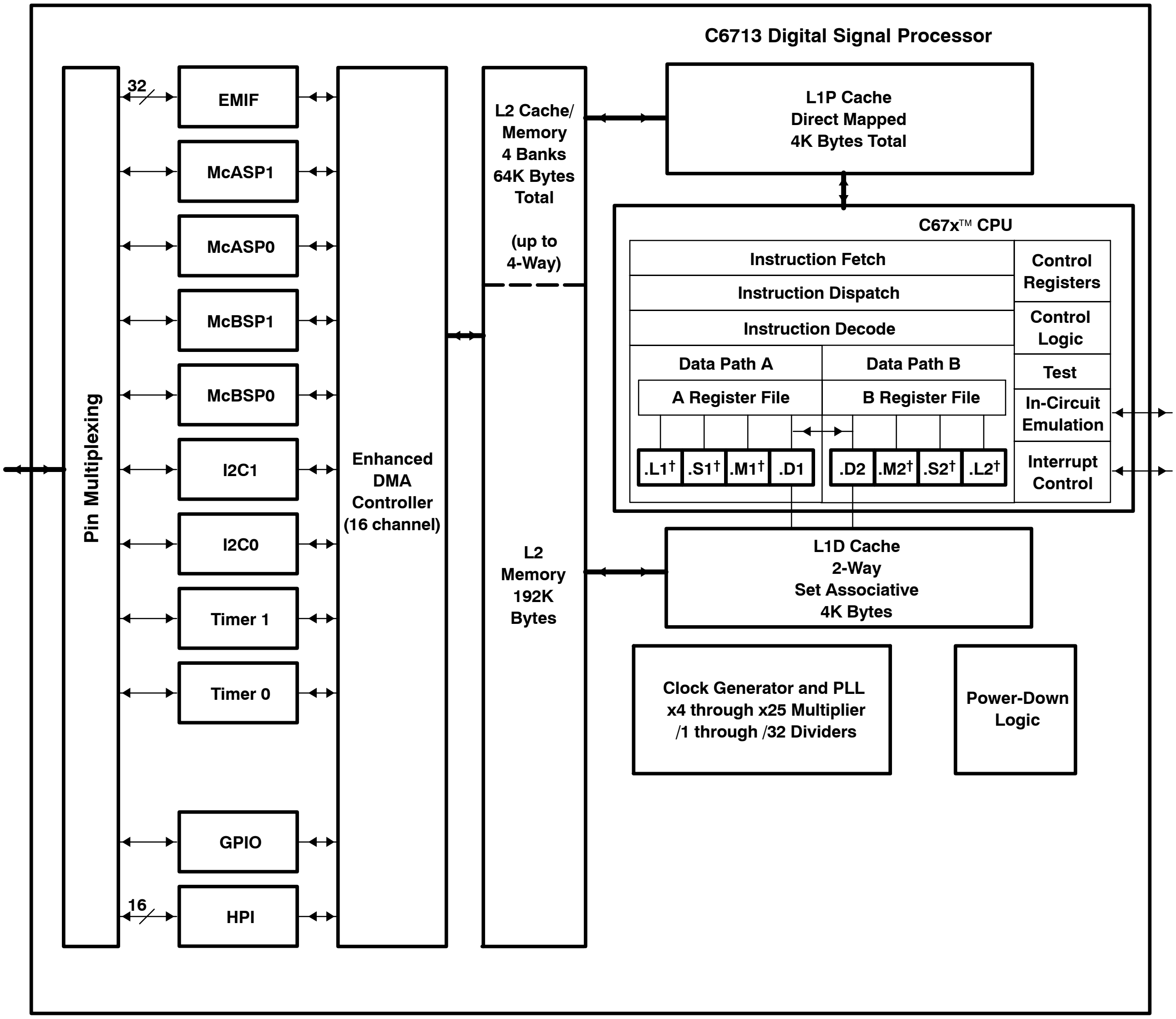
HARDWARE FEATURES		INTERNAL CLOCK SOURCE	C6713 (FLOATING-POINT DSP)	
			GDP	PYP
Peripherals Not all peripheral pins are available at the same time. (For more details, see the Device Configuration section.) Peripheral performance is dependent on chip-level configuration.	EMIF	SYSCLK3 or ECLKIN	1 (32 bit)	1 (16 bit)
	EDMA (16 Channels)	CPU clock frequency	1	
	HPI (16 bit)	SYSCLK2	1	
	McASPs	AUXCLK, SYSCLK2‡	2	
	I2Cs	SYSCLK2	2	
	McBSPs	SYSCLK2	2	
	32-Bit Timers	1/2 of SYSCLK2	2	
	GPIO Module	SYSCLK2	1	
On-Chip Memory	Size (Bytes)		264K	
	Organization		4K-Byte (4KB) L1 Program (L1P) Cache 4KB L1 Data (L1D) Cache 64KB Unified L2 Cache/Mapped RAM 192KB L2 Mapped RAM	
CPU ID+CPU Rev ID	Control Status Register (CSR.[31:16])		0x0203	
BSDL File	For the C6713 BSDL file, contact your Field Sales Representative.			
Frequency	MHz		225, 200	200, 167
Cycle Time	ns		4.4 ns (C6713GDP-225) 5 ns (C6713GDPA-200)	5 ns (C6713PYP-200) 6 ns (C6713PYPA-167)
Voltage	Core (V)		1.26 V [GDP Package]	1.2 V [PYP Package]
	I/O (V)		3.3 V	
Clock Generator Options	Prescaler Multiplier Postscaler		/1, /2, /3, ..., /32 x4, x5, x6, ..., x25 /1, /2, /3, ..., /32	
Packages	27 x 27 mm		272-Ball BGA (GDP)	−
	28 x 28 mm		−	208-Pin PowerPAD™ PQFP (PYP)
Process Technology	µm		0.13	
Product Status† Product Preview (PP) Advance Information (AI) Production Data (PD)			PD	PD

† PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

‡ AUXCLK is the McASP internal high-frequency clock source for serial transfers. SYSCLK2 is the McASP system clock used for the clock check (high-frequency) circuit.

C67x is a trademark of Texas Instruments.

functional block and CPU (DSP core) diagram



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

EMIF interfaces to:	McBSPs interface to:	McASPs interface to:
−SDRAM	−SPI Control Port	−I2S Multichannel ADC, DAC, Codec, DIR
−SBSRAM	−High-Speed TDM Codecs	−DIT: Multiple Outputs
−SRAM,	−AC97 Codecs	
−ROM/Flash, and	−Serial EEPROM	
−I/O devices		

CPU (DSP core) description

The TMS320C6713 floating-point digital signal processor is based on the C67x CPU. The CPU fetches VelociTI™ advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI™ VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

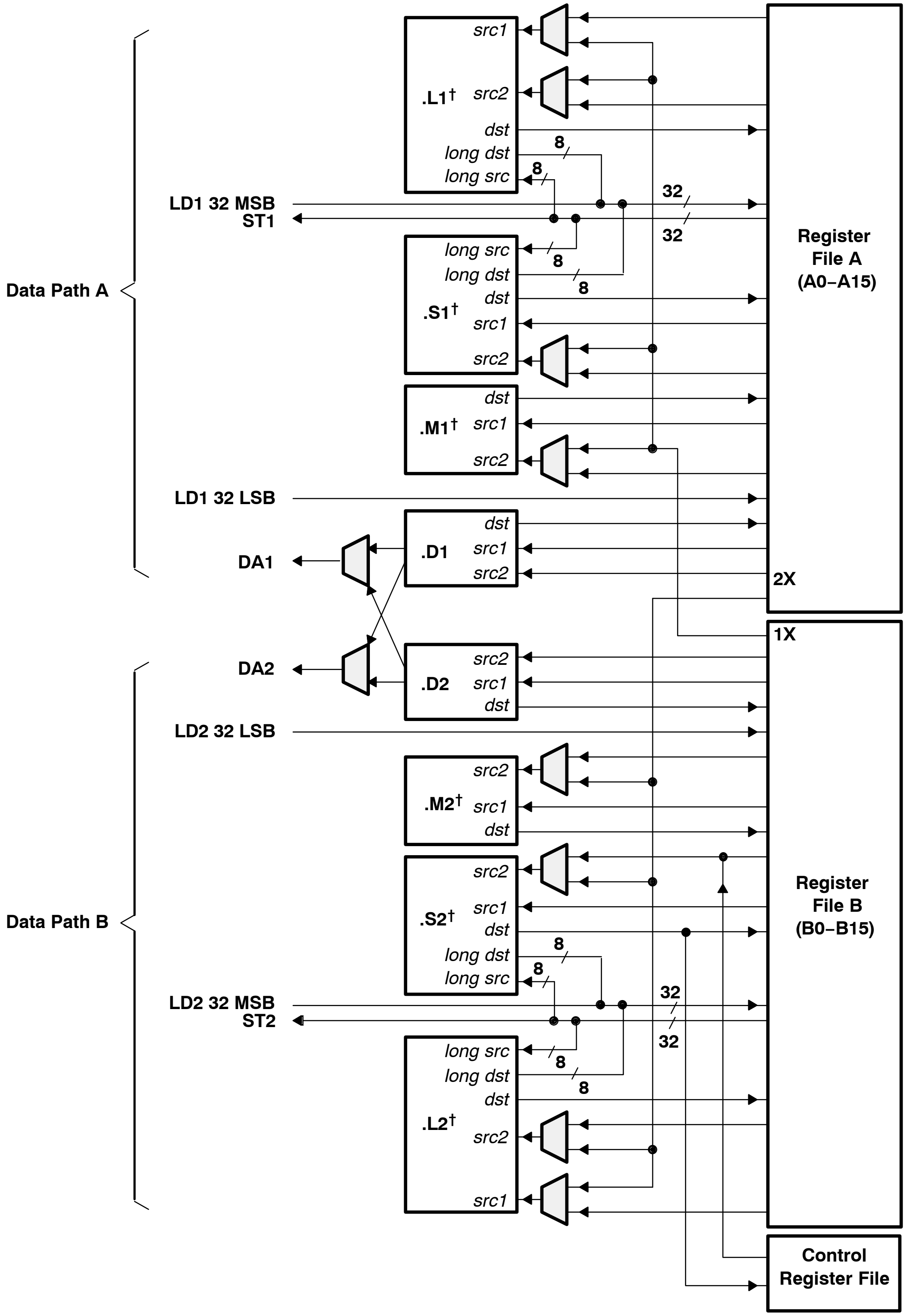
The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU (see the functional block and CPU diagram and Figure 1). The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all C62x instructions. In addition to C62x fixed-point instructions, the six out of eight functional units (.L1, .S1, .M1, .M2, .S2, and .L2) also execute floating-point instructions. The remaining two functional units (.D1 and .D2) also execute the new LDDW instruction which loads 64 bits per CPU side for a total of 128 bits per cycle.

Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically “true”). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

CPU (DSP core) description (continued)



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 1. TMS320C67x™ CPU (DSP Core) Data Paths

memory map summary

Table 3 shows the memory map address ranges of the C6713 device.

Table 3. TMS320C6713 Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Internal RAM (L2)	192K	0000 0000 – 0002 FFFF
Internal RAM/Cache	64K	0003 0000 – 0003 FFFF
Reserved	24M – 256K	0004 0000 – 017F FFFF
External Memory Interface (EMIF) Registers	256K	0180 0000 – 0183 FFFF
L2 Registers	128K	0184 0000 – 0185 FFFF
Reserved	128K	0186 0000 – 0187 FFFF
HPI Registers	256K	0188 0000 – 018B FFFF
McBSP 0 Registers	256K	018C 0000 – 018F FFFF
McBSP 1 Registers	256K	0190 0000 – 0193 FFFF
Timer 0 Registers	256K	0194 0000 – 0197 FFFF
Timer 1 Registers	256K	0198 0000 – 019B FFFF
Interrupt Selector Registers	512	019C 0000 – 019C 01FF
Device Configuration Registers	4	019C 0200 – 019C 0203
Reserved	256K – 516	019C 0204 – 019F FFFF
EDMA RAM and EDMA Registers	256K	01A0 0000 – 01A3 FFFF
Reserved	768K	01A4 0000 – 01AF FFFF
GPIO Registers	16K	01B0 0000 – 01B0 3FFF
Reserved	240K	01B0 4000 – 01B3 FFFF
I2C0 Registers	16K	01B4 0000 – 01B4 3FFF
I2C1 Registers	16K	01B4 4000 – 01B4 7FFF
Reserved	16K	01B4 8000 – 01B4 BFFF
McASP0 Registers	16K	01B4 C000 – 01B4 FFFF
McASP1 Registers	16K	01B5 0000 – 01B5 3FFF
Reserved	160K	01B5 4000 – 01B7 BFFF
PLL Registers	8K	01B7 C000 – 01B7 DFFF
Reserved	264K	01B7 E000 – 01BB FFFF
Emulation Registers	256K	01BC 0000 – 01BF FFFF
Reserved	4M	01C0 0000 – 01FF FFFF
QDMA Registers	52	0200 0000 – 0200 0033
Reserved	16M – 52	0200 0034 – 02FF FFFF
Reserved	720M	0300 0000 – 2FFF FFFF
McBSP0 Data Port	64M	3000 0000 – 33FF FFFF
McBSP1 Data Port	64M	3400 0000 – 37FF FFFF
Reserved	64M	3800 0000 – 3BFF FFFF
McASP0 Data Port	1M	3C00 0000 – 3C0F FFFF
McASP1 Data Port	1M	3C10 0000 – 3C1F FFFF
Reserved	1G + 62M	3C20 0000 – 7FFF FFFF
EMIF CE0[†]	256M	8000 0000 – 8FFF FFFF
EMIF CE1[†]	256M	9000 0000 – 9FFF FFFF
EMIF CE2[†]	256M	A000 0000 – AFFF FFFF
EMIF CE3[†]	256M	B000 0000 – BFFF FFFF
Reserved	1G	C000 0000 – FFFF FFFF

[†] The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space.

L2 memory structure expanded

Figure 2 shows the detail of the L2 memory structure.

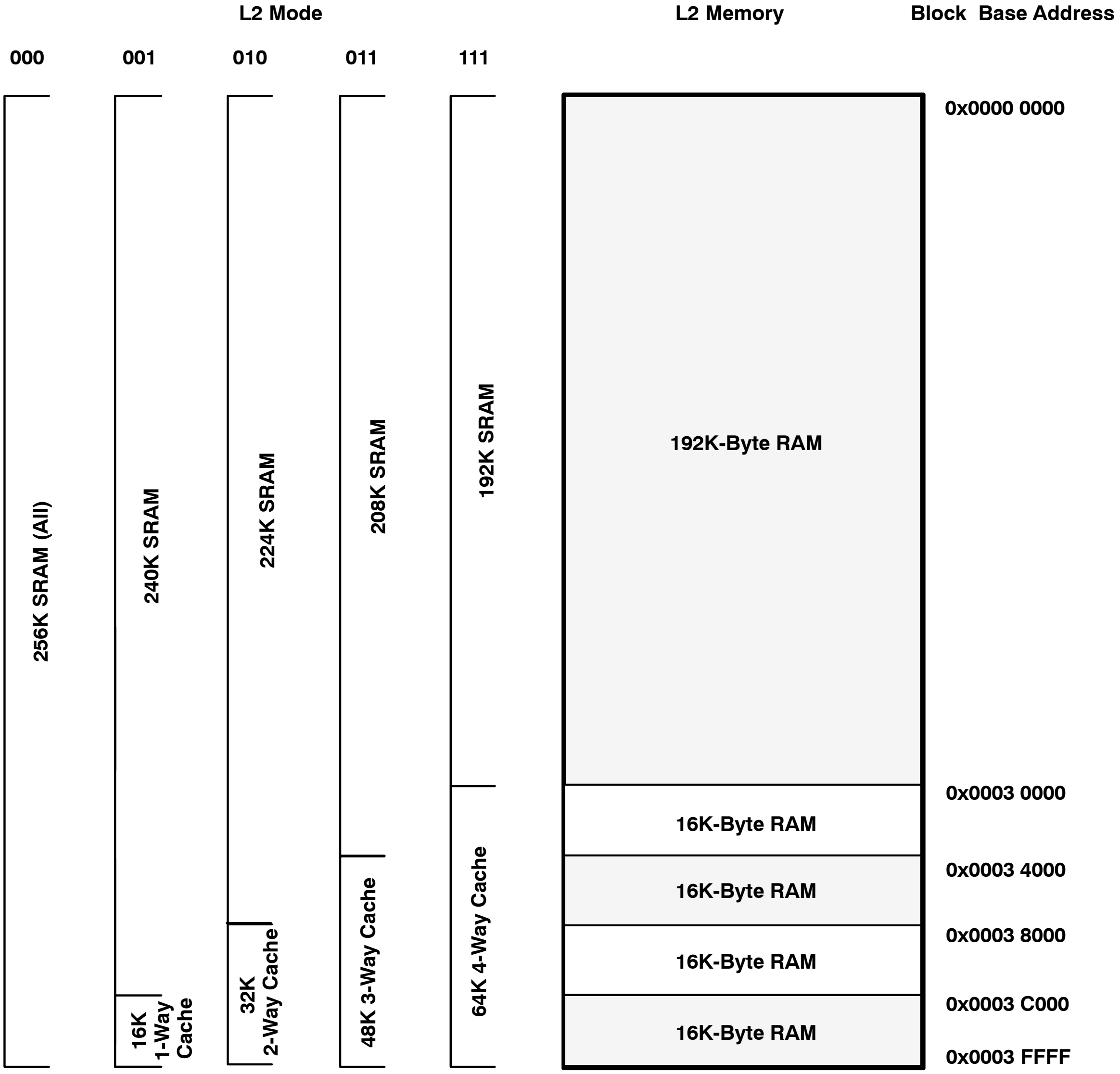


Figure 2. L2 Memory Configuration

peripheral register descriptions

Table 4 through Table 17 identify the peripheral registers for the C6713 device by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents, bit names, and their descriptions for the EMIF, EDMA, HPI, and McBSP modules, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 4. EMIF Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	GBLCTL	EMIF global control
0180 0004	CECTL1	EMIF CE1 space control
0180 0008	CECTL0	EMIF CE0 space control
0180 000C	−	Reserved
0180 0010	CECTL2	EMIF CE2 space control
0180 0014	CECTL3	EMIF CE3 space control
0180 0018	SDCTL	EMIF SDRAM control
0180 001C	SDTIM	EMIF SDRAM refresh control
0180 0020	SDEXT	EMIF SDRAM extension
0180 0024 − 0183 FFFF	−	Reserved

Table 5. L2 Cache Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 0000	CCFG	Cache configuration register
0184 4000	L2WBAR	L2 writeback base address register
0184 4004	L2WWC	L2 writeback word count register
0184 4010	L2WIBAR	L2 writeback-invalidate base address register
0184 4014	L2WIWC	L2 writeback-invalidate word count register
0184 4020	L1PIBAR	L1P invalidate base address register
0184 4024	L1PIWC	L1P invalidate word count register
0184 4030	L1DWIBAR	L1D writeback-invalidate base address register
0184 4034	L1DWIWC	L1D writeback-invalidate word count register
0184 5000	L2WB	L2 writeback all register
0184 5004	L2WBINV	L2 writeback-invalidate all register
0184 8200	MAR0	Controls CE0 range 8000 0000 − 80FF FFFF
0184 8204	MAR1	Controls CE0 range 8100 0000 − 81FF FFFF
0184 8208	MAR2	Controls CE0 range 8200 0000 − 82FF FFFF
0184 820C	MAR3	Controls CE0 range 8300 0000 − 83FF FFFF
0184 8240	MAR4	Controls CE1 range 9000 0000 − 90FF FFFF
0184 8244	MAR5	Controls CE1 range 9100 0000 − 91FF FFFF
0184 8248	MAR6	Controls CE1 range 9200 0000 − 92FF FFFF
0184 824C	MAR7	Controls CE1 range 9300 0000 − 93FF FFFF
0184 8280	MAR8	Controls CE2 range A000 0000 − A0FF FFFF
0184 8284	MAR9	Controls CE2 range A100 0000 − A1FF FFFF
0184 8288	MAR10	Controls CE2 range A200 0000 − A2FF FFFF
0184 828C	MAR11	Controls CE2 range A300 0000 − A3FF FFFF
0184 82C0	MAR12	Controls CE3 range B000 0000 − B0FF FFFF
0184 82C4	MAR13	Controls CE3 range B100 0000 − B1FF FFFF
0184 82C8	MAR14	Controls CE3 range B200 0000 − B2FF FFFF
0184 82CC	MAR15	Controls CE3 range B300 0000 − B3FF FFFF
0184 82D0 − 0185 FFFF	−	Reserved

peripheral register descriptions (continued)

Table 6. Interrupt Selector Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
019C 0000	MUXH	Interrupt multiplexer high	Selects which interrupts drive CPU interrupts 10−15 (INT10−INT15)
019C 0004	MUXL	Interrupt multiplexer low	Selects which interrupts drive CPU interrupts 4−9 (INT04−INT09)
019C 0008	EXTPOL	External interrupt polarity	Sets the polarity of the external interrupts (EXT_INT4−EXT_INT7)
019C 000C − 019F FFFF	−	Reserved	

Table 7. Device Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER DESCRIPTION	
019C 0200	DEVCFG	Device Configuration	Allows the user to control peripheral selection. This register also offers the user control of the EMIF input clock source. For more detailed information on the device configuration register, see the Device Configurations section of this data sheet.
019C 0204 − 019F FFFF	−	Reserved	
N/A	CSR	CPU Control Status Register	Identifies which CPU and defines the silicon revision of the CPU. This register also offers the user control of device operation. For more detailed information on the CPU Control Status Register, see the CPU CSR Register Description section of this data sheet.

Table 8. EDMA Parameter RAM†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0000 − 01A0 0017	−	Parameters for Event 0 (6 words) or Reload/Link Parameters for other Event
01A0 0018 − 01A0 002F	−	Parameters for Event 1 (6 words) or Reload/Link Parameters for other Event
01A0 0030 − 01A0 0047	−	Parameters for Event 2 (6 words) or Reload/Link Parameters for other Event
01A0 0048 − 01A0 005F	−	Parameters for Event 3 (6 words) or Reload/Link Parameters for other Event
01A0 0060 − 01A0 0077	−	Parameters for Event 4 (6 words) or Reload/Link Parameters for other Event
01A0 0078 − 01A0 008F	−	Parameters for Event 5 (6 words) or Reload/Link Parameters for other Event
01A0 0090 − 01A0 00A7	−	Parameters for Event 6 (6 words) or Reload/Link Parameters for other Event
01A0 00A8 − 01A0 00BF	−	Parameters for Event 7 (6 words) or Reload/Link Parameters for other Event
01A0 00C0 − 01A0 00D7	−	Parameters for Event 8 (6 words) or Reload/Link Parameters for other Event
01A0 00D8 − 01A0 00EF	−	Parameters for Event 9 (6 words) or Reload/Link Parameters for other Event
01A0 00F0 − 01A0 00107	−	Parameters for Event 10 (6 words) or Reload/Link Parameters for other Event
01A0 0108 − 01A0 011F	−	Parameters for Event 11 (6 words) or Reload/Link Parameters for other Event
01A0 0120 − 01A0 0137	−	Parameters for Event 12 (6 words) or Reload/Link Parameters for other Event
01A0 0138 − 01A0 014F	−	Parameters for Event 13 (6 words) or Reload/Link Parameters for other Event
01A0 0150 − 01A0 0167	−	Parameters for Event 14 (6 words) or Reload/Link Parameters for other Event
01A0 0168 − 01A0 017F	−	Parameters for Event 15 (6 words) or Reload/Link Parameters for other Event
01A0 0180 − 01A0 0197	−	Reload/link parameters for Event 0−15
01A0 0198 − 01A0 01AF	−	Reload/link parameters for Event 0−15
...		...
01A0 07E0 − 01A0 07F7	−	Reload/link parameters for Event 0−15
01A0 07F8 − 01A0 07FF	−	Scratch pad area (2 words)

† The C6713 device has 85 EDMA parameters total: 16 Event/Reload parameters and 69 Reload-only parameters.

peripheral register descriptions (continued)

For more details on the EDMA parameter RAM 6-word parameter entry structure, see Figure 3.

	31	0	EDMA Parameter
Word 0	EDMA Channel Options Parameter (OPT)		OPT
Word 1	EDMA Channel Source Address (SRC)		SRC
Word 2	Array/Frame Count (FRMCNT)	Element Count (ELECNT)	CNT
Word 3	EDMA Channel Destination Address (DST)		DST
Word 4	Array/Frame Index (FRMIDX)	Element Index (ELEIDX)	IDX
Word 5	Element Count Reload (ELERLD)	Link Address (LINK)	RLD

Figure 3. EDMA Channel Parameter Entries (6 Words) for Each EDMA Event

Table 9. EDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0800 − 01A0 FEFC	−	Reserved
01A0 FF00	ESEL0	EDMA event selector 0
01A0 FF04	ESEL1	EDMA event selector 1
01A0 FF08 − 01A0 FF0B	−	Reserved
01A0 FF0C	ESEL3	EDMA event selector 3
01A0 FF1F − 01A0 FFDC	−	Reserved
01A0 FFE0	PQSR	Priority queue status register
01A0 FFE4	CIPR	Channel interrupt pending register
01A0 FFE8	CIER	Channel interrupt enable register
01A0 FFEC	CCER	Channel chain enable register
01A0 FFF0	ER	Event register
01A0 FFF4	EER	Event enable register
01A0 FFF8	ECR	Event clear register
01A0 FFFC	ESR	Event set register
01A1 0000 − 01A3 FFFF	−	Reserved

peripheral register descriptions (continued)

Table 10. Quick DMA (QDMA) and Pseudo Registers†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0200 0000	QOPT	QDMA options parameter register
0200 0004	QSRC	QDMA source address register
0200 0008	QCNT	QDMA frame count register
0200 000C	QDST	QDMA destination address register
0200 0010	QIDX	QDMA index register
0200 0014 − 0200 001C	−	Reserved
0200 0020	QSOPT	QDMA pseudo options register
0200 0024	QSSRC	QDMA pseudo source address register
0200 0028	QSCNT	QDMA pseudo frame count register
0200 002C	QSDST	QDMA pseudo destination address register
0200 0030	QSIDX	QDMA pseudo index register

† All the QDMA and Pseudo registers are write-accessible only

Table 11. PLL Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B7 C000	PLLPID	Peripheral identification register (PID) [C6713 value: 0x00010801 for PLL Controller]
01B7 C004 − 01B7 C0FF	−	Reserved
01B7 C100	PLLCSR	PLL control/status register
01B7 C104 − 01B7 C10F	−	Reserved
01B7 C110	PLLM	PLL multiplier control register
01B7 C114	PLLDIV0	PLL controller divider 0 register
01B7 C118	PLLDIV1	PLL controller divider 1 register
01B7 C11C	PLLDIV2	PLL controller divider 2 register
01B7 C120	PLLDIV3	PLL controller divider 3 register
01B7 C124	OSCDIV1	Oscillator divider 1 register
01B7 C128 − 01B7 DFFF	−	Reserved

peripheral register descriptions (continued)

Table 12. McASP0 and McASP1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	**McASP1**		
3C00 0000 − 3C00 FFFF	3C10 0000 − 3C10 FFFF	RBUF/XBUFx	McASPx receive buffer or McASPx transmit buffer via the Peripheral Data Bus. (Used when RSEL or XSEL bits = 0 [these bits are located in the RFMT or XFMT registers, respectively].)
01B4 C000	01B5 0000	MCASPPIDx	Peripheral Identification register [C6713 value: 0x00100101 for McASP0 and for McASP1]
01B4 C004	01B5 0004	PWRDEMUx	Power down and emulation management register
01B4 C008	01B5 0008	−	Reserved
01B4 C00C	01B5 000C	−	Reserved
01B4 C010	01B5 0010	PFUNCx	Pin function register
01B4 C014	01B5 0014	PDIRx	Pin direction register
01B4 C018	01B5 0018	PDOUTx	Pin data out register
01B4 C01C	01B5 001C	PDIN/PDSETx	Pin data in / data set register Read returns: PDIN Writes affect: PDSET
01B4 C020	01B5 0020	PDCLRx	Pin data clear register
01B4 C024 − 01B4 C040	01B5 0024 − 01B5 0040	−	Reserved
01B4 C044	01B5 0044	GBLCTLx	Global control register
01B4 C048	01B5 0048	AMUTEx	Mute control register
01B4 C04C	01B5 004C	DLBCTLx	Digital Loop-back control register
01B4 C050	01B5 0050	DITCTLx	DIT mode control register
01B4 C054 − 01B4 C05C	01B5 0054 − 01B5 005C	−	Reserved
01B4 C060	01B5 0060	RGBLCTLx	Alias of GBLCTL containing only Receiver Reset bits, allows transmit to be reset independently from receive.
01B4 C064	01B5 0064	RMASKx	Receiver format unit bit mask register
01B4 C068	01B5 0068	RFMTx	Receive bit stream format register
01B4 C06C	01B5 006C	AFSRCTLx	Receive frame sync control register
01B4 C070	01B5 0070	ACLKRCTLx	Receive clock control register
01B4 C074	01B5 0074	AHCLKRCTLx	High-frequency receive clock control register
01B4 C078	01B5 0078	RTDMx	Receive TDM slot 0−31 register
01B4 C07C	01B5 007C	RINTCTLx	Receiver interrupt control register
01B4 C080	01B5 0080	RSTATx	Status register − Receiver
01B4 C084	01B5 0084	RSLOTx	Current receive TDM slot register
01B4 C088	01B5 0088	RCLKCHKx	Receiver clock check control register
01B4 C08C − 01B4 C09C	01B5 008C − 01B5 009C	−	Reserved
01B4 C0A0	01B5 00A0	XGBLCTLx	Alias of GBLCTL containing only Transmitter Reset bits, allows transmit to be reset independently from receive.
01B4 C0A4	01B5 00A4	XMASKx	Transmit format unit bit mask register
01B4 C0A8	01B5 00A8	XFMTx	Transmit bit stream format register
01B4 C0AC	01B5 00AC	AFSXCTLx	Transmit frame sync control register
01B4 C0B0	01B5 00B0	ACLKXCTLx	Transmit clock control register
01B4 C0B4	01B5 00B4	AHCLKXCTLx	High-frequency Transmit clock control register

peripheral register descriptions (continued)

Table 12. McASP0 and McASP1 Registers (Continued)

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	McASP1		
01B4 C0B8	01B5 00B8	XTDMx	Transmit TDM slot 0−31 register
01B4 C0BC	01B5 00BC	XINTCTLx	Transmit interrupt control register
01B4 C0C0	01B5 00C0	XSTATx	Status register − Transmitter
01B4 C0C4	01B5 00C4	XSLOTx	Current transmit TDM slot
01B4 C0C8	01B5 00C8	XCLKCHKx	Transmit clock check control register
01B4 C0D0 − 01B4 C0FC	01B5 00CC − 01B5 00FC	−	Reserved
01B4 C100	01B5 0100	DITCSRA0x	Left (even TDM slot) channel status register file
01B4 C104	01B5 0104	DITCSRA1x	Left (even TDM slot) channel status register file
01B4 C108	01B5 0108	DITCSRA2x	Left (even TDM slot) channel status register file
01B4 C10C	01B5 010C	DITCSRA3x	Left (even TDM slot) channel status register file
01B4 C110	01B5 0110	DITCSRA4x	Left (even TDM slot) channel status register file
01B4 C114	01B5 0114	DITCSRA5x	Left (even TDM slot) channel status register file
01B4 C118	01B5 0118	DITCSRB0x	Right (odd TDM slot) channel status register file
01B4 C11C	01B5 011C	DITCSRB1x	Right (odd TDM slot) channel status register file
01B4 C120	01B5 0120	DITCSRB2x	Right (odd TDM slot) channel status register file
01B4 C124	01B5 0124	DITCSRB3x	Right (odd TDM slot) channel status register file
01B4 C128	01B5 0128	DITCSRB4x	Right (odd TDM slot) channel status register file
01B4 C12C	01B5 012C	DITCSRB5x	Right (odd TDM slot) channel status register file
01B4 C130	01B5 0130	DITUDRA0x	Left (even TDM slot) user data register file
01B4 C134	01B5 0134	DITUDRA1x	Left (even TDM slot) user data register file
01B4 C138	01B5 0138	DITUDRA2x	Left (even TDM slot) user data register file
01B4 C13C	01B5 013C	DITUDRA3x	Left (even TDM slot) user data register file
01B4 C140	01B5 0140	DITUDRA4x	Left (even TDM slot) user data register file
01B4 C144	01B5 0144	DITUDRA5x	Left (even TDM slot) user data register file
01B4 C148	01B5 0148	DITUDRB0x	Right (odd TDM slot) user data register file
01B4 C14C	01B5 014C	DITUDRB1x	Right (odd TDM slot) user data register file
01B4 C150	01B5 0150	DITUDRB2x	Right (odd TDM slot) user data register file
01B4 C154	01B5 0154	DITUDRB3x	Right (odd TDM slot) user data register file
01B4 C158	01B5 0158	DITUDRB4x	Right (odd TDM slot) user data register file
01B4 C15C	01B5 015C	DITUDRB5x	Right (odd TDM slot) user data register file
01B4 C160 − 01B4 C17C	01B5 0160 − 01B5 017C	−	Reserved
01B4 C180	01B5 0180	SRCTL0x	Serializer 0 control register
01B4 C184	01B5 0184	SRCTL1x	Serializer 1 control register
01B4 C188	01B5 0188	SRCTL2x	Serializer 2 control register
01B4 C18C	01B5 018C	SRCTL3x	Serializer 3 control register
01B4 C190	01B5 0190	SRCTL4x	Serializer 4 control register
01B4 C194	01B5 0194	SRCTL5x	Serializer 5 control register
01B4 C198	01B5 0198	SRCTL6x	Serializer 6 control register
01B4 C19C	01B5 019C	SRCTL7x	Serializer 7 control register
01B4 C1A0 − 01B4 C1FC	01B5 01A0 − 01B5 01FC	−	Reserved

peripheral register descriptions (continued)

Table 12. McASP0 and McASP1 Registers (Continued)

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	McASP1		
01B4 C200	01B5 0200	XBUF0x	Transmit Buffer for Serializer 0 through configuration bus†
01B4 C204	01B5 0204	XBUF1x	Transmit Buffer for Serializer 1 through configuration bus†
01B4 C208	01B5 0208	XBUF2x	Transmit Buffer for Serializer 2 through configuration bus†
01B4 C20C	01B5 020C	XBUF3x	Transmit Buffer for Serializer 3 through configuration bus†
01B4 C210	01B5 0210	XBUF4x	Transmit Buffer for Serializer 4 through configuration bus†
01B4 C214	01B5 0214	XBUF5x	Transmit Buffer for Serializer 5 through configuration bus†
01B4 C218	01B5 0218	XBUF6x	Transmit Buffer for Serializer 6 through configuration bus†
01B4 C21C	01B5 021C	XBUF7x	Transmit Buffer for Serializer 7 through configuration bus†
01B4 C220 − 01B4 C27C	01B5 C220 − 01B5 027C	−	Reserved
01B4 C280	01B5 0280	RBUF0x	Receive Buffer for Serializer 0 through configuration bus‡
01B4 C284	01B5 0284	RBUF1x	Receive Buffer for Serializer 1 through configuration bus‡
01B4 C288	01B5 0288	RBUF2x	Receive Buffer for Serializer 2 through configuration bus‡
01B4 C28C	01B5 028C	RBUF3x	Receive Buffer for Serializer 3 through configuration bus‡
01B4 C290	01B5 0290	RBUF4x	Receive Buffer for Serializer 4 through configuration bus‡
01B4 C294	01B5 0294	RBUF5x	Receive Buffer for Serializer 5 through configuration bus‡
01B4 C298	01B5 0298	RBUF6x	Receive Buffer for Serializer 6 through configuration bus‡
01B4 C29C	01B5 029C	RBUF7x	Receive Buffer for Serializer 7 through configuration bus‡
01B4 C2A0 − 01B4 FFFF	01B5 02A0 − 01B5 3FFF	−	Reserved

† The transmit buffers for serializers 0 − 7 are accessible to the CPU via the peripheral bus if the XSEL bit = 1 (XFMT register).
‡ The receive buffers for serializers 0 − 7 are accessible to the CPU via the peripheral bus if the RSEL bit = 1 (RFMT register).

Table 13. I2C0 and I2C1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER DESCRIPTION
I2C0	I2C1		
01B4 0000	01B4 4000	I2COARx	I2Cx own address register
01B4 0004	01B4 4004	I2CIERx	I2Cx interrupt enable register
01B4 0008	01B4 4008	I2CSTRx	I2Cx interrupt status register
01B4 000C	01B4 400C	I2CCLKLx	I2Cx clock low-time divider register
01B4 0010	01B4 4010	I2CCLKHx	I2Cx clock high-time divider register
01B4 0014	01B4 4014	I2CCNTx	I2Cx data count register
01B4 0018	01B4 4018	I2CDRRx	I2Cx data receive register
01B4 001C	01B4 401C	I2CSARx	I2Cx slave address register
01B4 0020	01B4 4020	I2CDXRx	I2Cx data transmit register
01B4 0024	01B4 4024	I2CMDRx	I2Cx mode register
01B4 0028	01B4 4028	I2CISRCx	I2Cx interrupt source register
01B4 002C	01B4 402C	−	Reserved
01B4 0030	01B4 4030	I2CPSCx	I2Cx prescaler register
01B4 0034	01B4 4034	I2CPID10 I2CPID11	I2Cx Peripheral Identification register 1 [C6713 value: 0x0000 0101]
01B4 0038	01B4 4038	I2CPID20 I2CPID21	I2Cx Peripheral Identification register 2 [C6713 value: 0x0000 0005]
01B4 003C − 01B4 3FFF	01B4 403C − 01B4 7FFF	−	Reserved

peripheral register descriptions (continued)

Table 14. HPI Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
−	HPID	HPI data register	Host read/write access only
−	HPIA	HPI address register	Host read/write access only
0188 0000	HPIC	HPI control register	Both Host/CPU read/write access
0188 0004 − 018B FFFF	−	Reserved	

Table 15. Timer 0 and Timer 1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME	COMMENTS
TIMER 0	TIMER 1			
0194 0000	0198 0000	CTLx	Timer x control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0194 0004	0198 0004	PRDx	Timer x period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0194 0008	0198 0008	CNTx	Timer x counter register	Contains the current value of the incrementing counter.
0194 000C − 0197 FFFF	0198 000C − 019B FFFF	−	Reserved	−

Table 16. McBSP0 and McBSP1 Registers

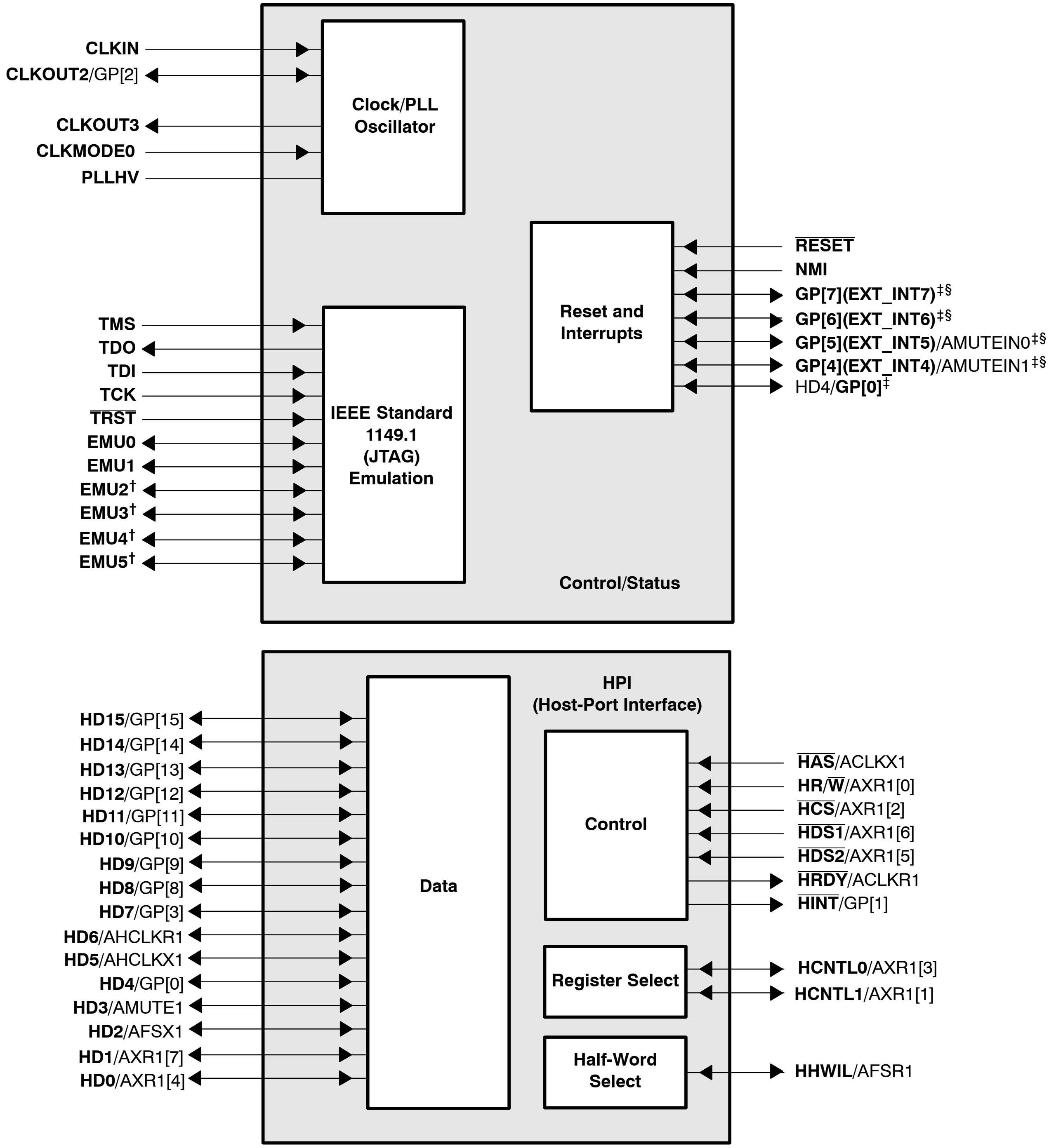
HEX ADDRESS RANGE		ACRONYM	REGISTER DESCRIPTION
McBSP0	McBSP1		
018C 0000	0190 0000	DRRx	McBSPx data receive register via Configuration Bus The CPU and EDMA controller can only read this register; they cannot write to it.
3000 0000 − 33FF FFFF	3400 0000 − 37FF FFFF	DRRx	McBSPx data receive register via Peripheral Data Bus
018C 0004	0190 0004	DXRx	McBSPx data transmit register via Configuration Bus
3000 0000 − 33FF FFFF	3400 0000 − 37FF FFFF	DXRx	McBSPx data transmit register via Peripheral Data Bus
018C 0008	0190 0008	SPCRx	McBSPx serial port control register
018C 000C	0190 000C	RCRx	McBSPx receive control register
018C 0010	0190 0010	XCRx	McBSPx transmit control register
018C 0014	0190 0014	SRGRx	McBSPx sample rate generator register
018C 0018	0190 0018	MCRx	McBSPx multichannel control register
018C 001C	0190 001C	RCERx	McBSPx receive channel enable register
018C 0020	0190 0020	XCERx	McBSPx transmit channel enable register
018C 0024	0190 0024	PCRx	McBSPx pin control register
018C 0028 − 018F FFFF	0190 0028 − 0193 FFFF	−	Reserved

peripheral register descriptions (continued)

Table 17. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B0 0000	GPEN	GPIO enable register
01B0 0004	GPDIR	GPIO direction register
01B0 0008	GPVAL	GPIO value register
01B0 000C	−	Reserved
01B0 0010	GPDH	GPIO delta high register
01B0 0014	GPHM	GPIO high mask register
01B0 0018	GPDL	GPIO delta low register
01B0 001C	GPLM	GPIO low mask register
01B0 0020	GPGC	GPIO global control register
01B0 0024	GPPOL	GPIO interrupt polarity register
01B0 0028 − 01B0 3FFF	−	Reserved

signal groups description



† These external pins are applicable to the GDP package only.

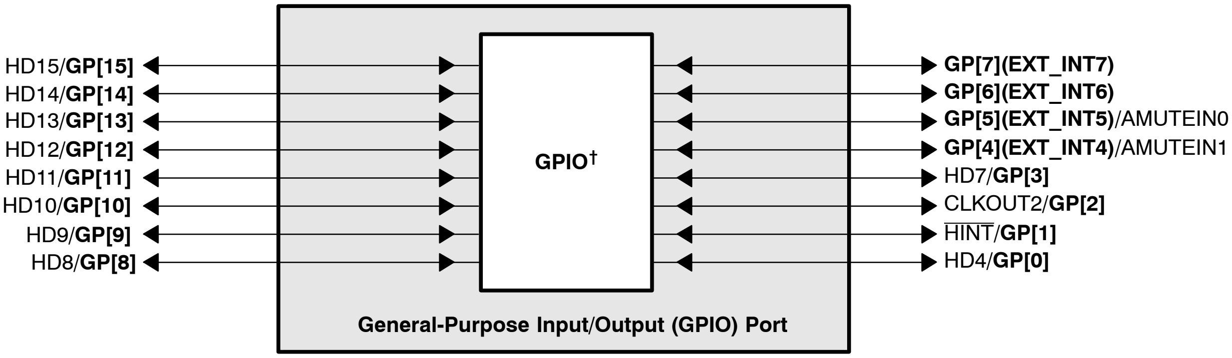
‡ The GP[15:0] pins, through interrupt sharing, are external interrupt capable via GPINT0. For more details, see the External Interrupt Sources section of this data sheet. For more details on interrupt sharing, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

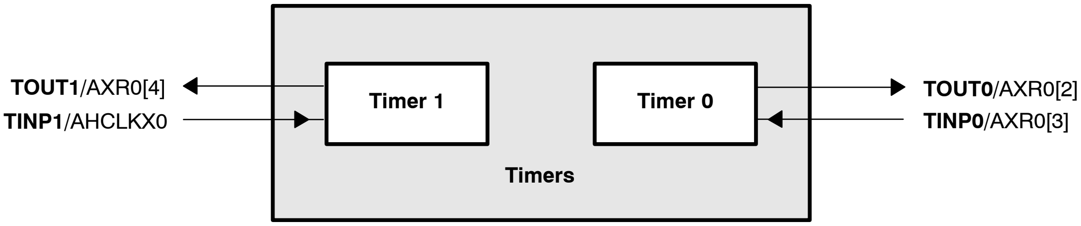
§ All of these pins are external interrupt sources. For more details, see the External Interrupt Sources section of this data sheet.

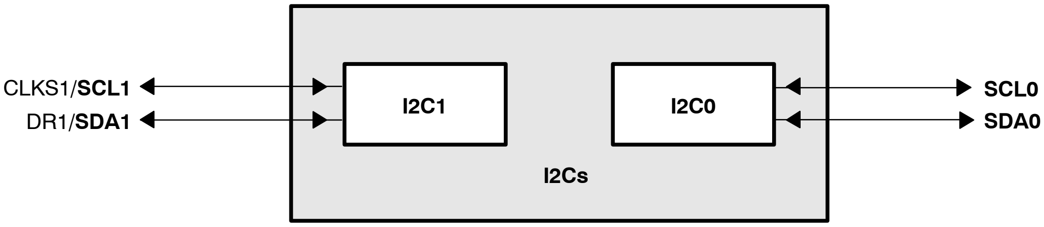
NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 4. CPU (DSP Core) and Peripheral Signals

signal groups description (continued)





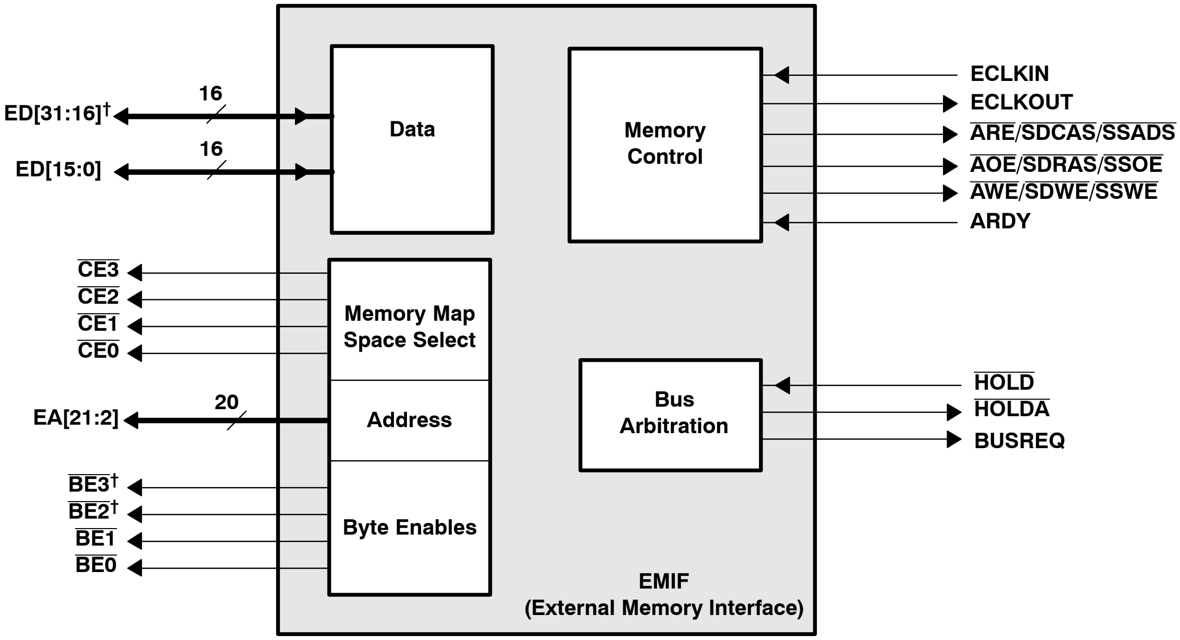


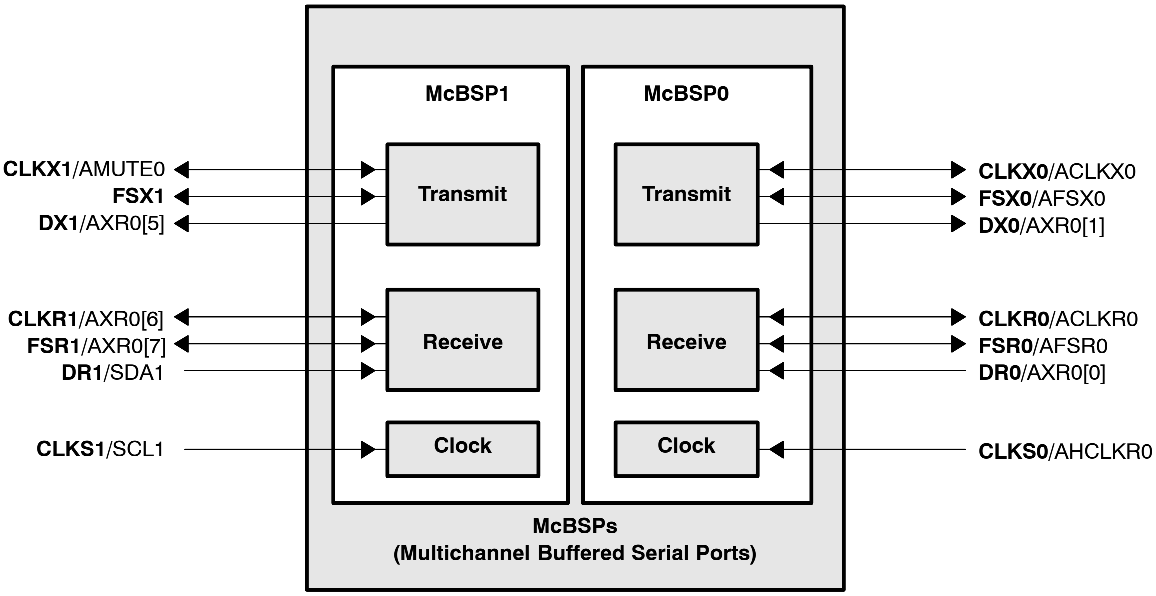
† The GP[15:0] pins, through interrupt sharing, are external interrupt capable via GPINT0. GP[15:0] are also external EDMA event source capable. For more details, see the External Interrupt Sources and External EDMA Event Sources sections of this data sheet.

NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 5. Peripheral Signals

signal groups description (continued)



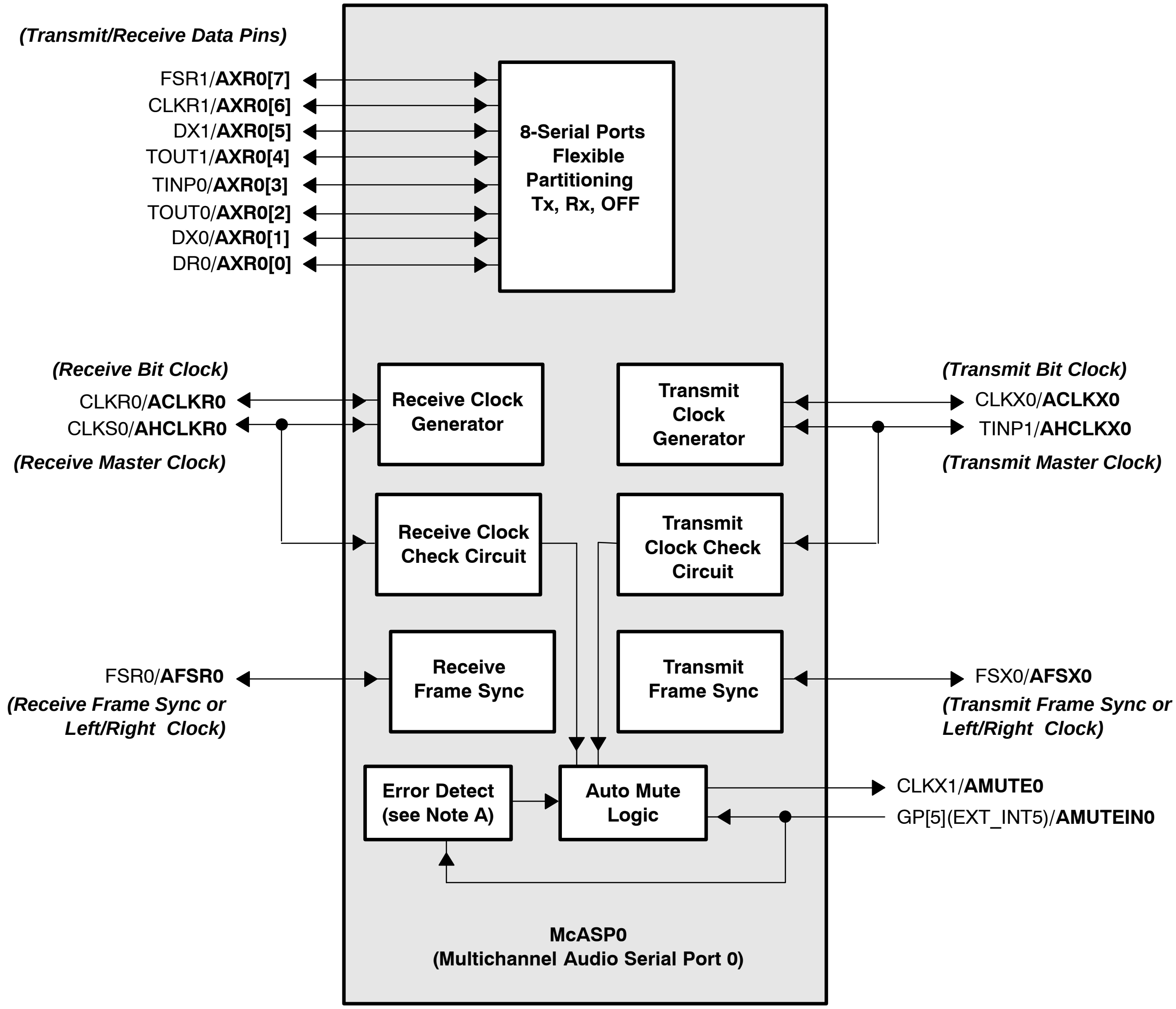


† These external pins are applicable to the GDP package only.

NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 5. Peripheral Signals (Continued)

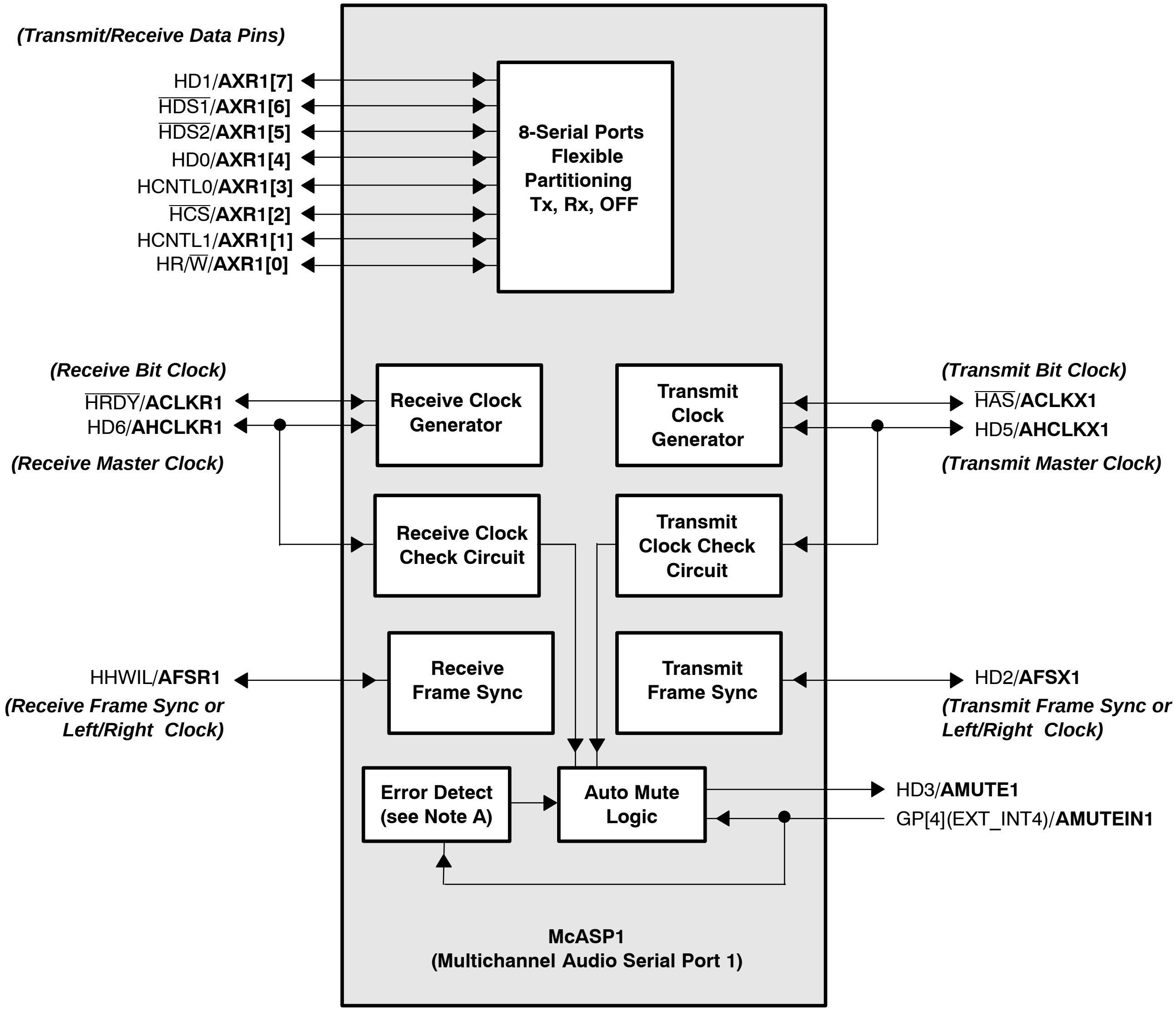
signal groups description (continued)



NOTES: A. The McASPs’ Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
B. On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.
C. Bolded and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 5. Peripheral Signals (Continued)

signal groups description (continued)



NOTES:
- A. The McASPs' Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
- B. On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.
- C. Bolded and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 5. Peripheral Signals (Continued)

DEVICE CONFIGURATIONS

On the C6713 device, bootmode and certain device configurations/peripheral selections are determined at device reset, while other device configurations/peripheral selections are software-configurable via the device configurations register (DEVCFG) [address location 0x019C0200] after device reset.

device configurations at device reset

Table 18 describes the C6713 device configuration pins, which are set up via internal or external pullup/pulldown resistors through the HPI data pins (HD[4:3] and HD8) and CLKMODE0 pin. These configuration pins must be in the desired state until reset is released. For more details on these device configuration pins, see the Terminal Functions table and the Debugging Considerations section of this data sheet.

Table 18. Device Configurations Pins at Device Reset (HD[4:3], HD8, and CLKMODE0)[†]

CONFIGURATION PIN	PYP	GDP	FUNCTIONAL DESCRIPTION
HD8	160	B17	Device Endian mode (LEND) 0 – System operates in Big Endian mode 1 – System operates in Little Endian mode (default)
HD[4:3] (BOOTMODE)	156, 154	C19, C20	Bootmode Configuration Pins (BOOTMODE) 00 – $\overline{\text{CE1}}$ width 32-bit, HPI boot/Emulation boot 01 – $\overline{\text{CE1}}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 – $\overline{\text{CE1}}$ width 16-bit, Asynchronous external ROM boot with default timings 11 – $\overline{\text{CE1}}$ width 32-bit, Asynchronous external ROM boot with default timings For more detailed information on these bootmode configurations, see the *bootmode* section of this data sheet.
CLKMODE0	205	C4	Clock generator input clock source select 0 – Reserved. Do not use. 1 – CLKIN square wave [default] **This pin *must* be pulled to the correct level even after reset.**

[†] All other HD pins (HD [15, 13:9, 7:5, 2:0]) have pullups/pulldowns (IPUs or IPDs). For proper device operation of the HD [15, 13:9, 7, 1, 0], ***do not*** oppose these pins with external pullups/pulldowns at reset; however, the HD[6, 5, 2] pins *can* be opposed and driven during reset.

DEVICE CONFIGURATIONS (CONTINUED)

peripheral pin selection at device reset

Some C6713 peripherals share the same pins (internally muxed) and are mutually exclusive (i.e., HPI, general-purpose input/output pins GP[15:8, 3, 1, 0] and McASP1).

- HPI, McASP1, and GPIO peripherals

  The HPI_EN (HD14 pin) is latched at reset. This pin selects whether the HPI peripheral pins or McASP1 peripheral pins and GP[15:8, 3, 1, 0] pins are functionally enabled (see Table 19).

Table 19. HPI_EN (HD14 Pin) Peripheral Selection (HPI or McASP1, and Select GPIO Pins)†

PERIPHERAL PIN SELECTION	PERIPHERAL PINS SELECTED		DESCRIPTION
HPI_EN (HD14 Pin) [173, C14]	HPI	McASP1 and GP[15:8,3,1,0]	
0		√	HPI_EN = 0 HPI pins are disabled; McASP1 peripheral pins and GP[15:8, 3, 1,0] pins are enabled. All multiplexed HPI/McASP1 and HPI/GPIO pins function as McASP1 and GPIO pins, respectively. To use the GPIO pins, the appropriate bits in the GPEN and GPDIR registers need to be configured.
1	√		HPI_EN = 1 HPI pins are enabled; McASP1 peripheral pins and GP[15:8, 3, 1,0] pins are disabled [default]. All multiplexed HPI/McASP1 and HPI/GPIO pins function as HPI pins.

† The HPI_EN (HD[14]) pin ***cannot*** be controlled via software.

DEVICE CONFIGURATIONS (CONTINUED)

peripheral selection/device configurations via the DEVCFG control register

The device configuration register (DEVCFG) allows the user to control the pin availability of the McBSP0, McBSP1, McASP0, I2C1, and Timer peripherals. The DEVCFG register also offers the user control of the EMIF input clock source and the timer output pins. For more detailed information on the DEVCFG register control bits, see Table 20 and Table 21.

Table 20. Device Configuration Register (DEVCFG) [Address location: 0x019C0200 – 0x019C02FF]

31–16
Reserved†
RW-0

15–5	4	3	2	1	0
Reserved†	EKSRC	TOUT1SEL	TOUT0SEL	MCBSP0DIS	MCBSP1DIS
RW-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R/W = Read/Write; -n = value after reset

† ***Do not*** write non-zero values to these bit locations.

Table 21. Device Configuration (DEVCFG) Register Selection Bit Descriptions

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. ***Do not*** write non-zero values to these bit locations.
4	EKSRC	EMIF input clock source bit. Determines which clock signal is used as the EMIF input clock. 0 = SYSCLK3 (from the clock generator) is the EMIF input clock source (default) 1 = ECLKIN external pin is the EMIF input clock source
3	TOUT1SEL	Timer 1 output (TOUT1) pin function select bit. Selects the pin function of the TOUT1/AXR0[4] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 1 output (TOUT1) pin (default) 1 = The pin functions as the McASP0 transmit/receive data pin 4 (AXR0[4]). The Timer 1 module is still active.
2	TOUT0SEL	Timer 0 output (TOUT0) pin function select bit. Selects the pin function of the TOUT0/AXR0[2] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 0 output (TOUT0) pin (default) 1 = The pin functions as the McASP0 transmit/receive data pin 2 (AXR0[2]). The Timer 0 module is still active.
1	MCBSP0DIS	Multichannel Buffered Serial Port 0 (McBSP0) disable bit. Selects whether McBSP0 or the McASP0 multiplexed peripheral pins are enabled or disabled. 0 = McBSP0 peripheral pins are enabled, McASP0 peripheral pins (AHCLKR0, ACLKR0, ACLKX0, AXR0[0], AXR0[1], AFSR0, and AFSX0) are disabled (default). [If the McASP0 data pins are available, the McASP0 peripheral is functional for DIT mode only.] 1 = McBSP0 peripheral pins are disabled, McASP0 peripheral pins (AHCLKR0, ACLKR0, ACLKX0, AXR0[0], AXR0[1], AFSR0, and AFSX0) are enabled.
0	MCBSP1DIS	Multichannel Buffered Serial Port 1 (McBSP1) disable bit. Selects whether McBSP1 or I2C1 and McASP0 multiplexed peripheral pins are enabled or disabled. 0 = McBSP1 peripheral pins are enabled, I2C1 peripheral pins (SCL1 and SDA1) and McASP0 peripheral pins (AXR0[7:5] and AMUTE0) are disabled (default) 1 = McBSP1 peripheral pins are disabled, I2C1 peripheral pins (SCL1 and SDA1) and McASP0 peripheral pins (AXR0[7:5] and AMUTE0) are enabled.

DEVICE CONFIGURATIONS (CONTINUED)

multiplexed pins

Multiplexed pins are pins that are shared by more than one peripheral and are internally multiplexed. Most of these pins are configured by software via the device configuration register (DEVCFG), and the others (specifically, the HPI pins) are configured by external pullup/pulldown resistors only at reset. The muxed pins that are configured by software can be programmed to switch functionalities at any time. The muxed pins that are configured by external pullup/pulldown resistors are mutually exclusive; only one peripheral has primary control of the function of these pins after reset. Table 22 summarizes the peripheral pins affected by the HPI_EN (HD14 pin) and DEVCFG register. Table 23 identifies the multiplexed pins on the C6713 device; shows the default (primary) function and the default settings after reset; and describes the pins, registers, etc. necessary to configure the specific multiplexed functions.

DEVICE CONFIGURATIONS (CONTINUED)

Table 22. Peripheral Pin Selection Matrix[†]

SELECTION BITS		PERIPHERAL PINS AVAILABILITY										
BIT NAME	**BIT VALUE**	**McASP0[‡]**	**McASP1**	**I2C0**	**I2C1**	**McBSP0**	**McBSP1**	**TIMER0**	**TIMER1**	**HPI**	**GPIO PINS**	**EMIF**
HPI_EN (boot config pin)	0		AHCLKX1 AHCLKR1 ACLKX1 ACLKR1 AFSX1 AFSR1 AMUTE1 AXR1[0] to AXR1[7]							None	GP[0:1], GP[3], GP[8:15] Plus: GP[2] ctrl'd by GP2EN bit	
	1		None							All	**NO** GP[0:1], GP[3], GP[8:15]	
MCBSP0DIS (DEVCFG bit)	0	None				All						
	1	ACLKK0 ACLKR0 AFSX0 AFSR0 AHCLKR0 AXR0[0] AXR0[1]				None						
MCBSP1DIS (DEVCFG bit)	0	**NO** AMUTE0 AXR0[5] AXR0[6] AXR0[7]			None		All					
	1	AMUTE0 AXR0[5] AXR0[6] AXR0[7]			All		None					
TOUT0SEL (DEVCFG bit)	0	**NO** AXR0[2]						TOUT0				
	1	AXR0[2]						**NO** TOUT0				
TOUT1SEL (DEVCFG bit)	0	**NO** AXR0[4]							TOUT1			
	1	AXR0[4]							**NO** TOUT1			

[†] Gray blocks indicate that the peripheral is not affected by the selection bit.

[‡] The McASP0 pins AXR0[3] and AHCLKX0 are shared with the timer input pins TINP0 and TINP1, respectively. See Table 23 for more detailed information.

DEVICE CONFIGURATIONS (CONTINUED)

Table 23. C6713 Device Multiplexed/Shared Pins

MULTIPLEXED PINS			DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
NAME	**PYP**	**GDP**			
CLKOUT2/GP[2]	82	Y12	CLKOUT2	GP2EN = 0 (GPEN register bit) GP[2] function disabled, CLKOUT2 enabled	When the CLKOUT2 pin is enabled , the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin. CLK2EN = 0: CLKOUT2 held high CLK2EN = 1: CLKOUT2 enabled to clock [default] To use these software-configurable GPIO pins, the GPxEN bits in the GP Enable Register and the GPxDIR bits in the GP Direction Register must be properly configured. GPxEN = 1: GP[x] pin enabled GPxDIR = 0: GP[x] pin is an input GPxDIR = 1: GP[x] pin is an output To use AMUTEIN0/1 pin function, the GP[5]/GP[4] pins must be configured as an input, the INEN bit set to 1, and the polarity through the INPOL bit selected in the associated McASP AMUTE register.
GP[5](EXT_INT5)/AMUTEIN0	6	C1	GP[5](EXT_INT5)	No Function GPxDIR = 0 (input) GP5EN = 0 (disabled) GP4EN = 0 (disabled) [(GPEN register bits) GP[x] function disabled]	
GP[4](EXT_INT4)/AMUTEIN1	1	C2	GP[4](EXT_INT4)		
CLKS0/AHCLKR0	28	K3	McBSP0 pin function	MCBSP0DIS = 0 (DEVCFG register bit) McASP0 pins disabled, McBSP0 pins enabled	By default, McBSP0 peripheral pins are enabled upon reset (McASP0 pins are disabled). To enable the McASP0 peripheral pins, the MCBSP0DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP0 peripheral pins).
DR0/AXR0[0]	27	J1			
DX0/AXR0[1]	20	H2			
FSR0/AFSR0	24	J3			
FSX0/AFSX0	21	H1			
CLKR0/ACLKR0	19	H3			
CLKX0/ACLKX0	16	G3			
CLKS1/SCL1	8	E1	McBSP1 pin function	MCBSP1DIS = 0 (DEVCFG register bit) I2C1 and McASP0 pins disabled, McBSP1 pins enabled	By default, McBSP1 peripheral pins are enabled upon reset (I2C1 and McASP0 pins are disabled). To enable the I2C1 and McASP0 peripheral pins, the MCBSP1DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP1 peripheral pins).
DR1/SDA1	37	M2			
DX1/AXR0[5]	32	L2			
FSR1/AXR0[7]	38	M3			
CLKR1/AXR0[6]	36	M1			
CLKX1/AMUTE0	33	L3			

DEVICE CONFIGURATIONS (CONTINUED)

Table 23. C6713 Device Multiplexed/Shared Pins (Continued)

MULTIPLEXED PINS			DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
NAME	PYP	GDP			
$\overline{\text{HINT}}$/GP[1]	135	J20	HPI pin function	HPI_EN (HD14 pin) = 1 (HPI enabled) McASP1 pins and eleven GPIO pins are disabled.	By default, the HPI peripheral pins are enabled at reset. McASP1 peripheral pins and eleven GPIO pins are disabled. To enable the McASP1 peripheral pins and the eleven GPIO pins, an external pulldown resistor must be provided on the HD14 pin setting HPI_EN = 0 at reset. To use these software-configurable GPIO pins, the GPxEN bits in the GP Enable Register and the GPxDIR bits in the GP Direction Register must be properly configured. GPxEN = 1: GP[x] pin enabled GPxDIR = 0: GP[x] pin is an input GPxDIR = 1: GP[x] pin is an output McASP1 pin direction is controlled by the PDIR[x] bits in the McASP1PDIR register.
HD15/GP[15]	174	B14			
HD14/GP[14]	173	C14			
HD13/GP[13]	172	A15			
HD12/GP[12]	168	C15			
HD11/GP[11]	167	A16			
HD10/GP[10]	166	B16			
HD9/GP[9]	165	C16			
HD8/GP[8]	160	B17			
HD7/GP[3]	164	A18			
HD4/GP[0]	156	C19			
HD1/AXR1[7]	152	D20			
HD0/AXR1[4]	147	E20			
HCNTL1/AXR1[1]	144	G19			
HCNTL0/AXR1[3]	146	G18			
HR/$\overline{\text{W}}$/AXR1[0]	143	G20			
$\overline{\text{HDS1}}$/AXR1[6]	151	E19			
$\overline{\text{HDS2}}$/AXR1[5]	150	F18			
$\overline{\text{HCS}}$/AXR1[2]	145	F20			
HD6/AHCLKR1	161	C17			
HD5/AHCLKX1	159	B18			
HD3/AMUTE1	154	C20			
HD2/AFSX1	155	D18			
HHWIL/AFSR1	139	H20			
$\overline{\text{HRDY}}$/ACLKR1	140	H19			
$\overline{\text{HAS}}$/ACLKX1	153	E18			
TINP0/AXR0[3]	17	G2	Timer 0 input function	McASP0PDIR = 0 (input) [specifically AXR0[3] bit]	By default, the Timer 0 input pin is enabled (and a shared input until the McASP0 peripheral forces an output). McASP0PDIR = 0 input, = 1 output
TOUT0/AXR0[2]	18	G1	Timer 0 output function	TOUT0SEL = 0 (DEVCFG register bit) [TOUT0 pin enabled and McASP0 AXR0[2] pin disabled]	By default, the Timer 0 output pin is enabled. To enable the McASP0 AXR0[2] pin, the TOUT0SEL bit in the DEVCFG register must be set to 1 (disabling the Timer 0 peripheral output pin function). The AXR2 bit in the McASP0PDIR register controls the direction (input/output) of the AXR0[2] pin McASP0PDIR = 0 input, = 1 output

DEVICE CONFIGURATIONS (CONTINUED)

Table 23. C6713 Device Multiplexed/Shared Pins (Continued)

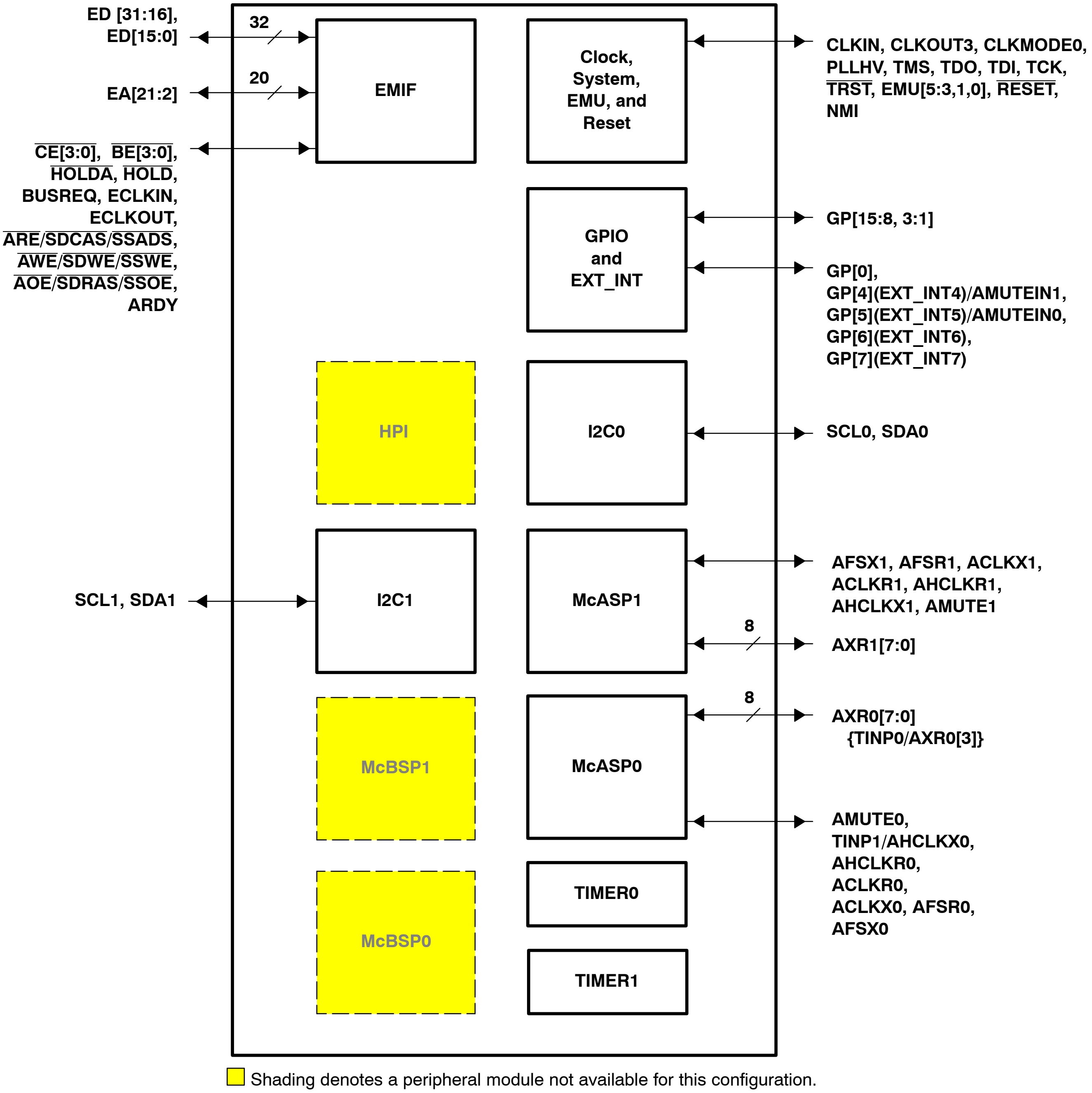
MULTIPLEXED PINS NAME	PYP	GDP	DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
TINP1/AHCLKX0	12	F2	Timer 1 input function	McASP0PDIR = 0 (input) [specifically AHCLKX bit]	By default, the Timer 1 input and McASP0 clock function are enabled as inputs. For the McASP0 clock to function as an output: McASP0PDIR = 1 (specifically the AHCLKX bit]
TOUT1/AXR0[4]	13	F1	Timer 1 output function	TOUT1SEL = 0 (DEVCFG register bit) [TOUT1 pin enabled and McASP0 AXR0[4] pin disabled]	By default, the Timer 1 output pin is enabled. To enable the McASP0 AXR0[4] pin, the TOUT1SEL bit in the DEVCFG register must be set to 1 (disabling the Timer 1 peripheral output pin function). The AXR4 bit in the McASP0PDIR register controls the direction (input/output) of the AXR0[4] pin McASP0PDIR = 0 input, = 1 output

configuration examples

Figure 6 through Figure 11 illustrate examples of peripheral selections that are configurable on this device.

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



DEVCFG Register Value:

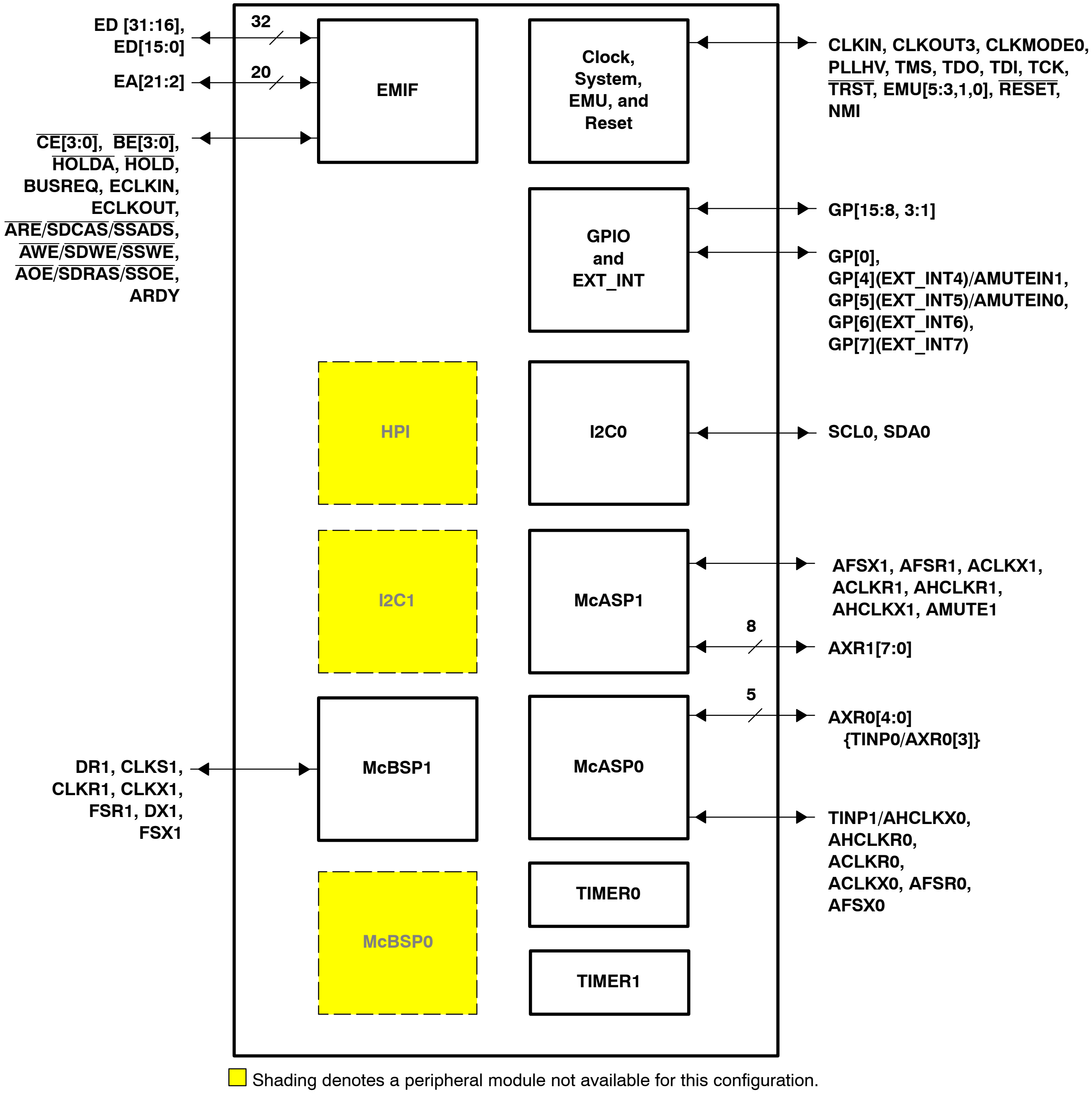
0x0000 000F
MCBSP0DIS = 1
MCBSP1DIS = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (enabling GPEN.[2])

Figure 6. Configuration Example A (2 I2C + 2 McASP + GPIO)

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



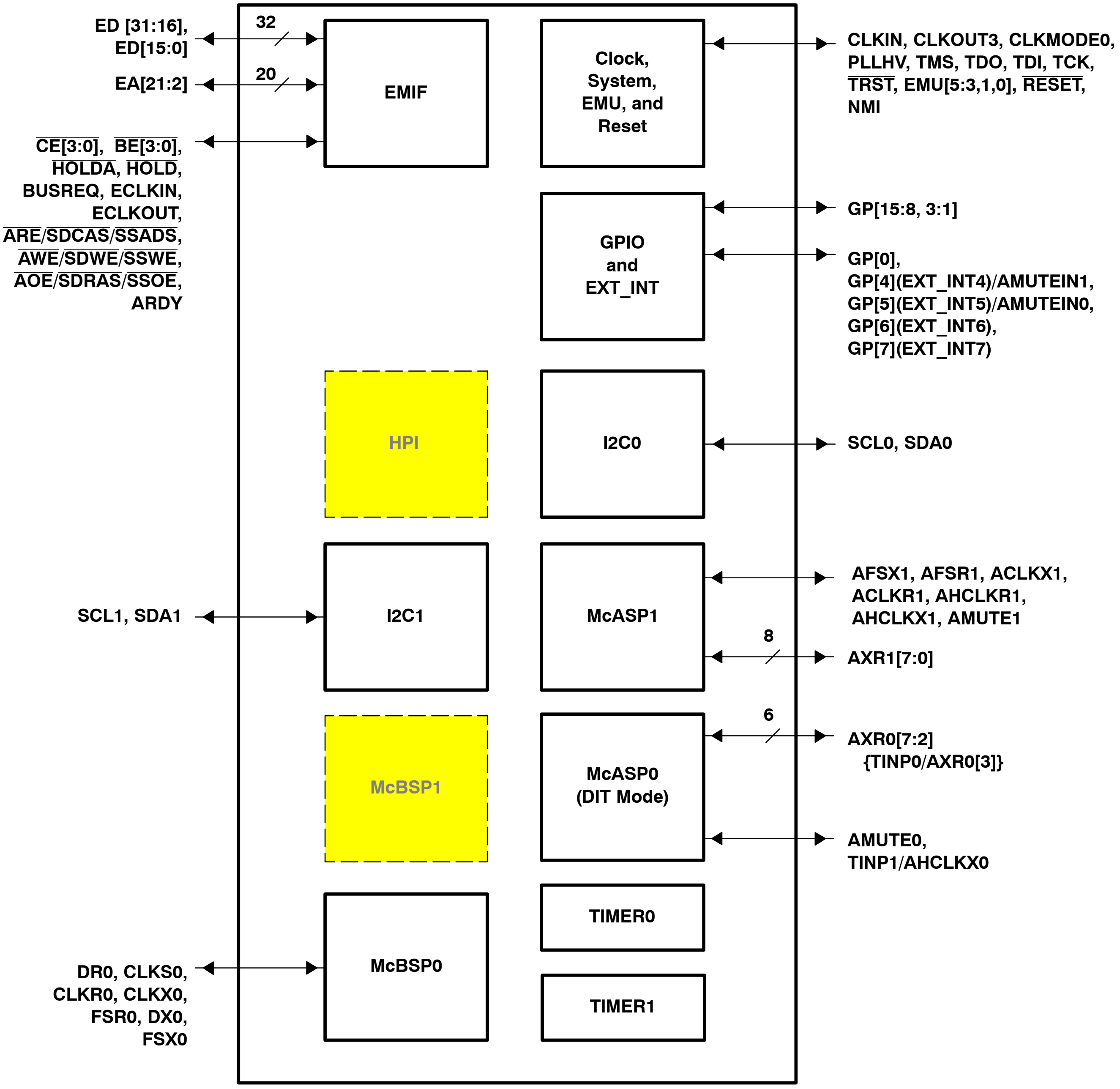
DEVCFG Register Value:
0x0000 000E
MCBSP0DIS = 1
MCBSP1DIS = 0
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (enabling GPEN.[2])

Figure 7. Configuration Example B (1 I2C + 1 McBSP + 2 McASP + GPIO)

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



🟨 Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value:

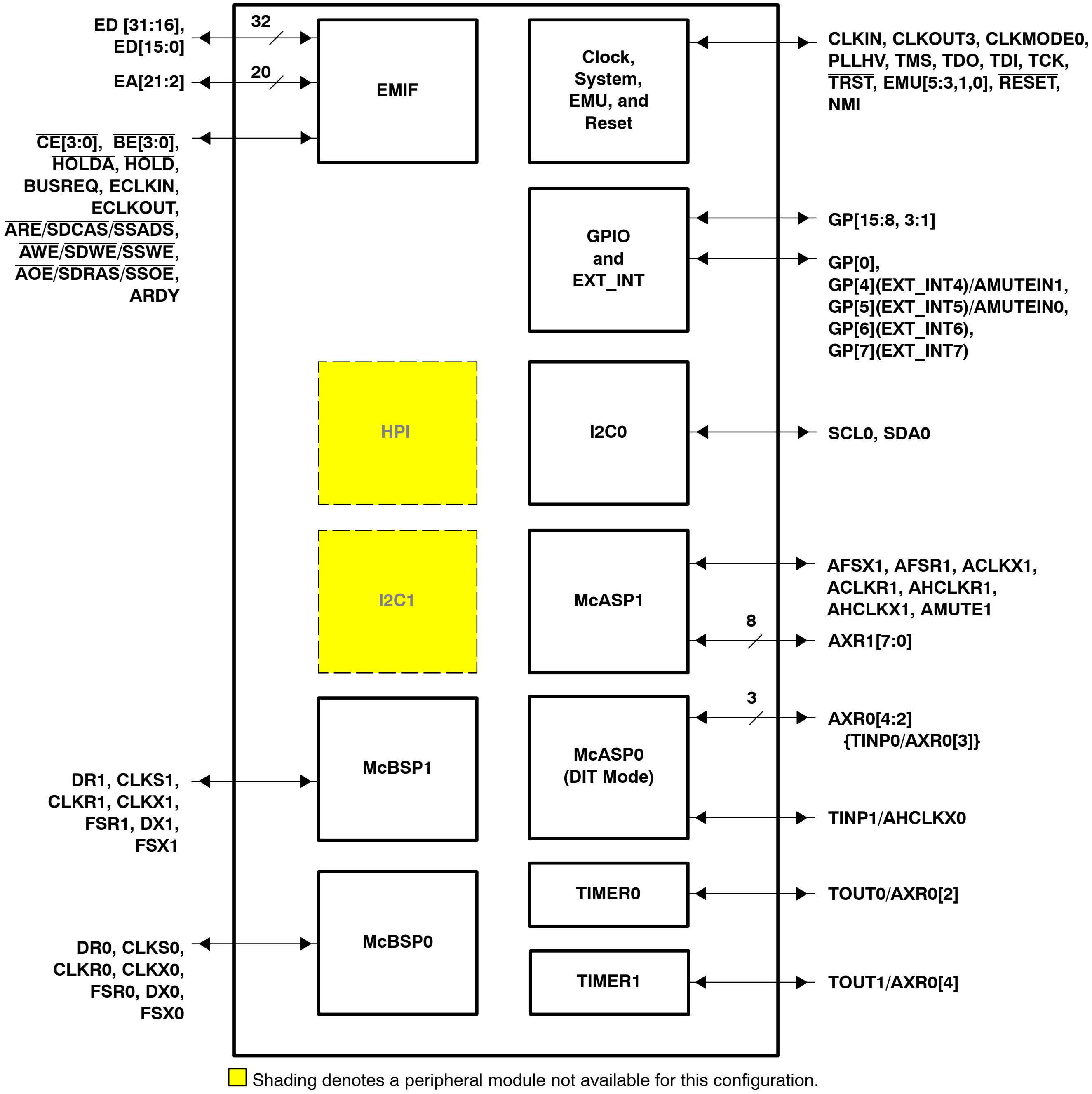
0x0000 000D
MCBSP0DIS = 0
MCBSP1DIS = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (enabling GPEN.[2])

Figure 8. Configuration Example C [2 I2C + 1 McBSP + 1 McASP + 1 McASP (DIT) + GPIO]

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



🟨 Shading denotes a peripheral module not available for this configuration.

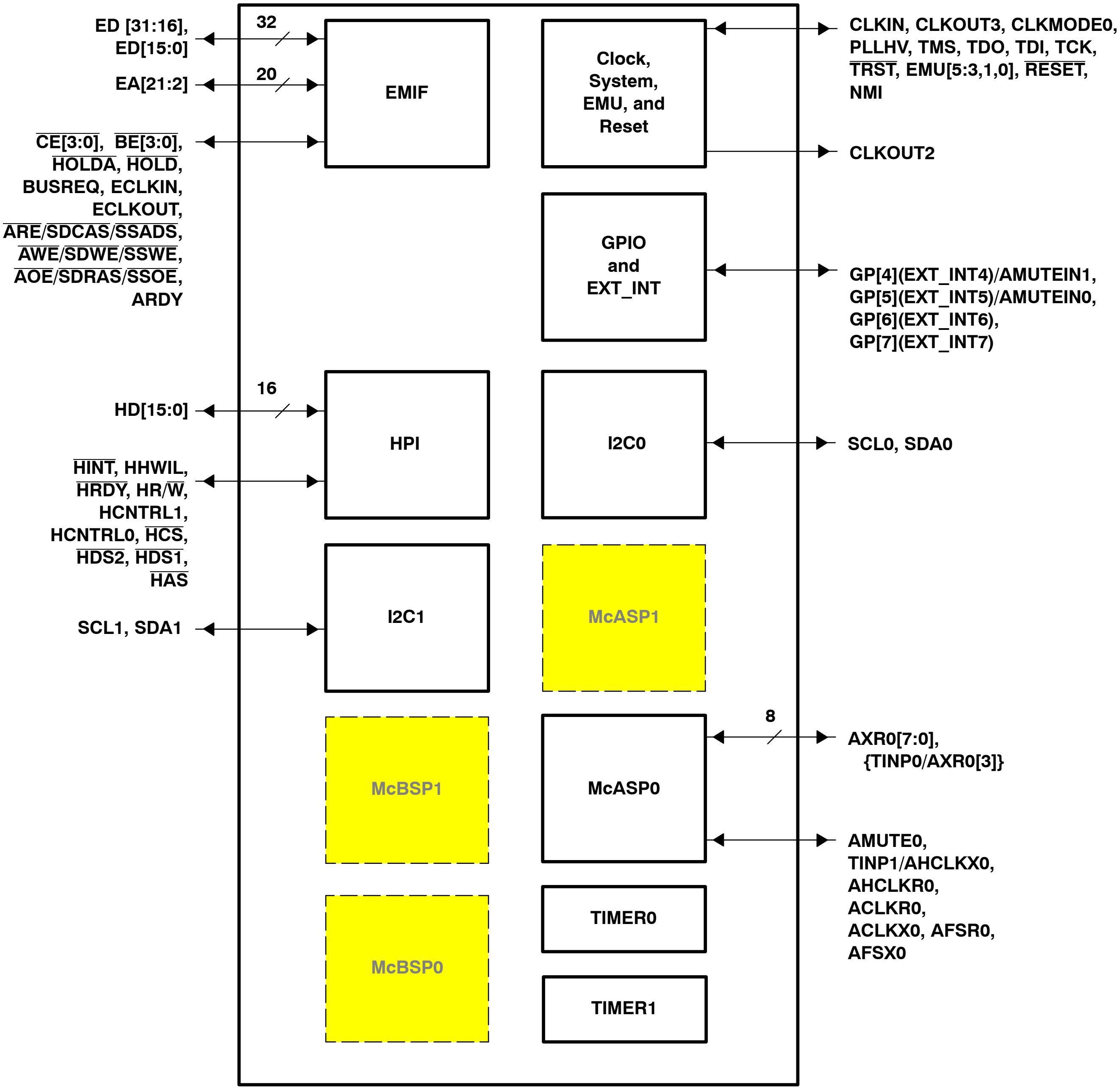
DEVCFG Register Value:
0x0000 000C
MCBSP0DIS = 0
MCBSP1DIS = 0
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (enabling GPEN.[2])

Figure 9. Configuration Example D [1 I2C + 2 McBSP + 1 McASP + 1 McASP (DIT) + GPIO + Timers]

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



🟨 Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value:

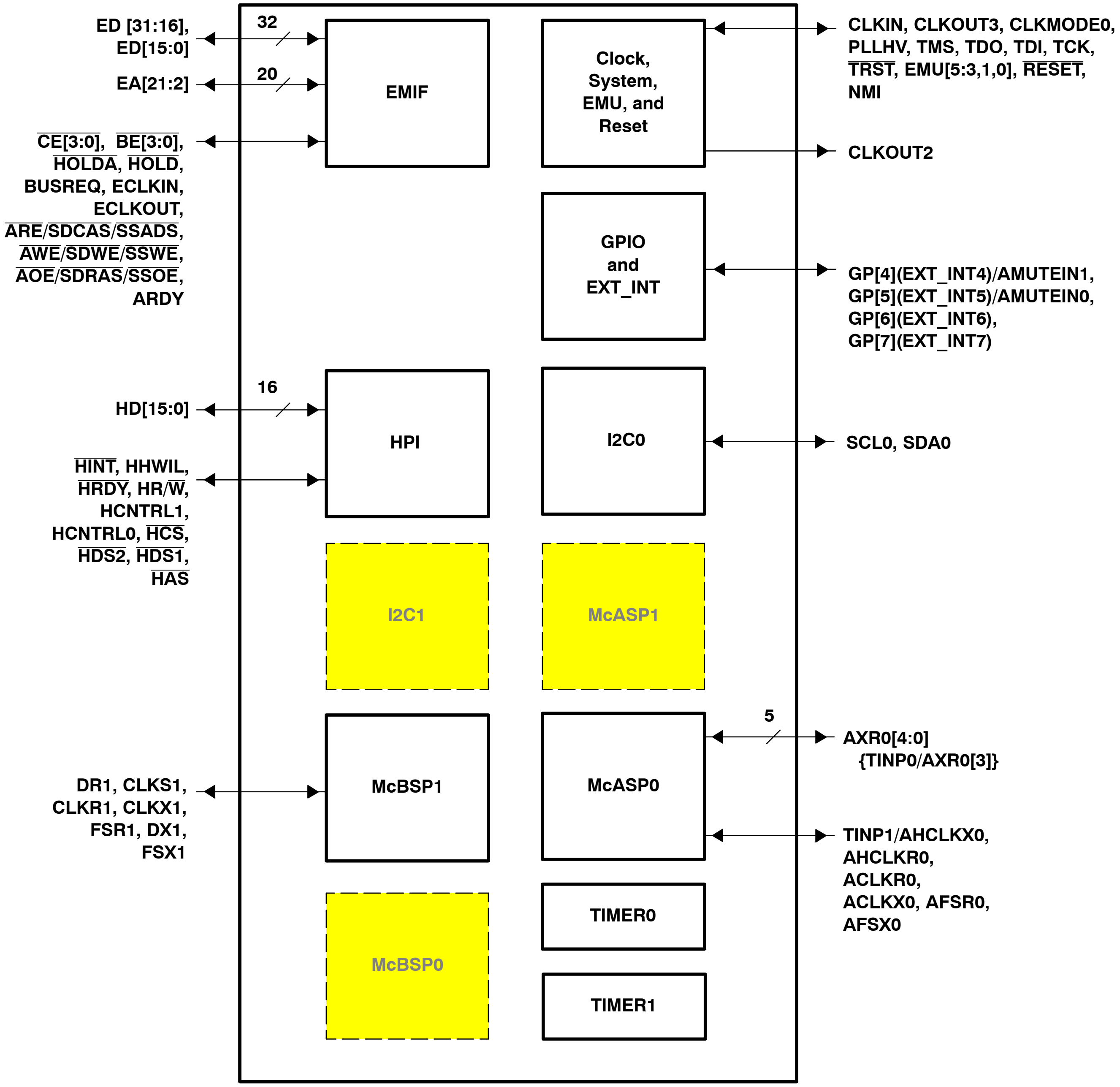
0x0000 000F
MCBSP0DIS = 1
MCBSP1DIS = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 1
GP2EN BIT = 0 (enabling GPEN.[2])

Figure 10. Configuration Example E (1 I2C + HPI + 1 McASP)

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



🟨 Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value:

0x0000 000E
MCBSP0DIS = 1
MCBSP1DIS = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 1
GP2EN BIT = 0 (enabling GPEN.[2])

Figure 11. Configuration Example F (1 McBSP + HPI + 1 McASP)

DEVICE CONFIGURATIONS (CONTINUED)

debugging considerations

It is recommended that external connections be provided to peripheral selection/device configuration pins, including HD[14, 8, 4, 3], and CLKMODE0. Although internal pullup resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes.

Internal pullup/pulldown resistors also exist on the non-configuration pins on the HPI data bus (HD[15, 13:9, 7:5, 2:0]). For proper device operation of the HD[15, 13:9, 7, 1, 0], ***do not*** oppose the internal pullup/pulldown resistors on these non-configuration pins with external pullup/pulldown resistors. If an external controller provides signals to these HD[15, 13:9, 7, 1, 0] non-configuration pins, these signals must be driven to the default state of the pins at reset, or not be driven at all. However, the HD[6, 5, 2] non-configuration pins *can* be opposed and driven during reset.

For the internal pullup/pulldown resistors for all device pins, see the terminal functions table.

TERMINAL FUNCTIONS

The terminal functions table identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see the Device Configurations section of this data sheet.

Terminal Functions

SIGNAL NAME	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
	PYP	GDP			
CLOCK/PLL CONFIGURATION					
CLKIN	204	A3	I	IPD	Clock Input
CLKOUT2/GP[2]	82	Y12	O/Z	IPD	Clock output at half of device speed (**O**/**Z**) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] pin (I/O/Z)
CLKOUT3	184	D10	O	IPD	Clock output programmable by OSCDIV1 register in the PLL controller.
CLKMODE0	205	C4	I	IPU	Clock generator input clock source select 0 – Reserved, do not use. 1 – CLKIN square wave [default] For proper device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor.
PLLHV	202	C5	A[§]		Analog power (3.3 V) for PLL (PLL Filter)
JTAG EMULATION					
TMS	192	B7	I	IPU	JTAG test-port mode select
TDO	187	A8	O/Z	IPU	JTAG test-port data out
TDI	191	A7	I	IPU	JTAG test-port data in
TCK	193	A6	I	IPU	JTAG test-port clock
$\overline{\text{TRST}}$	197	B6	I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the *IEEE 1149.1 JTAG Compatibility Statement* section of this data sheet.
EMU5	—	B12	I/O/Z	IPU	Emulation pin 5. Reserved for future use, leave unconnected.
EMU4	—	C11	I/O/Z	IPU	Emulation pin 4. Reserved for future use, leave unconnected.
EMU3	—	B10	I/O/Z	IPU	Emulation pin 3. Reserved for future use, leave unconnected.
EMU2	—	D3	I/O/Z	IPU	Emulation pin 2. Reserved for future use, leave unconnected.
EMU1 EMU0	185 186	B9 D9	I/O/Z	IPU	Emulation [1:0] pins • Select the device functional mode of operation EMU[1:0] Operation 00 Boundary Scan/Functional Mode (see Note) 01 Reserved 10 Reserved 11 Emulation/Functional Mode [default] (see the *IEEE 1149.1 JTAG Compatibility Statement* section of this data sheet) The DSP can be placed in Functional mode when the EMU[1:0] pins are configured for either Boundary Scan or Emulation. Note: When the EMU[1:0] pins are configured for Boundary Scan mode, the internal pulldown (IPD) on the $\overline{\text{TRST}}$ signal must ***not*** be opposed in order to operate in Functional mode. For the Boundary Scan mode drive EMU[1:0] *and* $\overline{\text{RESET}}$ pins low.
RESETS AND INTERRUPTS					
$\overline{\text{RESET}}$	176	A13	I	IPU	Device reset. When using Boundary Scan mode, drive the EMU[1:0] *and* $\overline{\text{RESET}}$ pins low.
NMI	175	C13	I	IPD	Nonmaskable interrupt • Edge-driven (rising edge)

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

[§] A = Analog signal

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GDP	TYPE†	IPD/ IPU‡	DESCRIPTION
RESETS AND INTERRUPTS (CONTINUED)					
GP[7](EXT_INT7)	7	E3	I/O/Z	IPU	General-purpose input/output pins (**I**/**O**/**Z**) which also function as external interrupts • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]), in addition to the GPIO registers. GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INEN bit in the associated McASP AMUTE register.
GP[6](EXT_INT6)	2	D2			
GP[5](EXT_INT5)/ AMUTEIN0	6	C1			
GP[4](EXT_INT4)/ AMUTEIN1	1	C2			
HOST-PORT INTERFACE (HPI)					
$\overline{\text{HINT}}$/GP[1]	135	J20	O/Z	IPU	Host interrupt (from DSP to host) (**O**) [default] or this pin can be programmed as a GP[1] pin (I/O/Z).
HCNTL1/AXR1[1]	144	G19	I	IPU	Host control − selects between control, address, or data registers (**I**) [default] or McASP1 data pin 1 (I/O/Z).
HCNTL0/AXR1[3]	146	G18	I	IPU	Host control − selects between control, address, or data registers (**I**) [default] or McASP1 data pin 3 (I/O/Z).
HHWIL/AFSR1	139	H20	I	IPU	Host half-word select − first or second half-word (not necessarily high or low order) (**I**) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z).
HR/$\overline{\text{W}}$/AXR1[0]	143	G20	I	IPU	Host read or write select (**I**) [default] or McASP1 data pin 0 (I/O/Z).
HD15/GP[15]	174	B14	I/O/Z	IPU	Host-port data pins (**I**/**O**/**Z**) [default] or general-purpose input/output pins (I/O/Z) • Used for transfer of data, address, and control • Also controls initialization of DSP modes at reset via pullup/pulldown resistors − Device Endian mode (HD8) 0 − Big Endian 1 − Little Endian − Boot mode (HD[4:3]) 00 − $\overline{\text{CE1}}$ width 32-bit, HPI boot/Emulation boot 01 − $\overline{\text{CE1}}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 − $\overline{\text{CE1}}$ width 16-bit, Asynchronous external ROM boot with default timings 11 − $\overline{\text{CE1}}$ width 32-bit, Asynchronous external ROM boot with default timings − HPI_EN (HD14) 0 − HPI disabled, McASP1 enabled 1 − HPI enabled, McASP1 disabled (default) Other HD pins (HD [15, 13:9, 7:5, 2:0] have pullups/pulldowns (IPUs/IPDs). For proper device operation of the HD[15, 13:9, 7, 1, 0], ***do not*** oppose these pins with external IPUs/IPDs at reset; however, the HD[6, 5, 2] pins *can* be opposed and driven at reset. For more details, see the Device Configurations section of this data sheet.
HD14/GP[14]	173	C14		IPU	
HD13/GP[13]	172	A15		IPU	
HD12/GP[12]	168	C15		IPU	
HD11/GP[11]	167	A16		IPU	
HD10/GP[10]	166	B16		IPU	
HD9/GP[9]	165	C16		IPU	
HD8/GP[8]	160	B17		IPU	
HD7/GP[3]	164	A18		IPU	
HD6/AHCLKR1	161	C17	I/O/Z	IPU	Host-port data pin 6 (**I**/**O**/**Z**) [default] or McASP1 receive high-frequency master clock (I/O/Z).
HD5/AHCLKX1	159	B18		IPU	Host-port data pin 5 (**I**/**O**/**Z**) [default] or McASP1 transmit high-frequency master clock (I/O/Z).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
	PYP	GDP			
HOST-PORT INTERFACE (HPI) (CONTINUED)					
HD4/GP[0]	156	C19	I/O/Z	IPD	Host-port data pin 4 (**I/O/Z**) [default] or this pin can be programmed as a GP[0] pin (I/O/Z).
HD3/AMUTE1	154	C20	I/O/Z	IPU	Host-port data pin 3 (**I/O/Z**) [default] or McASP1 mute output (O/Z).
HD2/AFSX1	155	D18		IPU	Host-port data pin 2 (**I/O/Z**) [default] or McASP1 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
HD1/AXR1[7]	152	D20		IPU	Host-port data pin 1 (**I/O/Z**) [default] or McASP1 data pin 7 (I/O/Z).
HD0/AXR1[4]	147	E20	I/O/Z	IPU	Host-port data pin 0 (**I/O/Z**) [default] or McASP1 data pin 4 (I/O/Z).
$\overline{\text{HAS}}$/ACLKX1	153	E18	I	IPU	Host address strobe (**I**) [default] or McASP1 transmit bit clock (I/O/Z).
$\overline{\text{HCS}}$/AXR1[2]	145	F20	I	IPU	Host chip select (**I**) [default] or McASP1 data pin 2 (I/O/Z).
$\overline{\text{HDS1}}$/AXR1[6]	151	E19	I	IPU	Host data strobe 1 (**I**) [default] or McASP1 data pin 6 (I/O/Z).
$\overline{\text{HDS2}}$/AXR1[5]	150	F18	I	IPU	Host data strobe 2 (**I**) [default] or McASP1 data pin 5 (I/O/Z) .
$\overline{\text{HRDY}}$/ACLKR1	140	H19	O/Z	IPD	Host ready (from DSP to host) (**O**) [default] or McASP1 receive bit clock (I/O/Z).
EMIF − COMMON SIGNALS TO ALL TYPES OF MEMORY[¶]					
$\overline{\text{CE3}}$	57	V6	O/Z	IPU	Memory space enables • Enabled by bits 28 through 31 of the word address • Only one asserted during any external data access
$\overline{\text{CE2}}$	61	W6	O/Z	IPU	
$\overline{\text{CE1}}$	103	W18	O/Z	IPU	
$\overline{\text{CE0}}$	102	V17	O/Z	IPU	
$\overline{\text{BE3}}$	—	V5	O/Z	IPU	Byte-enable control • Decoded from the two lowest bits of the internal address • Byte-write enables for most types of memory • Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{\text{BE2}}$	—	Y4	O/Z	IPU	
$\overline{\text{BE1}}$	108	U19	O/Z	IPU	
$\overline{\text{BE0}}$	110	V20	O/Z	IPU	
EMIF − BUS ARBITRATION[¶]					
$\overline{\text{HOLDA}}$	137	J18	O/Z	IPU	Hold-request-acknowledge to the host
$\overline{\text{HOLD}}$	138	J17	I	IPU	Hold request from the host
BUSREQ	136	J19	O/Z	IPU	Bus request output
EMIF − ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL[¶]					
ECLKIN	78	Y11	I	IPD	External EMIF input clock source
ECLKOUT	77	Y10	O/Z	IPD	EMIF output clock depends on the EKSRC bit (DEVCFG.[4]) and on EKEN bit (GBLCTL.[5]). EKSRC = 0 – ECLKOUT is based on the internal SYSCLK3 signal from the clock generator (default). EKSRC = 1 – ECLKOUT is based on the the external EMIF input clock source pin (ECLKIN) EKEN = 0 – ECLKOUT held low EKEN = 1 – ECLKOUT enabled to clock (default)
$\overline{\text{ARE}}$/SDCAS/ $\overline{\text{SSADS}}$	79	V11	O/Z	IPU	Asynchronous memory read enable/SDRAM column-address strobe/SBSRAM address strobe
$\overline{\text{AOE}}$/SDRAS/ $\overline{\text{SSOE}}$	75	W10	O/Z	IPU	Asynchronous memory output enable/SDRAM row-address strobe/SBSRAM output enable

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

[¶] To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
	PYP	GDP			
EMIF − ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL[¶] (CONTINUED)					
$\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/ $\overline{\text{SSWE}}$	83	V12	O/Z	IPU	Asynchronous memory write enable/SDRAM write enable/SBSRAM write enable
ARDY	56	Y5	I	IPU	Asynchronous memory ready input
EMIF − ADDRESS[¶]					
EA21	109	U18	O/Z	IPU	External address (word, half-word, and byte address) The EMIF adjusts the address based on memory width: Width Pins Address 32 21:2 21 through 2 16 21:2 20 through 1 8 21:2 19 through 0 For more details on address width adjustments, see the External Memory Interface (EMIF) chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).
EA20	101	Y18			
EA19	100	W17			
EA18	95	Y16			
EA17	99	V16			
EA16	92	Y15			
EA15	94	W15			
EA14	90	Y14			
EA13	91	W14			
EA12	93	V14			
EA11	86	W13			
EA10	76	V10			
EA9	74	Y9			
EA8	71	V9			
EA7	70	Y8			
EA6	69	W8			
EA5	68	V8			
EA4	64	W7			
EA3	63	V7			
EA2	62	Y6			
EMIF − DATA[¶]					
ED31	—	N3	I/O/Z	IPU	External data pins (ED[31:16] pins applicable to GDP package only)
ED30	—	P3			
ED29	—	P2			
ED28	—	P1			
ED27	—	R2			
ED26	—	R3			
ED25	—	T2			
ED24	—	T1			
ED23	—	U3			
ED22	—	U1			
ED21	—	U2			
ED20	—	V1			
ED19	—	V2			

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

[¶] To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GDP	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF − DATA¶ (CONTINUED)					
ED18	—	Y3	I/O/Z	IPU	External data pins (ED[31:16] pins applicable to GDP package only)
ED17	—	W4			
ED16	—	V4			
ED15	112	T19			
ED14	113	T20			
ED13	111	T18			
ED12	118	R20			
ED11	117	R19			
ED10	120	P20			
ED9	119	P18			
ED8	123	N20			
ED7	122	N19			
ED6	121	N18			
ED5	128	M20			
ED4	127	M19			
ED3	129	L19			
ED2	130	L18			
ED1	131	K19			
ED0	132	K18			
MULTICHANNEL AUDIO SERIAL PORT 1 (McASP1)					
GP[4](EXT_INT4)/ AMUTEIN1	1	C2	I/O/Z	IPU	General-purpose input/output pin 4 and external interrupt 4 (**I**/**O**/**Z**) [default] or McASP1 mute input (I/O/Z).
HD3/AMUTE1	154	C20	I/O/Z	IPU	Host-port data pin 3 (**I**/**O**/**Z**) [default] or McASP1 mute output (O/Z).
$\overline{\text{HRDY}}$/ACLKR1	140	H19	I/O/Z	IPD	Host ready (from DSP to host) (**O**) [default] or McASP1 receive bit clock (I/O/Z).
HD6/AHCLKR1	161	C17	I/O/Z	IPU	Host-port data pin 6 (**I**/**O**/**Z**) [default] or McASP1 receive high-frequency master clock (I/O/Z).
$\overline{\text{HAS}}$/ACLKX1	153	E18	I/O/Z	IPU	Host address strobe (**I**) [default] or McASP 1 transmit bit clock (I/O/Z).
HD5/AHCLKX1	159	B18	I/O/Z	IPU	Host-port data pin 5 (**I**/**O**/**Z**) [default] or McASP1 transmit high-frequency master clock (I/O/Z).
HHWIL/AFSR1	139	H20	I/O/Z	IPU	Host half-word select − first or second half-word (not necessarily high or low order) (**I**) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z).
HD2/AFSX1	155	D18	I/O/Z	IPU	Host-port data pin 2 (**I**/**O**/**Z**) [default] or McASP1 transmit frame sync or left/ right clock (LRCLK) (I/O/Z).
HD1/AXR1[7]	152	D20	I/O/Z	IPU	Host-port data pin 1 (**I**/**O**/**Z**) [default] or McASP1 TX/RX data pin 7 (I/O/Z).
$\overline{\text{HDS1}}$/AXR1[6]	151	E19	I/O/Z	IPU	Host data strobe 1 (**I**) [default] or McASP1 TX/RX data pin 6 (I/O/Z).
$\overline{\text{HDS2}}$/AXR1[5]	150	F18	I/O/Z	IPU	Host data strobe 2 (**I**) [default] or McASP1 TX/RX data pin 5 (I/O/Z).
HD0/AXR1[4]	147	E20	I/O/Z	IPU	Host-port data pin 0 (**I**/**O**/**Z**) [default] or McASP1 TX/RX data pin 4 (I/O/Z).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

¶ To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
MULTICHANNEL AUDIO SERIAL PORT 1 (McASP1) (CONTINUED)					
HCNTL0/AXR1[3]	146	G18	I/O/Z	IPU	Host control − selects between control, address, or data registers (**I**) [default] or McASP1 TX/RX data pin 3 (I/O/Z).
$\overline{\text{HCS}}$/AXR1[2]	145	F20	I/O/Z	IPU	Host chip select (**I**) [default] or McASP1 TX/RX data pin 2 (I/O/Z).
HCNTL1/AXR1[1]	144	G19	I/O/Z	IPU	Host control − selects between control, address, or data registers (**I**) [default] or McASP1 TX/RX data pin 1 (I/O/Z).
HR/$\overline{\text{W}}$/AXR1[0]	143	G20	I/O/Z	IPU	Host read or write select (**I**) [default] or McASP1 TX/RX data pin 0 (I/O/Z).
MULTICHANNEL AUDIO SERIAL PORT 0 (McASP0)					
GP[5](EXT_INT5)/ AMUTEIN0	6	C1	I/O/Z	IPU	General-purpose input/output pin 5 and external interrupt 5 (**I**/**O**/**Z**) [default] or McASP0 mute input (I/O/Z).
CLKX1/AMUTE0	33	L3	I/O/Z	IPD	McBSP1 transmit clock (**I**/**O**/**Z**) [default] or McASP0 mute output (O/Z).
CLKR0/ACLKR0	19	H3	I/O/Z	IPD	McBSP0 receive clock (**I**/**O**/**Z**) [default] or McASP0 receive bit clock (I/O/Z).
TINP1/AHCLKX0	12	F2	I/O/Z	IPD	Timer 1 input (**I**) [default] or McBSP0 transmit high-frequency master clock (I/O/Z).
CLKX0/ACLKX0	16	G3	I/O/Z	IPD	McBSP0 transmit clock (**I**/**O**/**Z**) [default] or McASP0 transmit bit clock (I/O/Z).
CLKS0/AHCLKR0	28	K3	I/O/Z	IPD	McBSP0 external clock source (as opposed to internal) (**I**) [default] or McASP0 receive high-frequency master clock (I/O/Z).
FSR0/AFSR0	24	J3	I/O/Z	IPD	McBSP0 receive frame sync (**I**/**O**/**Z**) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z).
FSX0/AFSX0	21	H1	I/O/Z	IPD	McBSP0 transmit frame sync (**I**/**O**/**Z**) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
FSR1/AXR0[7]	38	M3	I/O/Z	IPD	McBSP1 receive frame sync (**I**/**O**/**Z**) [default] or McASP0 TX/RX data pin 7 (I/O/Z).
CLKR1/AXR0[6]	36	M1	I/O/Z	IPD	McBSP1 receive clock (**I**/**O**/**Z**) [default] or McASP0 TX/RX data pin 6 (I/O/Z).
DX1/AXR0[5]	32	L2	I/O/Z	IPU	McBSP1 transmit data (**O**/**Z**) [default] or McASP0 TX/RX data pin 5 (I/O/Z).
TOUT1/AXR0[4]	13	F1	I/O/Z	IPD	Timer 1 output (**O**) [default] or McASP0 TX/RX data pin 4 (I/O/Z).
TINP0/AXR0[3]	17	G2	I/O/Z	IPD	Timer 0 input (**I**) [default] or McASP0 TX/RX data pin 3 (I/O/Z).
TOUT0/AXR0[2]	18	G1	I/O/Z	IPD	Timer 0 output (**O**) [default] or McASP0 TX/RX data pin 2 (I/O/Z).
DX0/AXR0[1]	20	H2	I/O/Z	IPU	McBSP0 transmit data (**O**/**Z**) [default] or McASP0 TX/RX data pin 1 (I/O/Z).
DR0/AXR0[0]	27	J1	I/O/Z	IPU	McBSP0 receive data (**I**) [default] or McASP0 TX/RX data pin 0 (I/O/Z).
TIMER 1					
TOUT1/AXR0[4]	13	F1	O	IPD	Timer 1 output (**O**) [default] or McASP0 TX/RX data pin 4 (I/O/Z).
TINP1/AHCLKX0	12	F2	I	IPD	Timer 1 input (**I**) [default] or McBSP0 transmit high-frequency master clock (I/O/Z).
TIMER0					
TOUT0/AXR0[2]	18	G1	O	IPD	Timer 0 output (**O**) [default] or McASP0 TX/RX data pin 2 (I/O/Z).
TINP0/AXR0[3]	17	G2	I	IPD	Timer 0 input (**I**) [default] or McASP0 TX/RX data pin 3 (I/O/Z).

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	IPD/ IPU‡	DESCRIPTION
	PYP	GDP			
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)					
CLKS1/SCL1	8	E1	I	—	McBSP1 external clock source (as opposed to internal) (**I**) [default] or I2C1 clock (I/O/Z). This pin does not have an internal pullup or pulldown. When this pin is used as a McBSP pin, this pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin.
CLKR1/AXR0[6]	36	M1	I/O/Z	IPD	McBSP1 receive clock (**I**/**O**/**Z**) [default] or McASP0 TX/RX data pin 6 (I/O/Z).
CLKX1/AMUTE0	33	L3	I/O/Z	IPD	McBSP1 transmit clock (**I**/**O**/**Z**) [default] or McASP0 mute output (O/Z).
DR1/SDA1	37	M2	I	—	McBSP1 receive data (**I**) [default] or I2C1 data (I/O/Z). This pin does not have an internal pullup or pulldown. When this pin is used as a McBSP pin, this pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin.
DX1/AXR0[5]	32	L2	O/Z	IPU	McBSP1 transmit data (**O**/**Z**) [default] or McASP0 TX/RX data pin 5 (I/O/Z).
FSR1/AXR0[7]	38	M3	I/O/Z	IPD	McBSP1 receive frame sync (**I**/**O**/**Z**) [default] or McASP0 TX/RX data pin 7 (I/O/Z).
FSX1	31	L1	I/O/Z	IPD	McBSP1 transmit frame sync
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)					
CLKS0/AHCLKR0	28	K3	I	IPD	McBSP0 external clock source (as opposed to internal) (**I**) [default] or McASP0 receive high-frequency master clock (I/O/Z).
CLKR0/ACLKR0	19	H3	I/O/Z	IPD	McBSP0 receive clock (**I**/**O**/**Z**) [default] or McASP0 receive bit clock (I/O/Z).
CLKX0/ACLKX0	16	G3	I/O/Z	IPD	McBSP0 transmit clock (**I**/**O**/**Z**) [default] or McASP0 transmit bit clock (I/O/Z).
DR0/AXR0[0]	27	J1	I	IPU	McBSP0 receive data (**I**) [default] or McASP0 TX/RX data pin 0 (I/O/Z).
DX0/AXR0[1]	20	H2	O/Z	IPU	McBSP0 transmit data (**O**/**Z**) [default] or McASP0 TX/RX data pin 1 (I/O/Z).
FSR0/AFSR0	24	J3	I/O/Z	IPD	McBSP0 receive frame sync (**I**/**O**/**Z**) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z).
FSX0/AFSX0	21	H1	I/O/Z	IPD	McBSP0 transmit frame sync (**I**/**O**/**Z**) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
INTER-INTEGRATED CIRCUIT 1 (I2C1)					
CLKS1/SCL1	8	E1	I/O/Z	—	McBSP1 external clock source (as opposed to internal) (**I**) [default] or I2C1 clock (I/O/Z). This pin *must* be externally pulled up. When this pin is used as an I2C pin, the value of the pullup resistor is dependent on the number of devices connected to the I2C bus. For more details, see the *Philips I^{2}C Specification Revision 2.1* (January 2000).
DR1/SDA1	37	M2	I/O/Z	—	McBSP1 receive data (**I**) [default] or I2C1 data (I/O/Z). This pin *must* be externally pulled up. When this pin is used as an I2C pin, the value of the pullup resistor is dependent on the number of devices connected to the I2C bus. For more details, see the *Philips I^{2}C Specification Revision 2.1* (January 2000).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
	PYP	GDP			
INTER-INTEGRATED CIRCUIT 0 (I2C0)					
SCL0	41	N1	I/O/Z	—	I2C0 clock. This pin *must* be externally pulled up. The value of the pullup resistor on this pin is dependent on the number of devices connected to the I2C bus. For more details, see the *Philips I*^{2}*C Specification Revision 2.1* (January 2000).
SDA0	42	N2	I/O/Z	—	I2C0 data. This pin *must* be externally pulled up. The value of the pullup resistor on this pin is dependent on the number of devices connected to the I2C bus. For more details, see *the Philips I*^{2}*C Specification Revision 2.1* (January 2000).
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)					
HD15/GP[15]	174	B14	I/O/Z	IPU	Host-port data pins (**I**/**O**/**Z**) [default] or general-purpose input/output pins (I/O/Z) and some function as boot configuration pins at reset. • Used for transfer of data, address, and control • Also controls initialization of DSP modes at reset via pullup/pulldown resistors As general-purpose input/output (GP[x]) functions, these pins are software-configurable through registers. The “GPxEN” bits in the GP Enable register and the GPxDIR bits in the GP Direction register must be properly configured: GPxEN = 1; GP[x] pin is enabled. GPxDIR = 0; GP[x] pin is an input. GPxDIR = 1; GP[x] pin is an output. For the functionality description of the Host-port data pins or the boot configuration pins, see the Host-Port Interface (HPI) portion of this table.
HD14/GP[14]	173	C14		IPU	
HD13/GP[13]	172	A15		IPU	
HD12/GP[12]	168	C15		IPU	
HD11/GP[11]	167	A16		IPU	
HD10/GP[10]	166	B16		IPU	
HD9/GP[9]	165	C16		IPU	
HD8/GP[8]	160	B17		IPU	
GP[7](EXT_INT7)	7	E3	I/O/Z	IPU	General-purpose input/output pins (**I**/**O**/**Z**) which also function as external interrupts • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]) GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INEN bit in the associated McASP AMUTE register.
GP[6](EXT_INT6)	2	D2			
GP[5](EXT_INT5)/ AMUTEIN0	6	C1			
GP[4](EXT_INT4)/ AMUTEIN1	1	C2			
HD7/GP[3]	164	A18	I/O/Z	IPU	Host-port data pin 7 (**I**/**O**/**Z**) [default] or general-purpose input/output pin 3 (I/O/Z)
CLKOUT2/GP[2]	82	Y12	I/O/Z	IPD	Clock output at half of device speed (**O**/**Z**) [default] or this pin can be programmed as GP[2] pin.
$\overline{\text{HINT}}$/GP[1]	135	J20	O	IPU	Host interrupt (from DSP to host) (**O**) [default] or this pin can be programmed as a GP[1] pin (I/O/Z).
HD4/GP[0]	156	C19	I/O/Z	IPD	Host-port data pin 4 (**I**/**O**/**Z**) [default] or this pin can be programmed as a GP[0] pin (I/O/Z).

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	IPD/ IPU[‡]	DESCRIPTION
	PYP	GDP			
RESERVED FOR TEST					
RSV	198	A5	O/Z	IPU	Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV	200	B5	A[§]		Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV	179	C12	O	—	Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV	—	D7	O/Z	IPD	Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV	178	D12	I	—	Reserved. This pin does ***not*** have an IPU. For proper C6713 device operation, the D12 pin **must** be externally pulled down with a 10-kΩ resistor.
RSV	181	A12		—	Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV	180	B11		—	Reserved. (Leave unconnected, **do not** connect to power or ground)

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

[‡] IPD = Internal pulldown, IPU = Internal pullup. [These IPD/IPU signal pins feature a 13-kΩ resistor (approximate) for the IPD or 18-kΩ resistor (approximate) for the IPU. An external pullup or pulldown resistor no greater than 4.4 kΩ and 2.0 kΩ, respectively, should be used to pull a signal to the opposite supply rail.]

[§] A = Analog signal

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	PYP	GDP		
SUPPLY VOLTAGE PINS				
DV_{DD}	—	A17	S	3.3-V supply voltage (see the power-supply decoupling portion of this data sheet)
	—	B3		
	—	B8		
	—	B13		
	—	C10		
	—	D1		
	—	D16		
	—	D19		
	—	F3		
	—	H18		
	—	J2		
	—	M18		
	—	R1		
	—	R18		
	—	T3		
	—	U5		
	—	U7		
	—	U12		
	—	U16		
	—	V13		
	—	V15		
	—	V19		
	—	W3		
	—	W9		
	—	W12		
	—	Y7		
	—	Y17		
	5	—		
	9	—		
	25	—		
	44	—		
	47	—		
	55	—		
	58	—		
	65	—		
	72	—		
	84	—		
	87	—		
	98	—		
	107	—		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	DESCRIPTION
	PYP	GDP		
SUPPLY VOLTAGE PINS (CONTINUED)				
DV_{DD}	114	—	S	3.3-V supply voltage (see the power-supply decoupling portion of this data sheet)
	126	—		
	141	—		
	162	—		
	183	—		
	188	—		
	206	—		
CV_{DD}	—	A4	S	1.2-V supply voltage [PYP package] 1.26-V supply voltage [GDP package] (see the power-supply decoupling portion of this data sheet)
	—	A9		
	—	A10		
	—	B2		
	—	B19		
	—	C3		
	—	C7		
	—	C18		
	—	D5		
	—	D6		
	—	D11		
	—	D14		
	—	D15		
	—	F4		
	—	F17		
	—	K1		
	—	K4		
	—	K17		
	—	L4		
	—	L17		
	—	L20		
	—	R4		
	—	R17		
	—	U6		
	—	U10		
	—	U11		
	—	U14		
	—	U15		
	—	V3		
	—	V18		
	—	W2		
	—	W19		

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	DESCRIPTION
	PYP	GDP		
SUPPLY VOLTAGE PINS (CONTINUED)				
CV_{DD}	3	—	S	1.2-V supply voltage [PYP package] 1.26-V supply voltage [GDP package] (see the power-supply decoupling portion of this data sheet)
	11	—		
	14	—		
	22	—		
	29	—		
	35	—		
	40	—		
	43	—		
	46	—		
	50	—		
	51	—		
	53	—		
	60	—		
	67	—		
	80	—		
	89	—		
	96	—		
	104	—		
	105	—		
	116	—		
	124	—		
	133	—		
	149	—		
	157	—		
	169	—		
	171	—		
	177	—		
	190	—		
	195	—		
	196	—		
	201	—		
	208	—		
GROUND PINS				
V_{SS}	—	A1	GND	Ground pins
	—	A2		
	—	A11		
	—	A14		
	—	A19		
	—	A20		
	—	B1		
	—	B4		

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	DESCRIPTION
	PYP	GDP		
GROUND PINS (CONTINUED)				
V_{SS}	—	B15	GND	Ground pins[#] The center thermal balls (J9−J12, K9−K12, L9−L12, M9−M12) [shaded] are all tied to ground and act as both electrical grounds and thermal relief (thermal dissipation).
	—	B20		
	—	C6		
	—	C8		
	—	C9		
	—	D4		
	—	D8		
	—	D13		
	—	D17		
	—	E2		
	—	E4		
	—	E17		
	—	F19		
	—	G4		
	—	G17		
	—	H4		
	—	H17		
	—	J4		
	—	J9		
	—	J10		
	—	J11		
	—	J12		
	—	K2		
	—	K9		
	—	K10		
	—	K11		
	—	K12		
	—	K20		
	—	L9		
	—	L10		
	—	L11		
	—	L12		
	—	M4		
	—	M9		
	—	M10		
	—	M11		
	—	M12		
	—	M17		

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
[#] Shaded pin numbers denote the center thermal balls.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	PYP	GDP		
GROUND PINS (CONTINUED)				
V_{SS}	—	N4	GND	Ground pins
	—	N17		
	—	P4		
	—	P17		
	—	P19		
	—	T4		
	—	T17		
	—	U4		
	—	U8		
	—	U9		
	—	U13		
	—	U17		
	—	U20		
	—	W1		
	—	W5		
	—	W11		
	—	W16		
	—	W20		
	—	Y1		
	—	Y2		
	—	Y13		
	—	Y19		
	—	Y20		
	4	—		
	10	—		
	15	—		
	23	—		
	26	—		
	30	—		
	34	—		
	39	—		
	45	—		
	48	—		
	49	—		
	52	—		
	54	—		
	59	—		
	66	—		
	73	—		
	81	—		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO.		TYPE[†]	DESCRIPTION
	PYP	GDP		
GROUND PINS (CONTINUED)				
V_{SS}	85	—	GND	Ground pins
	88	—		
	97	—		
	106	—		
	115	—		
	125	—		
	134	—		
	142	—		
	148	—		
	158	—		
	163	—		
	170	—		
	182	—		
	189	—		
	194	—		
	199	—		
	203	—		
	207	—		

[†] I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE): including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

C6000 and XDS are trademarks of Texas Instruments.

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX	Experimental device that is not necessarily representative of the final device's electrical specifications
TMP	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
TMS	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Experimental devices (TMX) may not be representative of a final product and Texas Instruments reserves the right to change or discontinue these products without notice.

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GDP), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -225 is 225 MHz).

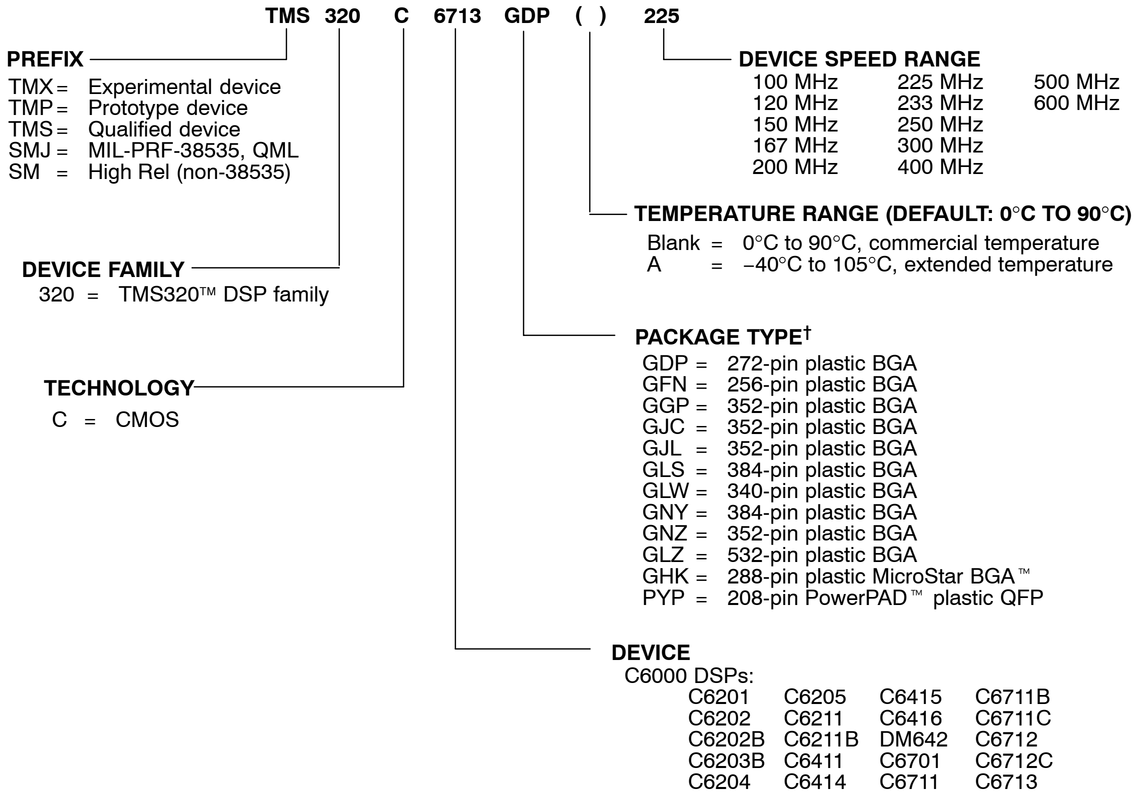
Figure 12 provides a legend for reading the complete device name for any TMS320C6000™ DSP family member.

TMS320 is a trademark of Texas Instruments.

device and development-support tool nomenclature (continued)

Table 24. TMS320C6713 Device Part Numbers (P/Ns) and Ordering Information

DEVICE ORDERABLE P/N	DEVICE SPEED	CORE and I/O VOLTAGE		OPERATING CASE TEMPERATURE RANGE
		CV_{DD} (CORE)	DV_{DD} (I/O)	
TMS320C6713GDP225	225 MHz/1350 MFLOPS	1.26 V	3.3 V	0°C to 90°C
TMS320C6713GDPA200	200 MHz/1200 MFLOPS	1.26 V	3.3 V	−40°C to 105°C
TMS320C6713PYP200	200 MHz/1200 MFLOPS	1.2 V	3.3 V	0°C to 90°C
TMS320C6713PYPA167	167 MHz/1000 MFLOPS	1.2 V	3.3 V	−40°C to 105°C



† BGA = Ball Grid Array
QFP = Quad Flatpack

Figure 12. TMS320C6000™ DSP Device Nomenclature (Including the TMS320C6713 Device)

MicroStar BGA and PowerPAD are trademarks of Texas Instruments.

documentation support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190) describes the functionality of the peripherals available on the C6000™ DSP platform of devices, such as the external memory interface (EMIF), host-port interface (HPI), multichannel buffered serial ports (McBSPs), enhanced direct-memory-access (EDMA) controller, and power-down modes. This guide also includes information on internal data and program memories. These C6713 peripherals are similar to the peripherals on the TMS320C6711 and TMS320C64x devices; therefore, see the TMS320C6711 (C6711 or C67x) peripheral information, and in some cases, where indicated, see the C64x information in the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

The *TMS320DA6000 DSP Multichannel Audio Serial Port (McASP) Reference Guide* (literature number SPRU041) describes the functionality of the McASP peripherals available on the C6713 device.

TMS320C6000 DSP Phase−Locked Loop (PLL) Controller Peripheral Reference Guide (literature number SPRU233) describes the functionality of the PLL peripheral available on the C6713 device.

TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide (literature number SPRU175) describes the functionality of the I2C peripherals available on the C6713 device.

The *PowerPAD Thermally Enhanced Package Technical Brief* (literature number SLMA002) focuses on the specifics of integrating a PowerPAD package into the printed circuit board design to make optimum use of the thermal efficiencies designed into the PowerPAD package.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x™/C67x™ devices, associated development tools, and third-party support.

The *Migrating from TMS320C6211(B)/C6711(B) to TMS320C6713* application report (literature number SPRA851) indicates the differences and describes the issues of interest related to the migration from the Texas Instruments TMS320C6211(B)/C6711(B), GFN package, to the TMS320C6713, GDP package.

The *TMS320C6713 Digital Signal Processor Silicon Errata* (literature number SPRZ191) describes the known exceptions to the functional specifications for particular silicon revisions of the TMS320C6713 device .

The *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889) discusses the power consumption for user applications with the TMS320C6713, TMS320C6712C, and TMS320C6711C DSP devices.

The *Using IBIS Models for Timing Analysis* application report (literature number SPRA839) describes how to properly use IBIS models to attain accurate timing analysis for a given system.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

See the Worldwide Web URL for the application report *How To Begin Development Today With the TMS320C6713 Floating-Point DSP* (literature number SPRA809), which describes in more detail the similarities/differences between the C6713 and C6711 C6000™ DSP devices.

C62x is a trademark of Texas Instruments.

CPU CSR register description

The CPU control status register (CSR) contains the CPU ID and CPU Revision ID (bits 16−31) as well as the status of the device power-down modes [PWRD field (bits 15−10)], program and data cache control modes, the endian bit (EN, bit 8) and the global interrupt enable (GIE, bit 0) and previous GIE (PGIE, bit 1). Figure 13 and Table 25 identify the bit fields in the CPU CSR register.

For more detailed information on the bit fields in the CPU CSR register, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190) and the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).

31 24	23 16
CPU ID	REVISION ID
R-0x02	R-0x03

15 10	9	8	7 6 5	4 2	1	0
PWRD	SAT	EN	PCC	DCC	PGIE	GIE
R/W-0	R/C-0	R-1	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Readable by the MVC instruction, R/W = Readable/Writeable by the MVC instruction; W = Read/write; -*n* = value after reset, -x = undefined value after reset, C = Clearable by the MVC instruction

Figure 13. CPU Control Status Register (CPU CSR)

CPU CSR register description (continued)

Table 25. CPU CSR Register Bit Field Description

BIT #	NAME	DESCRIPTION
31:24	CPU ID	CPU ID + REV ID. Read only. Identifies which CPU is used and defines the silicon revision of the CPU. CPU ID + REVISION ID (31:16) are combined for a value of: **0x0203** for C6713
23:16	REVISION ID	
15:10	PWRD	Control power-down modes. The values are always read as zero. 000000 = no power-down (default) 001001 = PD1, wake-up by an enabled interrupt 010001 = PD1, wake-up by an enabled or not enabled interrupt 011010 = PD2, wake-up by a device reset 011100 = PD3, wake-up by a device reset Others = Reserved
9	SAT	Saturate bit. Set when any unit performs a saturate. This bit can be cleared only by the MVC instruction and can be set only by a functional unit. The set by the a functional unit has priority over a clear (by the MVC instruction) if they occur on the same cycle. The saturate bit is set one full cycle (one delay slot) after a saturate occurs. This bit will not be modified by a conditional instruction whose condition is false.
8	EN	Endian bit. This bit is read-only. Depicts the device endian mode. 0 = Big Endian mode. 1 = Little Endian mode [default].
7:5	PCC	Program Cache control mode. L1D, Level 1 Program Cache 000/010 = Cache Enabled / Cache accessed and updated on reads. All other PCC values reserved.
4:2	DCC	Data Cache control mode. L1D, Level 1 Data Cache 000/010 = Cache Enabled / 2-Way Cache All other DCC values reserved
1	PGIE	Previous GIE (global interrupt enable); saves the Global Interrupt Enable (GIE) when an interrupt is taken. Allows for proper nesting of interrupts. 0 = Previous GIE value is 0. (default) 1 = Previous GIE value is 1.
0	GIE	Global interrupt enable bit. Enables (1) or disables (0) all interrupts except the reset interrupt and NMI (nonmaskable interrupt). 0 = Disables all interrupts (except the reset interrupt and NMI) [default] 1 = Enables all interrupts (except the reset interrupt and NMI)

interrupts and interrupt selector

The C67x DSP core supports 16 prioritized interrupts, which are listed in Table 26. The highest priority interrupt is INT_00 (dedicated to RESET) while the lowest priority is INT_15. The first four interrupts are non-maskable and fixed. The remaining interrupts (4−15) are maskable and default to the interrupt source listed in Table 26. However, their interrupt source may be reprogrammed to any one of the sources listed in Table 27 (Interrupt Selector). Table 27 lists the selector value corresponding to each of the alternate interrupt sources. The selector choice for interrupts 4−15 is made by programming the corresponding fields (listed in Table 26) in the MUXH (address 0x019C0000) and MUXL (address 0x019C0004) registers.

Table 26. DSP Interrupts

DSP INTERRUPT NUMBER	INTERRUPT SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT INTERRUPT EVENT
INT_00	−	−	RESET
INT_01	−	−	NMI
INT_02	−	−	Reserved
INT_03	−	−	Reserved
INT_04	MUXL[4:0]	00100	GPINT4†
INT_05	MUXL[9:5]	00101	GPINT5†
INT_06	MUXL[14:10]	00110	GPINT6†
INT_07	MUXL[20:16]	00111	GPINT7†
INT_08	MUXL[25:21]	01000	EDMAINT
INT_09	MUXL[30:26]	01001	EMUDTDMA
INT_10	MUXH[4:0]	00011	SDINT
INT_11	MUXH[9:5]	01010	EMURTDXRX
INT_12	MUXH[14:10]	01011	EMURTDXTX
INT_13	MUXH[20:16]	00000	DSPINT
INT_14	MUXH[25:21]	00001	TINT0
INT_15	MUXH[30:26]	00010	TINT1

Table 27. Interrupt Selector

INTERRUPT SELECTOR VALUE (BINARY)	INTERRUPT EVENT	MODULE
00000	DSPINT	HPI
00001	TINT0	Timer 0
00010	TINT1	Timer 1
00011	SDINT	EMIF
00100	GPINT4†	GPIO
00101	GPINT5†	GPIO
00110	GPINT6†	GPIO
00111	GPINT7†	GPIO
01000	EDMAINT	EDMA
01001	EMUDTDMA	Emulation
01010	EMURTDXRX	Emulation
01011	EMURTDXTX	Emulation
01100	XINT0	McBSP0
01101	RINT0	McBSP0
01110	XINT1	McBSP1
01111	RINT1	McBSP1
10000	GPINT0	GPIO
10001	Reserved	−
10010	Reserved	−
10011	Reserved	−
10100	Reserved	−
10101	Reserved	−
10110	I2CINT0	I2C0
10111	I2CINT1	I2C1
11000	Reserved	−
11001	Reserved	−
11010	Reserved	−
11011	Reserved	−
11100	AXINT0	McASP0
11101	ARINT0	McASP0
11110	AXINT1	McASP1
11111	ARINT1	McASP1

† Interrupt Events GPINT4, GPINT5, GPINT6, and GPINT7 are outputs from the GPIO module (GP). They originate from the device pins GP[4](EXT_INT4)/AMUTEIN1, GP[5](EXT_INT5)/AMUTEIN0, GP[6](EXT_INT6), and GP[7](EXT_INT7). These pins can be used as edge-sensitive EXT_INTx with polarity controlled by the External Interrupt Polarity Register (EXTPOL.[3:0]). The corresponding pins must first be *enabled* in the GPIO module by setting the corresponding enable bits in the GP Enable Register (GPEN.[7:4]), and configuring them as *inputs* in the GP Direction Register (GPDIR.[7:4]). These interrupts can be controlled through the GPIO module in addition to the simple EXTPOL.[3:0] bits. For more information on interrupt control via the GPIO module, see the GPIO module section of the the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

external interrupt sources

The C6713 device supports many external interrupt sources as indicated in Table 28. Control of the interrupt source is done by the associated module and is made available by enabling the corresponding binary interrupt selector value (see Table 27 Interrupt Selector shaded rows). Due to pin muxing and module usage, not all external interrupt sources are available at the same time.

Table 28. External Interrupt Sources and Peripheral Module Control

PIN NAME	INTERRUPT EVENT	MODULE
GP[15]	GPINT0	GPIO
GP[14]	GPINT0	GPIO
GP[13]	GPINT0	GPIO
GP[12]	GPINT0	GPIO
GP[11]	GPINT0	GPIO
GP[10]	GPINT0	GPIO
GP[9]	GPINT0	GPIO
GP[8]	GPINT0	GPIO
GP[7]	GPINT0 or GPINT7	GPIO
GP[6]	GPINT0 or GPINT6	GPIO
GP[5]	GPINT0 or GPINT5	GPIO
GP[4]	GPINT0 or GPINT4	GPIO
GP[3]	GPINT0	GPIO
GP[2]	GPINT0	GPIO
GP[1]	GPINT0	GPIO
GP[0]	GPINT0	GPIO

EDMA module and EDMA selector

The C67x EDMA supports up to 16 EDMA channels. Four of the sixteen channels (channels 8−11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices.

The EDMA selector registers that control the EDMA channels servicing peripheral devices are located at addresses 0x01A0FF00 (ESEL0), 0x01A0FF04 (ESEL1), and 0x01A0FF0C (ESEL3). These EDMA selector registers control the mapping of the EDMA events to the EDMA channels. Each EDMA event has an assigned EDMA selector code (see Table 30). By loading each EVTSELx register field with an EDMA selector code, users can map any desired EDMA event to any specified EDMA channel. Table 29 lists the default EDMA selector value for each EDMA channel.

See Table 31 and Table 32 for the EDMA Event Selector registers and their associated bit descriptions.

EDMA module and EDMA selector (continued)

Table 29. EDMA Channels

EDMA CHANNEL	EDMA SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT EDMA EVENT
0	ESEL0[5:0]	000000	DSPINT
1	ESEL0[13:8]	000001	TINT0
2	ESEL0[21:16]	000010	TINT1
3	ESEL0[29:24]	000011	SDINT
4	ESEL1[5:0]	000100	GPINT4
5	ESEL1[13:8]	000101	GPINT5
6	ESEL1[21:16]	000110	GPINT6
7	ESEL1[29:24]	000111	GPINT7
8	–	–	TCC8 (Chaining)
9	–	–	TCC9 (Chaining)
10	–	–	TCC10 (Chaining)
11	–	–	TCC11 (Chaining)
12	ESEL3[5:0]	001100	XEVT0
13	ESEL3[13:8]	001101	REVT0
14	ESEL3[21:16]	001110	XEVT1
15	ESEL3[29:24]	001111	REVT1

Table 30. EDMA Selector

EDMA SELECTOR CODE (BINARY)	EDMA EVENT	MODULE
000000	DSPINT	HPI
000001	TINT0	TIMER0
000010	TINT1	TIMER1
000011	SDINT	EMIF
000100	GPINT4	GPIO
000101	GPINT5	GPIO
000110	GPINT6	GPIO
000111	GPINT7	GPIO
001000	GPINT0	GPIO
001001	GPINT1	GPIO
001010	GPINT2	GPIO
001011	GPINT3	GPIO
001100	XEVT0	McBSP0
001101	REVT0	McBSP0
001110	XEVT1	McBSP1
001111	REVT1	McBSP1
010000−011111	Reserved	
100000	AXEVTE0	McASP0
100001	AXEVTO0	McASP0
100010	AXEVT0	McASP0
100011	AREVTE0	McASP0
100100	AREVTO0	McASP0
100101	AREVT0	McASP0
100110	AXEVTE1	McASP1
100111	AXEVTO1	McASP1
101000	AXEVT1	McASP1
101001	AREVTE1	McASP1
101010	AREVTO1	McASP1
101011	AREVT1	McASP1
101100	I2CREVT0	I2C0
101101	I2CXEVT0	I2C0
101110	I2CREVT1	I2C1
101111	I2CXEVT1	I2C1
110000	GPINT8	GPIO
110001	GPINT9	GPIO
110010	GPINT10	GPIO
110011	GPINT11	GPIO
110100	GPINT12	GPIO
110101	GPINT13	GPIO
110110	GPINT14	GPIO
110111	GPINT15	GPIO
111000−111111	Reserved	

EDMA module and EDMA selector (continued)

Table 31. EDMA Event Selector Registers (ESEL0, ESEL1, and ESEL3)

ESEL0 Register (0x01A0 FF00)

31 30	29 28 27 24	23 22	21 20 19 16
Reserved	EVTSEL3	Reserved	EVTSEL2
R−0	R/W−00 0011b	R−0	R/W−00 0010b

15 14	13 12 11 8	7 6	5 4 3 0
Reserved	EVTSEL1	Reserved	EVTSEL0
R−0	R/W−00 0001b	R−0	R/W−00 0000b

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL1 Register (0x01A0 FF04)

31 30	29 28 27 24	23 22	21 20 19 16
Reserved	EVTSEL7	Reserved	EVTSEL6
R−0	R/W−00 0111b	R−0	R/W−00 0110b

15 14	13 12 11 8	7 6	5 4 3 0
Reserved	EVTSEL5	Reserved	EVTSEL4
R−0	R/W−00 0101b	R−0	R/W−00 0100b

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL3 Register (0x01A0 FF0C)

31 30	29 28 27 24	23 22	21 20 19 16
Reserved	EVTSEL15	Reserved	EVTSEL14
R−0	R/W−00 1111b	R−0	R/W−00 1110b

15 14	13 12 11 8	7 6	5 4 3 0
Reserved	EVTSEL13	Reserved	EVTSEL12
R−0	R/W−00 1101b	R−0	R/W−00 1100b

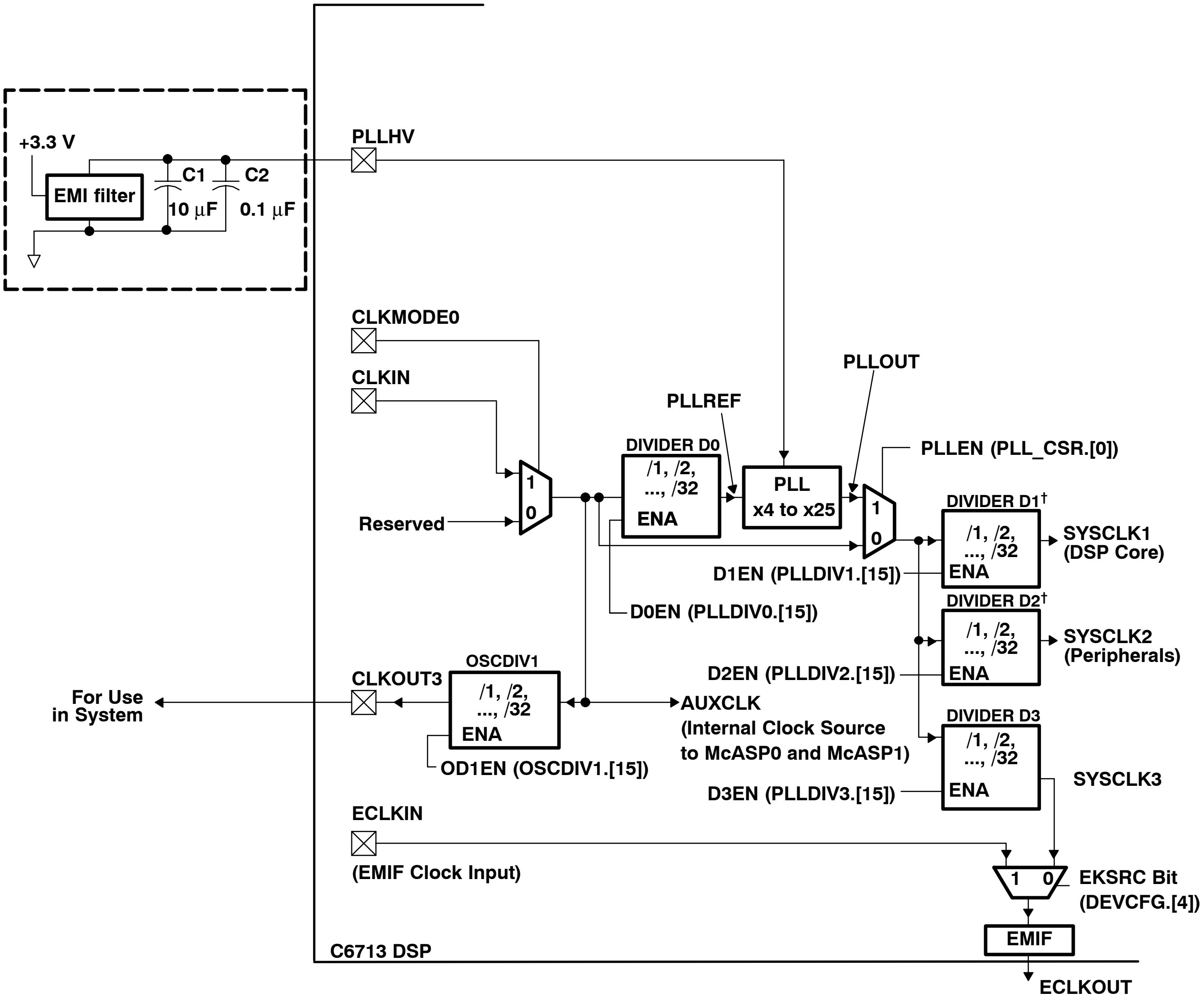
Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 32. EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description

BIT #	NAME	DESCRIPTION
31:30 23:22 15:14 7:6	Reserved	Reserved. Read-only, writes have no effect.
29:24 21:16 13:8 5:0	EVTSELx	EDMA event selection bits for channel x. Allows mapping of the EDMA events to the EDMA channels. The EVTSEL0 through EVTSEL15 bits correspond to the channels 0 to 15, respectively. These EVTSELx fields are user−selectable. By configuring the EVTSELx fields to the EDMA selector value of the desired EDMA sync event number (see Table 30), users can map any EDMA event to the EDMA channel. For example, if EVTSEL15 is programmed to 00 0001b (the EDMA selector code for TINT0), then channel 15 is triggered by Timer0 TINT0 events.

PLL and PLL controller

The TMS320C6713 includes a PLL and a flexible PLL Controller peripheral consisting of a prescaler (D0) and four dividers (OSCDIV1, D1, D2, and D3). The PLL controller is able to generate different clocks for different parts of the system (i.e., DSP core, Peripheral Data Bus, External Memory Interface, McASP, and other peripherals). Figure 14 illustrates the PLL, the PLL controller, and the clock generator logic.



† Dividers D1 and D2 must never be disabled. Never write a “0” to the D1EN or D2EN bits in the PLLDIV1 and PLLDIV2 registers.

NOTES:
- A. Place all PLL external components (C1, C2, and the EMI Filter) as close to the C67x™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
- B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI Filter).
- C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.
- D. EMI filter manufacturer TDK part number ACF451832-333, -223, -153, -103. Panasonic part number EXCCET103U.

Figure 14. PLL and Clock Generator Logic

PLL and PLL controller (continued)

The PLL Reset Time is the amount of wait time needed when resetting the PLL (writing PLLRST=1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL Reset Time value, see Table 33. The PLL Lock Time is the amount of time from when PLLRST = 0 with PLLEN = 0 (PLL out of reset, but still bypassed) to when the PLLEN bit can be safely changed to “1” (switching from bypass to the PLL path), see Table 33 and Figure 14.

Under some operating conditions, the maximum PLL Lock Time may vary from the specified typical value. For the PLL Lock Time values, see Table 33.

Table 33. PLL Lock and Reset Times

	MIN	TYP	MAX	UNIT
PLL Lock Time		75	187.5	µs
PLL Reset Time	125			ns

Table 34 shows the C6713 device’s CLKOUT signals, how they are derived and by what register control bits, and what is the default settings. For more details on the PLL, see the PLL and Clock Generator Logic diagram (Figure 14).

Table 34. CLKOUT Signals, Default Settings, and Control

CLOCK OUTPUT SIGNAL NAME	DEFAULT SETTING (ENABLED or DISABLED)	CONTROL BIT(s) (Register)	DESCRIPTION
CLKOUT2	ON (ENABLED)	D2EN = 1 (PLLDIV2.[15]) CK2EN = 1 (EMIF GBLCTL.[3])	SYSCLK2 selected [default]
CLKOUT3	ON (ENABLED)	OD1EN = 1 (OSCDIV1.[15])	Derived from CLKIN
ECLKOUT	ON (ENABLED); derived from SYSCLK3	EKSRC = 0 (DEVCFG.[4]) EKEN = 1 (EMIF GBLCTL.[5])	SYSCLK3 selected [default]. To select ECLKIN source: EKSRC = 1 (DEVCFG.[4]) and EKEN = 1 (EMIF GBLCTL.[5])

The input clock (CLKIN) is directly available to the McASP modules as AUXCLK for use as an internal high-frequency clock source. The input clock (CLKIN) may also be divided down by a programmable divider OSCDIV1 (/1, /2, /3, ..., /32) and output on the CLKOUT3 pin for other use in the system.

Figure 14 shows that the input clock source may be divided down by divider PLLDIV0 (/1, /2, ..., /32) and then multiplied up by a factor of x4, x5, x6, and so on, up to x25.

Either the input clock (PLLEN = 0) or the PLL output (PLLEN = 1) then serves as the high-frequency reference clock for the rest of the DSP system. The DSP core clock, the peripheral bus clock, and the EMIF clock may be divided down from this high-frequency clock (each with a unique divider) . For example, with a 30 MHz input if the PLL output is configured for 450 MHz, the DSP core may be operated at 225 MHz (/2) while the EMIF may be configured to operate at a rate of 75 MHz (/6). Note that there is a specific minimum and maximum reference clock (PLLREF) and output clock (PLLOUT) for the block labeled PLL in Figure 14, as well as for the DSP core, peripheral bus, and EMIF. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). See Table 35 for the PLL clocks input and output frequency ranges.

PLL and PLL controller (continued)

Table 35. PLL Clock Frequency Ranges†‡

CLOCK SIGNAL	GDP-225 GDPA-200 PYP-200 PYPA-167		UNIT
	MIN	MAX	
PLLREF (PLLEN = 1)	12	100	MHz
PLLOUT	140	600	MHz
SYSCLK1	–	Device Speed (DSP Core)	MHz
SYSCLK3 (EKSRC = 0)	–	100	MHz
AUXCLK	–	50§	MHz

† SYSCLK2 rate ***must*** be exactly half of SYSCLK1.

‡ Also see the electrical specification (timing requirements and switching characteristics parameters) in the input and output clocks section of this data sheet.

§ When the McASP module is *not* used, the AUXCLK maximum frequency can be any frequency up to the CLKIN maximum frequency.

The EMIF itself may be clocked by an external reference clock via the ECLKIN pin or can be generated on-chip as SYSCLK3. SYSCLK3 is derived from divider D3 off of PLLOUT (see Figure 14, PLL and Clock Generator Logic). The EMIF clock selection is programmable via the EKSRC bit in the DEVCFG register.

The settings for the PLL multiplier and each of the dividers in the clock generation block may be reconfigured via software at run time. If either the input to the PLL changes due to D0, CLKMODE0, or CLKIN, or if the PLL multiplier is changed, then software must enter bypass first and stay in bypass until the PLL has had enough time to lock (see electrical specifications). For the programming procedure, see the *TMS320C6000 DSP Phase-Locked Loop (PLL) Controller Peripheral Reference Guide* (literature number SPRU233).

SYSCLK2 is the internal clock source for peripheral bus control. SYSCLK2 (Divider D2) ***must*** be programmed to be half of the SYSCLK1 rate. For example, if D1 is configured to divide-by-2 mode (/2), then D2 ***must*** be programmed to divide-by-4 mode (/4). SYSCLK2 is also tied directly to CLKOUT2 pin (see Figure 14).

During the programming transition of Divider D1 and Divider D2 (resulting in SYSCLK1 and SYSCLK2 output clocks, see Figure 14), the order of programming the PLLDIV1 and PLLDIV2 registers must be observed to ensure that SYSCLK2 always runs at half the SYSCLK1 rate or slower. For example, if the divider ratios of D1 and D2 are to be changed from /1, /2 (respectively) to /5, /10 (respectively) then, the PLLDIV2 register must be programmed before the PLLDIV1 register. The transition ratios become /1, /2; /1, /10; and then /5, /10. If the divider ratios of D1 and D2 are to be changed from /3, /6 to /1, /2 then, the PLLDIV1 register must be programmed before the PLLDIV2 register. The transition ratios, for this case, become /3, /6; /1, /6; and then /1, /2. The final SYSCLK2 rate ***must*** be exactly half of the SYSCLK1 rate.

Note that Divider D1 and Divider D2 must ***always*** be enabled (i. e., D1EN and D2EN bits are set to “1” in the PLLDIV1 and PLLDIV2 registers).

The PLL Controller registers should be modified only by the CPU or via emulation. The HPI should ***not*** be used to directly access the PLL Controller registers.

For detailed information on the clock generator (PLL Controller registers) and their associated software bit descriptions, see Table 37 through Table 43.

PLL and PLL controller (continued)

Table 36. PLL Control/Status Register (PLLCSR) [0x01B7 C100]

<table>
<tr><td>31 28</td><td>27 24</td><td>23 20</td><td>19 16</td></tr>
<tr><td colspan="4">Reserved</td></tr>
<tr><td colspan="4">R−0</td></tr>
</table>

<table>
<tr><td>15 12</td><td>11 8</td><td>7</td><td>6</td><td>5 4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">Reserved</td><td>STABLE</td><td>Reserved</td><td>PLLRST</td><td>Reserved</td><td>PLLPWRDN</td><td>PLLEN</td></tr>
<tr><td colspan="3">R−0</td><td>R−x</td><td>R−0</td><td>RW−1</td><td>R/W−0</td><td>R/W−0b</td><td>RW−0</td></tr>
</table>

Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 37. PLL Control/Status Register (PLLCSR) Description

BIT #	NAME	DESCRIPTION
31:7	Reserved	Reserved. Read-only, writes have no effect.
6	STABLE	Clock Input Stable. This bit indicates if the clock input has stabilized. 0 – Clock input not yet stable. Clock counter is not finished counting (default). 1 – Clock input stable.
5:4	Reserved	Reserved. Read-only, writes have no effect.
3	PLLRST	Asserts RESET to PLL 0 – PLL Reset Released. 1 – PLL Reset Asserted (default).
2	Reserved	Reserved. The user ***must*** write a “0” to this bit.
1	PLLPWRDN	Select PLL Power Down 0 – PLL Operational (default). 1 – PLL Placed in Power-Down State.
0	PLLEN	PLL Mode Enable 0 – Bypass Mode (default). PLL disabled. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock. 1 – PLL Enabled. Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output.

PLL and PLL controller (continued)

Table 38. PLL Multiplier Control Register (PLLM) [0x01B7 C110]

31 28	27 24	23 20	19 16
Reserved			
R−0			

15 12	11 8	7 6 5	4	3 2 1 0
Reserved			PLLM	
R−0			R/W−0 0111	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 39. PLL Multiplier Control Register (PLLM) Description

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLM	PLL multiply mode [default is x7 (0 0111)]. 00000 = Reserved 10000 = x16 00001 = Reserved 10001 = x17 00010 = Reserved 10010 = x18 00011 = Reserved 10011 = x19 00100 = x4 10100 = x20 00101 = x5 10101 = x21 00110 = x6 10110 = x22 00111 = x7 10111 = x23 01000 = x8 11000 = x24 01001 = x9 11001 = x25 01010 = x10 11010 = Reserved 01011 = x11 11011 = Reserved 01100 = x12 11100 = Reserved 01101 = x13 11101 = Reserved 01110 = x14 11110 = Reserved 01111 = x15 11111 = Reserved PLLM select values 00000 through 00011 and 11010 through 11111 are *not* supported.

PLL and PLL controller (continued)

Table 40. PLL Wrapper Divider x Registers (PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3) [0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively]

31 28	27 24	23 20	19 16
Reserved			
R–0			

15	14 12	11 8	7 5	4	3	2	1	0
DxEN	Reserved			PLLDIVx				
R/W–1	R–0			R/W–x xxxx†				

Legend: R = Read only, R/W = Read/Write; -n = value after reset

† Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1 (0 0000), /1 (0 0000), /2 (0 0001), and /2 (0 0001), respectively.

CAUTION:
D1 and D2 should never be disabled. D3 should only be disabled if ECLKIN is used.

Table 41. PLL Wrapper Divider x Registers (Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3) Description‡

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	DxEN	Divider Dx Enable (where x denotes 0 through 3). 0 – Divider x Disabled. No clock output. 1 – Divider x Enabled (default). **These divider-enable bits are device-specific and must be set to 1 to enable.**
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLDIVx	PLL Divider Ratio [Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1, /1, /2, and /2, respectively]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

‡ Note that SYSCLK2 *must* run at half the rate of SYSCLK1. Therefore, the divider ratio of D2 must be two times slower than D1. For example, if D1 is set to /2, then D2 *must* be set to /4.

PLL and PLL controller (continued)

Table 42. Oscillator Divider 1 Register (OSCDIV1) [0x01B7 C124]

31 28 27 24 23 20 19 16
Reserved
R−0

15	14 12 11 8 7 5	4 3 2 1 0
OD1EN	Reserved	OSCDIV1
R/W−1	R−0	R/W−0 0111

Legend: R = Read only, R/W = Read/Write; -n = value after reset

The OSCDIV1 register controls the oscillator divider 1 for CLKOUT3. The CLKOUT3 signal does ***not*** go through the PLL path.

Table 43. Oscillator Divider 1 Register (OSCDIV1) Description

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	OD1EN	Oscillator Divider 1 Enable. 0 – Oscillator Divider 1 Disabled. 1 – Oscillator Divider 1 Enabled (default).
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	OSCDIV1	Oscillator Divider 1 Ratio [default is /8 (0 0111)]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

multichannel audio serial port (McASP) peripherals

The TMS320C6713 device includes two multi-channel audio serial port (McASP) interface peripherals (McASP1 and McASP0). The McASP is a serial port optimized for the needs of multi-channel audio applications. With two McASP peripherals, the TMS320C6713 device is capable of supporting two completely independent audio zones simultaneously.

Each McASP consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or alternatively, the transmit and receive sections may be synchronized. Each McASP module also includes a pool of 16 shift registers that may be configured to operate as either transmit data, receive data, or general-purpose I/O (GPIO).

The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP supports the TDM synchronous serial format.

Each McASP can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format. However, the transmit and receive formats need not be the same.

Both the transmit and receive sections of the McASP also support burst mode which is useful for non-audio data (for example, passing control information between two DSPs).

The McASP peripherals have additional capability for flexible clock generation, and error detection/handling, as well as error management.

McASP block diagram

Figure 15 illustrates the major blocks along with external signals of the TMS320C6713 McASP1 and McASP0 peripherals; and shows the 8 serial data [AXR] pins for each McASP. Each McASP also includes full general-purpose I/O (GPIO) control, so any pins not needed for serial transfers can be used for general-purpose I/O.

multichannel audio serial port (McASP) peripherals (continued)

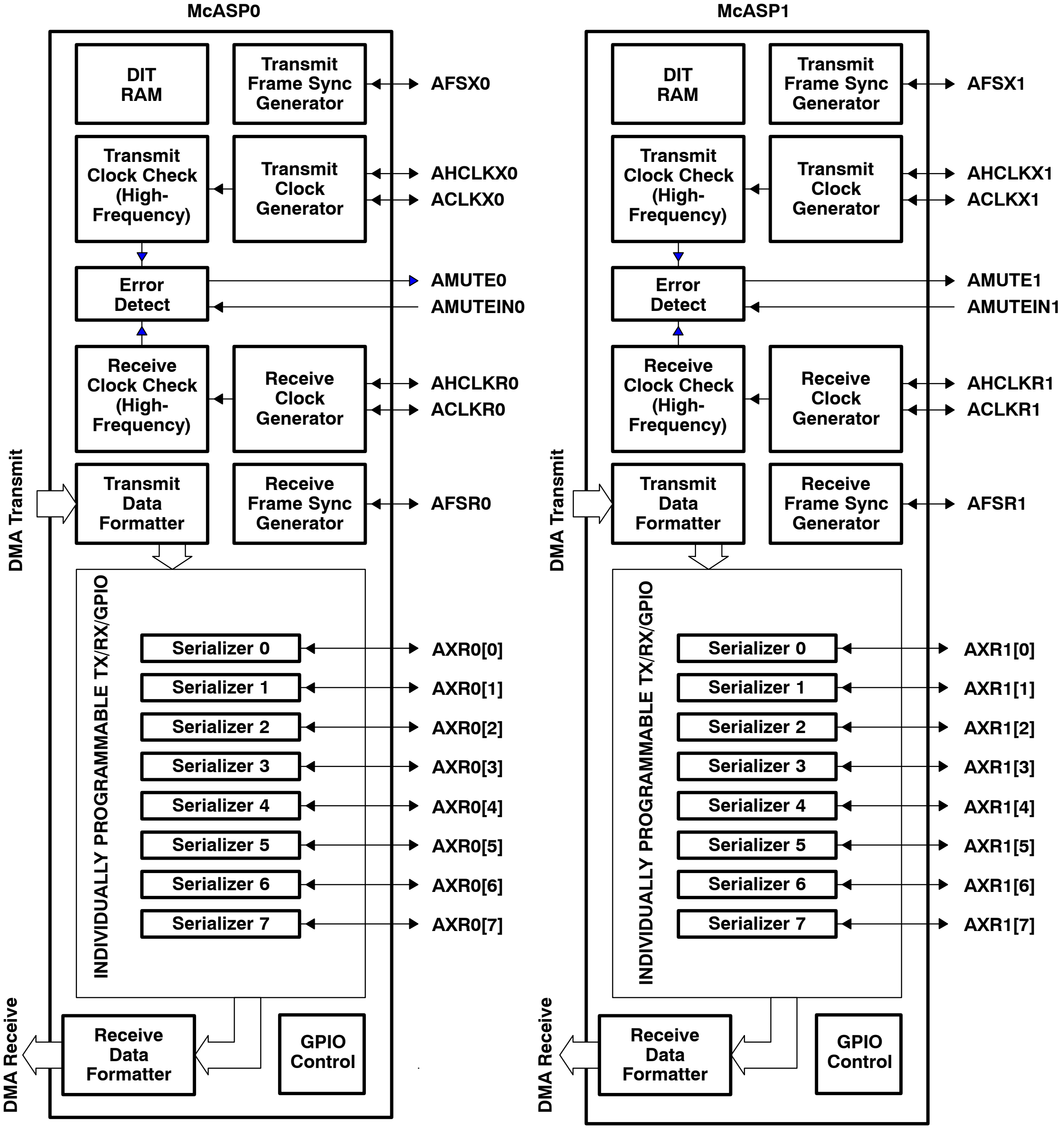


Figure 15. McASP0 and McASP1 Configuration

multichannel audio serial port (McASP) peripherals (continued)

multichannel time division multiplexed (TDM) synchronous transfer mode

The McASP supports a multichannel, time-division-multiplexed (TDM) synchronous transfer mode for both transmit and receive. Within this transfer mode, a wide variety of serial data formats are supported, including formats compatible with devices using the Inter-Integrated Sound (IIS) protocol.

TDM synchronous transfer mode is typically used when communicating between integrated circuits such as between a DSP and one or more ADC, DAC, CODEC, or S/PDIF receiver devices. In multichannel applications, it is typical to find several devices operating synchronized with each other. For example, to provide six analog outputs, three stereo DAC devices would be driven with the same bit clock and frame sync, but each stereo DAC would use a different McASP serial data pin carrying stereo data (2 TDM time slots, left and right).

The TDM synchronous serial transfer mode utilizes several control signals and one or more serial data signals:

- A bit clock signal (ACLKX for transmit, ACKLR for receive)
- A frame sync signal (AFSX for transmit, AFSR for receive)
- An (Optional) high frequency master clock (AHCLKX for transmit, AHCLKR for receive) from which the bit clock is derived
- One or more serial data pins (AXR for transmit and for receive).

Except for the optional high-frequency master clock, all of the signals in the TDM synchronous serial transfer mode protocol are synchronous to the bit clocks (ACLKX and ACLKR).

In the TDM synchronous transfer mode, the McASP continually transmits and receives data periodically (since audio ADCs and DACs operate at a fixed-data rate). The data is organized into frames, and the beginning of a frame is marked by a frame sync pulse on the AFSX, AFSR pin.

In a typical audio system, one frame is transferred per sample period. To support multiple channels, the choices are to either include more time slots per frame (and therefore operate with a higher bit clock) or to keep the bit clock period constant and use additional data pins to transfer the same number of channels. For example, a particular six-channel DAC might require three McASP serial data pins; transferring two channels of data on each serial data pin during each sample period (frame). Another similar DAC may be designed to use only a single McASP serial data pin, but clocked three times faster and transferring six channels of data per sample period. The McASP is flexible enough to support either type of DAC but a transmitter cannot be configured to do both at the same time.

For multiprocessor applications, the McASP supports any number of time slots per frame (between 2 and 32), and includes the ability to “disable” transfers during specific time slots.

In addition, to support of S/PDIF, AES-3, IEC-60958, CP-430 receivers chips whose natural block (McASP frame) size is 384 samples; the McASP receiver supports a 384 time slot mode. The advantage to using the 384 time slot mode is that interrupts may be generated synchronous to the S/PDIF, AES-3, IEC-60958, CP-430 receivers, for example the “last slot” interrupt.

burst transfer mode

The McASP also supports a burst transfer mode, which is useful for non-audio data (for example, passing control information between two DSPs). Burst transfer mode uses a synchronous serial format similar to TDM, except the frame sync is generated for each data word transferred. In addition, frame sync generation is not periodic or time-driven as in TDM mode but rather data-driven.

multichannel audio serial port (McASP) peripherals (continued)

supported bit stream formats for TDM and burst transfer modes

The serial data pins support a wide variety of formats. In the TDM and burst synchronous modes, the data may be transmitted / received with the following options:

- Time slots per frame: 1 (Burst/Data Driven), or 2,3...32 (TDM/Time-Driven).
- Time slot size: 8, 12, 16, 20, 24, 28, 32 bits per time slot
- Data size: 8, 12, 16, 20, 24, 28, 32 bits (must be less than or equal to time slot)
- Data alignment within time slot: Left- or Right-Justified
- Bit order: MSB or LSB first.
- Unused bits in time slot: Padded with 0, 1 or extended with value of another bit.
- Time slot delay from frame sync: 0,1, or 2 bit delay

The data format can be programmed independently for transmit and receive, and for McASP0 vs. McASP1. In addition, the McASP can automatically re-align the data as processed natively by the DSP (any format on a nibble boundary) adjusting the data in hardware to any of the supported serial bit stream formats (TDM, Burst, and DIT modes). This reduces the amount of bit manipulation that the DSP must perform and simplifies software architecture.

digital audio interface transmitter (DIT) transfer mode (transmitter only)

The McASP transmit section may also be configured in digital audio interface transmitter (DIT) mode where it outputs data formatted for transmission over an S/PDIF, AES-3, IEC-60958, or CP-430 standard link. These standards encode the serial data such that the equivalent of ’clock’ and ’frame sync’ are embedded within the data stream. DIT transfer mode is used as an interconnect between audio components and can transfer multichannel digital audio data over a single optical or coaxial cable.

From an internal DSP standpoint, the McASP operation in DIT transfer mode is similar to the two time slot TDM mode, but the data transmitted is output as a bi-phase mark encoded bit stream with preamble, channel status, user data, validity, and parity automatically stuffed into the bit stream by the McASP module. The McASP includes separate validity bits for even/odd subframes and two 384-bit register file modules to hold channel status and user data bits.

DIT mode requires at minimum:

- One serial data pin (if the AUXCLK is used as the reference [see the PLL and Clock Generator Logic Figure 14]) or
- One serial data pin plus either the AHCLKX or ACLKX pin (if an external clock is needed).

If additional serial data pins are used, each McASP may be used to transmit multiple encoded bit streams (one per pin). However, the bit streams will all be synchronized to the same clock and the user data, channel status, and validity information carried by each bit stream will be the same for all bit streams transmitted by the same McASP module.

The McASP can also automatically re-align the data as processed by the DSP (any format on a nibble boundary) in DIT mode; reducing the amount of bit manipulation that the DSP must perform and simplifies software architecture.

multichannel audio serial port (McASP) peripherals (continued)

McASP flexible clock generators

The McASP transmit and receive clock generators are identical. Each clock generator can accept a high-frequency master clock input (on the AHCLKX and AHCLKR pins).

The transmit and receive bit clocks (on the ACLKX and ACLKR pins) can also be sourced externally or can be sourced internally by dividing down the high-frequency master clock input (programmable factor /1, /2, /3, ... /4096). The polarity of each bit clock is individually programmable.

The frame sync pins are AFSX (transmit) and AFSR (receive). A typical usage for these pins is to carry the left-right clock (LRCLK) signal when transmitting and receiving stereo data. The frame sync signals are individually programmable for either internal or external generation, either bit or slot length, and either rising or falling edge polarity.

Some examples of the things that a system designer can use the McASP clocking flexibility for are:

- Input a high-frequency master clock (for example, 512f_S of the receiver), receive with an internally generated bit clock ratio of /8, while transmitting with an internally generated bit clock ratio of /4 or /2. [An example application would be to receive data from a DVD at 48 kHz but output up-sampled or decoded audio at 96 kHz or 192 kHz.]
- Transmit/receive data based one sample rate (for example, 44.1 kHz) using McASP0 while transmitting and receiving at a different sample rate (for example, 48 kHz) on McASP1.
- Use the DSP’s on-board AUXCLK to supply the system clock when the input source is an A/D converter.

McASP error handling and management

To support the design of a robust audio system, the McASP module includes error-checking capability for the serial protocol, data underrun, and data overrun. In addition, each McASP includes a timer that continually measures the high-frequency master clock every 32-SYSCLK2 clock cycles. The timer value can be read to get a measurement of the high-frequency master clock frequency and has a min-max range setting that can raise an error flag if the high-frequency master clock goes out of a specified range. The user would read the high-frequency transmit master clock measurement (AHCLKX0 or AHCLKX1) by reading the XCNT field of the XCLKCHK register and the user would read the high-frequency receive master clock measurement (AHCLKR0 or AHCLKR1) by reading the RCNT field of the RCLKCHK register.

Upon the detection of any one or more of the above errors (software selectable), or the assertion of the AMUTE_IN pin, the AMUTE output pin may be asserted to a high or low level (selectable) to immediately mute the audio output. In addition, an interrupt may be generated if enabled based on any one or more of the error sources.

McASP interrupts and EDMA events

The McASP transmitter and receiver sections each generate an event on every time slot. This event can be serviced by an interrupt or by the EDMA controller.

When using interrupts to service the McASP, each shift register buffer has a unique address in the McASP Registers space (see Table 3).

When using the EDMA to service the McASP, the McASP DATA Port space in Table 3 is accessed. In this case, the address least-significant bits are ignored. Writes to any address in this range access the transmitting buffers in order from lowest (serializer 0) to highest (serializer 15), skipping over disabled and receiving serializers. Likewise, reads from any address in this space access the receiving buffers in the same order but skip over disabled and transmitting buffers.

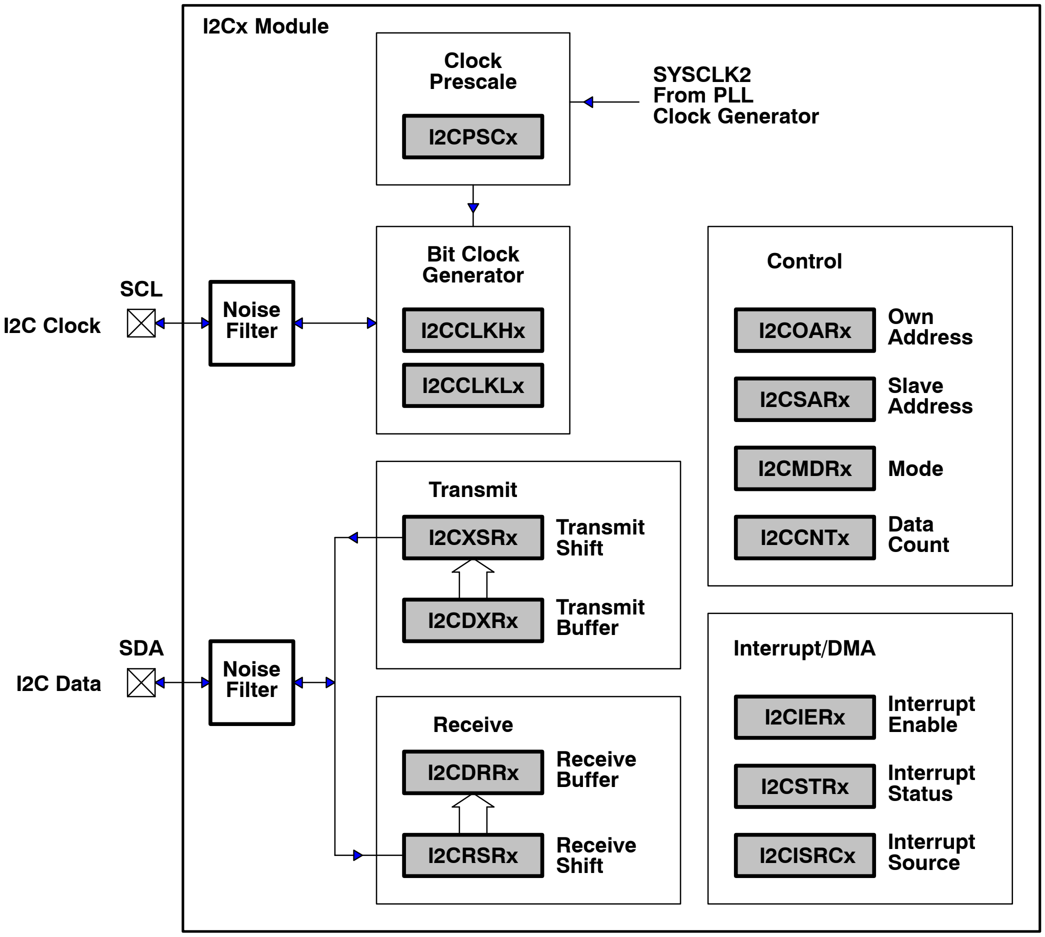
I2C

Having two I2C modules on the TMS320C6713 simplifies system architecture, since one module may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) while the other may be used to communicate with other controllers in a system or to implement a user interface.

The TMS320C6713 also includes two I2C serial ports for control purposes. Each I2C port supports:

- Compatible with *Philips I^{2}C Specification Revision 2.1* (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

Figure 16 is a block diagram of the I2Cx module.



NOTE A: Shading denotes control/status registers.

Figure 16. I2Cx Module Block Diagram

general-purpose input/output (GPIO)

To use the GP[15:0] software-configurable GPIO pins, the GPxEN bits in the GP Enable (GPEN) Register and the GPxDIR bits in the GP Direction (GPDIR) Register must be properly configured.

GPxEN = 1 GP[x] pin is enabled

GPxDIR = 0 GP[x] pin is an input

GPxDIR = 1 GP[x] pin is an output

where “x” represents one of the 15 through 0 GPIO pins

Figure 17 shows the GPIO enable bits in the GPEN register for the C6713 device. To use any of the GPx pins as general-purpose input/output functions, the corresponding GPxEN bit must be set to “1” (enabled). Default values are device-specific, so refer to Figure 17 for the C6713 default configuration.

31 24	23 16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP15 EN	GP14 EN	GP13 EN	GP12 EN	GP11 EN	GP10 EN	GP9 EN	GP8 EN	GP7 EN	GP6 EN	GP5 EN	GP4 EN	GP3 EN	GP2 EN	GP1 EN	GP0 EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R/W = Readable/Writeable; -*n* = value after reset, -x = undefined value after reset

Figure 17. GPIO Enable Register (GPEN) [Hex Address: 01B0 0000]

Figure 18 shows the GPIO direction bits in the GPDIR register. This register determines if a given GPIO pin is an input or an output providing the corresponding GPxEN bit is enabled (set to “1”) in the GPEN register. By default, all the GPIO pins are configured as input pins.

31 24	23 16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP15 DIR	GP14 DIR	GP13 DIR	GP12 DIR	GP11 DIR	GP10 DIR	GP9 DIR	GP8 DIR	GP7 DIR	GP6 DIR	GP5 DIR	GP4 DIR	GP3 DIR	GP2 DIR	GP1 DIR	GP0 DIR
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R/W = Readable/Writeable; -*n* = value after reset, -x = undefined value after reset

Figure 18. GPIO Direction Register (GPDIR) [Hex Address: 01B0 0004]

For more detailed information on general-purpose inputs/outputs (GPIOs), see the General Purpose Input/Output chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time (>1 second) if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

A dual-power supply with simultaneous sequencing can be used to eliminate the delay between core and I/O power up. A Schottky diode can also be used to tie the core rail to the I/O rail (see Figure 19).

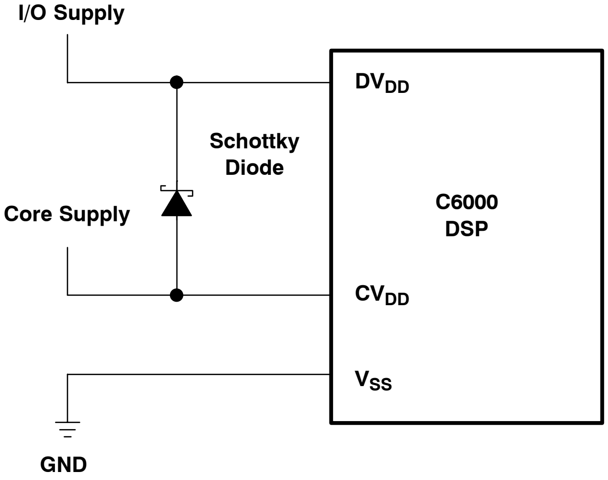


Figure 19. Schottky Diode Diagram

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

power-supply decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. Assuming 0603 caps, the user should be able to fit a total of 60 caps — 30 for the core supply and 30 for the I/O supply. These caps need to be close (no more than 1.25 cm maximum distance) to the DSP to be effective. Physically smaller caps are better, such as 0402, but the size needs to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime needs to be considered.

IEEE 1149.1 JTAG compatibility statement

The TMS320C6713 DSP requires that both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ resets be asserted upon power up to be properly initialized. While $\overline{\text{RESET}}$ initializes the DSP core, $\overline{\text{TRST}}$ initializes the DSP's emulation logic. Both resets are required for proper operation.

While both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ need to be asserted upon power up, only $\overline{\text{RESET}}$ needs to be released for the DSP to boot properly. $\overline{\text{TRST}}$ may be asserted indefinitely for normal operation, keeping the JTAG port interface and DSP's emulation logic in the reset state.

$\overline{\text{TRST}}$ only needs to be released when it is necessary to use a JTAG controller to debug the DSP or exercise the DSP's boundary scan functionality.

For maximum reliability, the TMS320C6713 DSP includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of an external pullup resistor on $\overline{\text{TRST}}$.

When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the DSP after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations. Following the release of $\overline{\text{RESET}}$, the low-to-high transition of $\overline{\text{TRST}}$ must be "seen" to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either Boundary Scan mode or Emulation mode. For more detailed information, see the terminal functions section of this data sheet.

EMIF device speed

The maximum EMIF speed on the C6713 device is 100 MHz. TI recommends utilizing I/O buffer information specification (IBIS) to analyze all AC timings to determine if the maximum EMIF speed is achievable for a given board layout. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839).

For ease of design evaluation, Table 44 contains IBIS simulation results showing the maximum EMIF-SDRAM interface speeds for the given example boards (TYPE) and SDRAM speed grades. Timing analysis should be performed to verify that all AC timings are met for the specified board layout. Other configurations are also possible, but again, timing analysis must be done to verify proper AC timings.

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (see the Terminal Functions table for the EMIF output signals).

Table 44. C6713 Example Boards and Maximum EMIF Speed

BOARD CONFIGURATION			SDRAM SPEED GRADE	MAXIMUM ACHIEVABLE EMIF-SDRAM INTERFACE SPEED
TYPE	EMIF INTERFACE COMPONENTS	BOARD TRACE		
1-Load Short Traces	One bank of one 32-Bit SDRAM	1 to 3-inch traces with proper termination resistors; Trace impedance ~ 50 Ω	143 MHz 32-bit SDRAM (−7)	100 MHz
			166 MHz 32-bit SDRAM (−6)	For short traces, SDRAM data output hold time on these SDRAM speed grades cannot meet EMIF input hold time requirement (see NOTE 1).
			183 MHz 32-bit SDRAM (−55)	
			200 MHz 32-bit SDRAM (−5)	
2-Loads Short Traces	One bank of two 16-Bit SDRAMs	1.2 to 3 inches from EMIF to each load, with proper termination resistors; Trace impedance ~ 78 Ω	125 MHz 16-bit SDRAM (−8E)	100 MHz
			133 MHz 16-bit SDRAM (−75)	100 MHz
			143 MHz 16-bit SDRAM (−7E)	100 MHz
			167 MHz 16-bit SDRAM (−6A)	100 MHz
			167 MHz 16-bit SDRAM (−6)	100 MHz
3-Loads Short Traces	One bank of two 32-Bit SDRAMs One bank of buffer	1.2 to 3 inches from EMIF to each load, with proper termination resistors; Trace impedance ~ 78 Ω	125 MHz 16-bit SDRAM (−8E)	For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1).
			133 MHz 16-bit SDRAM (−75)	100 MHz
			143 MHz 16-bit SDRAM (−7E)	100 MHz
			167 MHz 16-bit SDRAM (−6A)	100 MHz
			167 MHz 16-bit SDRAM (−6)	For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1).
3-Loads Long Traces	One bank of one 32-Bit SDRAM One bank of one 32-Bit SBSRAM One bank of buffer	4 to 7 inches from EMIF; Trace impedance ~ 63 Ω	143 MHz 32-bit SDRAM (−7)	83 MHz
			166 MHz 32-bit SDRAM (−6)	83 MHz
			183 MHz 32-bit SDRAM (−55)	83 MHz
			200 MHz 32-bit SDRAM (−5)	SDRAM data output hold time cannot meet EMIF input hold requirement (see NOTE 1).

NOTE 1: Results are based on IBIS simulations for the given example boards (**TYPE**). Timing analysis should be performed to determine if timing requirements can be met for the particular system.

bootmode

The C6713 device resets using the active-low signal $\overline{\text{RESET}}$ and the internal reset signal. While $\overline{\text{RESET}}$ is low, the internal reset is also asserted and the device is held in reset and is initialized to the prescribed reset state. Refer to reset timing for reset timing characteristics and states of device pins during reset. The release of the internal reset signal (see the Reset Phase 3 discussion in the Reset Timing section of this data sheet) starts the processor running with the prescribed device configuration and boot mode.

The C6713 has three types of boot modes:

- Host boot

  If host boot is selected, upon release of internal reset, the CPU is internally “stalled” while the remainder of the device is released. During this period, an external host can initialize the CPU’s memory space as necessary through the host interface, including internal configuration registers, such as those that control the EMIF or other peripherals. Once the host is finished with all necessary initialization, it must set the DSPINT bit in the HPIC register to complete the boot process. This transition causes the boot configuration logic to bring the CPU out of the “stalled” state. The CPU then begins execution from address 0. The DSPINT condition is not latched by the CPU, because it occurs while the CPU is still internally “stalled”. Also, DSPINT brings the CPU out of the “stalled” state only if the host boot process is selected. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP if required. After the CPU is out of the “stalled” state , the CPU needs to clear the DSPINT, otherwise, no more DSPINTs can be received.

- Emulation boot

  Emulation boot mode is a variation of host boot. In this mode, it is not necessary for a host to load code or to set DSPINT to release the CPU from the “stalled” state. Instead, the emulator will set DSPINT if it has not been previously set so that the CPU can begin executing code from address 0. Prior to beginning execution, the emulator sets a breakpoint at address 0. This prevents the execution of invalid code by halting the CPU prior to executing the first instruction. Emulation boot is a good tool in the debug phase of development.

- EMIF boot (using default ROM timings)

  Upon the release of internal reset, the 1K-Byte ROM code located in the beginning of $\overline{\text{CE1}}$ is copied to address 0 by the EDMA using the default ROM timings, while the CPU is internally “stalled”. The data should be stored in the endian format that the system is using. The boot process also lets you choose the width of the ROM. In this case, the EMIF automatically assembles consecutive 8-bit bytes or 16-bit half-words to form the 32-bit instruction words to be copied. The transfer is automatically done by the EDMA as a single-frame block transfer from the ROM to address 0. After completion of the block transfer, the CPU is released from the “stalled” state and start running from address 0.

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Supply voltage range, CV_{DD} (see Note 2)		−0.3 V to 1.8 V
Supply voltage range, DV_{DD} (see Note 2)		−0.3 V to 4 V
Input voltage range		−0.3 V to DV_{DD} + 0.5 V
Output voltage range		−0.3 V to DV_{DD} + 0.5 V
Operating case temperature ranges, T_C:	(default)	0°C to 90°C
	(A version) [GDPA-200 and PYPA-167]	–40°C to105°C
Storage temperature range, T_{stg}		–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to V_{SS}.

recommended operating conditions[‡]

			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core referenced to V_{SS}	PYP packages only	1.14	1.2	1.32	V
		GDP packages only	1.2	1.26	1.32	V
DV_{DD}	Supply voltage, I/O referenced to V_{SS}		3.13	3.3	3.47	V
$V_{(C-D)}$	Maximum supply voltage difference CV_{DD} – DV_{DD}				1.32	V
$V_{(D-C)}$	Maximum supply voltage difference DV_{DD} – CV_{DD}				2.75	V
V_{IH}	High-level input voltage	All signals except CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$	2			V
		CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$	2			V
V_{IL}	Low-level input voltage	All signals except CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$			0.8	V
		CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$			0.3*DV_{DD}	V
I_{OH}	High-level output current[§]	All signals except ECLKOUT, CLKOUT2, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			−8	mA
		ECLKOUT and CLKOUT2			−16	mA
I_{OL}	Low-level output current[§]	All signals except ECLKOUT, CLKOUT2, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			8	mA
		ECLKOUT and CLKOUT2			16	mA
		CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			3	mA
T_C	Operating case temperature	Default	0		90	°C
		A version (GDPA-200 and PYPA-167)	–40		105	

[‡] The core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.

[§] Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see the device-specific IBIS models.

electrical characteristics over recommended ranges of supply voltage and operating case temperature[†] (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All signals except SCL1, SDA1, SCL0, and SDA0	I_{OH} =MAX	2.4			V
V_{OL}	Low-level output voltage	All signals except SCL1, SDA1, SCL0, and SDA0	I_{OL} = MAX			0.4	V
		SCL1, SDA1, SCL0, and SDA0	I_{OL} = MAX			0.4	V
I_I	Input current	All signals except SCL1, SDA1, SCL0, and SDA0	V_I = V_{SS} to DV_{DD}			±170	uA
		SCL1, SDA1, SCL0, and SDA0				±10	uA
I_{OZ}	Off-state output current	All signals except SCL1, SDA1, SCL0, and SDA0	V_O = DV_{DD} or 0 V			±170	uA
		SCL1, SDA1, SCL0, and SDA0				±10	uA
I_{DD2V}	Core supply current[‡]		GDP, CV_{DD} = 1.26 V, CPU clock = 225 MHz		625		mA
			GDPA, CV_{DD} = 1.26 V, CPU clock = 200 MHz		560		mA
			PYP, CV_{DD} = 1.2 V, CPU clock = 200 MHz		565		mA
			PYPA, CV_{DD} = 1.2 V, CPU clock = 167 MHz		480		mA
I_{DD3V}	I/O supply current[‡]		C6713, DV_{DD} = 3.3 V, EMIF speed = 100 MHz		75		mA
C_i	Input capacitance					7	pF
C_o	Output capacitance					7	pF

[†] For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

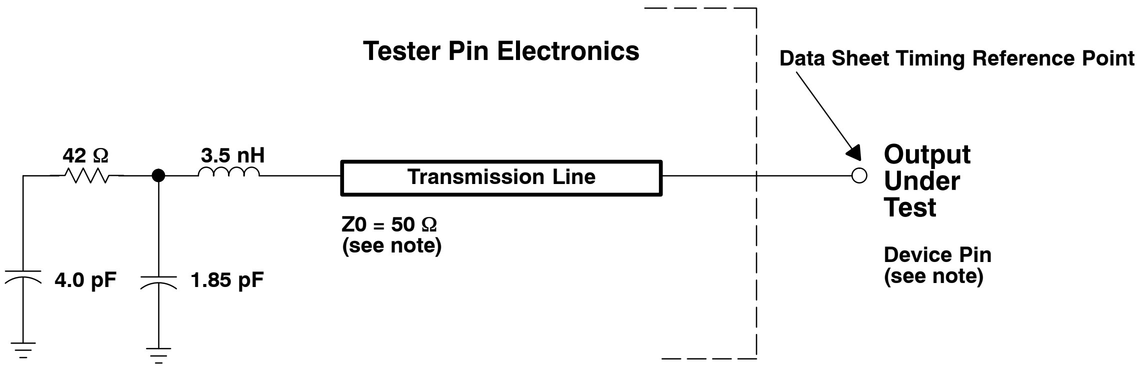
[‡] Measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. This model represents a device performing high-DSP-activity operations 50% of the time, and the remainder performing low-DSP-activity operations. The high/low-DSP-activity models are defined as follows:

High-DSP-Activity Model:
  CPU: 8 instructions/cycle with 2 LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions;
    L1 Program Memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit-switching)]
  McBSP: 2 channels at E1 rate
  Timers: 2 timers at maximum rate

Low-DSP-Activity Model:
  CPU: 2 instructions/cycle with 1 LDH instruction [L1 Data Memory: 16 bits/cycle; L1 Program Memory: 256 bits per 4 cycles;
    L2/EMIF EDMA: None]
  McBSP: 2 channels at E1 rate
  Timers: 2 timers at maximum rate

The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889).

PARAMETER MEASUREMENT INFORMATION



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 20. Test Load Circuit for AC Timing Measurements

signal transition levels

All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.

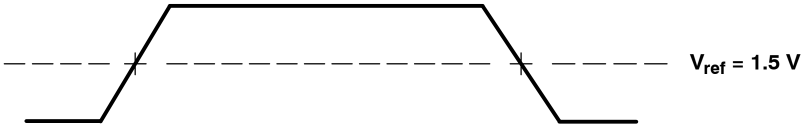


Figure 21. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

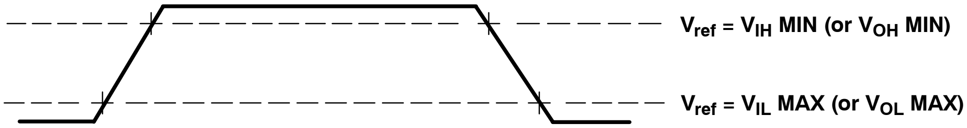


Figure 22. Rise and Fall Transition Time Voltage Reference Levels

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

timing parameters and board routing analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

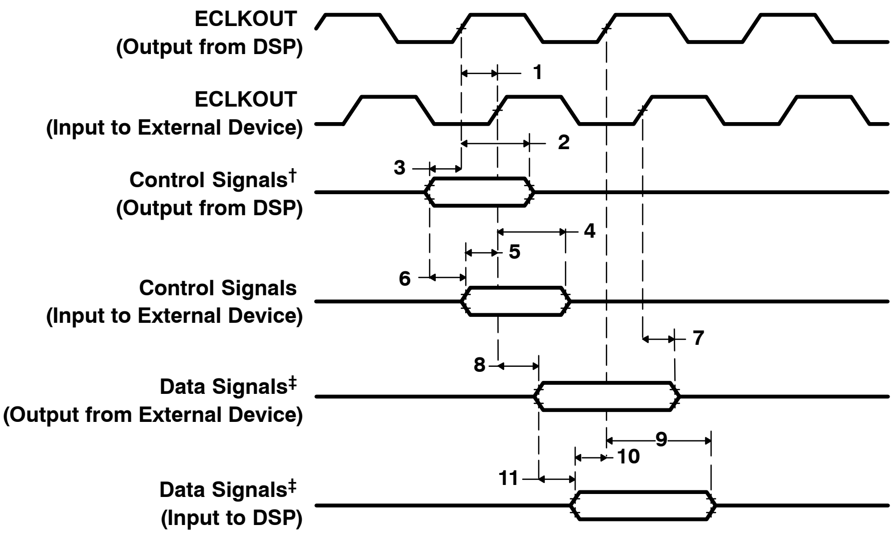
For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see Table 45 and Figure 23).

Figure 23 represents a general transfer between the DSP and an external device. The figure also represents board route delays and how they are perceived by the DSP and the external device.

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

Table 45. Board-Level Timings Example (see Figure 23)

NO.	DESCRIPTION
1	Clock route delay
2	Minimum DSP hold time
3	Minimum DSP setup time
4	External device hold time requirement
5	External device setup time requirement
6	Control signal route delay
7	External device hold time
8	External device access time
9	DSP hold time requirement
10	DSP setup time requirement
11	Data route delay



† Control signals include data for Writes.

‡ Data signals are generated during Reads from an external device.

Figure 23. Board-Level Input/Output Timings

INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN for C6713PYP-200 and C6713GDP-225†‡§ (see Figure 24)

NO.			PYP−200				GDP−225				UNIT
			PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN	5	83.3	5		4.4	83.3	4.4		ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.4C		0.4C		0.4C		0.4C		ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.4C		0.4C		0.4C		0.4C		ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN		5		5		5		5	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
§ See the *PLL and PLL controller* section of this data sheet.

timing requirements for CLKIN for C6713PYPA-167 and C6713GDPA-200†‡§ (see Figure 24)

NO.			PYPA−167				GDPA−200				UNIT
			PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN	6	83.3	6		5	83.3	5		ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.4C		0.4C		0.4C		0.4C		ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.4C		0.4C		0.4C		0.4C		ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN		5		5		5		5	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
§ See the *PLL and PLL controller* section of this data sheet.

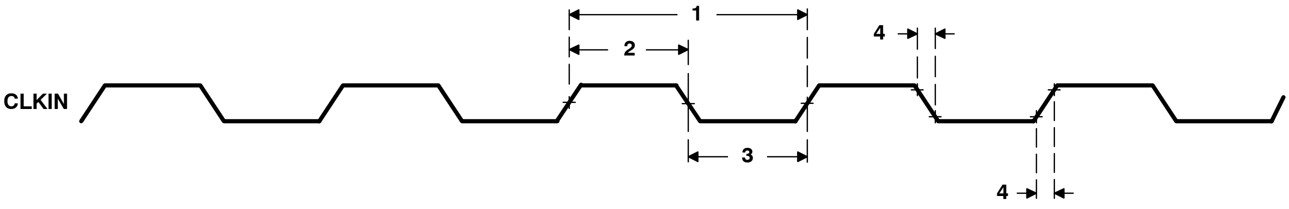


Figure 24. CLKIN Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT2[†‡] (see Figure 25)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{c(CKO2)}$	Cycle time, CLKOUT2	C2 − 0.8	C2 + 0.8	ns
2	$t_{w(CKO2H)}$	Pulse duration, CLKOUT2 high	(C2/2) − 0.8	(C2/2) + 0.8	ns
3	$t_{w(CKO2L)}$	Pulse duration, CLKOUT2 low	(C2/2) − 0.8	(C2/2) + 0.8	ns
4	$t_{t(CKO2)}$	Transition time, CLKOUT2		2	ns

[†] The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

[‡] C2 = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLK2 period, which ***must*** be set to CPU period divide-by-2.

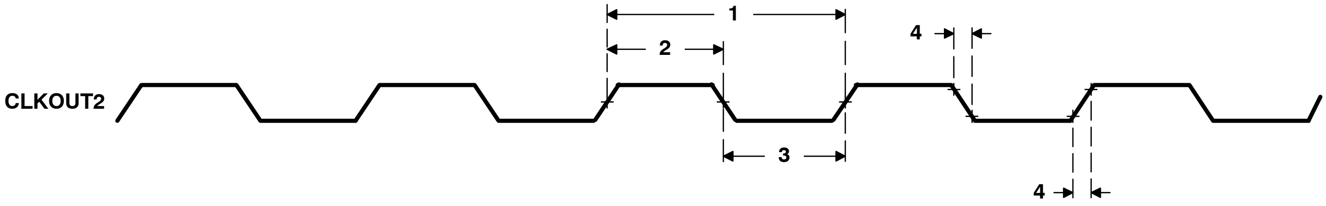


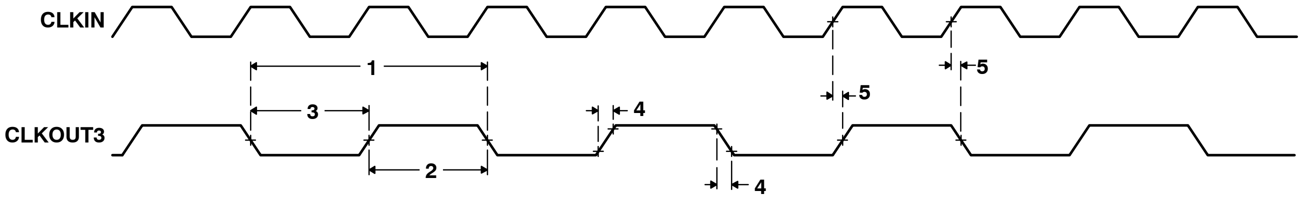
Figure 25. CLKOUT2 Timings

switching characteristics over recommended operating conditions for CLKOUT3[†§] (see Figure 26)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{c(CKO3)}$	Cycle time, CLKOUT3	C3 − 0.6	C3 + 0.6	ns
2	$t_{w(CKO3H)}$	Pulse duration, CLKOUT3 high	(C3/2) − 0.6	(C3/2) + 0.6	ns
3	$t_{w(CKO3L)}$	Pulse duration, CLKOUT3 low	(C3/2) − 0.6	(C3/2) + 0.6	ns
4	$t_{t(CKO3)}$	Transition time, CLKOUT3		2	ns
5	$t_{d(CLKINH\text{-}CKO3V)}$	Delay time, CLKIN high to CLKOUT3 valid	1.5	6.5	ns

[†] The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.

[§] C3 = CLKOUT3 period in ns. CLKOUT3 period is a divide-down of the CPU clock, configurable via the RATIO field in the PLLDIV3 register.



NOTE A: For this example, the CLKOUT3 frequency is CLKIN divide-by-2.

Figure 26. CLKOUT3 Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

timing requirements for ECLKIN[†] (see Figure 27)

NO.			PYPA–167 PYP–200 GDPA–200 GDP–225		UNIT
			MIN	MAX	
1	$t_{c(EKI)}$	Cycle time, ECLKIN	10		ns
2	$t_{w(EKIH)}$	Pulse duration, ECLKIN high	4.5		ns
3	$t_{w(EKIL)}$	Pulse duration, ECLKIN low	4.5		ns
4	$t_{t(EKI)}$	Transition time, ECLKIN		3	ns

[†] The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

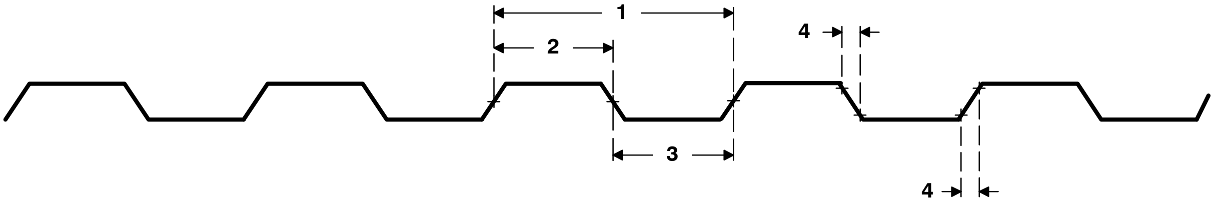


Figure 27. ECLKIN Timings

switching characteristics over recommended operating conditions for ECLKOUT[‡§#] (see Figure 28)

NO.	PARAMETER		PYPA–167 PYP–200 GDPA–200 GDP–225		UNIT
			MIN	MAX	
1	$t_{c(EKO)}$	Cycle time, ECLKOUT	E – 0.9	E + 0.9	ns
2	$t_{w(EKOH)}$	Pulse duration, ECLKOUT high	EH – 0.9	EH + 0.9	ns
3	$t_{w(EKOL)}$	Pulse duration, ECLKOUT low	EL – 0.9	EL + 0.9	ns
4	$t_{t(EKO)}$	Transition time, ECLKOUT		2	ns
5	$t_{d(EKIH-EKOH)}$	Delay time, ECLKIN high to ECLKOUT high	1	6.5	ns
6	$t_{d(EKIL-EKOL)}$	Delay time, ECLKIN low to ECLKOUT low	1	6.5	ns

[‡] The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
[§] E = ECLKIN period in ns
[¶] EH is the high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

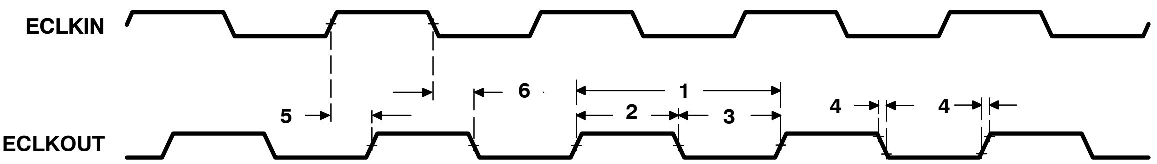


Figure 28. ECLKOUT Timings

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles[†‡§] (see Figure 29−Figure 30)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
3	$t_{su(EDV\text{-}AREH)}$	Setup time, EDx valid before $\overline{\text{ARE}}$ high	6.5		ns
4	$t_{h(AREH\text{-}EDV)}$	Hold time, EDx valid after $\overline{\text{ARE}}$ high	1		ns
6	$t_{su(ARDY\text{-}EKOH)}$	Setup time, ARDY valid before ECLKOUT high	3		ns
7	$t_{h(EKOH\text{-}ARDY)}$	Hold time, ARDY valid after ECLKOUT high	2.3		ns

[†] To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.

[‡] RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[§] E = ECLKOUT period in ns

switching characteristics over recommended operating conditions for asynchronous memory cycles[‡§¶] (see Figure 29−Figure 30)

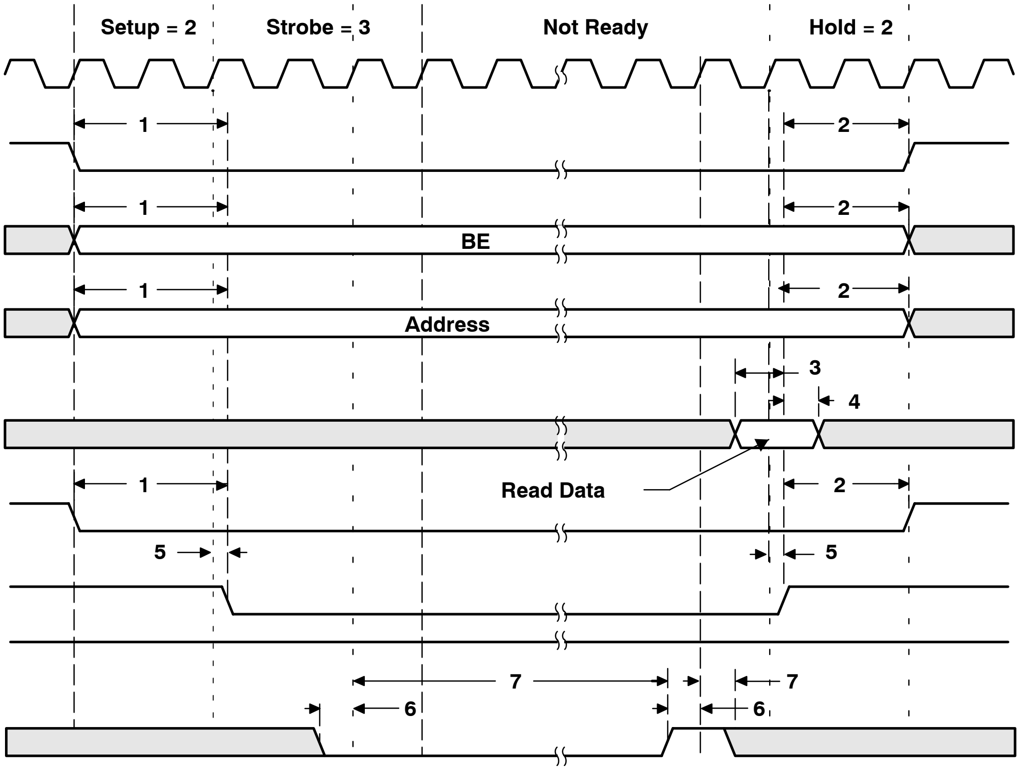
NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{osu(SELV\text{-}AREL)}$	Output setup time, select signals valid to $\overline{\text{ARE}}$ low	RS*E − 1.7		ns
2	$t_{oh(AREH\text{-}SELIV)}$	Output hold time, $\overline{\text{ARE}}$ high to select signals invalid	RH*E − 1.7		ns
5	$t_{d(EKOH\text{-}AREV)}$	Delay time, ECLKOUT high to $\overline{\text{ARE}}$ valid	1.5	7	ns
8	$t_{osu(SELV\text{-}AWEL)}$	Output setup time, select signals valid to $\overline{\text{AWE}}$ low	WS*E − 1.7		ns
9	$t_{oh(AWEH\text{-}SELIV)}$	Output hold time, $\overline{\text{AWE}}$ high to select signals invalid	WH*E − 1.7		ns
10	$t_{d(EKOH\text{-}AWEV)}$	Delay time, ECLKOUT high to $\overline{\text{AWE}}$ valid	1.5	7	ns

[‡] RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[§] E = ECLKOUT period in ns

[¶] Select signals include: $\overline{\text{CE}}$x, $\overline{\text{BE[3:0]}}$, EA[21:2], $\overline{\text{AOE}}$; and for writes, include ED[31:0].

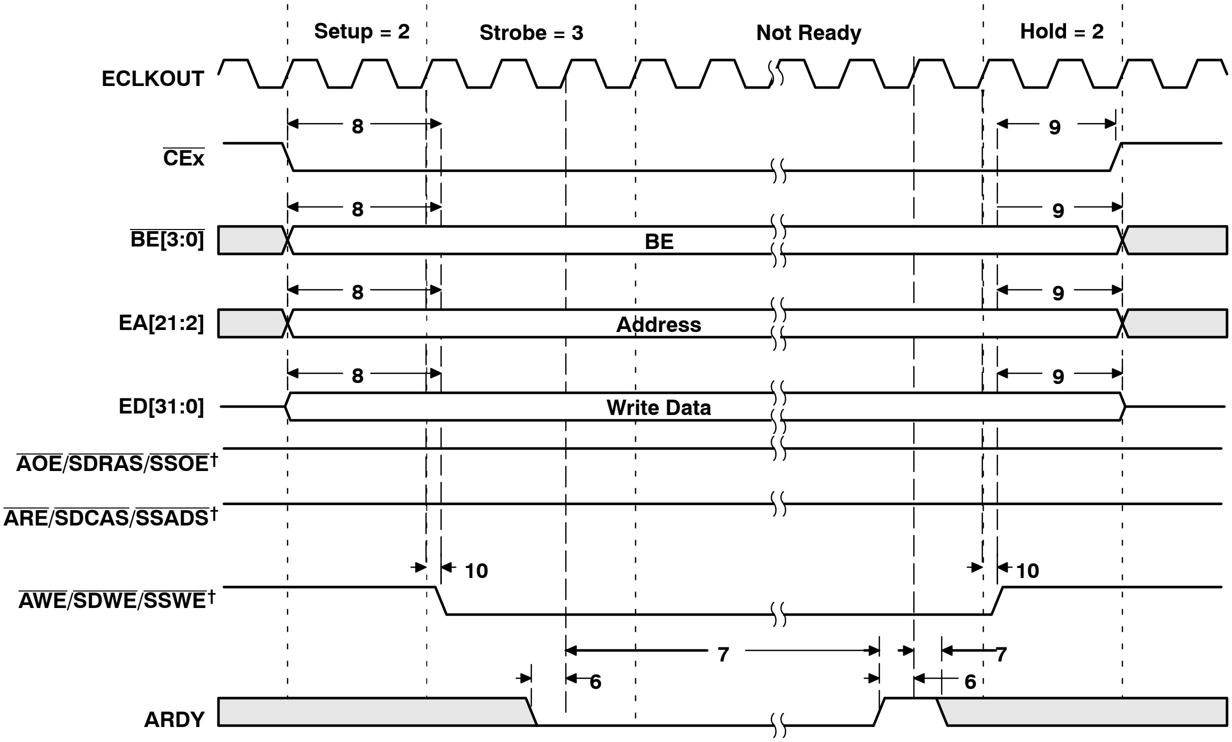
ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$, $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, and $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$ operate as $\overline{\text{AOE}}$ (identified under select signals), $\overline{\text{ARE}}$, and $\overline{\text{AWE}}$, respectively, during asynchronous memory accesses.

Figure 29. Asynchronous Memory Read Timing

ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† $\overline{\text{AOE}}$/SDRAS/SSOE, $\overline{\text{ARE}}$/SDCAS/SSADS, and $\overline{\text{AWE}}$/SDWE/SSWE operate as $\overline{\text{AOE}}$ (identified under select signals), $\overline{\text{ARE}}$, and $\overline{\text{AWE}}$, respectively, during asynchronous memory accesses.

Figure 30. Asynchronous Memory Write Timing

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles[†] (see Figure 31)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
6	$t_{su(EDV\text{-}EKOH)}$	Setup time, read EDx valid before ECLKOUT high	1.5		ns
7	$t_{h(EKOH\text{-}EDV)}$	Hold time, read EDx valid after ECLKOUT high	2.5		ns

[†] The C6713 SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

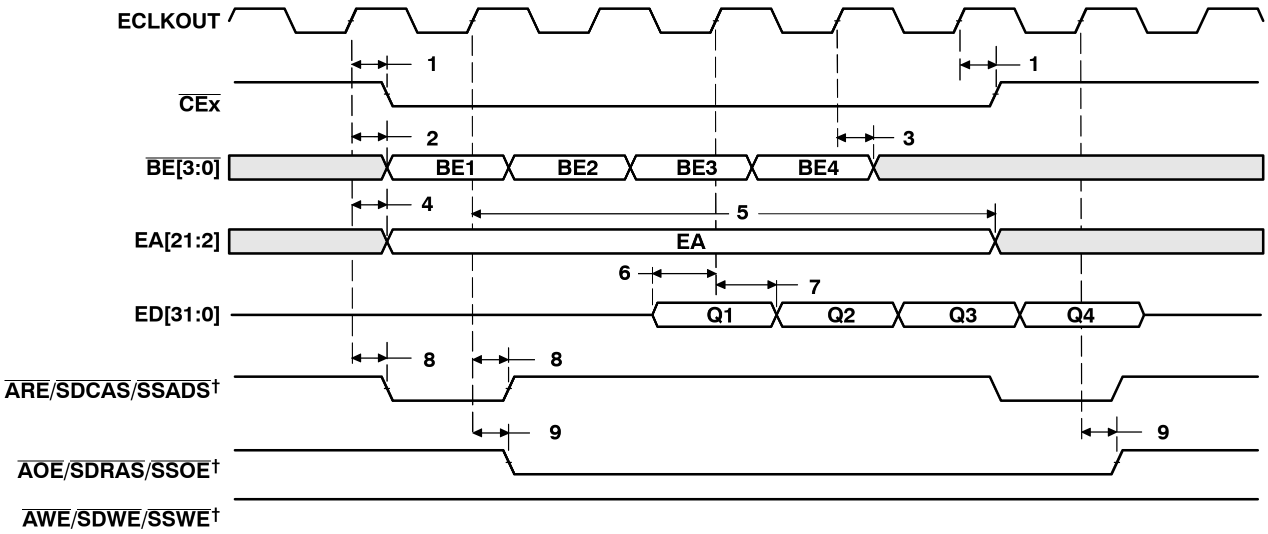
switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles[†‡] (see Figure 31 and Figure 32)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{d(EKOH\text{-}CEV)}$	Delay time, ECLKOUT high to $\overline{\text{CEx}}$ valid	1.2	7	ns
2	$t_{d(EKOH\text{-}BEV)}$	Delay time, ECLKOUT high to $\overline{\text{BEx}}$ valid		7	ns
3	$t_{d(EKOH\text{-}BEIV)}$	Delay time, ECLKOUT high to $\overline{\text{BEx}}$ invalid	1.2		ns
4	$t_{d(EKOH\text{-}EAV)}$	Delay time, ECLKOUT high to EAx valid		7	ns
5	$t_{d(EKOH\text{-}EAIV)}$	Delay time, ECLKOUT high to EAx invalid	1.2		ns
8	$t_{d(EKOH\text{-}ADSV)}$	Delay time, ECLKOUT high to $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$ valid	1.2	7	ns
9	$t_{d(EKOH\text{-}OEV)}$	Delay time, ECLKOUT high to, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ valid	1.2	7	ns
10	$t_{d(EKOH\text{-}EDV)}$	Delay time, ECLKOUT high to $\overline{\text{EDx}}$ valid		7	ns
11	$t_{d(EKOH\text{-}EDIV)}$	Delay time, ECLKOUT high to $\overline{\text{EDx}}$ invalid	1.2		ns
12	$t_{d(EKOH\text{-}WEV)}$	Delay time, ECLKOUT high to $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$ valid	1.2	7	ns

[†] The C6713 SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

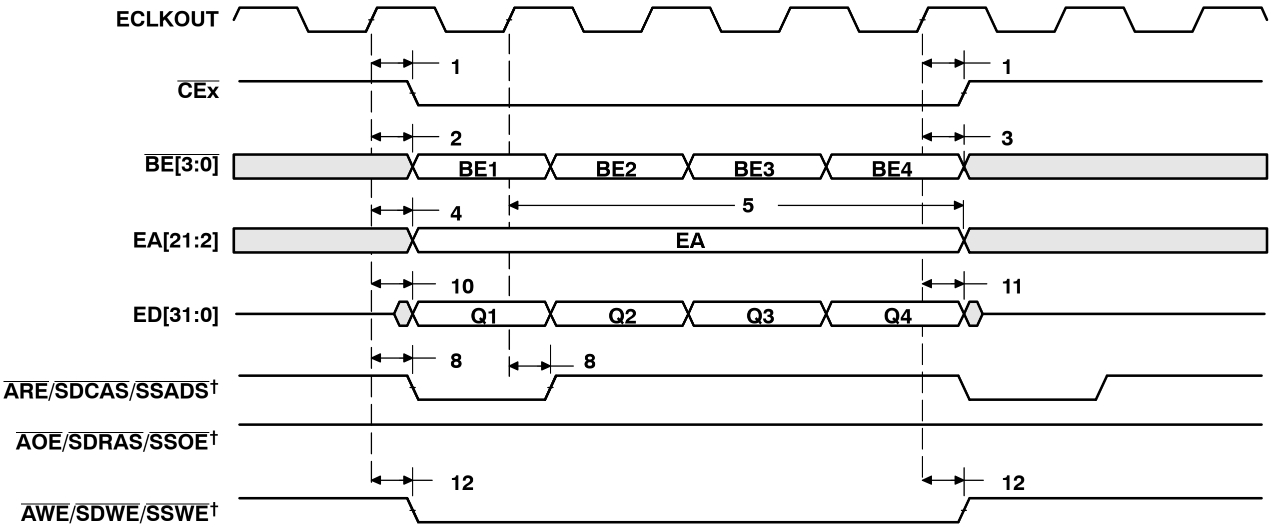
[‡] $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)



† $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

Figure 31. SBSRAM Read Timing



† $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$, respectively, during SBSRAM accesses.

Figure 32. SBSRAM Write Timing

SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles[†] (see Figure 33)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
6	$t_{\text{su(EDV-EKOH)}}$	Setup time, read EDx valid before ECLKOUT high	1.5		ns
7	$t_{\text{h(EKOH-EDV)}}$	Hold time, read EDx valid after ECLKOUT high	2.5		ns

[†] The C6713 SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

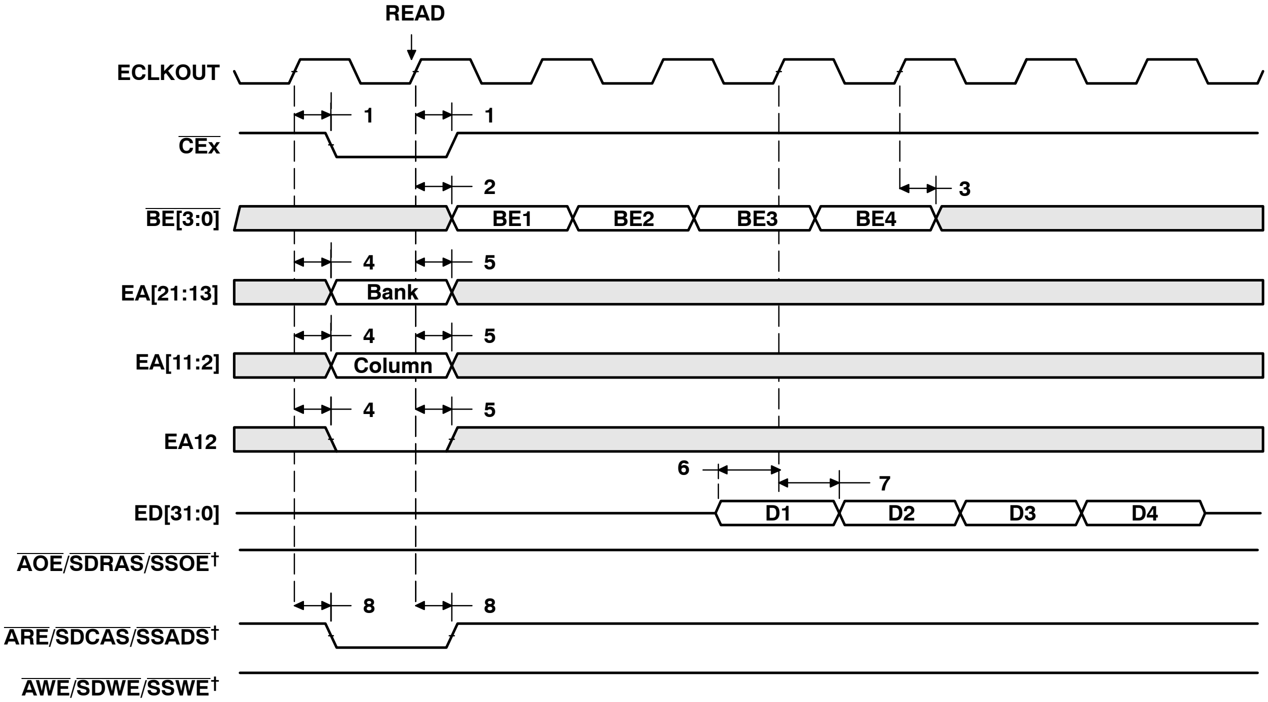
switching characteristics over recommended operating conditions for synchronous DRAM cycles[†‡] (see Figure 33−Figure 39)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{\text{d(EKOH-CEV)}}$	Delay time, ECLKOUT high to $\overline{\text{CE}}$x valid	1.5	7	ns
2	$t_{\text{d(EKOH-BEV)}}$	Delay time, ECLKOUT high to $\overline{\text{BE}}$x valid		7	ns
3	$t_{\text{d(EKOH-BEIV)}}$	Delay time, ECLKOUT high to $\overline{\text{BE}}$x invalid	1.5		ns
4	$t_{\text{d(EKOH-EAV)}}$	Delay time, ECLKOUT high to EAx valid		7	ns
5	$t_{\text{d(EKOH-EAIV)}}$	Delay time, ECLKOUT high to EAx invalid	1.5		ns
8	$t_{\text{d(EKOH-CASV)}}$	Delay time, ECLKOUT high to $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$ valid	1.5	7	ns
9	$t_{\text{d(EKOH-EDV)}}$	Delay time, ECLKOUT high to $\overline{\text{ED}}$x valid		7	ns
10	$t_{\text{d(EKOH-EDIV)}}$	Delay time, ECLKOUT high to $\overline{\text{ED}}$x invalid	1.5		ns
11	$t_{\text{d(EKOH-WEV)}}$	Delay time, ECLKOUT high to $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$ valid	1.5	7	ns
12	$t_{\text{d(EKOH-RAS)}}$	Delay time, ECLKOUT high to, $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ valid	1.5	7	ns

[†] The C6713 SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

[‡] $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

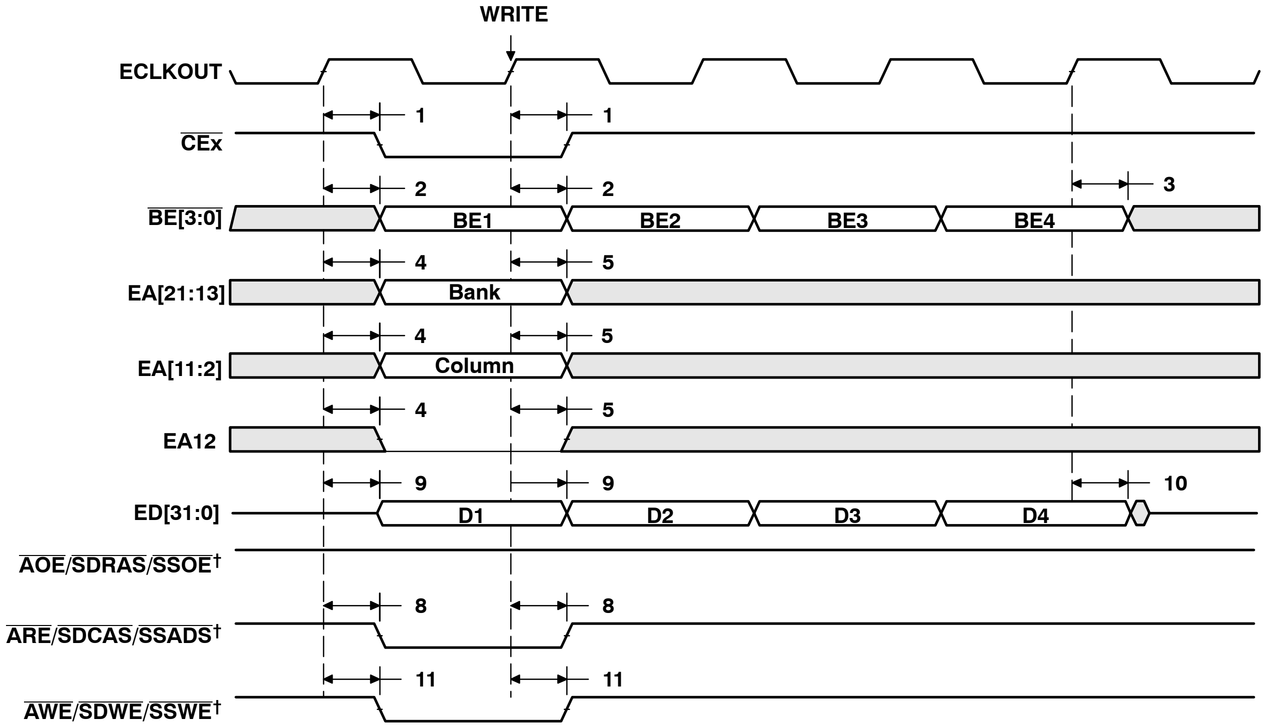
SYNCHRONOUS DRAM TIMING (CONTINUED)



† $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

Figure 33. SDRAM Read Command (CAS Latency 3)

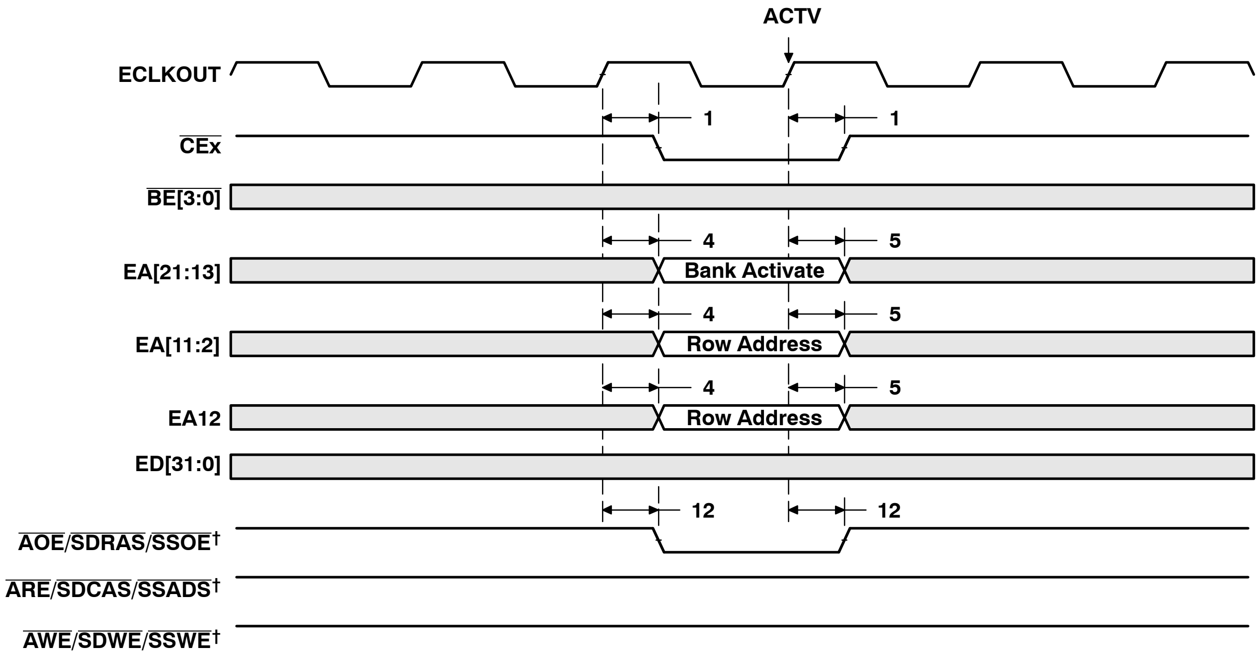
SYNCHRONOUS DRAM TIMING (CONTINUED)



† $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, and $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

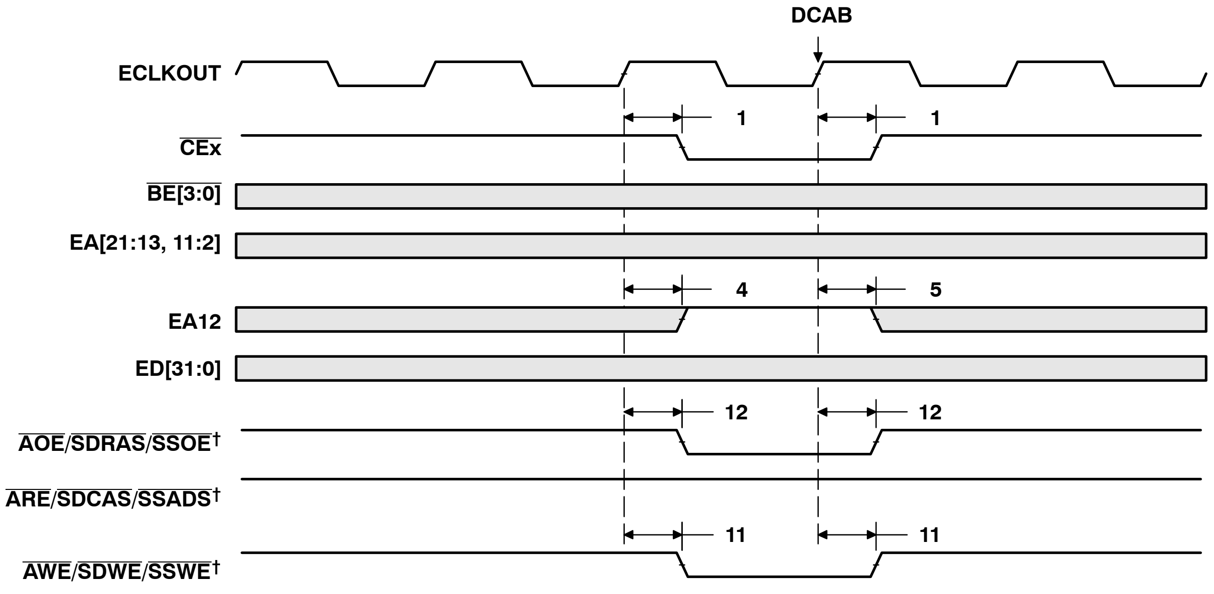
Figure 34. SDRAM Write Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

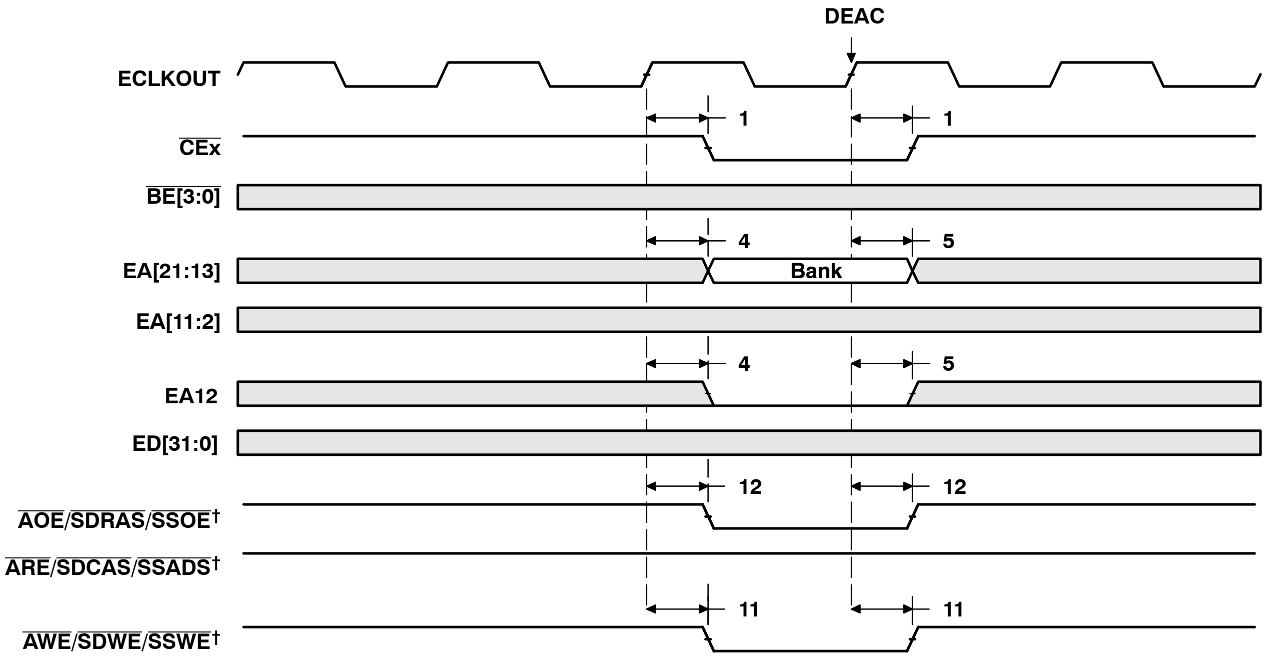
Figure 35. SDRAM ACTV Command



† $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

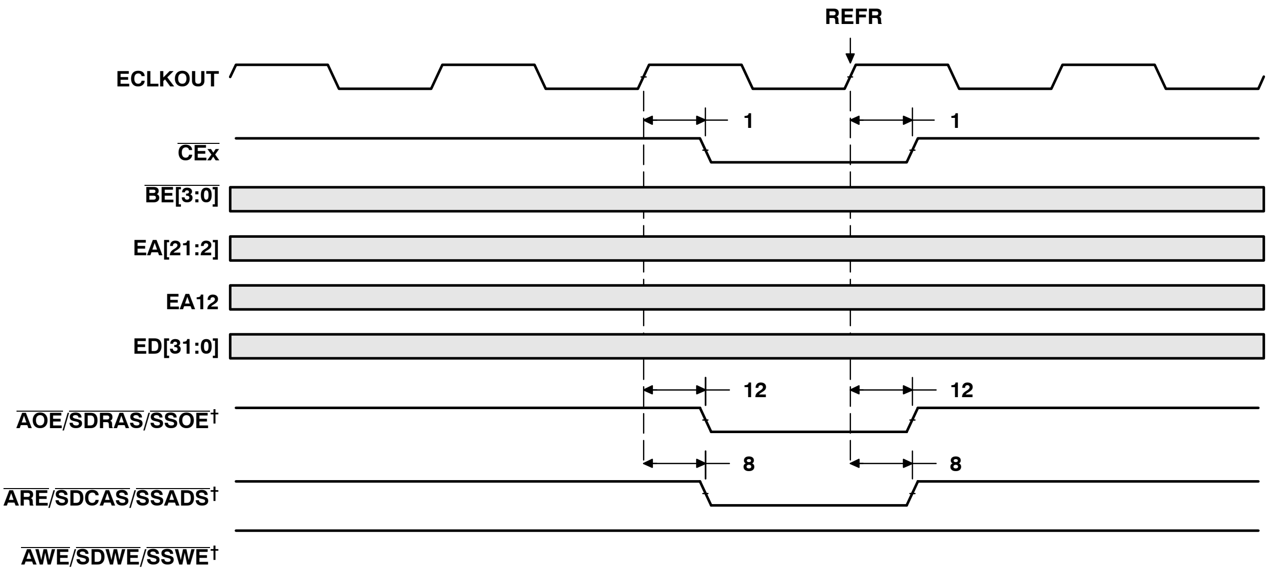
Figure 36. SDRAM DCAB Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, and $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

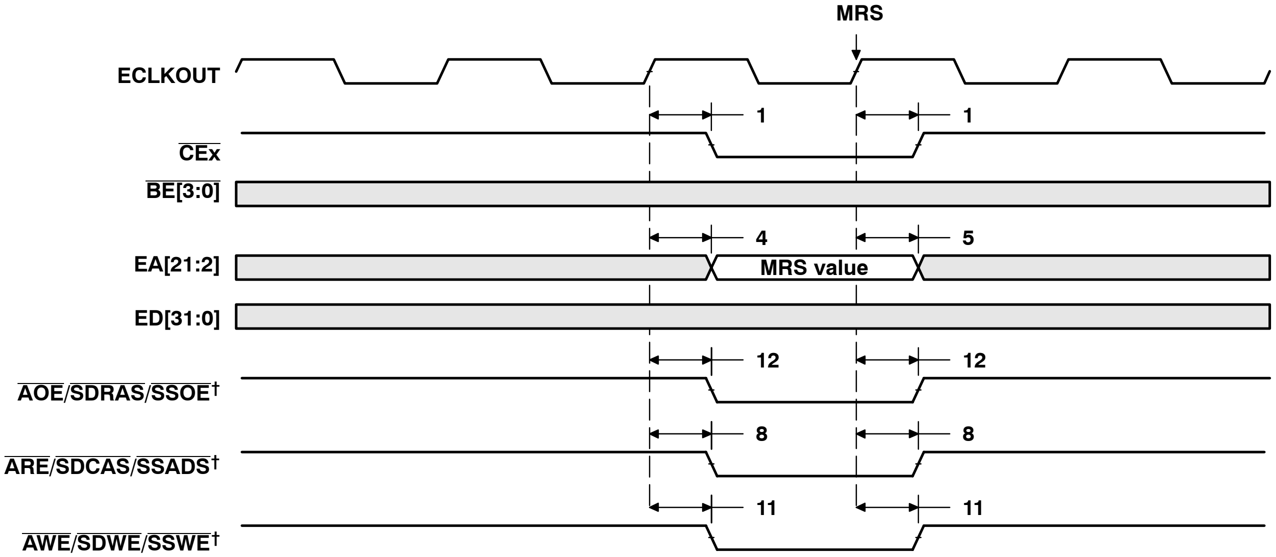
Figure 37. SDRAM DEAC Command



† $\overline{\text{ARE}}/\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{AWE}}/\overline{\text{SDWE}}/\overline{\text{SSWE}}$, and $\overline{\text{AOE}}/\overline{\text{SDRAS}}/\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

Figure 38. SDRAM REFR Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, and $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, and $\overline{\text{SDRAS}}$, respectively, during SDRAM accesses.

Figure 39. SDRAM MRS Command

$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ TIMING

timing requirements for the $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ cycles† (see Figure 40)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
3	$t_{h(HOLDAL-HOLDL)}$	Hold time, $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low	E		ns

† E = ECLKOUT period in ns

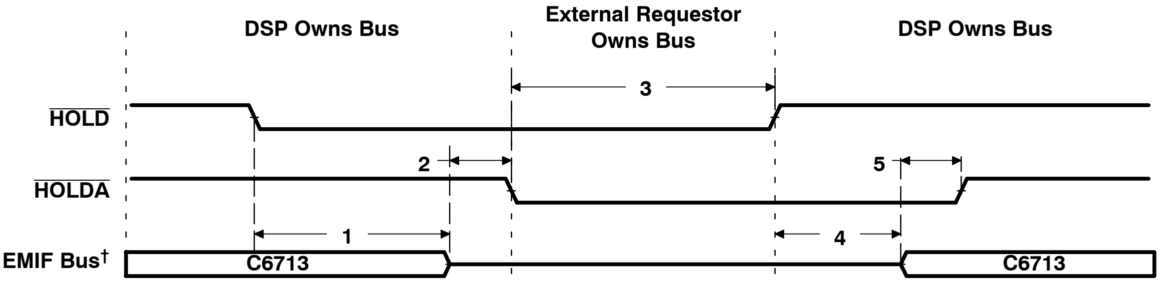
switching characteristics over recommended operating conditions for the $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ cycles†‡ (see Figure 40)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{d(HOLDL-EMHZ)}$	Delay time, $\overline{\text{HOLD}}$ low to EMIF Bus high impedance	2E	§	ns
2	$t_{d(EMHZ-HOLDAL)}$	Delay time, EMIF Bus high impedance to $\overline{\text{HOLDA}}$ low	0	2E	ns
4	$t_{d(HOLDH-EMLZ)}$	Delay time, $\overline{\text{HOLD}}$ high to EMIF Bus low impedance	2E	7E	ns
5	$t_{d(EMLZ-HOLDAH)}$	Delay time, EMIF Bus low impedance to $\overline{\text{HOLDA}}$ high	0	2E	ns

† E = ECLKOUT period in ns

‡ EMIF Bus consists of $\overline{\text{CE[3:0]}}$, $\overline{\text{BE[3:0]}}$, ED[31:0], EA[21:2], $\overline{\text{ARE/SDCAS/SSADS}}$, $\overline{\text{AOE/SDRAS/SSOE}}$, and $\overline{\text{AWE/SDWE/SSWE}}$.

§ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.



† EMIF Bus consists of $\overline{\text{CE[3:0]}}$, $\overline{\text{BE[3:0]}}$, ED[31:0], EA[21:2], $\overline{\text{ARE/SDCAS/SSADS}}$, $\overline{\text{AOE/SDRAS/SSOE}}$, and $\overline{\text{AWE/SDWE/SSWE}}$.

Figure 40. $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ Timing

BUSREQ TIMING

switching characteristics over recommended operating conditions for the BUSREQ cycles (see Figure 41)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{d(EKOH\text{-}BUSRV)}$	Delay time, ECLKOUT high to BUSREQ valid	1.5	7.2	ns

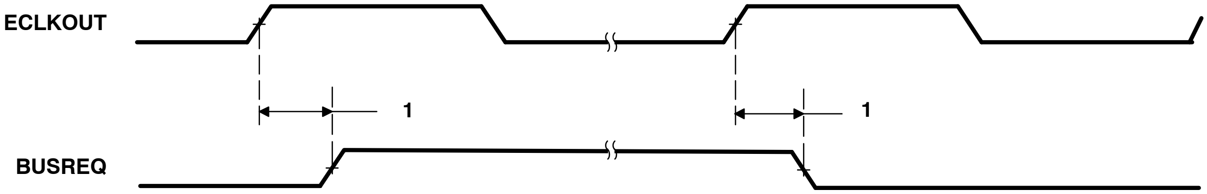


Figure 41. BUSREQ Timing

RESET TIMING

timing requirements for reset[†‡] (see Figure 42)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{w(RST)}$	Pulse duration, $\overline{\text{RESET}}$	100		ns
13	$t_{su(HD)}$	Setup time, HD boot configuration bits valid before $\overline{\text{RESET}}$ high[§]	2P		ns
14	$t_{h(HD)}$	Hold time, HD boot configuration bits valid after $\overline{\text{RESET}}$ high[§]	2P		ns

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

[‡] For the C6713 device, the PLL is bypassed immediately after the device comes out of reset. The PLL Controller can be programmed to change the PLL mode in software. For more detailed information on the PLL Controller, see the *TMS320C6000 DSP Phase-Lock Loop (PLL) Controller Peripheral Reference Guide* (literature number SPRU233).

[§] The Boot and device configurations bits are latched asynchronously when RESET is transitioning high. The Boot and device configurations bits consist of: HD[14, 8, 4:3].

switching characteristics over recommended operating conditions during reset[¶] (see Figure 42)

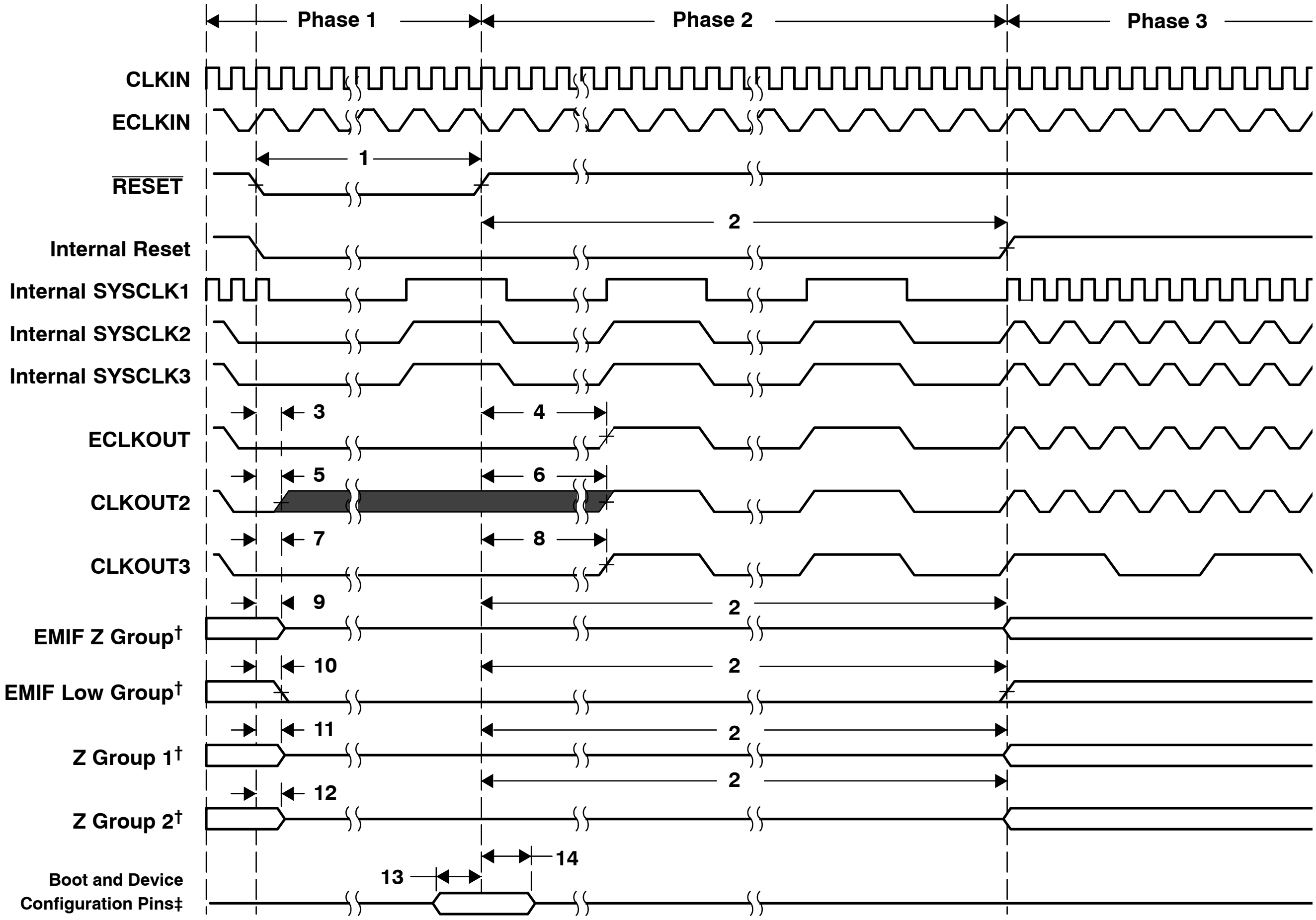
NO.	PARAMETER			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
				MIN	MAX	
2	$t_{d(RSTH-ZV)}$	Delay time, external $\overline{\text{RESET}}$ high to internal reset high and all signal groups valid[#‖]	CLKMODE0 = 1		512 x CLKIN period	ns
3	$t_{d(RSTL-ECKOL)}$	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT low		0		ns
4	$t_{d(RSTH-ECKOV)}$	Delay time, $\overline{\text{RESET}}$ high to ECLKOUT valid			6P	ns
5	$t_{d(RSTL-CKO2IV)}$	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid		0		ns
6	$t_{d(RSTH-CKO2V)}$	Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid			6P	ns
7	$t_{d(RSTL-CKO3L)}$	Delay time, $\overline{\text{RESET}}$ low to CLKOUT3 low		0		ns
8	$t_{d(RSTH-CKO3V)}$	Delay time, $\overline{\text{RESET}}$ high to CLKOUT3 valid			6P	ns
9	$t_{d(RSTL-EMIFZHZ)}$	Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance[‖]		0		ns
10	$t_{d(RSTL-EMIFLIV)}$	Delay time, $\overline{\text{RESET}}$ low to EMIF low group (BUSREQ) invalid[‖]		0		ns
11	$t_{d(RSTL-Z1HZ)}$	Delay time, $\overline{\text{RESET}}$ low to Z group 1 high impedance[‖]		0		ns
12	$t_{d(RSTL-Z2HZ)}$	Delay time, $\overline{\text{RESET}}$ low to Z group 2 high impedance[‖]		0		ns

[¶] P = 1/CPU clock frequency in ns.
Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, then the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, P = SYSCLK1 = 160 ns while internal reset is asserted.

[#] The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when RESET is deasserted, the actual delay time may vary.

[‖] EMIF Z group consists of: EA[21:2], ED[31:0], $\overline{\text{CE}}$[3:0], $\overline{\text{BE}}$[3:0], $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ and $\overline{\text{HOLDA}}$
EMIF low group consists of: BUSREQ
Z group 1 consists of: CLKR0/ACLKR0, CLKR1/AXR0[6], CLKX0/ACLKX0, CLKX1/AMUTE0, FSR0/AFSR0, FSR1/AXR0[7], FSX0/AFSX0, FSX1, DX0/AXR0[1], DX1/AXR0[5], TOUT0/AXR0[2], TOUT1/AXR0[4], SDA0 and SCL0.
Z group 2 consists of: All other HPI, McASP0/1, GPIO, and I2C1 signals.

RESET TIMING (CONTINUED)



† EMIF Z group consists of: EA[21:2], ED[31:0], $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, $\overline{ARE}$/$\overline{SDCAS}$/$\overline{SSADS}$, $\overline{AWE}$/$\overline{SDWE}$/$\overline{SSWE}$, $\overline{AOE}$/$\overline{SDRAS}$/$\overline{SSOE}$ and $\overline{HOLDA}$

EMIF low group consists of: BUSREQ

Z group 1 consists of: CLKR0/ACLKR0, CLKR1/AXR0[6], CLKX0/ACLKX0, CLKX1/AMUTE0, FSR0/AFSR0, FSR1/AXR0[7], FSX0/AFSX0, FSX1, DX0/AXR0[1], DX1/AXR0[5], TOUT0/AXR0[2], TOUT1/AXR0[4], SDA0 and SCL0.

Z group 2 consists of: All other HPI, McASP0/1, GPIO, and I2C1 signals.

‡ Boot and device configurations consist of: HD[14, 8, 4:3].

Figure 42. Reset Timing

Reset Phase 1: The $\overline{\text{RESET}}$ pin is asserted. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 2: The $\overline{\text{RESET}}$ pin is deasserted but the internal reset is stretched. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 3: Both the $\overline{\text{RESET}}$ pin and internal reset are deasserted. During this time, all internal clocks are running at their default divide-down frequency of CLKIN. The CPU clock (SYSCLK1) is running at CLKIN frequency. The peripheral clock (SYSCLK2) is running at CLKIN frequency divide-by-2. The EMIF internal clock source (SYSCLK3) is running at CLKIN frequency divide-by-2. SYSCLK3 is reflected on the ECLKOUT pin (when EKSRC bit = 0 [default]). CLKOUT3 is running at CLKIN frequency divide-by-8.

EXTERNAL INTERRUPT TIMING

timing requirements for external interrupts† (see Figure 43)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{w(ILOW)}$	Width of the NMI interrupt pulse low	2P		ns
		Width of the EXT_INT interrupt pulse low	4P		ns
2	$t_{w(IHIGH)}$	Width of the NMI interrupt pulse high	2P		ns
		Width of the EXT_INT interrupt pulse high	4P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

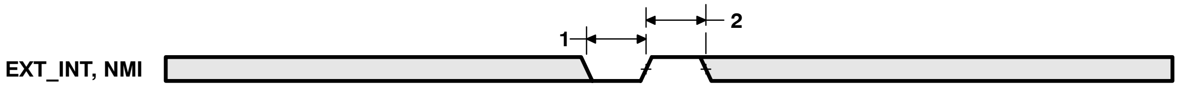


Figure 43. External/NMI Interrupt Timing

MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING

timing requirements for McASP (see Figure 44 and Figure 45)

NO.				PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
				MIN	MAX	
1	$t_{c(AHCKRX)}$	Cycle time, AHCLKR/X		20		ns
2	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR/X high or low		7.5		ns
3	$t_{c(ACKRX)}$	Cycle time, ACLKR/X	ACLKR/X ext	33		ns
4	$t_{w(ACKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X ext	14		ns
5	$t_{su(AFRXC\text{-}ACKRX)}$	Setup time, AFSR/X input valid before ACLKR/X latches data	ACLKR/X int	6		ns
			ACLKR/X ext	3		ns
6	$t_{h(ACKRX\text{-}AFRX)}$	Hold time, AFSR/X input valid after ACLKR/X latches data	ACLKR/X int	0		ns
			ACLKR/X ext	3		ns
7	$t_{su(AXR\text{-}ACKRX)}$	Setup time, AXR input valid before ACLKR/X latches data	ACLKR/X int	8		ns
			ACLKR/X ext	3		ns
8	$t_{h(ACKRX\text{-}AXR)}$	Hold time, AXR input valid after ACLKR/X latches data	ACLKR/X int	1		ns
			ACLKR/X ext	3		ns

switching characteristics over recommended operating conditions for McASP[†] (see Figure 44 and Figure 45)

NO.	PARAMETER			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
				MIN	MAX	
9	$t_{c(AHCKRX)}$	Cycle time, AHCLKR/X		20		ns
10	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR/X high or low		(AH/2) − 2.5		ns
11	$t_{c(ACKRX)}$	Cycle time, ACLKR/X	ACLKR/X int	33		ns
12	$t_{w(ACKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X int	(A/2) − 2.5		ns
13	$t_{d(ACKRX\text{-}AFRX)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	−1	5	ns
			ACLKR/X ext	0	10	ns
14	$t_{d(ACKX\text{-}AXRV)}$	Delay time, ACLKX transmit edge to AXR output valid	ACLKR/X int	−1	5	ns
			ACLKR/X ext	0	10	ns
15	$t_{dis(ACKRX-AXRHZ)}$	Disable time, AXR high impedance following last data bit from ACLKR/X transmit edge	ACLKR/X int	−1	10	ns
			ACLKR/X ext	−1	10	ns

[†] AH = AHCLKR/X period in ns.
A = ACLKR/X period in ns.

MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING (CONTINUED)

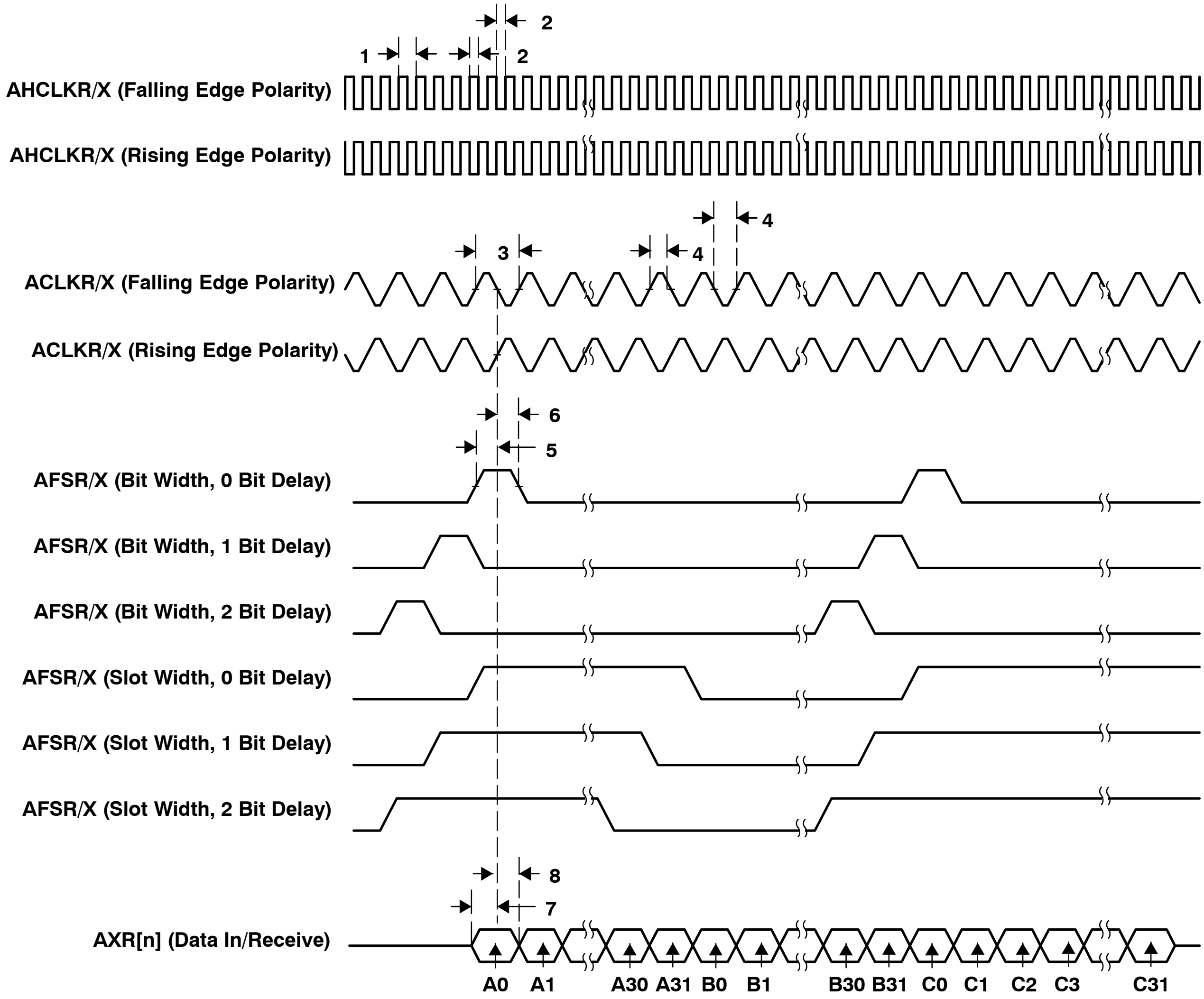


Figure 44. McASP Input Timings

MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING (CONTINUED)

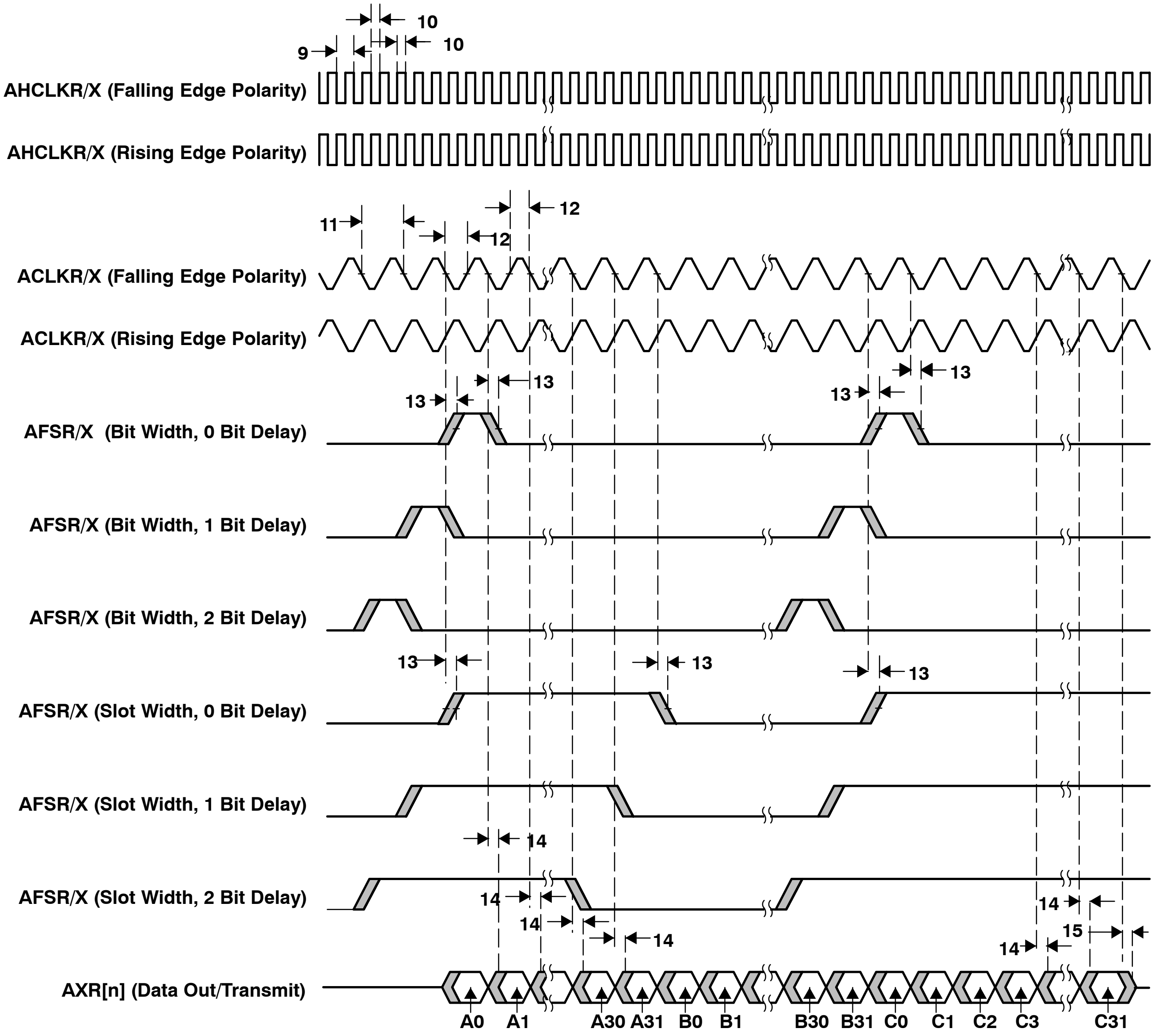


Figure 45. McASP Output Timings

INTER-INTEGRATED CIRCUITS (I2C) TIMING

timing requirements for I2C timings[†] (see Figure 46)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		μs
2	$t_{su(SCLH\text{-}SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μs
3	$t_{h(SCLL\text{-}SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		μs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		μs
6	$t_{su(SDAV\text{-}SDLH)}$	Setup time, SDA valid before SCL high	250		100[‡]		ns
7	$t_{h(SDA\text{-}SDLL)}$	Hold time, SDA valid after SCL low (For I^{2}C bus™ devices)	0[§]		0[§]	0.9[¶]	μs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μs
9	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1C_b[#]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1C_b[#]	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1C_b[#]	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1C_b[#]	300	ns
13	$t_{su(SCLH\text{-}SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b[#]	Capacitive load for each bus line		400		400	pF

[†] The I^{2}C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

[‡] A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-Bus Specification) before the SCL line is released.

[§] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[¶] The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

[#] C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

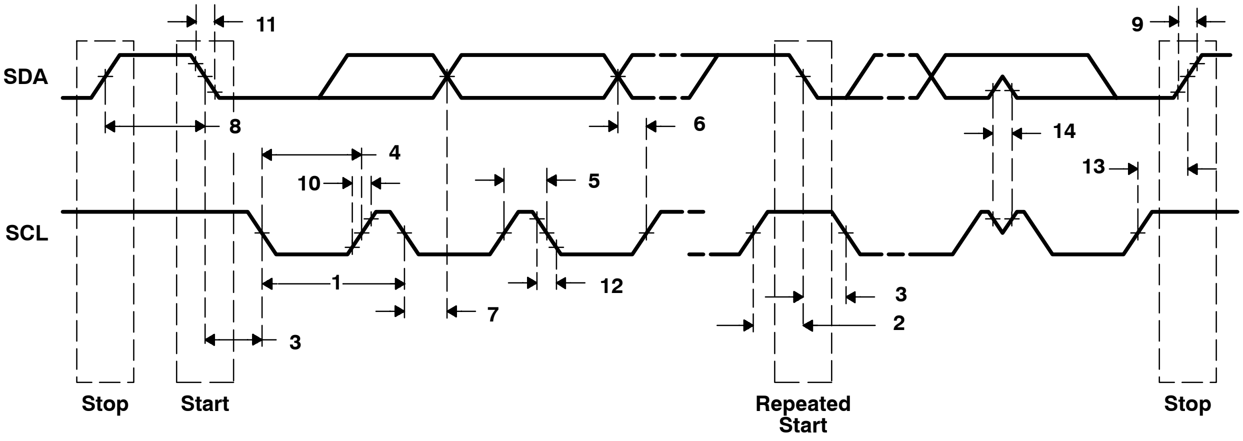


Figure 46. I^{2}C Receive Timings

INTER-INTEGRATED CIRCUITS (I2C) TIMING (CONTINUED)

switching characteristics for I2C timings† (see Figure 47)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SDLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SDLL-SDAV)}$	Valid time, SDA valid after SCL low (For I^{2}C bus™ devices)	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$†	300	ns
25	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$†	300	ns
26	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$†	300	ns
27	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$†	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

† C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

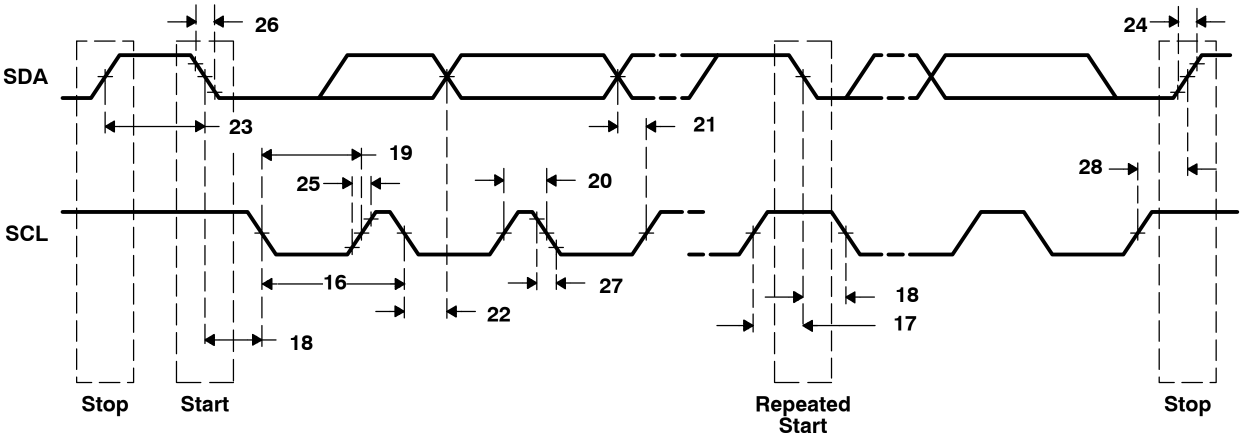


Figure 47. I^{2}C Transmit Timings

HOST-PORT INTERFACE TIMING

timing requirements for host-port interface cycles[†][‡] (see Figure 48, Figure 49, Figure 50, and Figure 51)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{\text{su(SELV-HSTBL)}}$	Setup time, select signals[§] valid before $\overline{\text{HSTROBE}}$ low	5		ns
2	$t_{\text{h(HSTBL-SELV)}}$	Hold time, select signals[§] valid after $\overline{\text{HSTROBE}}$ low	4		ns
3	$t_{\text{w(HSTBL)}}$	Pulse duration, $\overline{\text{HSTROBE}}$ low	4P		ns
4	$t_{\text{w(HSTBH)}}$	Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses	4P		ns
10	$t_{\text{su(SELV-HASL)}}$	Setup time, select signals[§] valid before $\overline{\text{HAS}}$ low	5		ns
11	$t_{\text{h(HASL-SELV)}}$	Hold time, select signals[§] valid after $\overline{\text{HAS}}$ low	3		ns
12	$t_{\text{su(HDV-HSTBH)}}$	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	5		ns
13	$t_{\text{h(HSTBH-HDV)}}$	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	3		ns
14	$t_{\text{h(HRDYL-HSTBL)}}$	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	2		ns
18	$t_{\text{su(HASL-HSTBL)}}$	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	2		ns
19	$t_{\text{h(HSTBL-HASL)}}$	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	2		ns

[†] $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

[‡] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

[§] Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$, and HHWIL.

switching characteristics over recommended operating conditions during host-port interface cycles[†][‡] (see Figure 48, Figure 49, Figure 50, and Figure 51)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
5	$t_{\text{d(HCS-HRDY)}}$	Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}$[¶]	1	12	ns
6	$t_{\text{d(HSTBL-HRDYH)}}$	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high[#]	3	12	ns
7	$t_{\text{d(HSTBL-HDLZ)}}$	Delay time, $\overline{\text{HSTROBE}}$ low to HD low impedance for an HPI read	2		ns
8	$t_{\text{d(HDV-HRDYL)}}$	Delay time, HD valid to $\overline{\text{HRDY}}$ low	2P − 4		ns
9	$t_{\text{oh(HSTBH-HDV)}}$	Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high	3	12	ns
15	$t_{\text{d(HSTBH-HDHZ)}}$	Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance	3	12	ns
16	$t_{\text{d(HSTBL-HDV)}}$	Delay time, $\overline{\text{HSTROBE}}$ low to HD valid	3	12	ns
17	$t_{\text{d(HSTBH-HRDYH)}}$	Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ high[‖]	3	12	ns

[†] $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

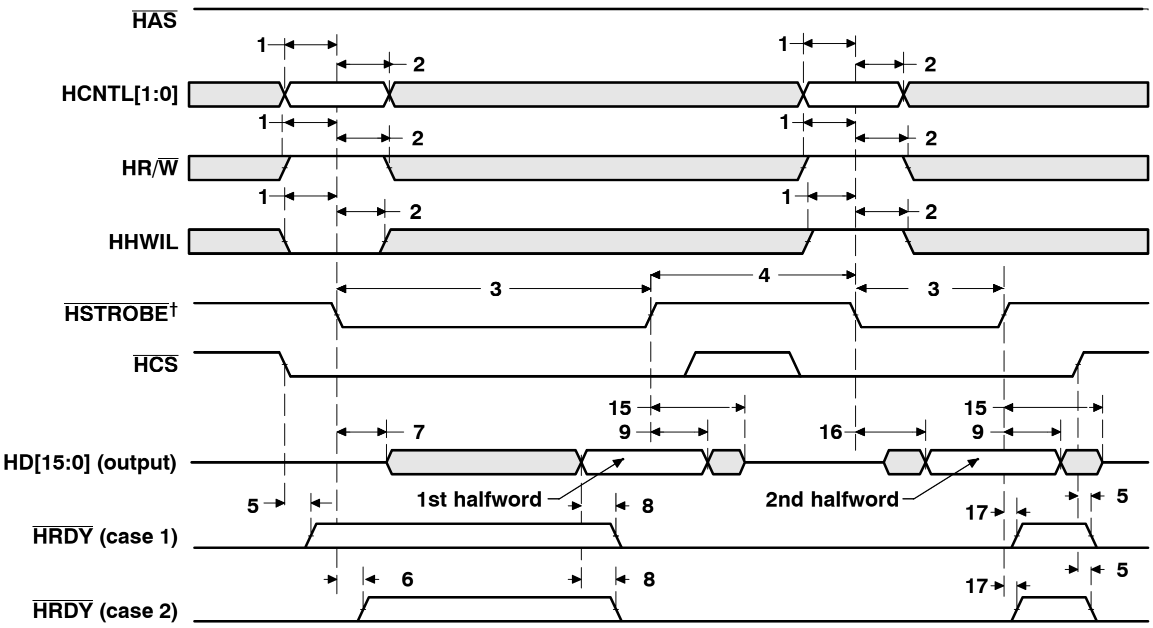
[‡] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

[¶] $\overline{\text{HCS}}$ enables $\overline{\text{HRDY}}$, and $\overline{\text{HRDY}}$ is always low when $\overline{\text{HCS}}$ is high. The case where $\overline{\text{HRDY}}$ goes high when $\overline{\text{HCS}}$ falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

[#] This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of $\overline{\text{HSTROBE}}$, the HPI sends the request to the EDMA internal address generation hardware, and $\overline{\text{HRDY}}$ remains high until the EDMA internal address generation hardware loads the requested data into HPID.

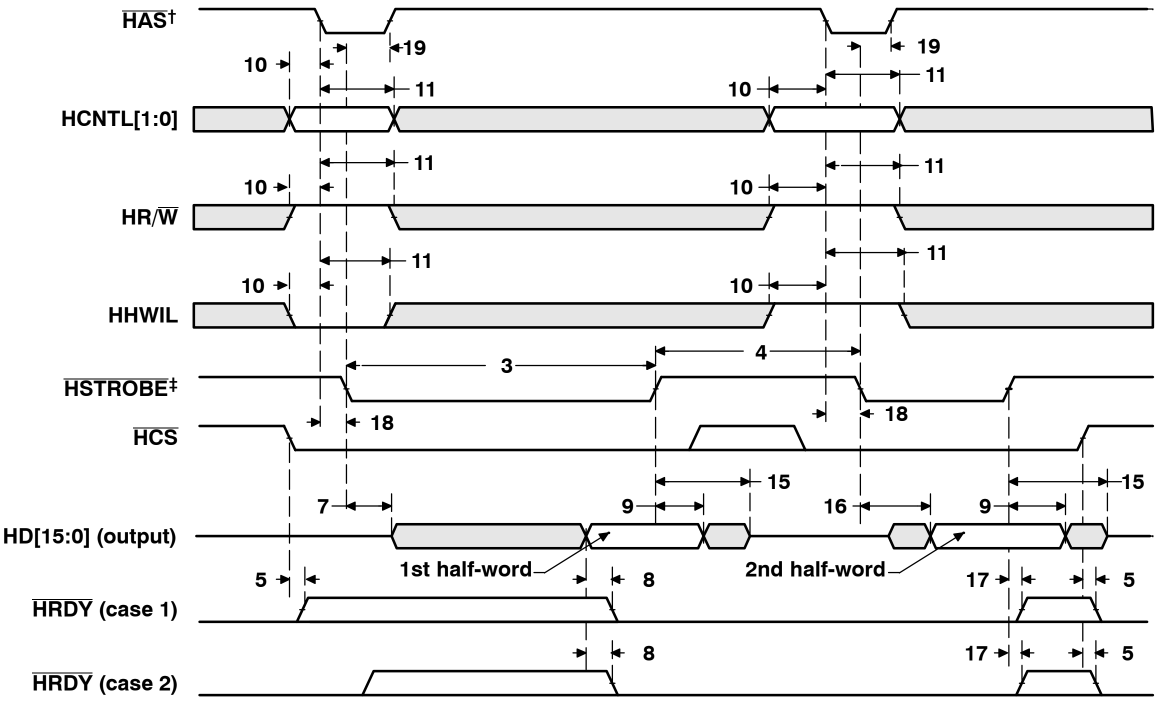
[‖] This parameter is used after the second half-word of an HPID write or autoincrement read. $\overline{\text{HRDY}}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{\text{HRDY}}$ signal.

HOST-PORT INTERFACE TIMING (CONTINUED)



† $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

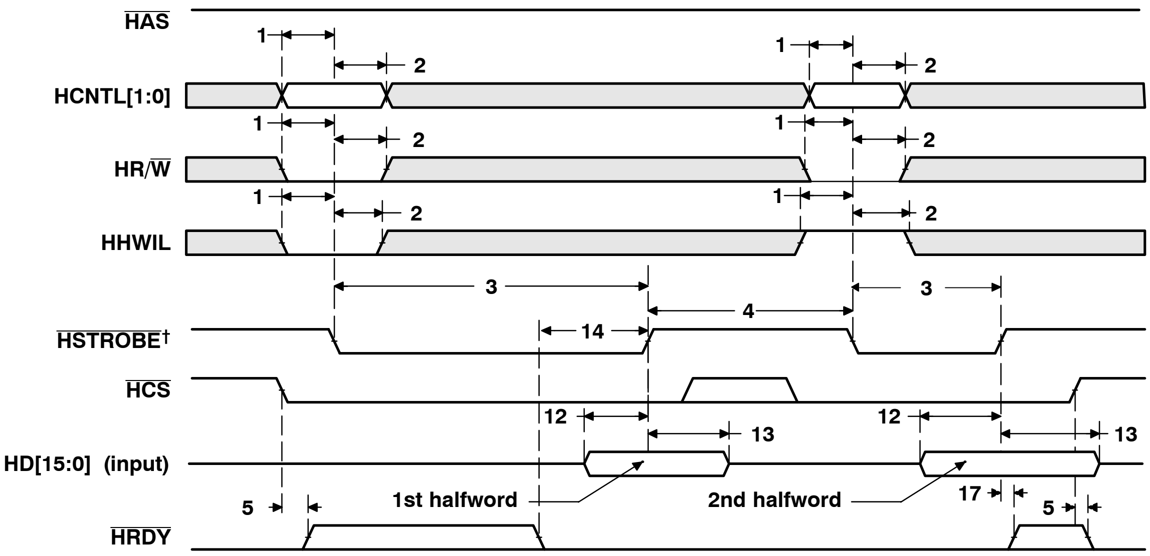
Figure 48. HPI Read Timing ($\overline{\text{HAS}}$ Not Used, Tied High)



† For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
‡ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

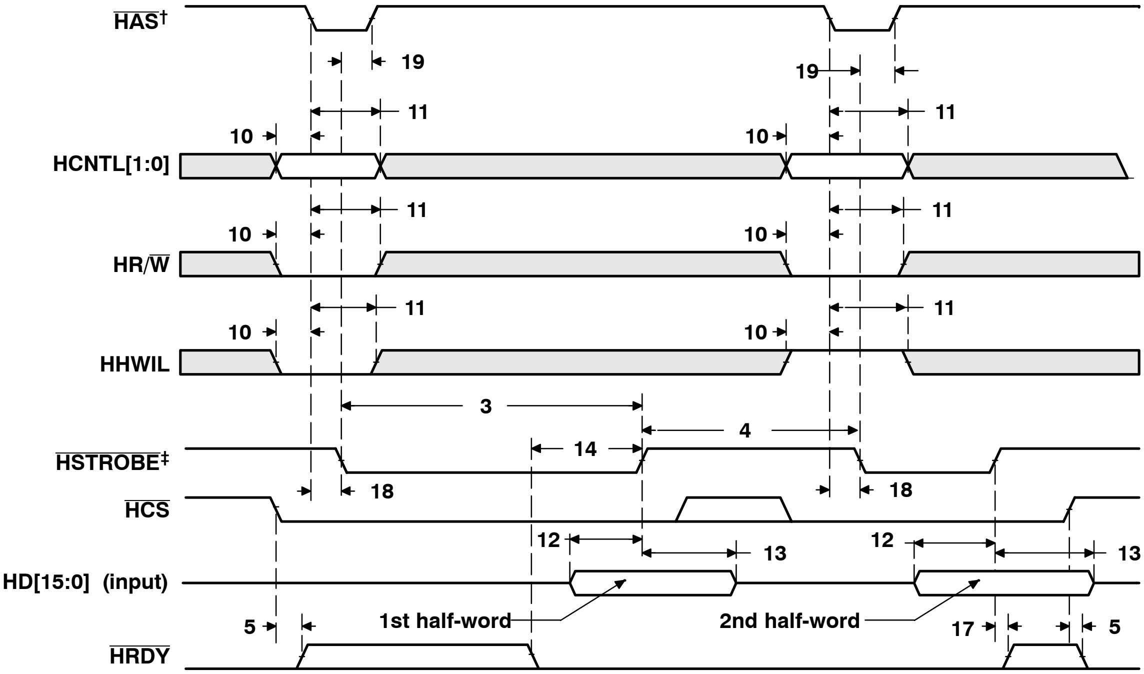
Figure 49. HPI Read Timing ($\overline{\text{HAS}}$ Used)

HOST-PORT INTERFACE TIMING (CONTINUED)



† $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

Figure 50. HPI Write Timing ($\overline{\text{HAS}}$ Not Used, Tied High)



† For correct operation, strobe the $\overline{\text{HAS}}$ signal only once per $\overline{\text{HSTROBE}}$ active cycle.
‡ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

Figure 51. HPI Write Timing ($\overline{\text{HAS}}$ Used)

MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP[†‡] (see Figure 52)

NO.				PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P[§]		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	0.5 * $t_{c(CKRX)}$ −1[¶]		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	9		ns
			CLKR ext	1		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	8		ns
			CLKR ext	0		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	4		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	9		ns
			CLKX ext	1		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

[‡] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

[§] The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 225-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

[¶] This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the resonable range of 40/60 duty cycle.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP[†][‡] (see Figure 52)

NO.	PARAMETER			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
				MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		1.8	10	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P[§][¶]		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C − 1[#]	C + 1[#]	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	−2	3	ns
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	−2	3	ns
			CLKX ext	2	9	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	−1	4	ns
			CLKX ext	1.5	10	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	−3.2 + D1[‖]	4 + D2[‖]	ns
			CLKX ext	0.5 + D1[‖]	10+ D2[‖]	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	−1	4.5	ns
			FSX ext	2	9	

[†] CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

[‡] Minimum delay times also represent minimum output hold times.

[§] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

[¶] The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 225-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

[#] C = H or L
S = sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see ¶ footnote above).

[‖] Extra delay from CLKX high to DX valid applies *only* to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 2P, D2 = 4P

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

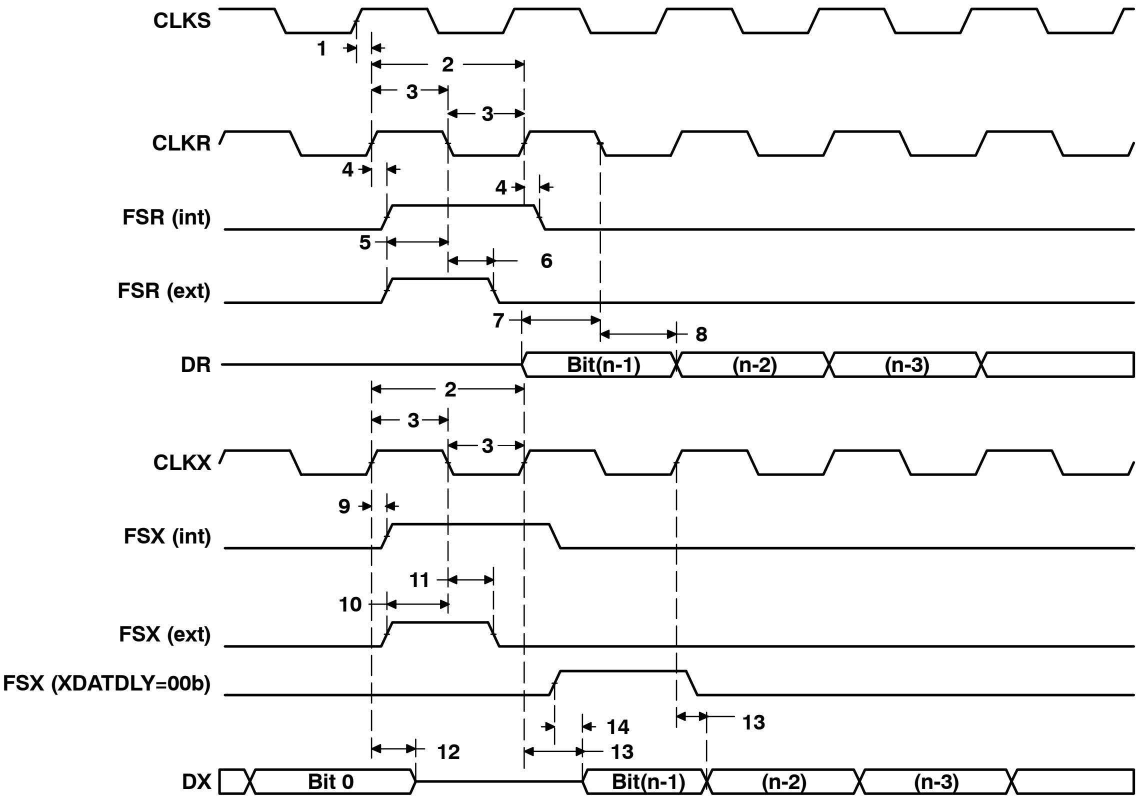


Figure 52. McBSP Timings

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for FSR when GSYNC = 1 (see Figure 53)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	4		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		ns

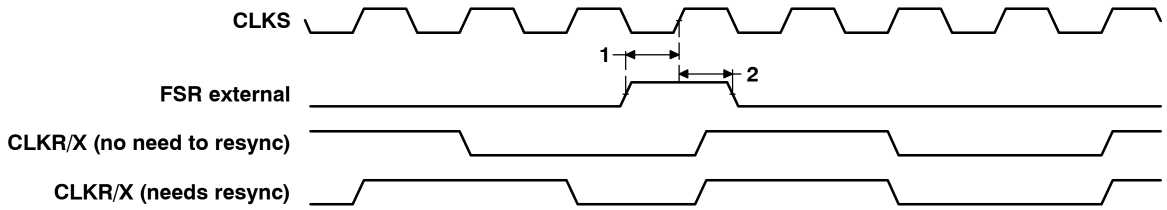


Figure 53. FSR Timing When GSYNC = 1

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0[†‡] (see Figure 54)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	12		2 − 6P		ns
5	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0[†‡] (see Figure 54)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER[§]		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low[¶]	T − 2	T + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high[#]	L − 2	L + 3			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	L − 2	L + 3			ns
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			2P + 3	6P + 17	ns
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

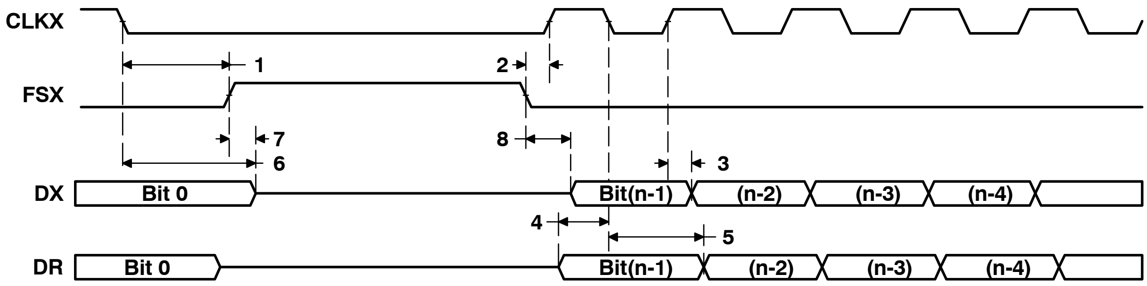


Figure 54. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 55)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 55)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	L − 2	L + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	T − 2	T + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	H − 2	H + 4	4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

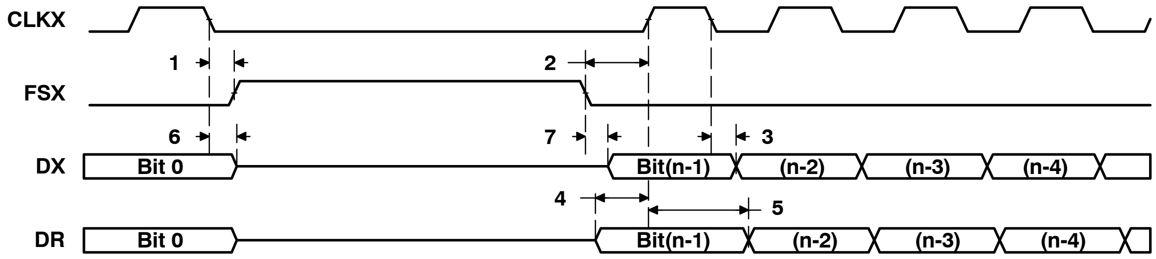


Figure 55. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 56)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV\text{-}CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH\text{-}DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 56)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH\text{-}FXL)}$	Hold time, FSX low after CLKX high¶	T − 2	T + 3			ns
2	$t_{d(FXL\text{-}CKXL)}$	Delay time, FSX low to CLKX low#	H − 2	H + 3			ns
3	$t_{d(CKXL\text{-}DXV)}$	Delay time, CLKX low to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXH\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	H − 2	H + 3			ns
7	$t_{dis(FXH\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			2P + 3	6P + 17	ns
8	$t_{d(FXL\text{-}DXV)}$	Delay time, FSX low to DX valid			4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

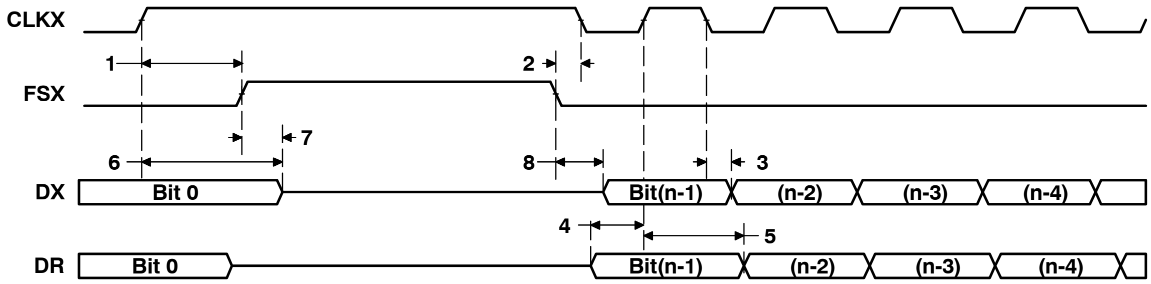


Figure 56. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1[†‡] (see Figure 57)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1[†‡] (see Figure 57)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225				UNIT
			MASTER[§]		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high[¶]	H − 2	H + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low[#]	T − 2	T + 3			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	L − 2	L + 4	4P + 2	8P + 17	ns

[†] P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
[‡] For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
[§] S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero

[¶] FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

[#] FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

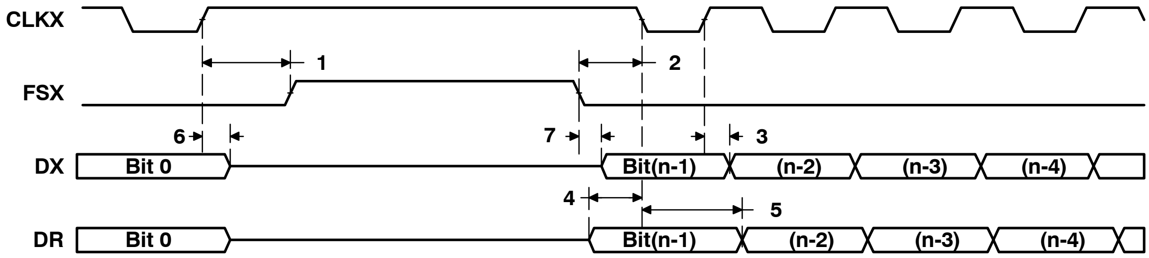


Figure 57. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

TIMER TIMING

timing requirements for timer inputs† (see Figure 58)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{w(TINPH)}$	Pulse duration, TINP high	2P		ns
2	$t_{w(TINPL)}$	Pulse duration, TINP low	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

switching characteristics over recommended operating conditions for timer outputs† (see Figure 58)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
3	$t_{w(TOUTH)}$	Pulse duration, TOUT high	4P − 3		ns
4	$t_{w(TOUTL)}$	Pulse duration, TOUT low	4P − 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

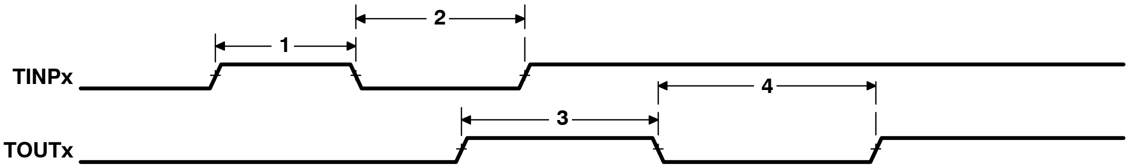


Figure 58. Timer Timing

GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING

timing requirements for GPIO inputs†‡ (see Figure 59)

NO.			PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	4P		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	4P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

‡ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.

switching characteristics over recommended operating conditions for GPIO outputs†§ (see Figure 59)

NO.	PARAMETER		PYPA−167 PYP−200 GDPA−200 GDP−225		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	12P − 3		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	12P − 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

§ The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

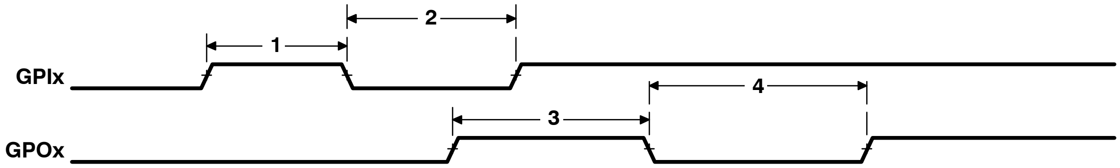


Figure 59. GPIO Port Timing

JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 60)

NO.			PYPA–167 PYP–200 GDPA–200 GDP–225		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	35		ns
3	$t_{su(TDIV-TCKH)}$	Setup time, TDI/TMS/$\overline{\text{TRST}}$ valid before TCK high	10		ns
4	$t_{h(TCKH-TDIV)}$	Hold time, TDI/TMS/$\overline{\text{TRST}}$ valid after TCK high	7		ns

switching characteristics over recommended operating conditions for JTAG test port (see Figure 60)

NO.	PARAMETER		PYPA–167 PYP–200 GDPA–200 GDP–225		UNIT
			MIN	MAX	
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	15	ns

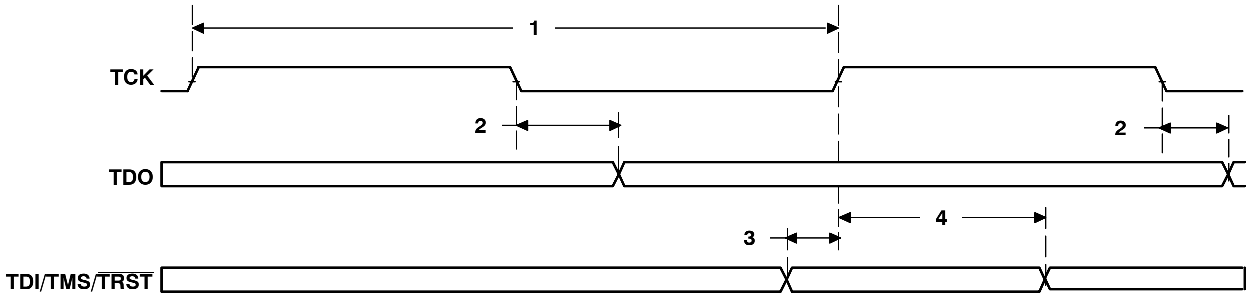
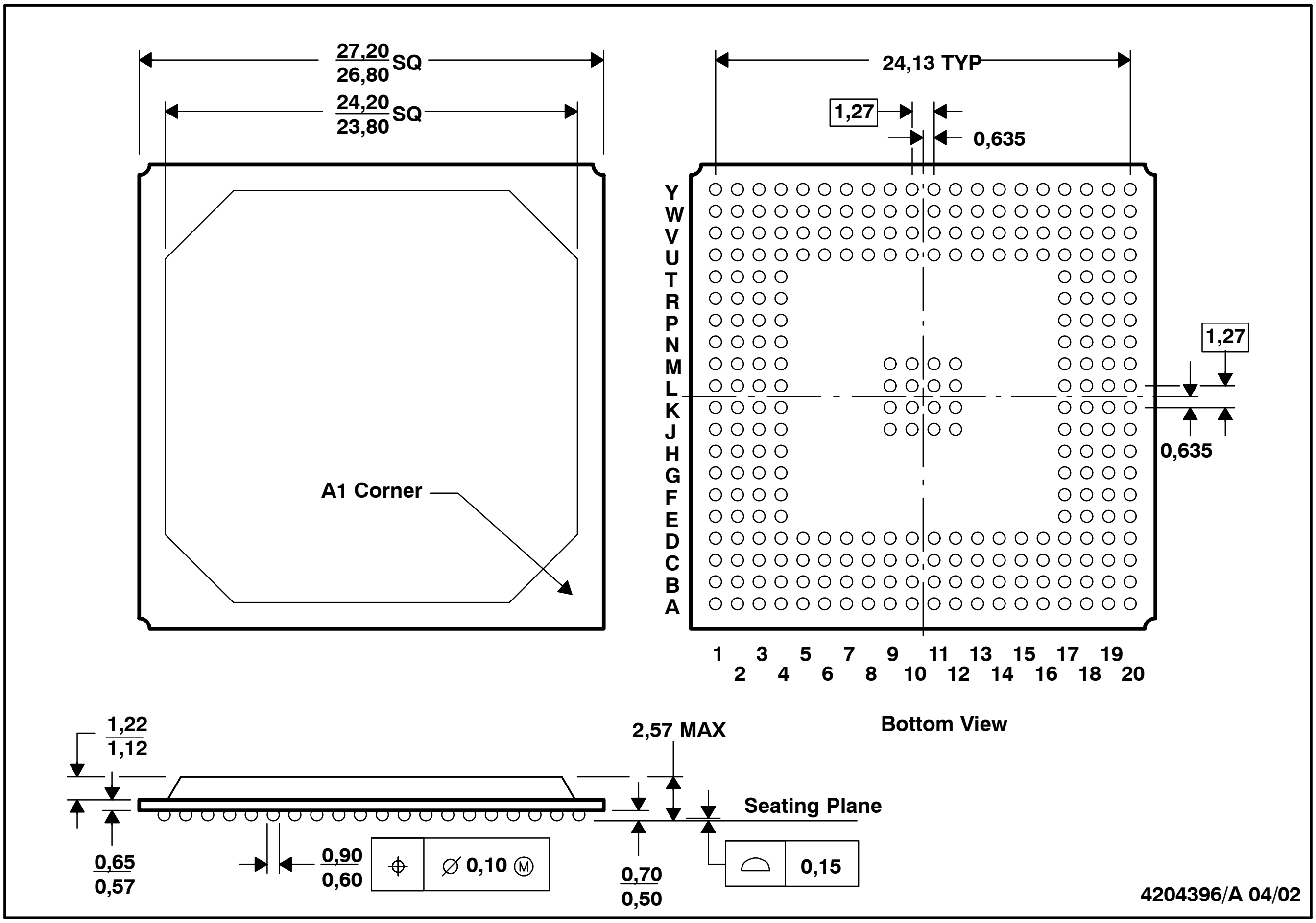


Figure 60. JTAG Test-Port Timing

MECHANICAL DATA

GDP (S−PBGA−N272) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151

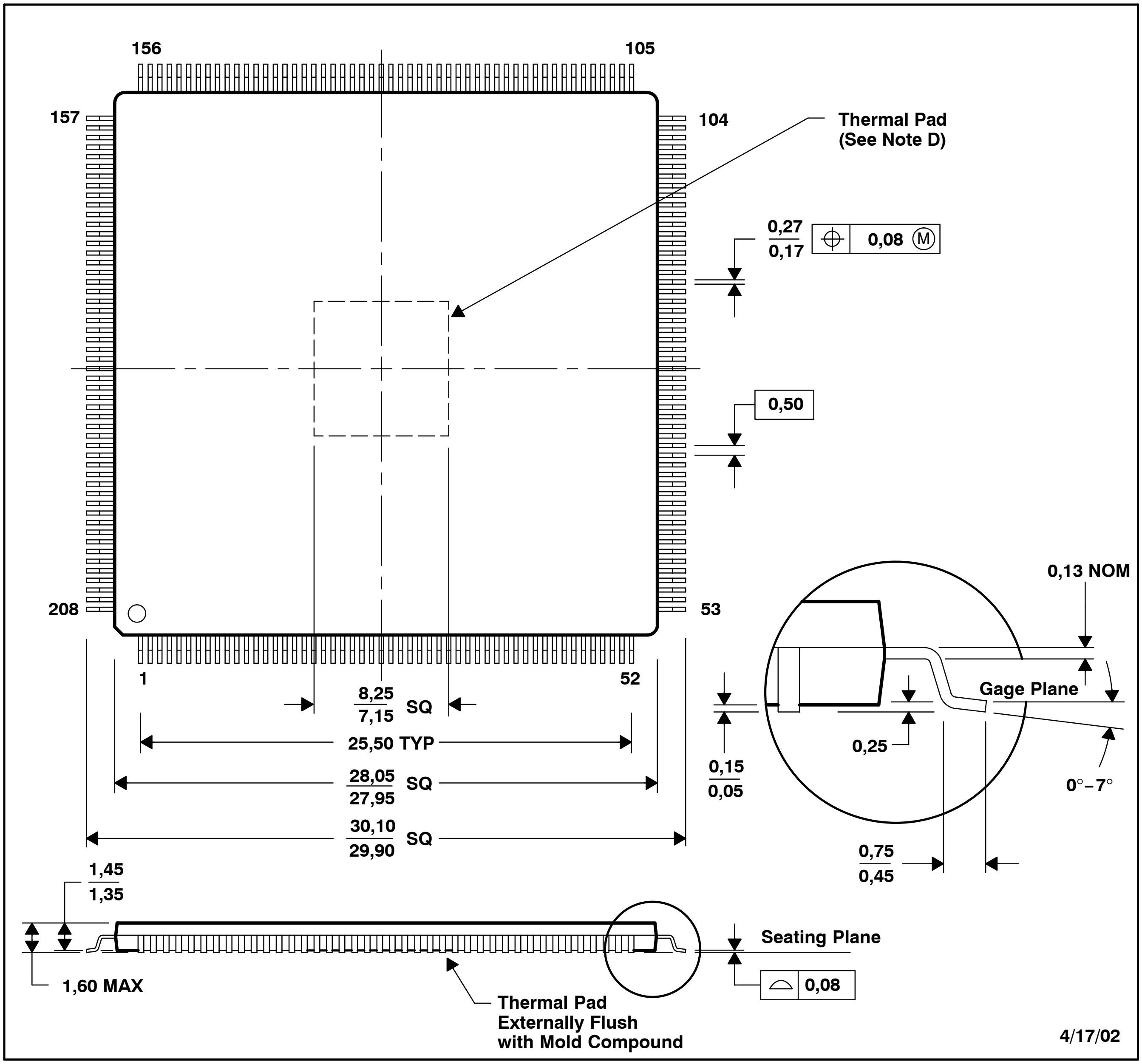
thermal resistance characteristics (S-PBGA package)

NO			°C/W	Air Flow (m/s)†
Two Signals, Two Planes (4-Layer Board)				
1	$R\Theta_{JC}$	Junction-to-case	9.7	N/A
2	Psi_{JT}	Junction-to-package top	1.5	0.0
3	$R\Theta_{JB}$	Junction-to-board	19	N/A
4	$R\Theta_{JA}$	Junction-to-free air	22	0.0
5	$R\Theta_{JA}$	Junction-to-free air	21	0.5
6	$R\Theta_{JA}$	Junction-to-free air	20	1.0
7	$R\Theta_{JA}$	Junction-to-free air	19	2.0
8	$R\Theta_{JA}$	Junction-to-free air	18	4.0
9	Psi_{JB}	Junction-to-board	16	0.0

† m/s = meters per second

MECHANICAL DATA

TMS320C6713 Device-Specific PYP (S-PQFP-G208) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. The generic drawing (ECN# 4146966) is subject to change without notice and will affect this drawing.
C. Body dimensions include mold flash or protrusions.
D. For proper device thermal performance, the thermal pad ***must*** be soldered to an external thermal plane. This pad is electrically and thermally connected to the backside of the die.
For the TMS320C6713 208-Pin PowerPAD plastic quad flatpack, the external thermal pad dimensions are: 7.2 x 7.2 mm and the thermal pad is externally flush with the mold compound.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA (CONTINUED)

thermal resistance characteristics (S-PQFP-G208 package)

NO			°C/W
Junction-to-Pad			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
1	$R\Theta_{JP}$	Junction-to-pad, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.2
Junction-to-Package Top			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
2	Psi_{JT}	Junction-to-package top, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.18
3	Psi_{JT}	Junction-to-package top, 7.5 x 7.5 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.23
Two Signals (2-Layer Board)			
4	Psi_{JT}	Junction-to-package top, 26 x 26 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	0.18
5	Psi_{JT}	Junction-to-package top, 7.5 x 7.5 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	0.23
Junction-to-Still Air			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
6	$R\Theta_{JA}$	Junction-to-still air, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	13
7	$R\Theta_{JA}$	Junction-to-still air, 7.5 x 7.5 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	20
Two Signals (2-Layer Board)			
8	$R\Theta_{JA}$	Junction-to-still air, 26 x 26 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	14
9	$R\Theta_{JA}$	Junction-to-still air, 7.5 x 7.5 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	20

REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS186D device-specific data sheet to make it an SPRS186E revision.

Scope: Applicable updates to the C67x device family, specifically relating to the C6713 devices, have been incorporated. Added and updated device-specific information to support the characterization of the C6713 devices which are at the production data (PD) stage of development.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
9	Description section: Deleted “boot from a serial EEPROM” from the “The two I2C ports on the TMS320C6713 allow the DSP ...” paragraph
10	Device characteristics section; Table 2, Characteristics of the C6713 Processor: Changed the 32-Bit Timers, “Internal Clock Source” from “1/4 of SYSCLK1” to “1/**2** of SYSCLK**2**”
30	Table 18, Device Configurations Pins at Device Reset (HD[4:3], HD8, and CLKMODE0): Added the HD[6, 5, 2] exclusion to the “All other HD pins (HD [15, 13:9, 7:5, 2:0])” footnote
44	Debugging considerations section: Added the HD[6, 5, 2] exclusion to the “Internal pullup/pulldown resistors ...” paragraph
47	Terminal Functions table, HOST-PORT INTERFACE (HPI), Host-port data pins DESCRIPTION: Added the HD[6, 5, 2] exclusion to the “Other HD pins ...” paragraph
64	Documentation support section: Added reference to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889).
71	EDMA module and EDMA selector section, Table 29, EDMA Channels: Changed the **“DEFAULT SELECTOR VALUE (BINARY)”** value for XEVT0 from “001000” to “001**1**00” Changed the **“DEFAULT SELECTOR VALUE (BINARY)”** value for REVT0 from “001001” to “001**1**01” Changed the **“DEFAULT SELECTOR VALUE (BINARY)”** value for XEVT1 from “001010” to “001**1**10” Changed the **“DEFAULT SELECTOR VALUE (BINARY)”** value for REVT1 from “001011” to “001**1**11”
75	PLL and PLL controller section: Deleted SYSCLK2 row along with MAX value from Table 35, PLL Clock Frequency Ranges: Added footnote stating “SYSCLK2 rate ***must*** be exactly half of SYSCLK1” Added footnote stating “When the McASP module is *not* used, the AUXCLK maximum frequency can be any frequency up to the CLKIN maximum frequency.” Added new ending sentence to the “During the programming transition of Divider D1 ...” paragraph
86	General-purpose input/output (GPIO) section: Added *new* GPIO section with device-specific GPEN register
88	IEEE 1149.1 JTAG compatibility statement section: Replaced paragraph “It is recommended that when using this type of JTAG controller, ...” with *new* paragraph “When using this type of JTAG controller, assert ...”
89	EMIF device speed section: Replaced/updated all “EMIF device speed” paragraphs Added new Table 44, “C6713 Example Boards and Maximum EMIF Speed”
90	Bootmode section: Updated/changed the paragraph explanation for all three boot modes: Host boot, Emulation boot, and EMIF boot to reflect the internally “stalled” state of the CPU

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
91	Absolute maximum ratings over operating case temperature range section: Changed the Supply voltage range, CV_{DD} **from** “−0.3 V to 1.35 V“ **to** “−0.3 V to 1.8 V“
92	Electrical characteristics over recommended ranges of supply voltage and operating case temperature table: Added “The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889).” to the end of the “Measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. ...” paragraph
112	Reset Timing, timing requirements for reset table Changed the Boot and device configurations bits footnote to “The Boot and device configurations bits are latched asynchronously when RESET is **transitioning high**. ...”
114	EXTERNAL INTERRUPT TIMING section timing requirements for external interrupts table: Split the descriptions of NMI and EXT_INT interrupts pulse low/high Changed MIN value of “Width of the EXT_INT interrupt pulse low” (parameter #1) from “2P” to “4P” Changed MIN value of “Width of the EXT_INT interrupt pulse high” (parameter #2) from “2P” to “4P”

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