RCV336DPFL/SP V.34 Data, V.17 Fax, AudioSpan, Voice, Speakerphone, Modem Data Pump

Introduction

The Rockwell RCV336DPFL/SP is a V.34 modem data pump family that supports data rates up to 33600 bps, fax operation up to 14400 bps, AudioSpan, voice coding/decoding (optional), and speakerphone (optional). The following models are available:

Model	Voice	Speakerphone
RC336DPFL	No	No
RCV336DPFL	Yes	No
RCV336DPFL/SP	Yes	Yes

As a data modem, the modem can operate in 2-wire, full-duplex, synchronous/asynchronous modes at rates up to 33600 bps. Using V.34 techniques to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps to 2400 bps with automatic fallback to V.32 bis.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

Facsimile models support Group 3 facsimile send and receive speeds up to 14400 bps.

AudioSpan (analog simultaneous audio/voice and data) operation supports data rates with audio of 4.8 kbps in V.61 modulation, 4.8 to 14.4 kbps in ML144 modulation, or 4.8 to 21.6 kbps in ML288 modulation.

The speakerphone model supports position-independent full-duplex speakerphone (FDSP) operation using a dual internal integrated analog circuit to interface with the telephone line and the audio input/out (i.e., a headset, handset, or a microphone with external speaker).

Voice models include an Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec). The codec compresses and decompresses voice signals to allow efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a 7.2 kHz sample rate.

A voice pass-through mode in all models allows the host to transmit and receive uncompressed audio signals

The modem operates over the public switched telephone network (PSTN) through the appropriate line termination.

The RCV336DPFL/SP offers low power consumption in a small footprint, low profile PQFP package, meeting PCMCIA Type II envelope requirements for PC Cards and battery-powered portable applications.

Additional information is provided in the RCV336DPFL/SP Modem Designer's Guide (Order No. 1061).

Features

- 2-wire full-duplex
  - 33.6 kbps, V.34, V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21
  - Bell 212 and 103
- 2-wire half-duplex
  - V.17, V.33, V.29, V.27 ter, and V.21 channel 2
  - Bell 208
  - Short train option in V.17 and V.27 ter
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel (V.34 and V.32 bis)
- Automatic mode selection (AMS)
- Automatic rate adaption (ARA)
- Digital near-end and far-end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer
- AudioSpan (simultaneous audio/voice and data)
  - ITU-T V.61 modulation (4.8 kbps data plus audio)
  - ML144 modulation (4.8 to 14.4 kbps data plus audio)
  - ML288 modulation (4.8 to 21.6 kbps data plus audio)
  - Audio/silence detection (ML144) and handset echo cancellation
  - Handset, headset, or half-duplex speakerphone
- Full-duplex speakerphone (optional)
  - Acoustic and line echo cancellation
  - Programmable microphone AGC
  - Microphone volume selection and muting
  - Speaker volume control and muting; room monitor
- ADPCM voice mode (optional)
- Voice pass-through mode
- TTL and CMOS compatible DTE interface
  - ITU-T V.24 (EIA/TIA-232-E) (data/control)
  - Microprocessor bus (data/configuration/control)
- Dynamic range: -9 dBm to -43 dBm
- Adjustable speaker output to monitor received signal
- DMA support interrupt lines
- Two 16-byte FIFO data buffers for burst data transfer
- NRZI encoding/decoding
- 511 pattern generation/detection
- Diagnostic capability
- V.8, V.8 bis signaling
- V.13 signaling
- V.54 inter-DCE signaling
- V.54 local analog and remote digital loopback
- +5V operation
- Typical power consumption:
  - Normal Mode: 620 mW; Sleep Mode: 9 mW
- Low profile, small footprint package
  - One 100-pin PQFP

Technical Description

The modem functional interface is illustrated in Figure 1

Configurations and Rates

The selectable modem configurations, signaling rates, and data rates are listed in Table 1.

Automatic Mode Selection

When automatic mode selection (AMS) is enabled, the modem configures itself to the highest compatible data rate supported by the remote modem (AUTO bit). Automode operation in V.32 bis, V.32 V.22 bis, V.22, V.21, V.23, Bell 212A, and Bell 103 modes is in accordance with EIA/TIA-PN2330.

Automatic Rate Adaption (ARA)

In V.34 and V.32 bis modes, automatic rate adaption (ARA) can be enabled to select the highest data rate possible based on the measured eye quality monitor (EQM) (EARC bit). This selection occurs during handshake/retrain and rate renegotiation.

Tone Generation

The modem can generate single or dual voice-band tones from 0 Hz to 3600 Hz with a resolution of 0.15 Hz and an accuracy of ± 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.34, V.32 bis, V.32, V.17, V.33, V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, and is compatible with Bell 208, 212A, or 103, depending on the configuration.

Transmitted Data Spectrum

The transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.34, V.32 bis, V.32, V.17, V.33, V.29	Square root of 12.5%
V.27 ter, Bell 208	Square root of 50%
V.22 bis/V.22, Bell 212A	Square root of 75%

RTS - CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 2.

Transmit Level

The transmitter output level is selectable from 0 dBm to -15 dBm in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned by changing a gain constant in modem DSP RAM. The maximum V.34/V.32 bis/V.32 transmit level for acceptable receive performance should not exceed –9 dBm.

Note: In V.34 mode, the transmit level may be automatically changed during the handshake. This automatic adjustment of the transmit level may be disabled via a parameter in DSP RAM.

Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

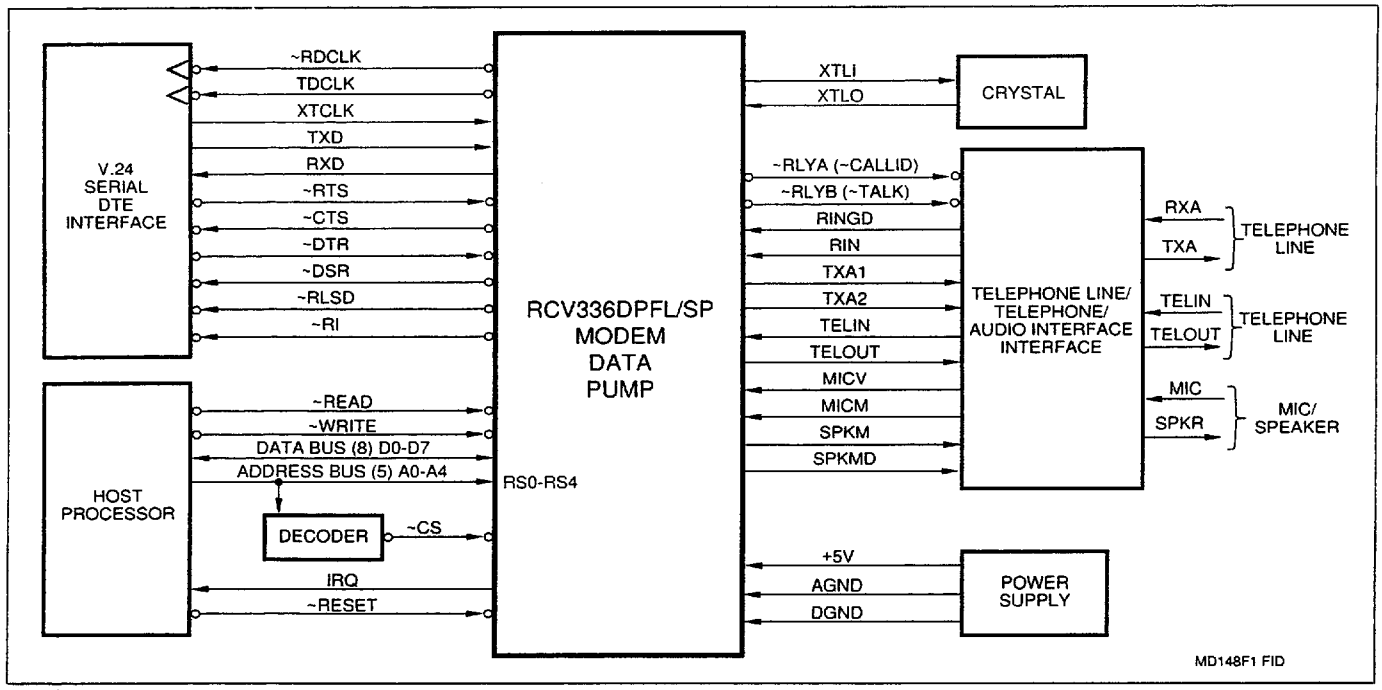

Figure 1. RCV336DPFL/SP MDP Functional Interface

Table 1. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Symbol Rate (Symbols/Sec.)	Bits/Symbol - Data	Bits/Symbol - TCM	Constellation Points
V.34 33600 TCM	TCM	Note 2	33600	Note 2	Note 2	Note 2	Note 2
V.34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V.34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V.34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V.34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V.34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V.34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V.34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V.34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V.34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V.34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V.34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V.34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V.34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V.32 bis 14400 TCM	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM	TCM	1800	12000	2400	5	1	64
V.32 bis 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 bis 7200 TCM	TCM	1800	7200	2400	3	1	16
V.32 bis 4800	QAM	1800	4800	2400	2	0	4
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 600	DPSK	1200/2400	600	600	1	0	4
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
Bell 208 4800	DPSK	1800	4800	1600	3	0	8
Bell 212A	DPSK	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.17 14400 TCM/V.33[3]	TCM	1800	14400	2400	6	1	128
V.17 12000 TCM/V.33[3]	TCM	1800	12000	2400	5	1	64
V.17 9600 TCM[3]	TCM	1800	9600	2400	4	1	32
V.17 7200 TCM[3]	TCM	1800	7200	2400	3	1	16
V.29 9600[3]	QAM	1700	9600	2400	4	0	16
V.29 7200[3]	QAM	1700	7200	2400	3	0	8
V.29 4800[3]	QAM	1700	4800	2400	2	0	4
V.27 4800[3]	DPSK	1800	4800	1600	3	0	8
V.27 2400[3]	DPSK	1800	2400	1200	2	0	4
V.21 Channel 2[3]	FSK	1750	300	300	1	0	–
Tone Transmit	–	–	–	–	–	–	–

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation QAM: Quadrature Amplitude Modulation
   FSK: Frequency Shift Keying DPSK: Differential Phase Shift Keying
2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V.34 Low Carrier	V.34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

3. Models with fax support only.

Table 2. RTS-CTS Response Times

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
V.34, V.32 bis, V.32	± 2 ms	N/A	N/A
V.33/V.17 Long	N/A	1393 ms[2]	15 ms[4]
V.33/V.17 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.26	N/A	60 ms	10 ms
V.22 bis, V.22, Bell 212A	± 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM. (Full-duplex modes only.)
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

Answer Tone

The modem generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero (V.8, V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21). The answer tone has 180° phase reversals every 0.45 second to disable network echo cancellers (V.8, V.32 bis, V.32).

Receive Level

The modem satisfies performance requirements for received line signal levels from –9 dBm to –43 dBm measured at the Receiver Analog (RXA) (TIP and RING) input (-15 dBm at RIN).

Note: A 6 dB pad is required between TIP and RING and the RIN input.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (~RLSD) is off. ~RLSD can be clamped off (RLSDE bit).

Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.34/V.32 bis/V.32 operation. The combined echo span of near and far cancellers can be up to 40 ms. The proportion allotted to each end is automatically determined by the modem. The delay between near-end and far-end echoes can be up to 1.2 seconds.

AudioSpan Modes

AudioSpan provides full-duplex analog simultaneous audio/voice and data over a single telephone line. AudioSpan can send any type of audio waveform, including music. Data can be sent with or without error correction. The audio/voice interface can be in the form of a headset, handset, or a microphone and speaker (half-duplex speakerphone).

V.61 Modulation. AudioSpan can operate in V.61 modulation at a data rate with audio of 4800 bps.

ML144 Modulation. AudioSpan can operate in ML144 (V.32) modulation at a 4.8 to 14.4 kbps data rate with audio where lower data rates provide higher audio quality.

ML288 Modulation. AudioSpan can operate in ML288 (V.34 type) modulation at a 4.8 to 21.64 kbps data rate with audio where lower data rates provide higher audio quality.

Speakerphone Voice/Audio Paths (Optional)

The modem incorporates a dual integrated analog interface. The voice/audio transmit and receive signals can be routed through several paths. The voice/audio paths are available in the speakerphone mode configuration and are selected through DSP RAM.

The voice/audio input can be taken from one of four different sources: telephone line input (RIN), handset (TELIN), microphone (MICM or MICV).

The speaker output (SPKM) can originate from one of five different sources: RIN, TELIN, MICM or MICV or from the modem's internal voice playback mode.

The voice/audio output may be routed to the telephone line output (TXA1 and TXA2) or handset (TELOUT).

The voice paths can be switched to allow an audio input to be routed to the telephone line output through a variable gain for applications such as music-on-hold.

The "room monitor" mode allows the modem to receive audio from its surroundings and concurrently transmit the audio to a remote site.

ADPCM Voice Mode (Optional)

Transmit Voice. 16-bit compressed transmit voice can be sent to the modem ADPCM codec for decompression then to the digital-to-analog converter (DAC) by the host.

Receive Voice. 16-bit received voice samples from the modem analog-to-digital converter (ADC) can be sent to

the ADPCM codec for compression, and then be read by the host.

Voice Pass-Through Mode

Transmit Voice. 16-bit transmit voice samples can be sent to the modem DAC from the host.

Receive Voice. 16-bit received voice samples from the modem ADC can be read by the host.

Data Formats

Serial Synchronous Data

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

Selectable clock: Internal, external, or slave.

Serial Asynchronous Data

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200 or 600 bps +1% (or +2.3%), –2.5%;

0-300 bps (V.21 and Bell 103);

1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CCITT CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit deletion, CCITT CRC-16 or CRC-32 checking.

Parallel Asynchronous Data

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200 or 600 bps +1% (or 2.3%), –2.5%;

1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

Async/Sync and Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converters operate in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to –2.5%
- Extended overspeed range: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break handling is performed as described in V.14.

Asynchronous characters are accepted on the TXD serial input and are issued on the RXD serial output.

V.54 Inter-DCE Signaling

The modem supports V.54 inter-DCE signaling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgment, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

V.13 Remote RTS Signaling

The modem supports V.13 remote RTS signaling. Transmission and detection of signaling bit patterns in response to a change of state in the RTS bit or the ~RTS input signal are provided. The RRTSE bit enables V.13 signaling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local ~RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The modem automatically clamps and unclamps ~RLSD.

Auto-Dialing and Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection, and a comprehensive supervisory tone detection scheme. The major parameters are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The tone detection sample rate is 9600 Hz in V.8 and V.34 modes and is 7200 Hz in non-V.34 modes. The default call progress filter coefficients are based on a 7200 Hz sampling rate and apply to non-V.34 modes only. The maximum detection bandwidth is equal to one-half the sample rate.

The tone detectors default bandwidths and thresholds are:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*

* Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.

511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (control bit S511). Use of this bit pattern during self-test eliminates the need for external test equipment.

In-Band Secondary Channel

A full-duplex in-band secondary channel is provided in V.34 (all speeds) and V.32 bis/V.32 (7200 bps and above) modes. Control bit SECEN enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode.

In V.34 modes, the secondary channel rate is 200 bps.

In V.32 bis/V.32 modes, the secondary channel rate is 150 bps. This rate is also host programmable in V.32 bis/V.32 modes.

Transmit and Receive FIFO Data Buffers

Two 16-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 16 bytes of transmit data and input up to 16 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits indicate the corresponding FIFO buffer half full (8 or more bytes loaded) status. TXFNF and RXFNE bits indicate the TX FIFO buffer not full and RX FIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state.

DMA Support Interrupt Request Lines

DMA support is available in synchronous, asynchronous, and HDLC parallel data modes. Control bit DMAE enables and disables DMA support. When DMA support is enabled, the modem ~RI and ~DSR lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

CCITT CRC-32 Support

CCITT CRC-32 generation/checking may be selected instead of the default CCITT CRC-16 in HDLC mode using DSP RAM access.

Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (TXD) and parallel (RBUFFER) form.

Telephone Line Interface

Line Transformer Interface. V.34/V.32 bis/V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. These modes use the same bandwidth for transmission of data in both directions. Any non-linear distortion generated by the DAA in the transmit direction cannot be canceled by the modem's echo canceller and interferes with data reception. The designer must, therefore, ensure that the total harmonic distortion seen at the RXA input to the modem be at least 45 dB below the minimum level of received signal. Due to the wider bandwidth requirement at a symbol rate of 3429 baud, the DAA must maintain linearity from 150 Hz to 3950 Hz.

Relay Control. Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook and talk/data relays. The talk/data relay output can optionally be used for pulse dial.

Speaker Interface

A SPKM output is provided with on/off and volume control logic incorporated in the modem, requiring only an external amplifier to drive a loudspeaker.

Hardware Interface Signals

A functional interconnect diagram showing the typical modem connection in a system is illustrated in Figure 2. Any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). An active low signal is indicated by a tilde preceding the signal name (e.g., ~RESET).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., ~RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The pin assignments for the modem packaged in a 100-pin PQFP are shown Figure 3 and are listed in Table 3.

The modem hardware interface signals are described in Table 4.

The digital interface characteristics are defined in Table 5.

The analog interface characteristics are defined Table 6.

The power requirements are defined in Table 7.

The absolute maximum ratings are defined in Table 8.

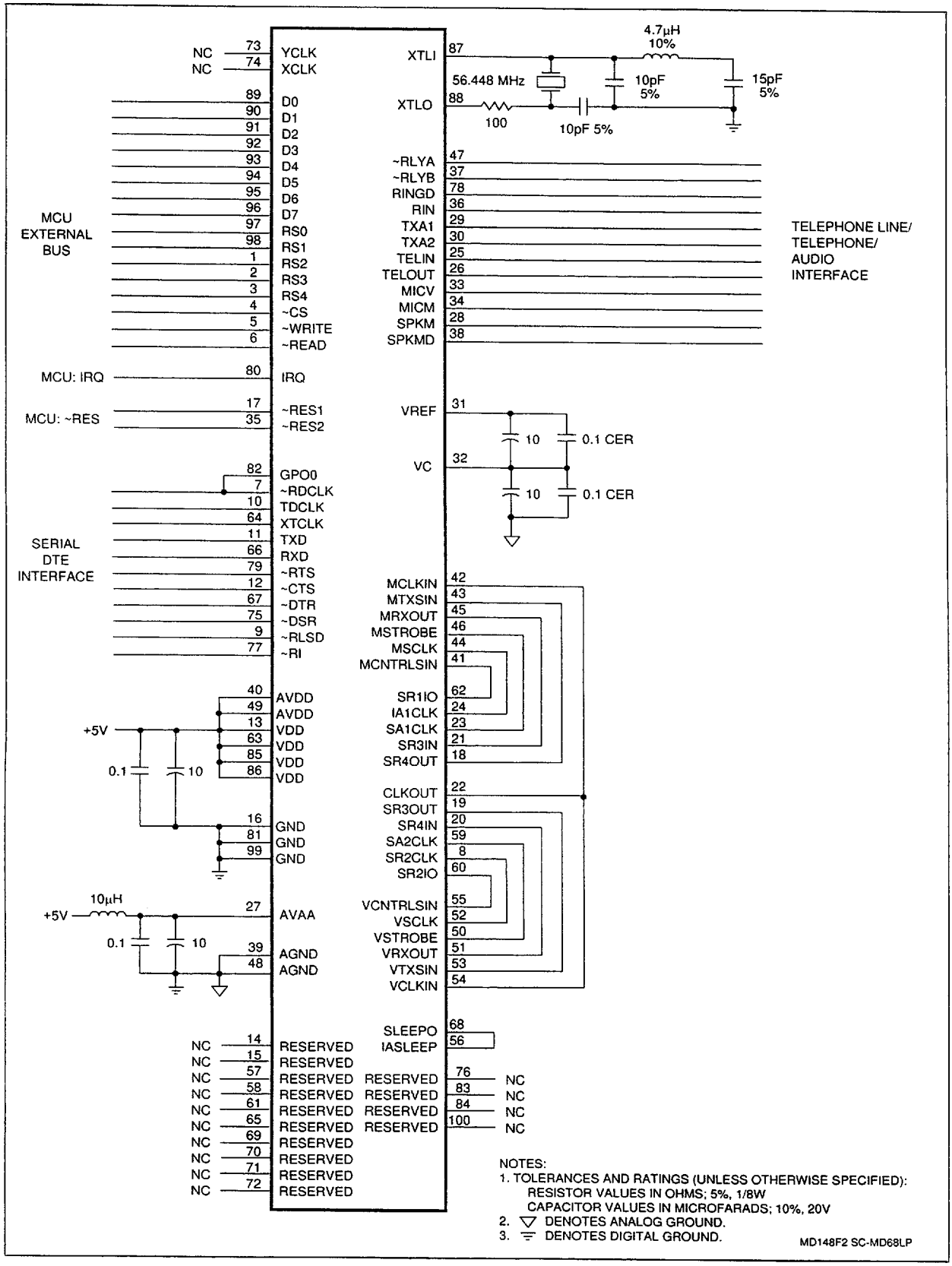

Figure 2. MDP Hardware Interface Signals

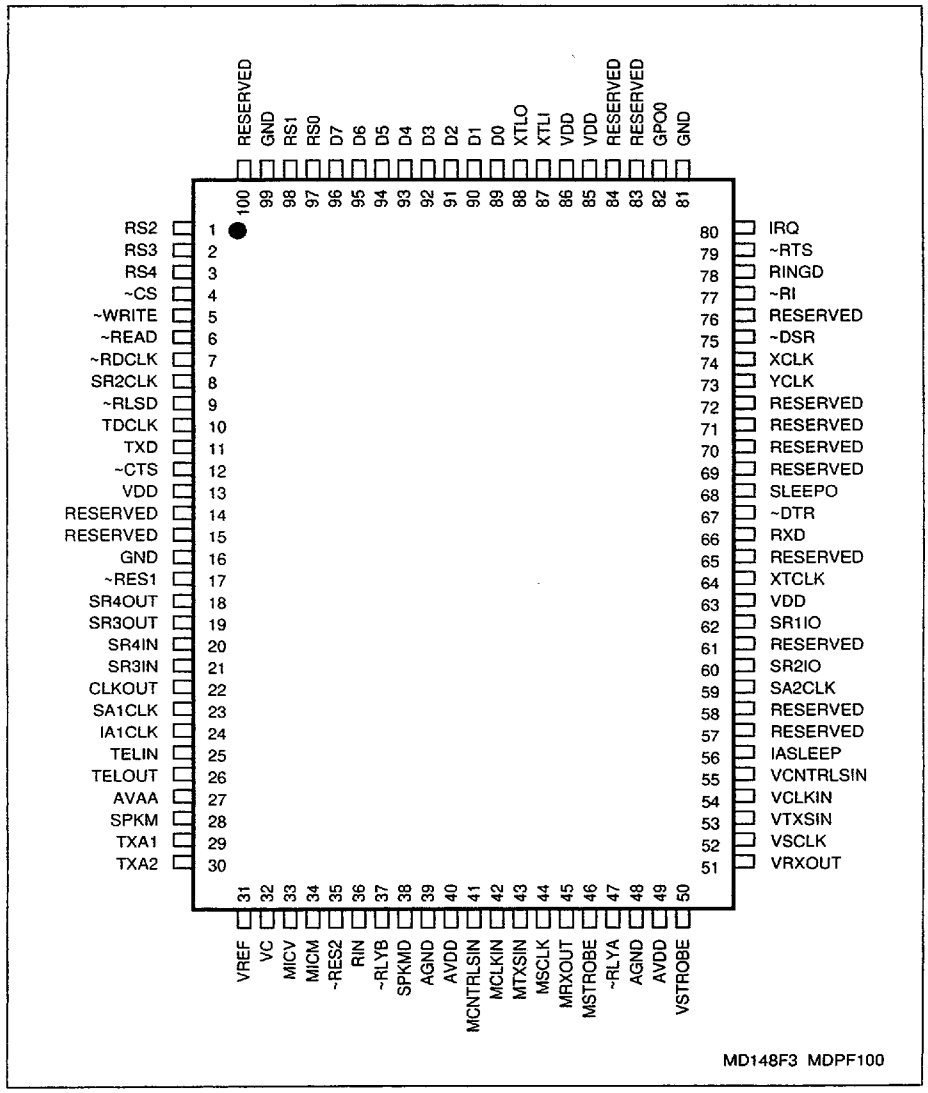

Figure 3. MDP Pin Signals - 100-Pin PQFP

Table 3. MDP Pin Signals - 100-Pin PQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	RS2	IA	Host Parallel Interface	51	VRXOUT	DI	To SR4IN (20)
2	RS3	IA	Host Parallel Interface	52	VSCLK	DI	To SR2CLK (8)
3	RS4	IA	Host Parallel Interface	53	VTXSIN	DI	To SR3OUT (19)
4	~CS	IA	Host Parallel Interface	54	VCLKIN	DI	To CLKOUT (22)
5	~WRITE	IA	Host Parallel Interface	55	VCNTRLSIN	DI	To SR2IO (60)
6	~READ	IA	Host Parallel Interface	56	IASLEEP	DI	To SLEEPO (68)
7	~RDCLK	OA	DTE Serial Interface	57	RESERVED		NC
8	SR2CLK	DI	To VSCLK (52)	58	RESERVED		NC
9	~RLSD	OA	DTE Serial Interface	59	SA2CLK	DI	To VSTROBE (50)
10	TDCLK	OA	DTE Serial Interface	60	SR2IO	DI	To VCNTRLSIN (55)
11	TXD	IA	DTE Serial Interface	61	RESERVED		NC
12	~CTS	OA	DTE Serial Interface	62	SR1IO	DI	To MCNTRLSIN (41)
13	VDD	PWR	+5VD	63	VDD	PWR	+5VD
14	RESERVED		NC	64	XTCLK	IA	DTE Serial Interface
15	RESERVED		NC	65	RESERVED		NC
16	GND	GND	DGND	66	RXD	OA	DTE Serial Interface
17	~RES1		PIF: ~RESET SIF: Reset circuit	67	~DTR	IA	DTE Serial Interface
18	SR4OUT	DI	To MTXSIN (43)	68	SLEEPO	DI	To IASLEEP (56)
19	SR3OUT	DI	To VTXSIN (53)	69	RESERVED		NC
20	SR4IN	DI	To VRXOUT (51)	70	RESERVED		NC
21	SR3IN	DI	To MRXOUT (45)	71	RESERVED		NC
22	CLKOUT	DI	To MCLKIN (42) & VCLKIN (54)	72	RESERVED		NC
23	SA1CLK	DI	To MSTROBE (46)	73	YCLK		NC
24	IA1CLK	DI	To MSCLK (44)	74	XCLK		NC
25	TELIN	I(DA)	Line/Audio Interface	75	~DSR	OA	DTE Serial Interface
26	TELOUT	O(DD)	Line/Audio Interface	76	RESERVED		NC
27	AVAA	PWR	+5VA	77	~RI	OA	DTE Serial Interface
28	SPKM	O(DF)	Line/Audio Interface	78	RINGD	IA	Line/Audio Interface
29	TXA1	O(DD)	Line/Audio Interface	79	~RTS	IA	DTE Serial Interface
30	TXA2	O(DD)	Line/Audio Interface	80	IRQ	OA	Host Parallel Interface
31	VREF	MI	To VC through capacitors	81	GND	GND	DGND
32	VC	MI	To AGND through capacitors	82	GPO0	DI	To ~RDCLK (7)
33	MICV	I(DA)	Line/Audio Interface	83	RESERVED		NC
34	MICM	I(DA)	Line/Audio Interface	84	RESERVED		NC
35	~RES2		PIF: ~RESET SIF: Reset circuit	85	VDD	PWR	+5VD
36	RIN	I(DA)	Line/Audio Interface	86	VDD	PWR	+5VD
37	~RLYB (~TALK)	OD	Line/Audio Interface	87	XTLI	I	Crystal/Clock Circuit
38	SPKMD	O(DF)	Line/Audio Interface	88	XTLO	O	Crystal/Clock Circuit
39	AGND	GND	AGND	89	D0	IA/OB	Host Parallel Interface
40	AVDD	PWR	+5VD	90	D1	IA/OB	Host Parallel Interface
41	MCNTRLSIN	DI	To SR1IO (62)	91	D2	IA/OB	Host Parallel Interface
42	MCLKIN	DI	To CLKOUT (22)	92	D3	IA/OB	Host Parallel Interface
43	MTXSIN	DI	To SR4OUT (18)	94	D4	IA/OB	Host Parallel Interface
44	MSCLK	DI	To IA1CLK (24)	94	D5	IA/OB	Host Parallel Interface
45	MRXOUT	DI	To SR3IN (21)	95	D6	IA/OB	Host Parallel Interface
46	MSTROBE	DI	To SA1CLK (23)	96	D7	IA/OB	Host Parallel Interface
47	~RLYA (~CALLID)	OD	Line/Audio Interface	97	RS0	IA	Host Parallel Interface
48	AGND	GND	AGND	98	RS1	IA	Host Parallel Interface
49	AVDD	PWR	+5VD	99	GND	GND	DGND
50	VSTROBE	DI	To SA2CLK (59)	100	RESERVED		NC

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB = Digital input; OA, OB = Digital output.
   - I(DA) = Analog input; O(DD), O(DF) = Analog output.
   - DI = Device interconnect.
2. NC = No external connection allowed (may have internal connection).
3. Interface Legend:
   - MDP = Modem Data Pump
   - DTE = Data Terminal Equipment
   - PIF = Parallel host interface
   - SIF = Serial DTE interface

Table 4. MDP Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	I, O	**Crystal In and Crystal Out.** Connect the MDP to an external crystal circuit consisting of a 56.448 MHz crystal, three capacitors, and an inductor.
~RES1, ~RES2	IA	**Reset.** ~RESET low holds the modem in the reset state. ~RESET going high releases the modem from the reset state and initiates normal operation using power turn-on (default) values. ~RESET must be held low for at least 3 µs. The modem is ready to use 400 ms after the low-to-high transition of ~RESET.
VDD, AVDD	PWR	**+ 5V Digital Power Supply.** To +5V± 5% and digital circuits power supply filter.
AVAA	PWR	**+ 5V Analog Power Supply.** To +5V± 5% and analog circuits power supply filter.
GND	GND	**Digital Ground.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
		MCU INTERFACE
		Address, data, control, and interrupt hardware interface signals allow modem connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the modem interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus. The modem decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4, while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7, while the least significant data bit is D0.
~CS	IA	**Chip Select.** ~CS selects the modem for microprocessor bus operation. ~CS is typically generated by decoding host address bus lines.
~READ	IA	**Read Enable.** During a read cycle (~READ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the modem. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.
~WRITE	IA	**Write Enable.** During a write cycle (~WRITE asserted), data from the data bus is copied into the selected modem interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	**Interrupt Request.** The modem IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in the modem interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon modem application. The IRQ output is driven by a TTL-compatible CMOS driver.

Table 8. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		DTE SERIAL INTERFACE
		Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/RS-232-D voltage levels.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output.
~RTS	IA	**Request to Send.** Activating ~RTS causes the modem to transmit data on TXD when ~CTS becomes active. The ~RTS pin is logically ORed with the RTS bit.
~CTS	OA	**Clear To Send.** ~CTS active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 2 .
~RLSD	OA	**Received Line Signal Detector.** ~RLSD active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. One of four ~RLSD receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than -43 dBm. The ~RLSD on and off thresholds are host programmable in DSP RAM.
~DTR	IA	**Data Terminal Ready.** In V.34, V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating ~DTR initiates the handshake sequence, provided that the DATA bit is a 1. If in answer mode, the modem immediately sends answer tone. In V.21, V.23, or Bell 103 configuration, activating ~DTR causes the modem to enter the data state provided that the DATA bit is a 1. If in answer mode, the modem immediately sends answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS. During the data mode, deactivating ~DTR causes the transmitter and receiver to turn off and return to the idle state. The ~DTR input and the DTR control bit are logically ORed.
~DSR	OA	**Data Set Ready.** ~DSR ON indicates that the modem is in the data transfer state. ~DSR OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the ~DSR output.
~RI	OA	**Ring Indicator.** ~RI output follows the ringing signal present on the line with a low level (0 V) during the ON time. and a high level (+5 V) during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the ~RI output.
TDCLK	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The TDCLK source can be internal, external (input on XTCLK), or slave (to ~RDCLK) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
~RDCLK	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock (~RDCLK) for USRT timing. The ~RDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The ~RDCLK low-to-high transitions coincide with the center of the received data bits.

Table 8. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TELEPHONE LINE/TELEPHONE/AUDIO INTERFACE SIGNALS AND REFERENCE VOLTAGE		
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
RINGD	IA	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the ~RI output signal as well as the RI bit.
~RLYA (~OHRC, ~CALLID)	OD	**Relay A Control.** The ~RLYA open collector output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and a must-operate voltage no greater than 4.0 VDC. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYA is controlled by host setting/resetting of the RA bit. In a typical application, ~RLYA is connected to the normally open Off-Hook relay (~OHRC). In this case, ~RLYA active closes the relay to connect the modem to the telephone line. Alternatively, in a typical application, ~RLYA is connected to the normally open Caller ID relay (~CALLID). When the modem detects a Calling Number Delivery (CND) message, the ~RLYA output is asserted to close the Caller ID relay in order to AC couple the CND information to the modem RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition).
~RLYB (~TALK)	OD	**Relay A Control.** The ~RLYB open collector output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and a must-operate voltage no greater than 4.0 VDC. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYB is controlled by host setting/resetting of the RB bit. In a typical application, ~RLYB is connected to the normally closed Talk/Data relay (~TALK). In this case, ~RLYB active opens the relay to disconnect the handset from the telephone line.
MICM	I(DA)	**Modem Microphone Input.** MICM is a single-ended microphone input. The input impedance is > 70k Ω.
MICV	I(DA)	**Voice Microphone Input.** MICV is a single-ended microphone input. The input impedance is > 70k Ω.
SPKM	O(DF)	**Modem Speaker Analog Output.** The SPKM analog output reflects the received analog input signal. The SPKM on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKM output is clamped to the voltage at the VC pin. The SPKM output can drive an impedance as low as 300 ohms. In a typical application, the SPKM output is an input to an external LM386 audio power amplifier.
SPKMD	OA	**Modem Speaker Digital Output.** The SPKMD digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.
VREF	REF	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC	REF	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.

Table 8. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		MODEM INTERCONNECT/NO CONNECT
GPO0	DI	To ~RDCLK (7)
SLEEPO	DI	To IASLEEP (56)
IASLEEP	DI	To SLEEPO (68)
MSCLK	DI	To IA1CLK (24)
CLKOUT	DI	To MCLKIN (42) & VCLKIN (54)
SR1IO	DI	To MCNTRLSIN (41)
SR3IN	DI	To MRXOUT (45)
IA1CLK	DI	To MSCLK (44)
SA1CLK	DI	To MSTROBE (46)
SR4OUT	DI	To MTXSIN (43)
MCLKIN	DI	To CLKOUT (22)
VCLKIN	DI	To CLKOUT (22)
MSTROBE	DI	To SA1CLK (23)
VSTROBE	DI	To SA2CLK (59)
MCNTRLSIN	DI	To SR1IO (62)
VSCLK	DI	To SR2CLK (8)
VCNTRLSIN	DI	To SR2IO (60)
MRXOUT	DI	To SR3IN (21)
VTXSIN	DI	To SR3OUT (19)
VRXOUT	DI	To SR4IN (20)
MTXSIN	DI	To SR4OUT (18)
SR2IO	DI	To VCNTRLSIN (55)
SR4IN	DI	To VRXOUT (51)
SR2CLK	DI	To VSCLK (52)
SA2CLK	DI	To VSTROBE (50)
SR3OUT	DI	To VTXSIN (53)
XCLK	O	Clock Frequency Divided by 1. Reserved. Leave open.
YCLK	O	Clock Frequency Divided by 2. Reserved. Leave open.
RESERVED		Reserved Function. May be connected to internal circuit. Leave open.

Table 5. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA and IB		2.0	–	V_{CC}		
Type ID		0.8 V_{CC}	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	
Input Low Voltage	V_{IL}	0.3		0.8	VDC	
Input Low Current	I_{IL}	–	–	40	µA	
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}		–	–	VDC	
Type OA		3.5	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD						I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0.4 to V_{CC}-1

Table 6. Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		AC Input Voltage Range	1.1 VP-P
		Reference Voltage	+2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P (with reference to ground and a 600 Ω load)
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 200 mV
SPKM	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 20 mV

Table 7. Current and Power Requirements

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)
Normal mode	124	136	620	715
Sleep mode	1.8	—	9.0	—

Notes:
1. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.
2. Input Ripple ≤ 0.1 Vpeak-peak.
3. Crystal frequency = 56.448 MHz.

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA