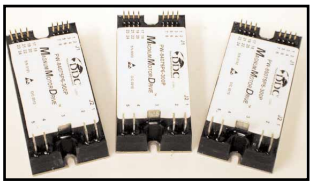
MAGNUM MOTOR DRIVE SERIES™ PW-8X075P6

75A, 600V MAGNUM MOTOR DRIVES



FEATURES

- *600 Vdc Drive for 270 Vdc Motors*
- *75 Amps @25°C, 50 Amps @85°C*
- *Operates with Brushless, Brush, and Induction Motors*
- *Input to Output Ground Isolation with Floating Output Stage*
- *Short Circuit Protection*
- *Trapezoidal or Sinusoidal Compatible*
- *DSP/Microprocessor Compatible*
- *PW-83075P6 - Half-Bridge Drive*
- *PW-84075P6 - Half-Bridge Drive with Current Sense*
- *PW-85075P6 - Half-Bridge Drive with Regenerative Clamp*

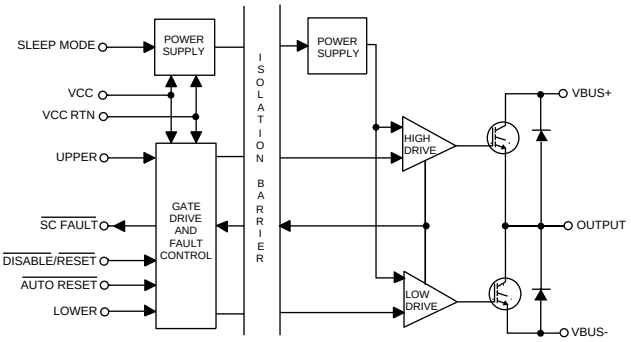


FIGURE 1A. PW-83075P6 BLOCK DIAGRAM

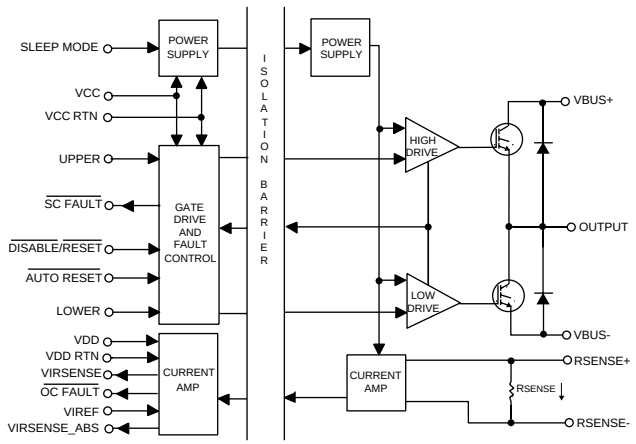


FIGURE 1B. PW-84075P6 BLOCK DIAGRAM

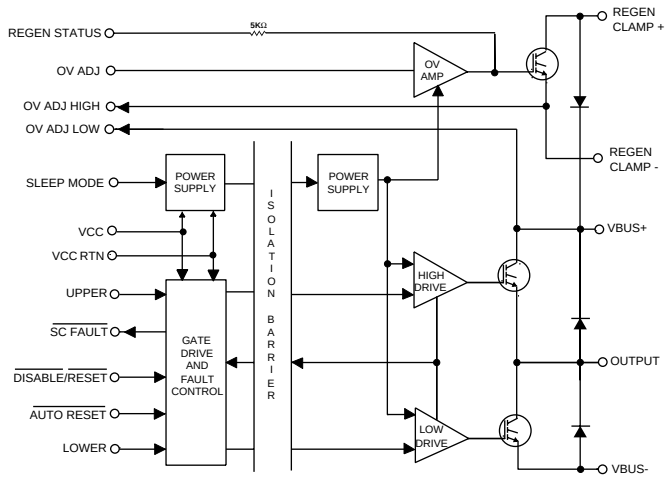


FIGURE 1C. PW-85075P6 BLOCK DIAGRAM

DESCRIPTION

The PW-83075P6, PW-84075P6 and PW-85075P6 are half-bridge drive modules containing isolated switch drivers, a pair of solid state switches, and an isolated power supply. In addition, the PW-84075P6 contains current sensing feedback and the PW-85075P6 contains a regenerative clamp protection circuit. The three modules can be used in any combination to create drives for brush, brushless DC, or AC induction motors. The current sense signal and logic inputs are compatible with DSP/microprocessors and/or FPGA/ASIC circuits used to control the motor drives. These modular drives are capable of operating from either a ±135Vdc or 270Vdc power source that is electrically isolated from the logic input signals. The modules are fault tolerant from output shorts, loss of any or all power supplies, and power supply sequencing.

APPLICATIONS

The high reliability and flexibility of these drives make them suitable for Military and Aerospace applications. Among the many applications are: actuator systems for primary and secondary flight controls on aircraft, fan and compressor motor drives for environment conditioning, pump motors for fuel and hydraulic fluid, antenna and radar positioning, and thrust vector position control of missiles, drones, and RPV's.

TABLE 1. PW-8X075P6 ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
Drive Supply Voltage	V_{BUS}+ to V_{BUS}-	600	Vdc
Logic Power-In Supply Voltage	V_{CC}	5.5	Vdc
Input Logic Voltage	UPPER, LOWER, $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$, SLEEPMODE, $\overline{\text{AUTO RESET}}$	5.5	Vdc
Reference Input Voltage	V_{IREF}	V_{DD} + 0.5	Vdc
Continuous Output Current	I_O	75	A
Peak Output Current (10 ms)	I_{PEAK}	150	A
Storage Temperature Range	Tcs	-65 to +125	°C
Intermittent Case Operating Temperature	T_{CI}	-55 to +125	°C
Continuous Case Operating Temperature	Tc	-55 to +100	°C
Junction Temperature, Power Devices	Tj	+150	°C
Junction Temperature, Other Components	T_J	+125	°C
Ground Isolation Voltage (Note 1)	V_{ISO}	2500	Vdc

Note 1: From $V_{CC\text{-}RTN}$ to V_{BUS}+, V_{BUS}-, OUTPUT, REGEN CLAMP+, R_{SENSE}+, R_{SENSE}-.

TABLE 2. PW-8X075P6 SPECIFICATIONS
(V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, TC = -55°C TO +100°C FOR MIN, MAX VALUES, TC = +25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT STAGE						
Drive Supply Voltage (motor)	V_{BUS}+ TO V_{BUS}-	Unipolar/Bipolar		270	600	Vdc
Output Switch Transistors (each)						
Continuous Current Drive	I_O	+25°C case			75	A
		+85°C case			50	A
Turn-on energy per pulse	$E_{T\text{-}ON}$	V_{CE} = 270V, I = 50A T_j = +125° C		4.0		mJ
Turn-off energy per pulse	$E_{T\text{-}OFF}$	V_{CE} = 270V, I = 50A T_j = +125° C		2.4		mJ
Peak Current	I_{PEAK}	+85°C case,≤15 ms			100	A
Short Circuit Trip Current (Note 1)	I_{SC}	≤5 µs	200	350	400	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$	I_O = 50A		2.2	2.6	Vdc
FLYBACK DIODE						
Forward Voltage	V_F	I_O = 50A		1.7	1.9	Vdc
Reverse Recovery Time @ T_j = +125° C	T_{rr}	I_O = 50A		175		ns
Reverse recovery Peak Current	Irm	di/dt = 480A/µs IF = 50A (90 °C)		19	33	A
Reverse Leakage Current @ T_j = +25° C	I_r	VBUS = 480Vdc		30	325	µA
Reverse Leakage Current @T_j = +125° C	I_r	VBUS = 480Vdc			17	mA
OUTPUT SWITCHING CHARACTERISTICS (See FIGURE 5)						
Turn-on Propagation Delay	t_d(on)		150	430	650	ns
Turn-off Propagation Delay	t_d(off)		740	790	1800	ns
Disable Propagation Delay	t_{sd}		25	33	45	µs
Turn-on Rise Time	t_r		100		200	ns
Turn-off Fall Time	t_f		140		200	ns
Sleep_Mode Delay	tsleepu			3.7		ms
Output Switching Frequency	fPWM		0		35	KHz
Control Inputs						
UPPER, LOWER, DISABLE/RESET						
AUTO RESET		V_{CC} = 4.5V				
High Level Input Voltage	VIH		1.55	2.5	3.15	Vdc
Low Level Input Voltage	VIL		0.9	1.6	2.45	Vdc
Hysteresis Voltage	VHYST		0.4	0.9	2.1	Vdc
UPPER, LOWER						
High Level Input Current	IIH	Vin = V_{CC}	22	23	24	µA
Low Level Input Current	IIL	Vin = 0V	0	0.1	100	nA
RESET/DISABLE						
High Level Input Current	IIH	Vin = V_{CC}		0		µA
Low Level Input Current	IIL	Vin = 0V	22	23	24	µA
AUTO_RESET						
High Level Input Current	IIH	Vin = V_{CC}		0		µA
Low Level Input Current	IIL	Vin = 0V	1.3	1.4	1.5	mA
SLEEP_MODE						
High Level Input Voltage	VIH	V_{CC} = 4.5V	2.4			Vdc
Low Level Input Voltage	VIL	V_{CC} = 4.5V			0.8	Vdc
High Level Input Current	IIH	Vin = V_{CC}		0.1		µA
Low Level Input Current	IIL	Vin = 0V	0.4		0.5	mA

TABLE 2. PW-8X075P6 SPECIFICATIONS
(T_C = +25°C, V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO +100°C FOR MIN, MAX VALUES)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
UPPER-LOWER DEADTIME	tdead		1.0			µs
AUTO_RESET Delay to output off	tdoff.auto			202		ms
AUTO_RESET Delay to output enabled	tdon.auto			3.0		ms
RESET pulsewidth to clear SC_FAULT	tpw.reset		200			ns
Cycle time between AUTO_RESET retries	tcycle.auto	(See Note 2)	40	100		ms
CONTROL OUTPUTS						
SC_FAULT						
High Level Output Current	ISCFLTH	Vo = V_{CC}	22	23	24	µA
Low Level Output Current	ISCFLTL	Vo = 0.4V	5	10		mA
THERMAL						
Maximum Thermal Resistance - IGBT	θjc	Each Output Switch		0.5	0.55	°C/W
- Diode	θjc			0.8	0.87	°C/W
Junction Temperature Range	Tj		-55		+150	°C
Case Operating Temperature	Tc		-55		+100	°C
Case Storage Temperature	Tcs		-65		+150	°C
MECHANICAL						
Maximum Lead Soldering Temp	Ts				+250	°C
Mounting Torque					3	in-lbs
Weight					3.1 (88)	oz (gr)

Note 1: V_{BUS}+ to V_{BUS}- must be ≥ 10V (during short circuit) for short circuit protection to operate.
Note 2: AUTO_RESET tied to SC_FAULT

TABLE 3. PW-83075P6 SPECIFICATIONS
(T_C= +25°C)

Power and Logic Supply						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	V
Logic Supply Current	ICC	SLEEP MODE		11		mA
		F_{pwm} = 25Khz		110	200	mA

TABLE 4. PW-84075P6 SPECIFICATIONS
(T_C= +25°C V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Amplifier						
$V_{IRsense}$ Gain	Gvout	V_{IREF} = 5.0V		29.76		mV/A
$V_{IRsense}$ Gain Error	Evout		-6		6	%
$V_{IRsense}$ Offset	Vos	V_{IREF} = 5.0V	-30		30	mV
$V_{IRsense}$ Offset Drift	TCVos	V_{IREF} = 5.0V	-90		110	ppm/°C
$V_{IRsense}$ Gain %	Gvout%	0A = Vref/2		0.595		%V_{IREF}/A
$V_{IRsense}$ Offset %	Vos%V_{IREF}		-0.6		0.6	%V_{IREF}
$V_{IRsense}$ Offset % Drift	TCVos%		-18		22	ppm of V_{IREF}/°C
I_VABS Gain	Gvabs	0A = 0V		59.52		mV/A
I_VABS Gain Error	Evabs		-8		8	%
I_VABS Offset	Vosabs	V_{IREF} = 5.0V	-131		131	mV
I_VABS Offset Drift	TCVosabs	V_{IREF} = 5.0V	-90		110	ppm/°C
I_VABS Gain %	Gvout%	0A = 0V		1.19		%V_{IREF}/A
I_VABS Offset %	Vosabs% V_{IREF}		-2.6		2.6	%V_{IREF}
I_VABS Offset % Drift	TCVosabs%		-18		22	ppm of V_{IREF}/°C
Delay Time	tdelay	-55 to 100 °C		9	20	µs
Bandwidth	fBW	-55 to 100 °C	20	30		kHz
Linear Range	Irange	-55 to 100 °C		±50		A
OC_FAULT Trip Level	IOC	-55 to 100 °C	±75	±85	±95	A
Trip Delay Time	T_{IOC}	-55 to 100 °C		66		us
Reference Voltage Current Input	Iviref	-55 to 100 °C		0.26	1	mA
Reference Voltage Input	V_{IREF}	-55 to 100 °C	4.0		V_{DD}	Vdc
OC_FAULT (-55 to 100 °C)						
High Level Output Current	IOCFLTH	Vo = V_{DD}		0.2	15	uA
Low Level Output Current	IOCFLTL	Vo = 0.8V	4			mA
Power & Logic Supply (-55 to 100 °C)						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	V
Logic Supply Current	ICC	SLEEP MODE		11		mA
		F_{pwm} = 25Khz		136	200	mA
Current Amplifier Supply Current	IDD		8	10	20	mA

TABLE 5. PW-85075P6 SPECIFICATIONS
(V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, TC = -55°C TO +100°C FOR MIN, MAX VALUES, TC = +25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Over Voltage Transistor						
Continuous Current Drive	Io	+25°C Case			35	A
		+85°C Case			30	A
Peak Current	I_{PEAK}	+85°C Case, 15 ms			60	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$			2.0	3.0	Vdc
Reverse Leakage @ T_J = +25°C	Ir	600 Vdc			250	µA
Reverse Leakage @ T_J = +125°C	Ir	600 Vdc			1.0	mA
Over Voltage flyback Diode						
Reverse Leakage @ Tc = +25°C	Ir	480 Vdc		20	50	µA
Reverse Leakage @ Tc = +125°C	Ir	480 Vdc		1	7	mA
Over Voltage Trip	Vtrip	no external adjustments	358	400	440	Vdc
Trip Level Hysteresis	Vhyst		34	40	45	Vdc
Power and Logic Supply						
Voltage	V_{CC}		4.5	5	5.5	V
Current	ICC	Sleep Mode		11		mA
		F_{pwm} = 25Khz		137	250	mA
REGEN STATUS (ref. to REGEN CLAMP-)						
High Level Output Voltage	VOHstatus	No Load	13.8	15	15.6	Vdc
Low Level Output Voltage	VOLstatus	No Load		0.2	0.4	Vdc
Output resistance	Rstatus		4.2	4.75	4.8	KΩ
Vtrip rise to status ON Delay	tdon.status			36		µs
Vtrip fall status OFF Delay	tdoff.status			48		µs
THERMAL						
Maximum Thermal Resistance	θjc	Over Voltage Switch		0.8	1.2	°C/W

INTRODUCTION

The PW-8X075P6 is a universal modular half-bridge motor drive intended for use with brush, brushless DC and AC induction motors in aerospace applications.

The isolation barrier, which separates the power and control stage, attenuates the ground noise generated from high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and the need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals.

A built in power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies for the gate drive circuitry and allows switching duty cycles from 0 - 100%.

In addition, the PW-84075P6 provides current sensing of either motor current or DC bus current. This current signal can be used as a feedback signal in a servo drive to create a torque loop.

The output power transistors on all modules are protected from a short circuit applied to the output pin. When a short circuit condition is detected, the output transistor is shut down and a flag *"SC_FAULT"* is made active (logic low (L)) indicating a short has occurred.

All output power transistors can be protected from regenerative bus overvoltage when utilizing dynamic braking with the addition of one PW-85075P6 module. When an overvoltage condition is detected, the overvoltage switch is enabled and an external (user supplied, application specific) load dump resistor is connected across the high voltage bus. During an overvoltage condition, the status flag "REGEN STATUS" is active (logic low (L)) indicating an overvoltage condition is occurring.

MODULE AND I/O OPERATION

UPPER, LOWER (INPUTS)

The UPPER and LOWER are active high CMOS Schmitt-trigger inputs and control the gate drives of the output transistors. (TTL compatibility requires external pull-up resistors) Each input is electrically isolated from the output. A deadband, as shown in FIGURE 2, between UPPER and LOWER inputs is necessary to prevent output cross conduction.

$\overline{\text{SC FAULT}}$ (OUTPUT)

The $\overline{\text{SC FAULT}}$ is an active low open collector output signal that indicates when the output of the module has experienced a short circuit condition with faults cleared. The signal is inactive at a logic high (H). The signal goes active, logic low (L), when a short circuit condition is detected. See **SHORT CIRCUIT PROTECTION** for more detail. $\overline{\text{SC FAULT}}$ remains active (L) until $\overline{\text{DISABLE/RESET}}$ is made active (L).

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ (INPUT)

$\overline{\text{DISABLE/RESET}}$ is an active low CMOS Schmitt-trigger input that is active when a logic low is applied. When $\overline{\text{DISABLE/RESET}}$ is held active it does two things: 1.) Resets the $\overline{\text{SC FAULT}}$ (if it was active), and 2.) Disables the output (makes the output high impedence). If this line is used solely to clear $\overline{\text{SC FAULT}}$ then it only needs to be pulsed active then inactive. The width of the active pulse must be at least the width of the trip reset pulse (100ns) to ensure that SC FAULT is cleared properly. When this line is inactive, the OUTPUT is allowed to respond to the other control lines of the module (UPPER, LOWER, SLEEP).
Note: TTL compatibility requires an external pull-up resistor.

$\overline{\text{AUTO RESET}}$ (INPUT)

When the $\overline{\text{AUTO RESET}}$, active low (L) is tied to $\overline{\text{SC FAULT}}$, the protection circuit will reset automatically after the short circuit fault has occurred, enabling the output to respond to the input commands. See **SHORT CIRCUIT PROTECTION** for more detail.

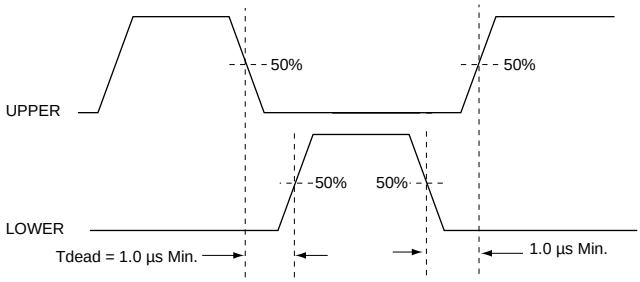


FIGURE 2. PW-8X075P6 DEAD BAND REQUIREMENT

SHORT CIRCUIT PROTECTION

The PW-8X075P6 modules have provisions for complete short circuit protection from either a hard or soft short to the V_{BUS}+ or V_{BUS}- lines. Each output transistor on all PW-8X075P6 modules is protected from a hard (direct, low impedence) short to the V_{BUS}+ or V_{BUS}- lines by circuitry that detects the desaturation voltage for that transistor during a short condition. Once a hard short circuit condition is detected, the active output transistors are shut down and SC FAULT output is set active (logic low (L)). The SC FAULT signal can be used by the controller as a signal to initiate a fault routine to reset or shut down the system. The DISABLE/RESET can be used to shut down the gate drivers if a short persists. If the AUTO RESET is tied to SC FAULT, the circuit will automatically reset when a fault occurs. This inactivates SC FAULT and reactivates the output transistor within 40 to 100ms. If the short is still present, the circuit will repeat the shut down and automatically reset until the short is clear. Protecting against a soft-short requires using a PW-84075 for current sensing and external circuitry. When a soft-short occurs, the external circuit can set DISABLE/RESET low (L) to shut down the gate drivers.

SLEEP MODE (INPUT)

The SLEEP MODE input turns the internal power supply on or off. A logic high (H) on the SLEEP MODE input disables the internal power supply, disabling the motor drive output. No damage will occur to the motor drive during turn on or turn off of the power supply. Additionally, no special power up sequence is required. A logic low (L) enables the power supply and allows the motor drive to operate normally.
The UPPER and LOWER logic gate driver inputs should not be active while transitioning in and out of sleep mode. If the UPPER and LOWER logic inputs must be active while entering sleep mode then DISABLE/RESET must be held active while coming out of sleep mode.

V_{CC}, $V_{CC\text{-}RTN}$ (INPUTS)

The V_{CC} and $V_{CC\text{-}RTN}$ are power connections that supply input power to the internal power supply, the gate drive and fault control circuits.

V_{BUS}+, V_{BUS}- (INPUTS)

V_{BUS}+ and V_{BUS}- are the high voltage power connections to the output stage. The high voltage can be either unipolar (+V and ground) or bipolar (+/- V). Care must be taken to ensure that the transient bus voltage V_{BUS} at the module terminals never exceeds the absolute maximum excursions during switching. External capacitor filtering will be required (See DDC applications note AN/H-7).

OUTPUT (OUTPUT)

The output connects to one input of the motor and applies V_{BUS}+, V_{BUS}-, or high impedance to the motor based on the state of the control inputs. It is capable of sourcing or sinking up to 75 Amps, and the output can withstand a short circuit to V_{BUS}+ or V_{BUS}- without any damage by automatically turning itself off (Zstate).

V_{DD}, V_{DD} RTN (APPLIES TO THE PW-84075P6 ONLY)

The V_{DD} and V_{DD} RTN supply input power to the current amplifier.

$V_{IRSENSE}$ (OUTPUT) (APPLIES TO PW-84075P6 ONLY)

The voltage on the $V_{IRsense}$ pin represents current passing through RSENSE in the direction shown in the block diagram. This $V_{IRsense}$ voltage is scaled by the input voltage at V_{IREF}, where

$$V_{IRsense} = (V_{IREF}/2) + (V_{IREF}/168) * I\_RSENSE$$

Note: I_RSENSE is current through RSENSE.

Zero amps in RSENSE is indicated when $V_{IRsense} = V_{IREF}/2$. A voltage greater (less) than $V_{IREF}/2$ indicates a positive (negative) current flow through RSENSE with a value defined by the $V_{IRsense}$ equation. $V_{IRsense}$ is electrically isolated from the output stage. A Positive (negative) current flow from R_{SENSE}+ to R_{SENSE}- produces a positive (negative) voltage measurement (See figure 2A). When the power supply is shut down (SLEEP MODE input high), the voltage at $V_{IRsense}$ will indicate 0V.

V_{IREF} (INPUT) (APPLIES TO PW-84075P6 ONLY)

A precision voltage reference from an external source is connected to the V_{IREF} pin to set the output voltage scale for $V_{IRsense}$ and $V_{IRsense\_ABS}$. **Note:** The accuracy of the $V_{IRsense}$ and $V_{IRsense\_ABS}$ outputs are subject to the accuracy and temperature coefficient of V_{IREF}. These must be taken into account in calculating the overall accuracy of $V_{IRsense}$.

R_{SENSE}+, R_{SENSE}- (INPUTS) (APPLIES TO PW-84075P6 ONLY)

The R_{SENSE}+ and R_{SENSE}- pins are conected to an internal shunt resistor and monitoring circuitry. These pins can be connected anywhere within the isolation restrictions on the pins (600V to power pins, 2500V to logic pins). These pins are typically connected in series with the output, V_{BUS}+ or V_{BUS}-, to measure motor drive current.

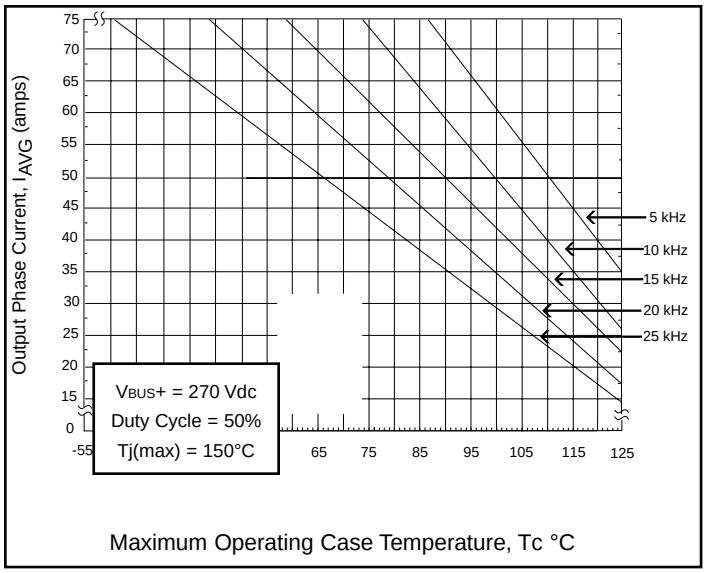


FIGURE 3. PW-8X075P6 OUTPUT PHASE CURRENT VS. MAXIMUM OPERATING CASE TEMPERATURE

$V_{IRSENSE\_ABS}$ (OUTPUT) (APPLIES TO PW-84075P6 ONLY)

$V_{IRsense\_ABS}$ output voltage is the absolute value of the $V_{IRsense}$ voltage signal. $V_{IRsense\_ABS}$ is zero volts when there is no current flowing through the RSENSE resistor. It will increase towards the value of V_{IREF} as the current in RSENSE approaches either -85 or +85 amps (measurement limits of $V_{IRsense}$). $V_{IRsense\_ABS}$ is an open source output and is "wire-OR-able". When two or more $V_{IRsense\_ABS}$ outputs are "wire-OR-ed", the highest voltage will appear on the common signal. A typical use for combining these outputs is for determining when an overload condition has occurred. The $V_{IRsense\_ABS}$ voltage is scaled by the input voltage $V_{IRsense}$ where:

$$V_{IRsense\_ABS} = 2 \times [V_{IRsense} - V_{IREF}/2]$$

$\overline{\text{OC FAULT}}$ (OUTPUT) (APPLIES TO PW-84075P6 ONLY)

$\overline{\text{OC FAULT}}$ is an active low open drain output. $\overline{\text{OC FAULT}}$ goes active when the current flowing through RSENSE has exceeded the $\overline{\text{OC\_FAULT}}$ trip level. This signal is not latched like $\overline{\text{SC FAULT}}$, and goes inactive as soon as the overcurrent condition stops.

REGEN STATUS (OUTPUT) (APPLIES TO PW-85075P6 ONLY)

The REGEN STATUS pin is referenced to REGEN CLAMP-. It indicates the state of the regen clamp switch (H = on, L = off). An external opto-isolator input can be connected between REGEN STATUS and REGEN CLAMP- to translate this status to logic circuits if desired. The REGEN STATUS output is connected to the 0V amplifier through a 5K resistor. When the regen clamp switch is active (inactive), the 0V amp sources +15V (0V) through the 5K resistor. (see Fig. 1C)

OV_ADJ (INPUT) (APPLIES TO PW-85075P6 ONLY)

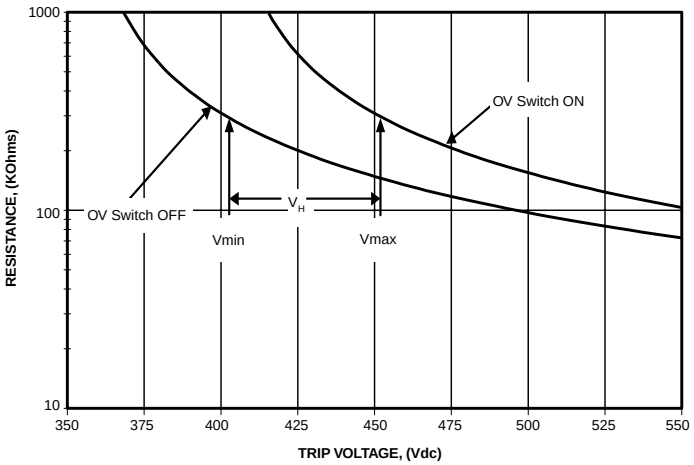
The PW-85075P6 is internally set for a trip voltage of 400V. To set a different trip voltage, an external OV adjust resistor (Ref. R21on FIGURES 9A and 9B) is connected from the OV_ADJ pin to either the OV_ADJ_HIGH or the OV_ADJ_LOW pin. This resistor should be selected for the trip voltage, Vmax, for the regen clamp switch to turn on. (See FIGURES 4A and 4B)

NOTE:

OV_ADJ_LOW (pin 22), OV_ADJ_HIGH (pin 17), and OV_ADJ (pin 20) are available on the control side of the module for ease of connecting the external OV adjust resistor.

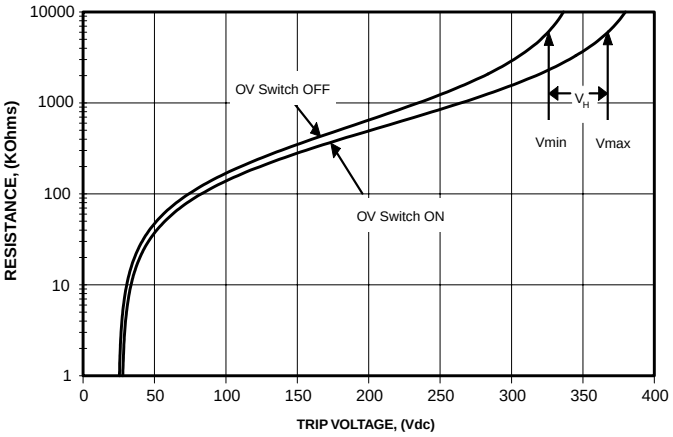
REGEN CLAMP+, REGEN CLAMP- (OUTPUTS) (APPLIES TO PW-85075P6 ONLY) (REF. R20 ON FIGURES 9A AND 9B)

An external load dump resistor is connected between REGEN CLAMP+ and V_{BUS}+. When V_{BUS}+ reaches the over voltage trip level set by the OV_ADJ, the internal clamp circuit will apply the load dump resistor from V_{BUS}+ to the REGEN CLAMP-, thereby dissipating the regenerative energy in the external resistor. In addition, REGEN CLAMP- has to be externally connected to V_{BUS}- for the clamp circuit to work properly. This connection (PCB traces or wire) has to be able to carry the regenerative current.



NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 4A. PW-8X075P6 TYPICAL OVER VOLTAGE TRIP VS. OV ADJUST SETTING WITH AN EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_HIGH



NOTE: V_H = HYSTERESIS VOLTAGE

FIGURE 4B. PW-8X075P6 TYPICAL OVER VOLTAGE TRIP VS. OV ADJUST SETTING WITH AN EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_LOW

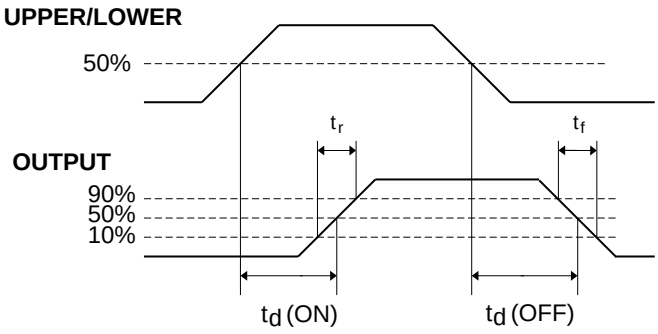


FIGURE 5. PW-8X075P6 INPUT/OUTPUT TIMING RELATIONSHIP

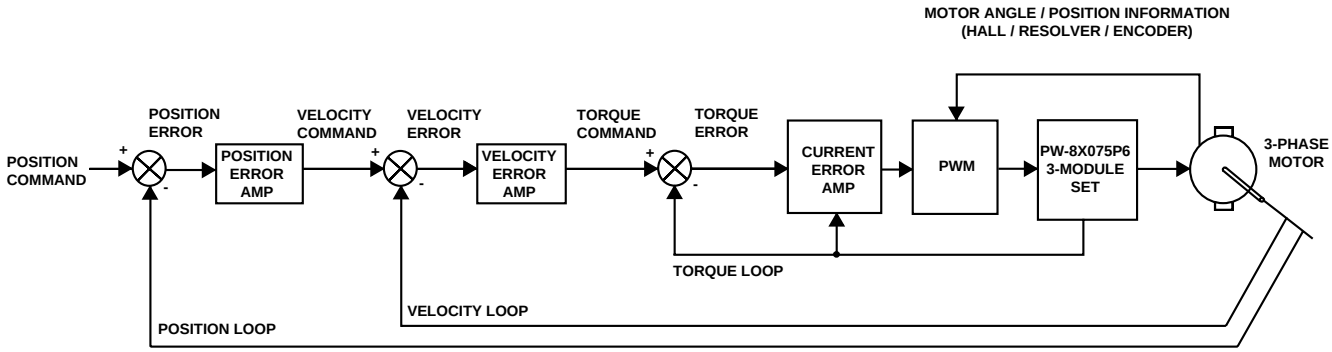


FIGURE 6. TYPICAL POSITION AND VELOCITY CONTROL LOOP

TABLE 6. PW-8X075P6 TRUTH TABLE

UPPER	LOWER	$\overline{\text{DISABLE}}$/ RESET	SLEEP-MODE	$\overline{\text{SC-FAULT}}$	OUT
0	0	X	X	X	Z
1	0	1	0	1	BUS+
0	1	1	0	1	BUS-
1	1	X	X	X	Z
1	0	1	0	0	*
0	1	1	0	0	*
X	X	0	X	X	Z
X	X	X	1	X	Z

X = Indicates that this input is irrelevant
Z = High Impedance (off).
*= Fault will disable the transistor that caused the fault. The output state could be Z or ON.

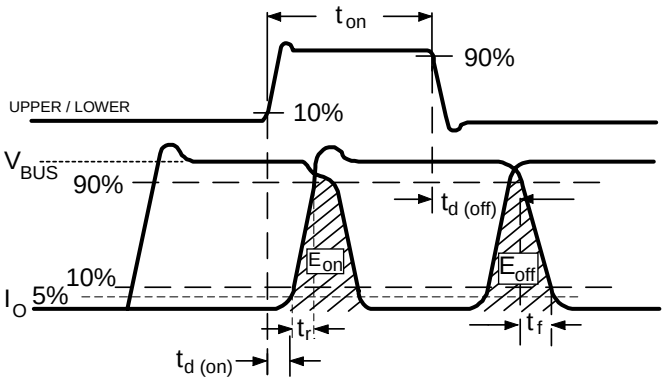


FIGURE 7. OUTPUT CHARACTERISTICS

POWER DISSIPATION (see FIGURE 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses. Consider the following operating conditions

TCASE = 85 °C
VBUS = +270V
I_O = 40A (see FIGURE 7);)
ton = 50µs (see FIGURE 7); T = 100µs (period)
$V_{CE(SAT)}$ = 2.2V (see TABLE 2)
t_r = 200ns (see Figure 7); t_f = 200ns (see FIGURE 7)
fpwm = 10kHz (switching frequency)
V_F is the diode forward voltage, TABLE 2, I_o = 50A, TC = +25°C
V_F(avg) = 1.35V

$T_{J\ MAX}$ = 150 °C (Table 2, T_J) Θ_{JC} = 55 °C/W (Table 2)

1. Conduction Losses (P_C)

$P_C = I_o \times V_{CE(SAT)} \times (ton / T)$
P_C = 45A x 2.2V x (50µs / 100µs)
P_C = 44W

2. Switching Losses (P_S)

$P_S = (E_{ON} + E_{OFF}) \times fpwm$
$E_{ON} = (E_{T\text{-}ON} \times (VBUS / 270) \times (I_O/50A))$
$E_{ON} = (4.0 \times (270 / 270) \times (40 / 50))$
E_{ON} = 3.2 mJ

$E_{OFF} = (E_{T\text{-}OFF} \times (V_{BUS}/270) \times (I_o/50))$
$E_{OFF} = (2.4\ mJ \times (270/270) \times (40/50))$
E_{OFF} = 1.92 mJ
$P_S = 10000 \times (.0032 + .00192)$
P_S = 51.2W

3. Flyback diode Losses (Pdf)

$Pdf = I_o \times V_F(avg) \times (1- (ton / T))$
Pdf = 50A x 1.35V x [1 - (50µs / 100µs)]
Pdf = 33.8W

Transistor Power Dissipation (P_T)

$$P_T = P_C + P_S = 95.2W$$

To calculate the maximum power dissipation of the output transistor / diode pair as a function of the case temperature, use the following equation.

$$P_{MAX} = ((T_{JMAX} - T_{CASE}) / \Theta_{JC})$$

$$118W = ((150\ °C - 85\ °C) / 0.55\ °C/W)$$

CHARACTERISTIC CURVES FOR OUTPUT POWER TRANSISTORS ON PW-8X075P6

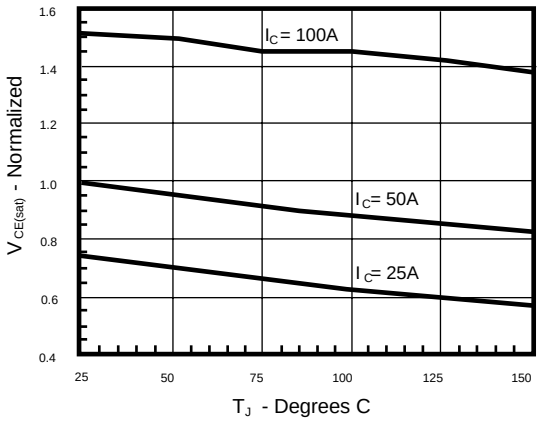


FIGURE 8A. TEMPERATURE DEPENDENCE OF $V_{CE(SAT)}$;

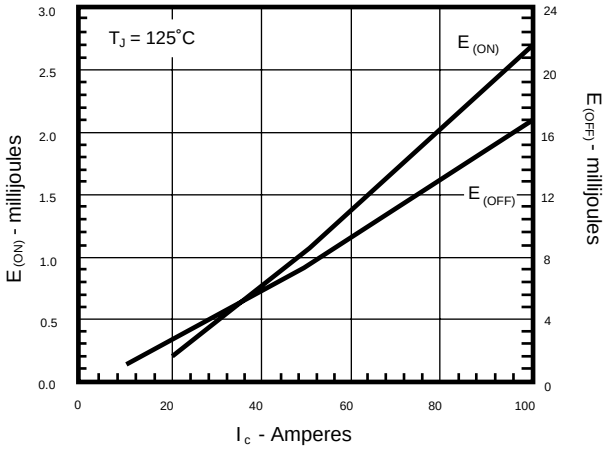


FIGURE 8B. DEPENDENCE OF E_{ON} AND E_{OFF} ON I_C

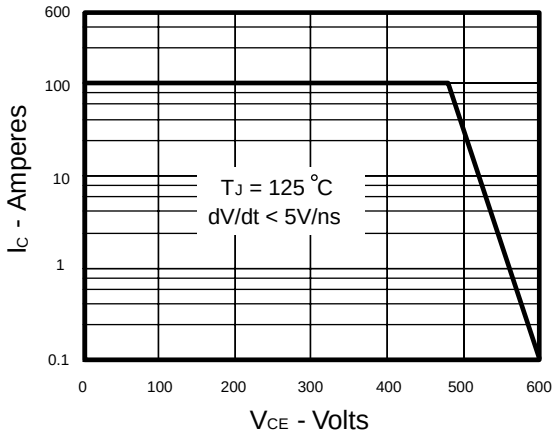


FIGURE 8C. TURN-OFF SAFE OPERATING AREA

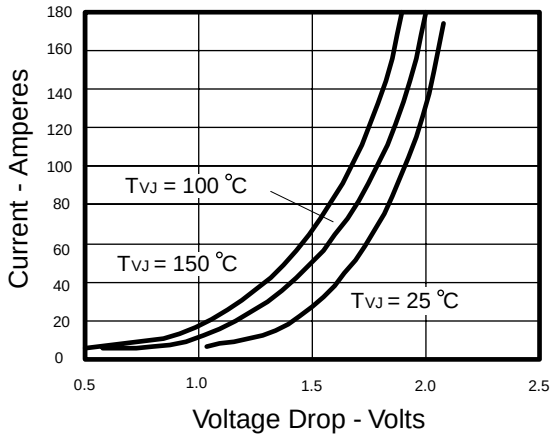


FIGURE 8D. MAXIMUM FORWARD VOLTAGE DROP

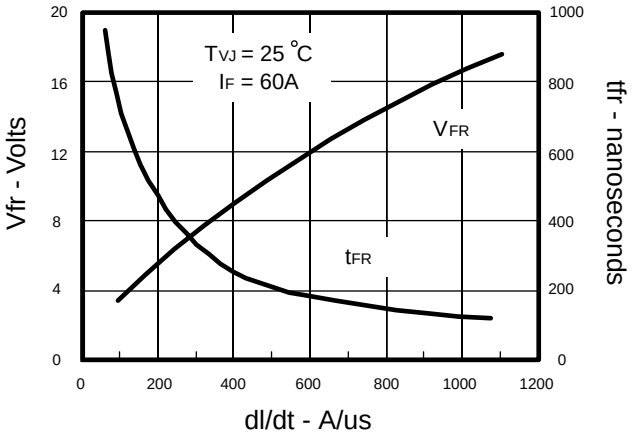


FIGURE 8E. PEAK FORWARD VOLTAGE V_{FR} AND FORWARD RECOVERY TIME T_{FR}

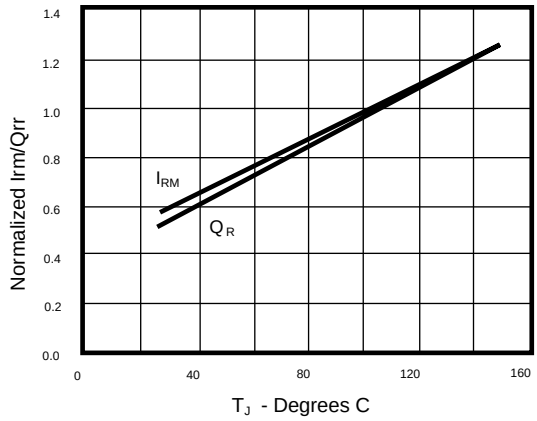


FIGURE 8F. JUNCTION TEMPERATURE DEPENDENCE OF I_{RM} AND Q_R

CHARACTERISTIC CURVES FOR OUTPUT POWER TRANSISTORS ON PW-8X075P6

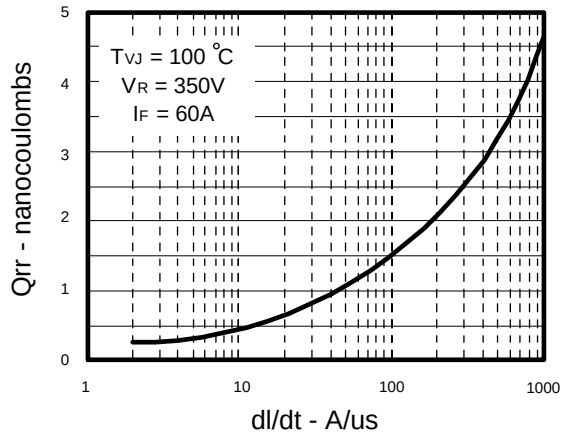


FIGURE 8G. MAXIMUM REVERSE RECOVERY CHARGE

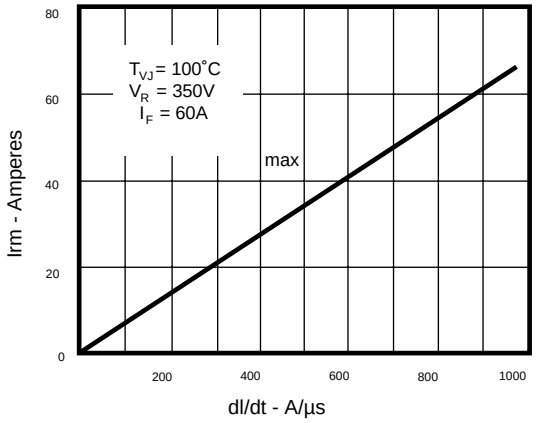


FIGURE 8H. PEAK REVERSE RECOVERY CURRENT

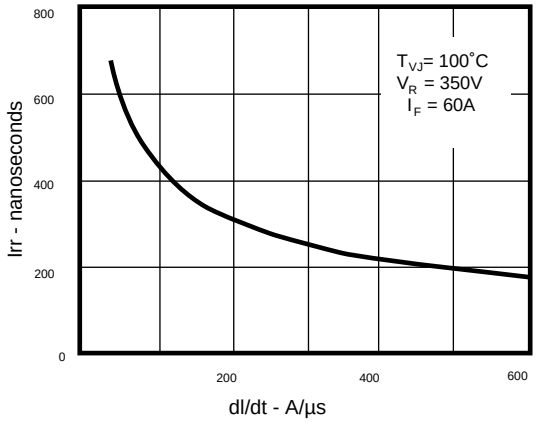


FIGURE 8I. MAXIMUM REVERSE RECOVERY TIME

CHARACTERISTIC CURVES FOR OVERVOLTAGE SWITCH TRANSISTORS ON PW-85075P6

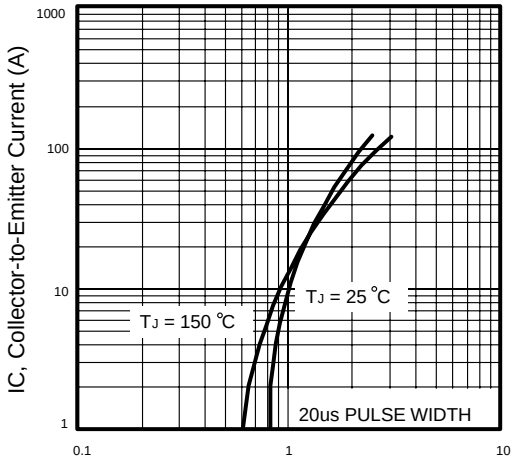


FIGURE 9A. TYPICAL OUTPUT CHARACTERISTICS

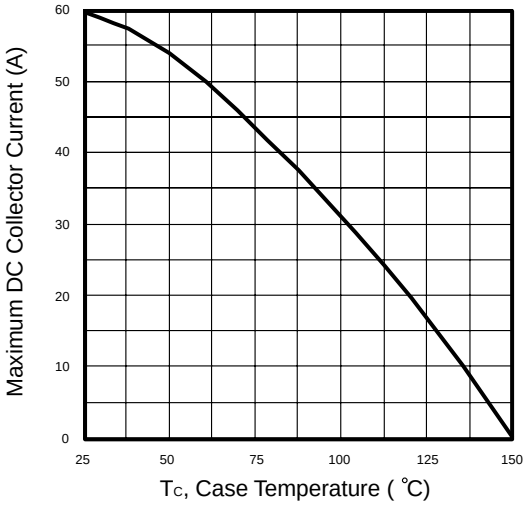


FIGURE 9B. MAXIMUM COLLECTOR CURRENT VS. CASE TEMPERATURE

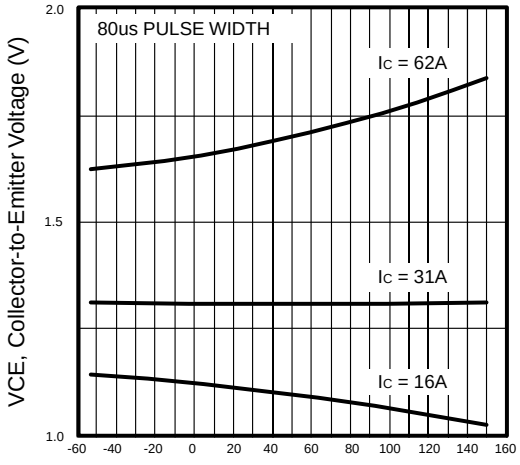


FIGURE 9C. COLLECTOR-TO-EMITTER VOLTAGE VS. JUNCTION TEMPERATURE

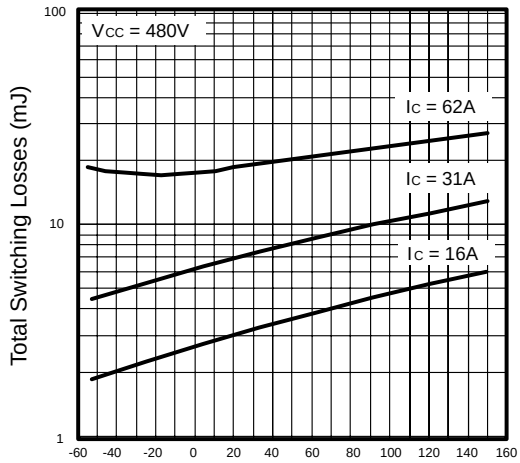


FIGURE 9D. TYPICAL SWITCHING LOSSES VS. JUNCTION TEMPERATURE

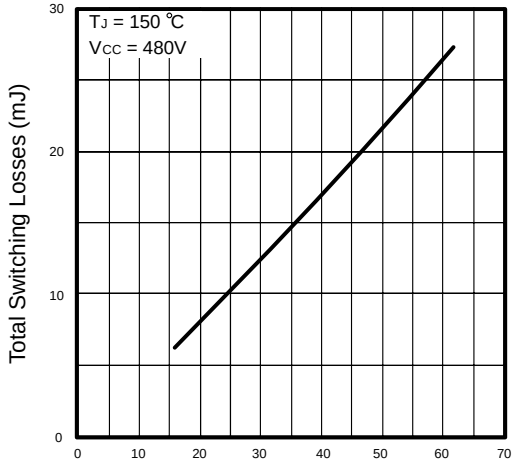


FIGURE 9E. TYPICAL SWITCHING LOSSES VS. COLLECTOR-TO-EMITTER CURRENT

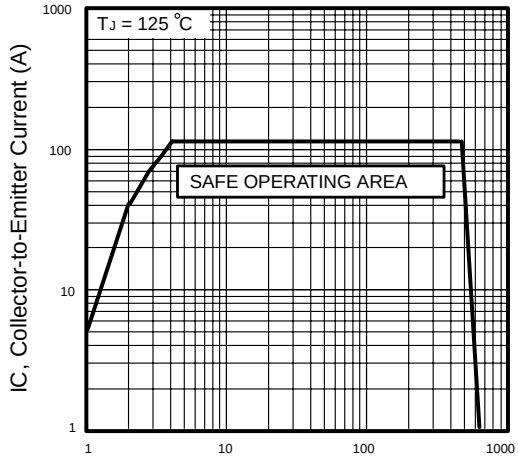


FIGURE 9F. TURN-OFF SAFE OPERATING AREA

TABLE 7: PIN ASSIGNMENTS			
PIN #	FUNCTIONS DESCRIPTION		
	PW-83075P6	***PW-84075P6***	***PW-85075P6***
Control			
1	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$	$\overline{\text{DISABLE}}/\overline{\text{RESET}}$
2	V_{CC}	V_{CC}	V_{CC}
3	UPPER	UPPER	UPPER
4	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$
5	LOWER	LOWER	LOWER
6	SLEEP MODE	SLEEP MODE	SLEEP MODE
7	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$
8	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$
17	N/C	V_{IREF}	OV_ADJ_HIGH*
18	N/C	$V_{IRsense}$	REGEN STATUS
19	N/C	$V_{IRsense\_ABS}$	N/C
20	N/C	V_{DD}	OV_ADJ
21	N/C	$V_{DD\text{-}RTN}$	N/C
22	N/C	$\overline{\text{OC FAULT}}$	OV_ADJ_LOW*
23	N/C	N/C	N/C
24	N/C	N/C	N/C
Power			
25	N/C	R_{SENSE}-	REGEN CLAMP+
26	N/C	R_{SENSE}+	REGEN CLAMP-
27	V_{BUS}+	V_{BUS}+	V_{BUS}+
28	OUTPUT	OUTPUT	OUTPUT
29	V_{BUS}-	V_{BUS}-	V_{BUS}-

* Connection for external OV adjust resistor only.

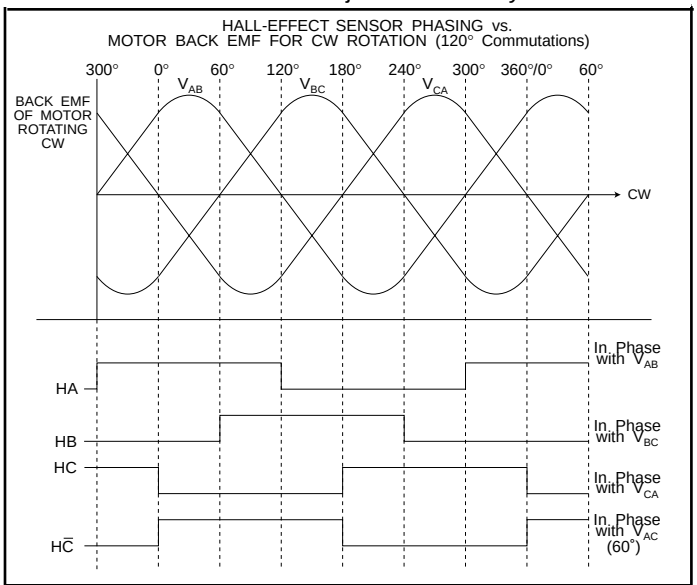


FIGURE H1. HALL PHASING

APPLICATIONS:

POSITION OR VELOCITY CONTROL USING DSP

Figure 9A shows an example of position and/or velocity control hook-up with inner torque loop using the Digital Signal Processor (DSP) for motor control. Using software, the DSP can be implemented with one of several motor control algorithms such as FOC (Field Oriented Control) with SVM (Space Vector modulation).

TORQUE HOOK-UP USING UC-1625 MOTOR CONTROLLER

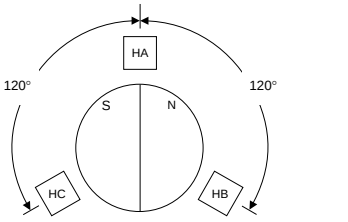
Figure 9B shows an example of torque control loop with regenerative clamp protection using UC-1625, two PW-84075P6, and one PW-85075P6. Two PW-84075P6 (½ bridge with current sense) sense the current in motor phase A and C. $V_{IRsense\_ABS}$ pins on each of the PW-84075P6 can be tied together to generate a single composite analog output which is compared to the torque commanded input to produce an error signal. UC1625 uses this error signal to regulate the output current (or torque) by controlling the duty cycle of the output transistors.

For the case when a resolver is available instead of Hall-effect devices, the circuit shown in Figure 9C converts the resolver (sin and cos) signals to Hall signals which can be used to commutate the output transistors.

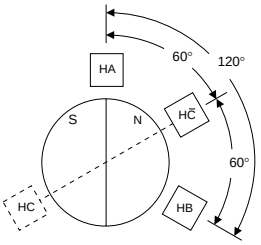
HALL SIGNAL COMMUTATION

The hall A, B, C signals are logic signals from the motor Hall-effect sensors. The UC-1625 uses a phasing convention referred to as 120 degree spacing; that is, the output of HA is in phase with motor back EMF voltage VAB, HB is in phase VBC, and HC is in phase with VCA. Logic “1” (or HIGH) is defined by an input greater than 2.4Vdc or an open circuit to the controller; Logic “0”(or LOW) is defined as any Hall voltage input less than 0.8Vdc.

The UC-1625 will operate with Hall phasing of 60° or 120° electrical spacing. If 60° commutation is used, then the output of HC must be inverted as shown in FIGURES H1 and H2. In FIGURE H1 the Hall sensor outputs are shown with the corresponding back emf voltage they are in phase with.

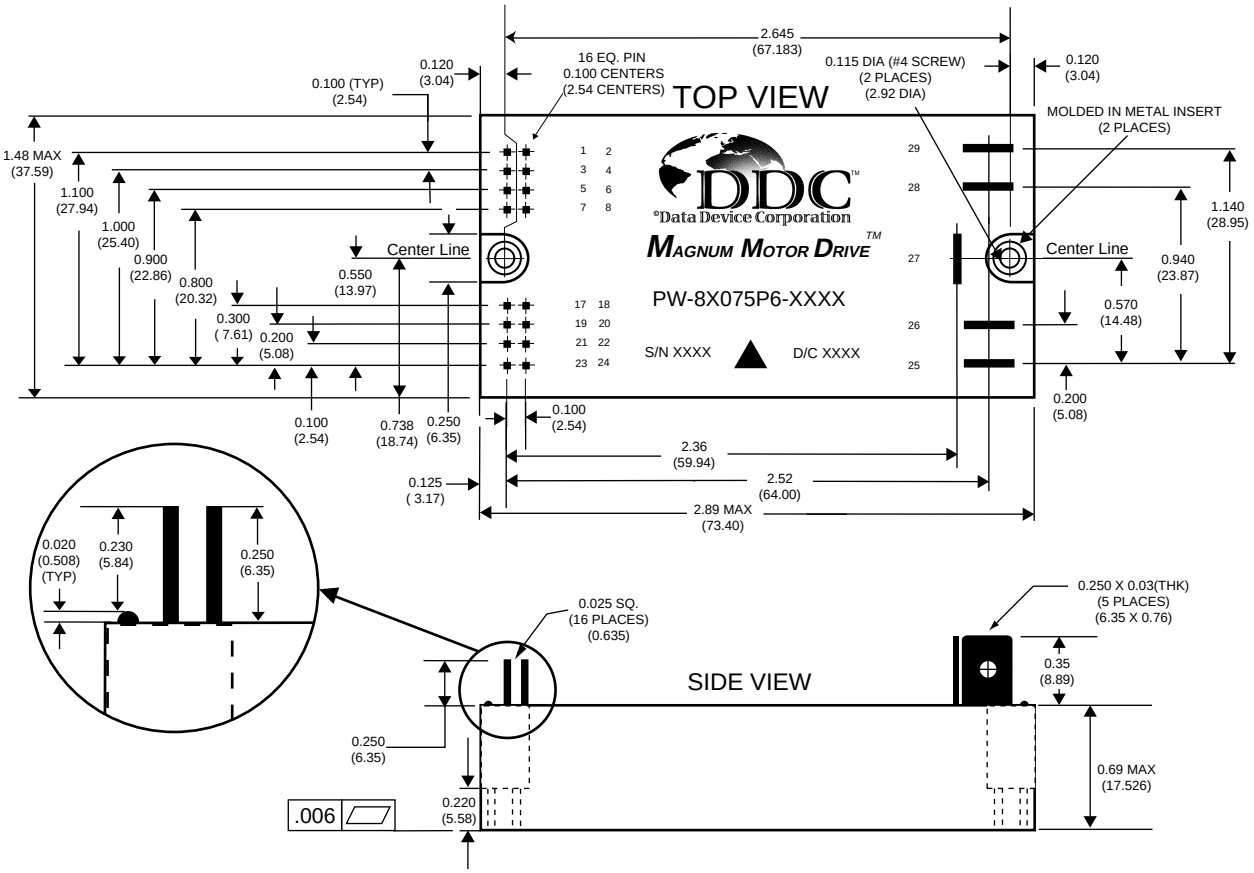


REMOTE POSITION SENSOR (HALL) SPACING FOR 120 DEGREE COMMUTATION



REMOTE POSITION SENSOR (HALL) SPACING FOR 60 DEGREE COMMUTATION

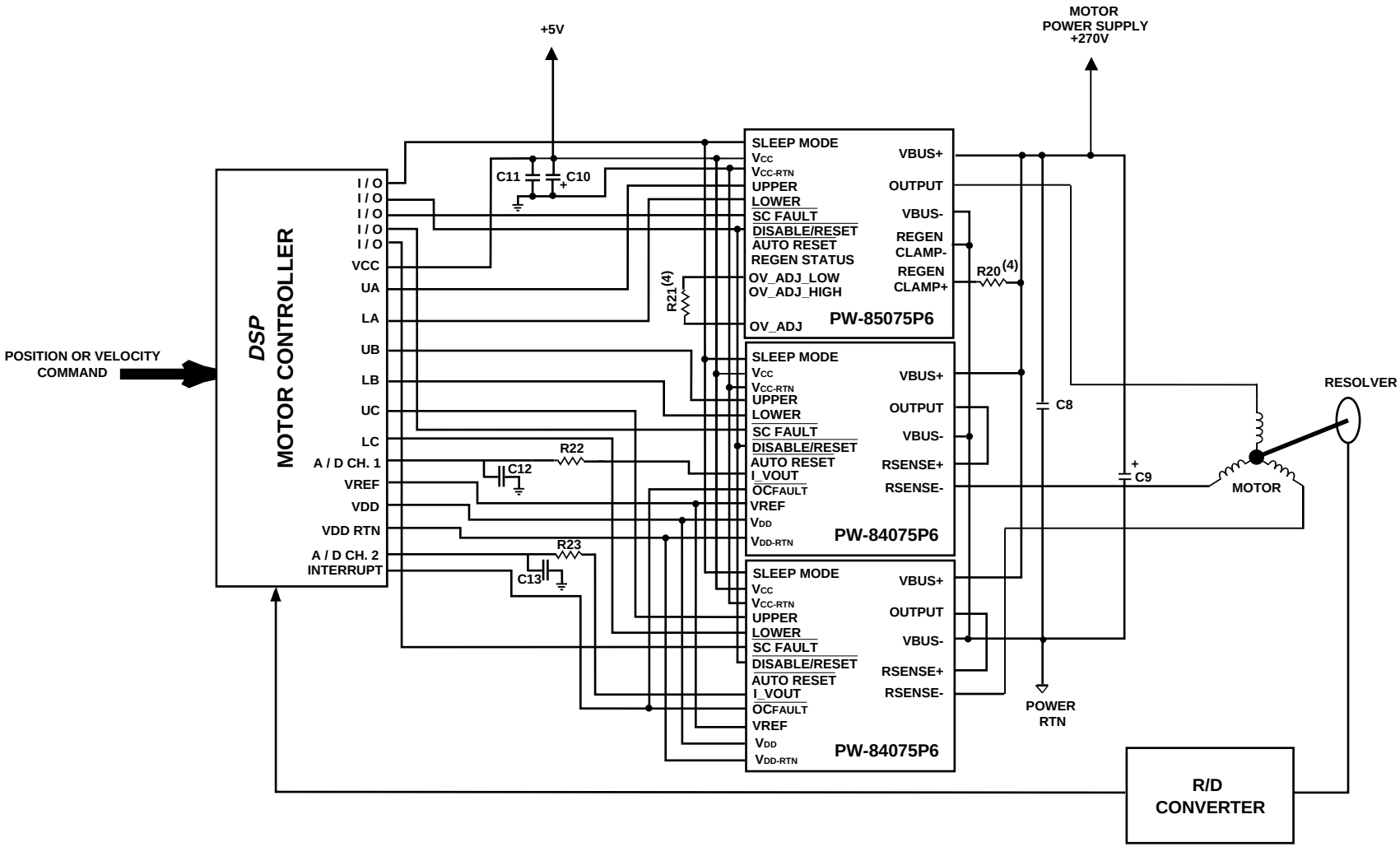
FIGURE H2. HALL SENSOR SPACING



NOTES:
1. Dimensions are in inches (MM).

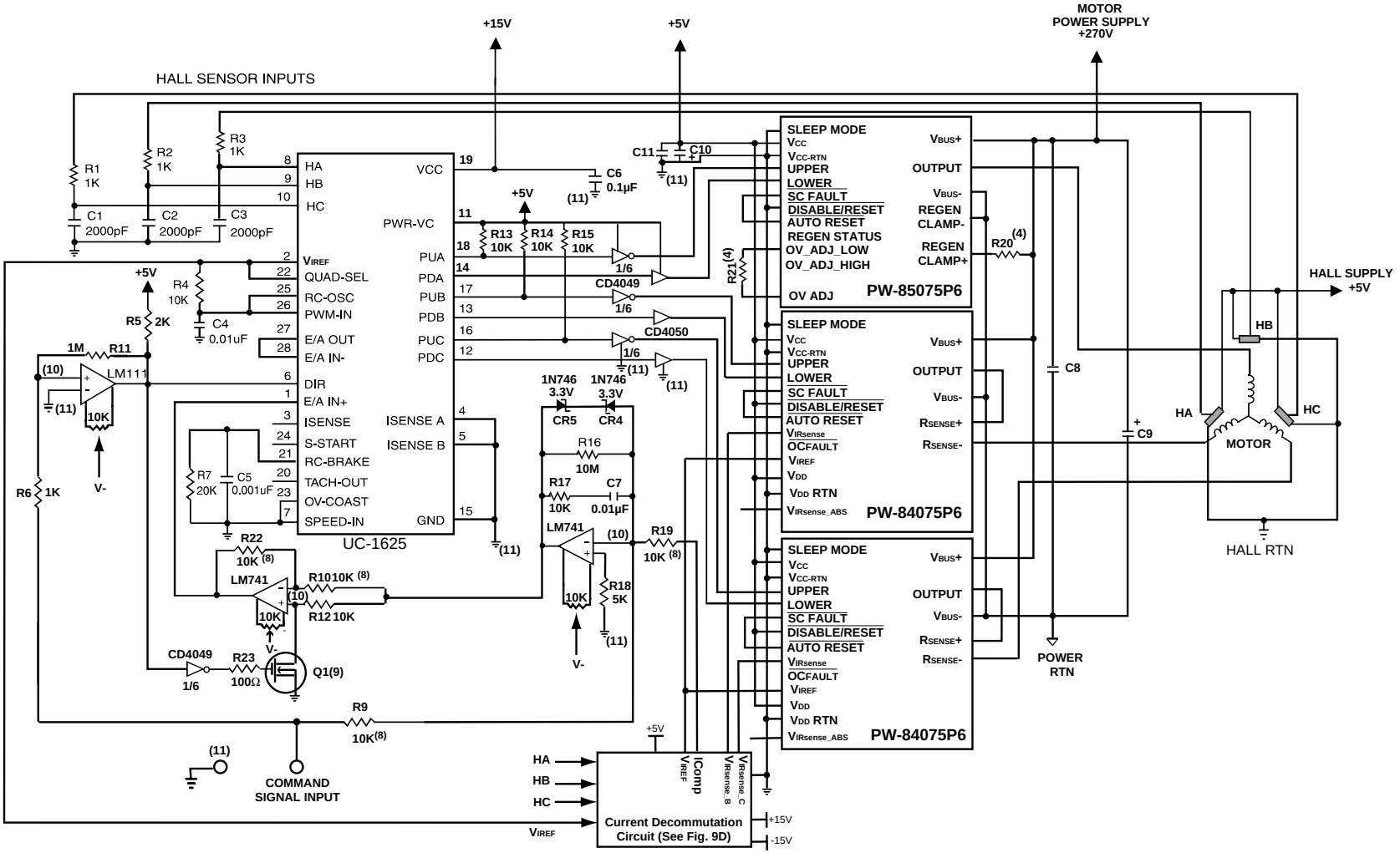
MOUNTING CONSIDERATIONS:
1. Minimum spacing center line to center line - 1.5 inches (38.1 mm)
2. Mounting torque using 4-40 stainless steel mounting screws - 5 to 6.5 in.-lbs.

FIGURE 8. PW-8X075P6 OUTLINE



NOTES:
1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, *PW-82351 Motor Drive Power Supply*, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, *PW-82351 Motor Drive Power Supply,* equation 1.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV Adjust and Regen description for details)

FIGURE 9A. PW-8X075P6 POSITION OR VELOCITY HOOK-UP USING DSP MOTOR CONTROLLER



NOTES:

1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, *PW-82351 Motor Drive Power Supply*, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, *PW-82351 Motor Drive Power Supply,* equation 1.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 and R21 is application specific.
5. All resistors have a tolerance of ±10%, unless otherwise specified.
6. The CD4050 converts the +15V logic output of the UC-1625 to +5V logic signals.
7. The CD4049 (or equivalent) inverts the upper signal from the UC-1625.
8. 1% or better, depending on required accuracy.
9. Q_1 can be either IRML2402 or IRMU014 ir IRLD014.
10. These high impedance inputs and summing junctions of the operational amplifiers are highly sensitive to noise.
11. These grounds should be closely tied together to reduce ground noise effect.
12. Connect Hall sensor inputs to motor shaft position sensors that are 120 electrical degrees apart. Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals are inverted.

FIGURE 9B. PW-8X075P6 TORQUE HOOK-UP USING UC-1625 MOTOR CONTROLLER

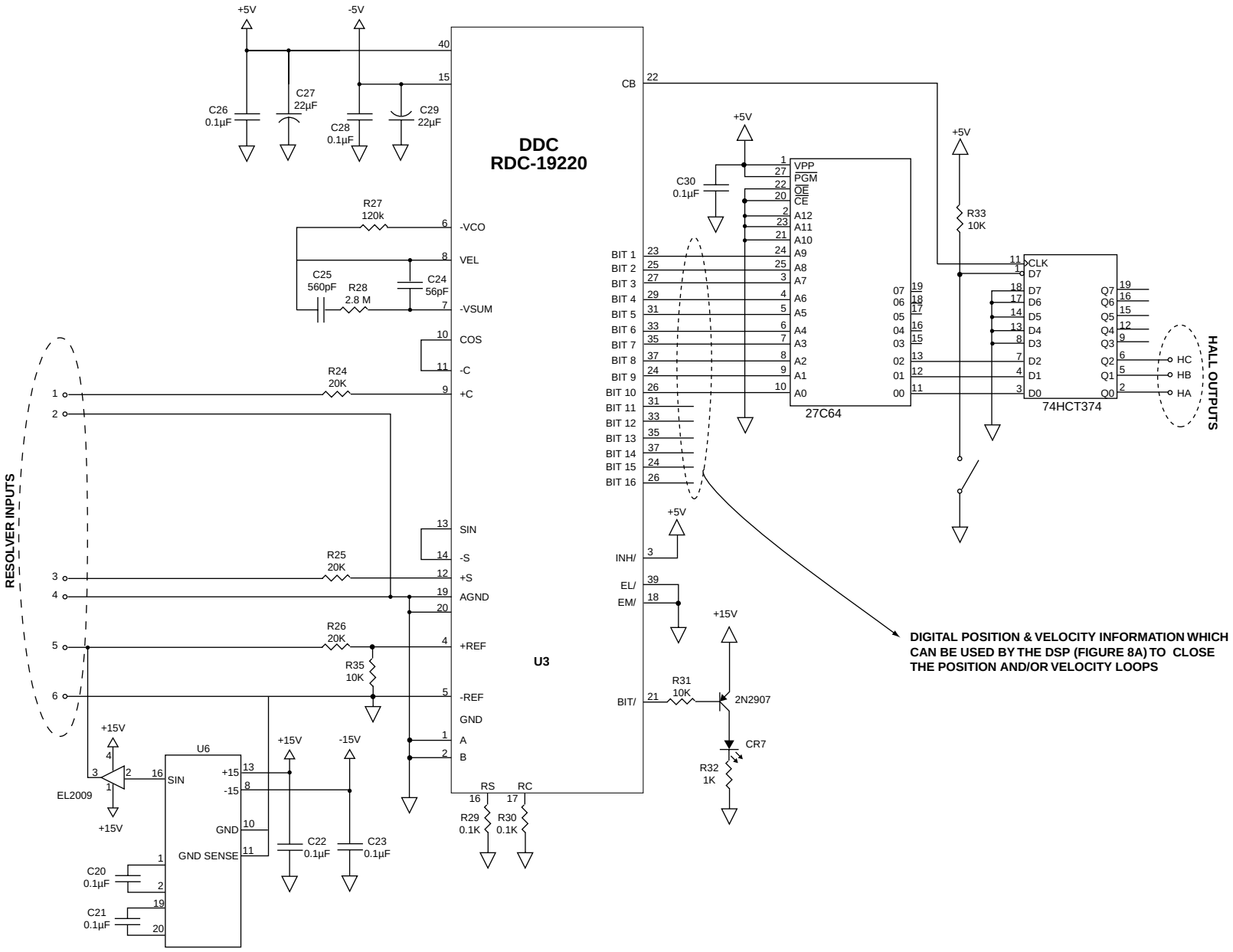
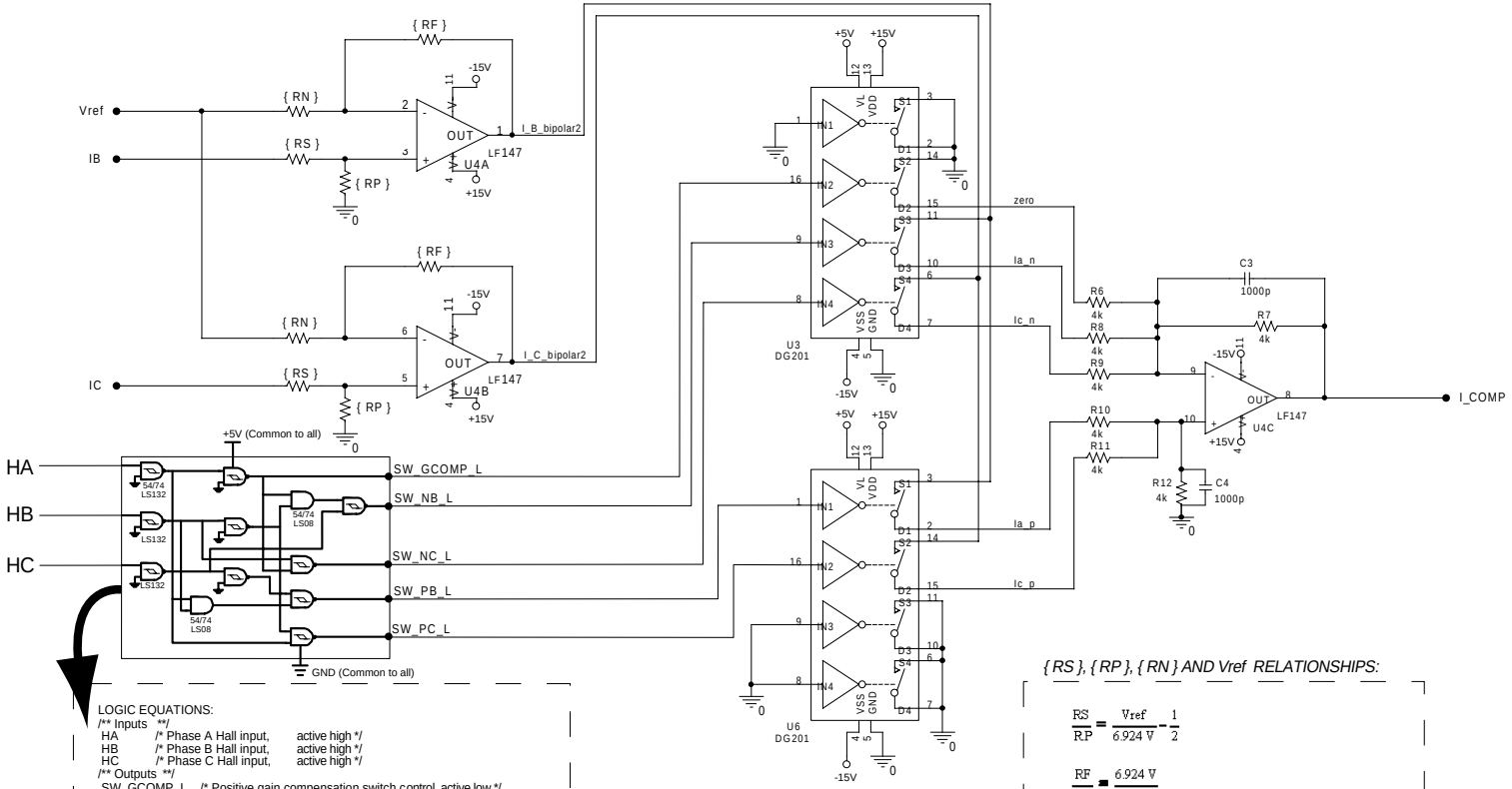


FIGURE 9C. RESOLVER TO HALL SIGNAL CONVERSION CIRCUIT




```
LOGIC EQUATIONS:
/** Inputs  **/
  HA        /* Phase A Hall input,      active high */
  HB        /* Phase B Hall input,      active high */
  HC        /* Phase C Hall input,      active high */
/** Outputs  **/
  SW_GCOMP_L   /* Positive gain compensation switch control, active low */
  SW_NB_L      /* Switch control for negative B current, active low  */
  SW_NC_L      /* Switch control for negative C current, active low  */
  SW_PB_L      /* Switch control for positive B current, active low  */
  SW_PC_L      /* Switch control for positive C current, active low */
/** Equations  **/
/** Operator definition =>  ! = NOT, & = AND,  # = OR  **/
!SW_GCOMP_L = ( !HA)
!SW_NB_L = (HA & HB & !HC)
!SW_NC_L =( HA & !HB)
!SW_PB_L = (!HA & !HB & HC)
!SW_PC_L = (!HA & HB)
TABLE [HA,HB,HC] => [SW_GCOMP_L,SW_NA_L,SW_NC_L,SW_PA_L,SW_PC_L]
    'b'000 => 'b'   01111;
    'b'001 => 'b'   01101;
    'b'010 => 'b'   01110;
    'b'011 => 'b'   01110;
    'b'100 => 'b'   11011;
    'b'101 => 'b'   11011;
    'b'110 => 'b'   10111;
    'b'111 => 'b'   11111;
```

{ RS }, { RP }, { RN } AND Vref RELATIONSHIPS:

$$\frac{RS}{RP} = \frac{Vref}{6.924\ V} - \frac{1}{2}$$

$$\frac{RF}{RN} = \frac{6.924\ V}{2 \cdot Vref}$$

At Vref=4V	RF := 3.09·kΩ	RS := 1.07·kΩ
	RN := 3.57·kΩ	RP := 13.7·kΩ
At Vref=4.096V	RF := 4.75·kΩ	RS := 1.37·kΩ
	RN := 5.62·kΩ	RP := 15·kΩ
At Vref=5V	RF := 10.2·kΩ	RS := 2.55·kΩ
	RN := 14.7·kΩ	RP := 11.5·kΩ

FIGURE 9D. PW-8X075P6 CURRENT DECOMMUTATION CIRCUIT

ORDERING INFORMATION

PW - 8 X 075 PX - X X 0

Process Requirements:
- 0 = Standard DDC Procedures no Burn-In
- 2 = High Reliability Processing with Burn-In

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 3 = -0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data
- 9 = -55°C to 85°C

Voltage Rating
- 6 = 600V

Current Rating
- 075 = 75A

Features
- 3 = Standard ½ Bridge
- 4 = Standard ½ Bridge w/ current sense
- 5 = Standard ½ Bridge w/ regenerative voltage clamp

NOTES

NOTES

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Ireland - Tel: +353-21-341065, Fax: +353-21-341568
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany - Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
Sweden - Tel: +46-(0)8-54490044, Fax +46-(0)8-7550570
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