



Fast CMOS

Registered Transceivers

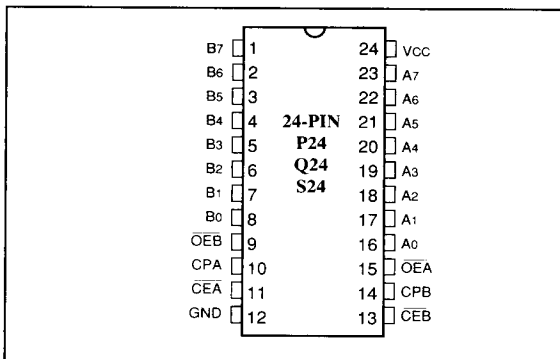
- PI74FCT2952/2953AT have the same speed and drive of Bipolar FAST™ "F" series, at CMOS power levels.
 - "B" speeds at 7.5 ns max.
 - "C" speeds at 6.3 ns max.
 - "D" speeds are an industry first, at 4.5 ns max.
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, $I_{OL} = 64 \text{ mA}$
- Extremely low static power (1 mW, typ.)
- Industry standard pinout, plug into existing "74F" sockets for speed enhancement at reduced power levels
- Hysteresis on all inputs
- Packaged in 24-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT2952T and the PI74FCT2953T are 8-bit registered transceivers designed with two 8-bit back-to-back registers to store data flowing in both directions between two bidirectional buses. Separate clock enable and 3-state output enable signals are provided for each register. The PI74FCT2952T is a non-inverting option of the PI74FCT2953T.

All products are available in three package types: 24-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

NOTE: PI74FCT2952T function is shown.

PI74FCT2952/2953T Product Pin Configuration

Product Pin Description

Pin Name	Description
A0-A7	A Register Inputs or B Register Outputs
B0-B7	B Register Inputs or A Register Outputs
CPA	Clock for A Register
CPB	Clock for B Register
OEA	Output Enable for B Register
OEB	Output Enable for A Register
CEA	Clock Enable for A Register
CEB	Clock Enable for B Register
GND	Ground
Vcc	Power

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PI74FCT2952/2953T Register Truth Table⁽¹⁾
(Applies to A or B Register)

Function	Inputs			Internal
	D _N	CP	CE	Q _N
Hold Data	X	X	H	NC
Load Data	L	↑	L	L
	H	↑	L	H

PI74FCT2952/2953T Output Control Table⁽¹⁾

Function	Internal		Y-Outputs	
	OE	Q _N	2952	2953
Disable Outputs	H	X	Z	Z
Enable Outputs	L	L	L	H
	L	H	H	L

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 NC = No Change
 ↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to Vcc
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = 0°C to +70°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -8.0 mA IOH = -15.0 mA	2.4	3.3		V
			2.0	3.0		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max., VIN = 2.7 V Except I/O Pins I/O Pins			5	μA
					15	μA
IIL	Input LOW Current	VCC = Max., VIN = 0.5 V Except I/O Pins I/O Pins			-5	μA
					-15	μA
II	Input HIGH Current	VCC = Max., VIN = VCC (Max.)			20	μA
VIK	Clamp Diode Voltage	VCC = Min., IIS = -18 mA		-0.7	-1.2	V
IOS	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5 V	—	—	100	μA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0 V	6	10	pF
COUT	Output Capacitance	VOUT = 0 V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.5	1.5	mA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4 V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OEA or OEB = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.0	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4 V V _{IN} = GND		2.5	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.3	7.8 ⁽⁵⁾	
			V _{IN} = 3.4 V V _{IN} = GND		6.5	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0 V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT2952T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT2952AT		FCT2952BT		FCT2952CT		FCT2952DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.5	ns
tPHL	CPA, CPB, to AN, BN										
tPZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	5.6	ns
tPZL	OEA, OEB, to AN, BN										
tPHZ	Output Disable Time		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.3	ns
tPLZ	OEA, OEB, to AN, BN										
tSU	Set-up Time HIGH or LOW, AN, BN to CPA, CPB		2.5	—	2.5	—	2.5	—	1.5	—	ns
tH	Hold Time HIGH or LOW, AN, BN to CPA, CPB		2.0	—	1.5	—	1.5	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0	—	3.0	—	3.0	—	2.0	—	ns	
tH	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0	—	2.0	—	2.0	—	1.0	—	ns	
tW	Pulse Width HIGH ⁽³⁾ or LOW, CPA or CPB	3.0	—	3.0	—	3.0	—	3.0	—	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT2953T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT2953AT		FCT2953BT		FCT2953CT		FCT2953DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
TP _{LH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.5	ns
TP _{HL}	CPA, CPB, to AN, BN										
TP _{ZH}	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	5.6	ns
TP _{ZL}	OEA, OEB, to AN, BN										
TP _{HZ}	Output Disable Time		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.3	ns
TP _{LZ}	OEA, OEB, to AN, BN										
TS _U	Set-up Time HIGH or LOW, AN, BN to CPA, CPB		2.5	—	2.5	—	2.5	—	2.0	—	ns
TH	Hold Time HIGH or LOW, AN, BN to CPA, CPB		2.0	—	1.5	—	1.5	—	1.0	—	ns
TS _U	Set-up Time HIGH or LOW, CEA, CEB to CPA, CPB	3.0	—	3.0	—	3.0	—	2.0	—	ns	
TH	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB	2.0	—	2.0	—	2.0	—	1.0	—	ns	
tw	Pulse Width HIGH ⁽³⁾ or LOW, CPA or CPB	3.0	—	3.0	—	3.0	—	3.0	—	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
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