19-4590; Rev 0; 4/09

EVALUATION KIT AVAILABLE

1-Phase Quick-PWM NVIDIA CPU Controller

MAX17409

General Description

The MAX17409 is a 1-phase Quick-PWM™ step-down VID power-supply controller for NVIDIA® graphics power. The Quick-PWM control provides instantaneous response to fast-load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17409 is intended for two different notebook processor core applications: either bucking down the battery directly to create the core voltage, or bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection.

The MAX17409 is available in a 28-pin, 4mm x 4mm TQFN package.

Applications

NVIDIA GPU Core Power Supplies

Voltage-Positioned Step-Down Converters

2-to-4 Li+ Cells Battery to Processor Core Supply Converters

Notebooks/Desktops/Servers

Features

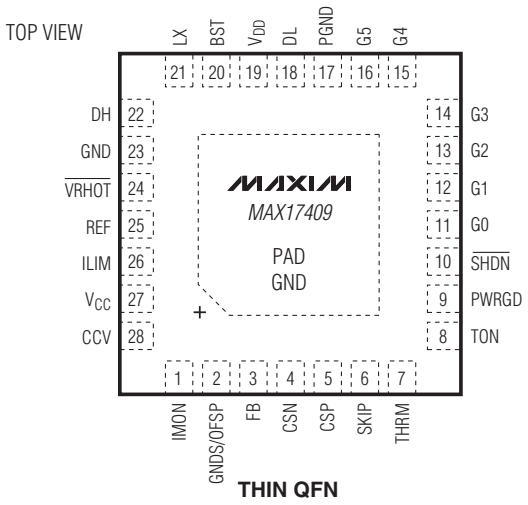
- ♦ 1-Phase Quick-PWM Controller
- ♦ ±6mV V_{OUT} Accuracy Over Line, Load, and Temperature
- ♦ 6-Bit Graphics DAC (12.5mV LSB)
- ♦ Active Voltage Positioning with Adjustable Gain
- ♦ Accurate Droop and Current Limit
- ♦ Remote Output and Ground Sense
- ♦ Buffered 2V Reference Output for Offsets
- ♦ Power-Good Window Comparator
- ♦ Temperature Comparator
- ♦ Drives Large Synchronous Rectifier FETs
- ♦ 2V to 26V Power Input Range
- ♦ Adjustable Switching Frequency (600kHz max)
- ♦ Output Overvoltage and Undervoltage Protection
- ♦ Soft-Startup and Soft-Shutdown
- ♦ Internal Boost Diodes

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17409GTI+	-40°C to +105°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



Quick-PWM is a trademark of Maxim Integrated Products, Inc.

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1-Phase Quick-PWM NVIDIA CPU Controller

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD} to GND .....-0.3V to +6V
G0–G5 to GND .....-0.3V to +6V
CSP, CSN to GND .....-0.3V to +6V
ILIM, THRM, $\overline{VRHOT}$, PWRGD to GND .....-0.3V to +6V
SKIP to GND .....-0.3V to +6V
CCV, FB, IMON, REF to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 1) .....-0.3V to +30V
TON to GND .....-0.3V to +30V
GNDS/OFSP, PGND to GND (Note 2) .....-0.3V to +0.3V
Internal Driver (Note 2)
DL to PGND .....-0.3V to (V_{DD} + 0.3V)
BST to GND .....-0.3V to +36V
LX to BST .....-6V to +0.3V
BST to V_{DD} .....-0.3V to +30V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin 4mm x 4mm TQFN
(derate 21.3mW/°C above +70°C) 1702mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ might be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode, which disables fault protection.

Note 2: Measurements valid using a 20MHz bandwidth limit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
DC Output-Voltage Accuracy		Measured at FB with respect to GNDS; includes load-regulation error (Note 4)		-6		+6	mV
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
GNDS Input Range				-200		+200	mV
GNDS/OFSP Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.97	1.00	1.03	V/V
GNDS/OFSP Input Bias Current	I_{GNDS}			-2		+2	µA
REF Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 100µA		1.98	2.000	2.02	V
		I_{REF} = 0 to 1mA		1.97	2.000	2.02	
Dynamic VID Slew-Rate Accuracy				11.0	12.5	14.0	mV/µs
Soft-Start/Soft-Shutdown Slew-Rate Accuracy				1.248	1.56	1.872	mV/µs
On-Time (Note 5)	t_{ON}	V_{IN} = 12V, V_{FB} = 1.2V	R_{TON} = 96.75kΩ	142	167	192	ns
			R_{TON} = 200kΩ	300	333	366	
			R_{TON} = 303.25kΩ	425	500	575	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH (Note 5)			300	375	ns
TON Shutdown Input Current		$\overline{SHDN}$ = GND, V_{IN} = 26V, V_{CC} = V_{DD} = 0 or 5V			0.01	0.1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, SKIP = 5V, FB forced above the regulation point			1.5	3	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, SKIP = 0V, FB forced above the regulation point, T_A = +25°C			0.02	1	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
FAULT PROTECTION							
Output Overvoltage Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to unloaded output voltage		250	300	350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB		1.45	1.50	1.55	V
		Minimum OVP threshold; measured at FB			0.8		
Output Overvoltage Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold			10		µs
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		-450	-400	-350	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{SHDN}$ goes high		3	5	8	ms
PWRGD Threshold		Measured at FB with respect to unloaded output voltage, 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD Transition Blanking Time	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 4) based on the slew rate			20		µs
PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
PWRGD Output Low Voltage		I_{SINK} = 3mA				0.4	V
PWRGD Leakage Current		High state, PWRGD forced to 5V				1	µA
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV typical hysteresis, controller disabled below this level		4.05	4.25	4.48	V
CSN Discharge Resistance in UVLO		V_{CC} = V_{DD} = 4.0V			8		Ω

1-Phase Quick-PWM NVIDIA CPU Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL COMPARATOR AND PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge; typical hysteresis = 100mV		29.2	30	30.8	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold; falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{\overline{VRHOT}}$	Low state			2	8	Ω
$\overline{VRHOT}$ Leakage Current	$I_{\overline{VRHOT}}$	High state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage	I_{THRM}	V_{THRM} = 0 to 5V, T_A = +25°C		-100		+100	nA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			160		°C
VALLEY CURRENT LIMIT AND DROOP							
Current-Limit Threshold Voltage (Positive Adjustable)	V_{LIMIT}	V_{CSP} - V_{CSN}	V_{REF} - V_{ILIM} = 100mV	7	10	13	mV
			V_{REF} - V_{ILIM} = 500mV	45	50	55	
Current-Limit Threshold Voltage (Positive Default)		ILIM = V_{CC}, V_{CSP} - V_{CSN}		20	22.5	25	mV
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	V_{CSP} - V_{CSN}, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{PGND} - V_{LX}			1		mV
CSP, CSN Common-Mode Input Range				0		1.9	V
CSP, CSN Input Current		T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current		T_A = +25°C		-100		+100	nA
Droop Amplifier (GMD) Offset		(V_{CSP} - V_{CSN}) at I_{FB} = 0		-0.75		+0.75	mV
Droop Amplifier (GMD) Transconductance		$\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; FB = CSN = 0.45V to 2.0V, and (V_{CSP} - V_{CSN}) = -15.0mV to +15.0mV		592	600	608	µS
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.7	
DH Gate-Driver Source Current	$I_{DH(SOURCE)}$	DH forced to 2.5V, BST - LX forced to 5V			2.2		A
DH Gate-Driver Sink Current	$I_{DH(SINK)}$	DH forced to 2.5V, BST - LX forced to 5V			2.7		A
DL Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL forced to 2.5V			2.7		A
DL Gate-Driver Sink Current	$I_{DL(SINK)}$	DL forced to 2.5V			8		A
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V			10	20	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT MONITOR						
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta(V_{CSP} - V_{CSN})$, V_{CSN} = 0.5V to 1.0V	4.9	5.0	51	mS
Current-Monitor Offset Referred to V(CSP,CSN)		I_{IMON} = 0	-1.0		+1.0	mV
IMON Clamp Voltage	V_{IMON}	I_{IMON} = -1.0mA	1.05	1.10	1.15	V
LOGIC AND I/O						
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, SKIP	2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, SKIP			1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	G0–G5	0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	G0–G5			0.33	V
Logic-Input Current		T_A = +25°C, $\overline{SHDN}$, SKIP, G0–G5 = 0 or 5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
DC Output-Voltage Accuracy		Measured at FB with respect to GNDS, includes load regulation error (Note 4)		-10		+10	mV
GNDS Input Range		For positive offset and remote-sense errors		-200		+200	mV
GNDS/OFSP Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.95		1.05	V/V
REF Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 100µA		1.97		2.03	V
		I_{REF} = 0 to 1mA		1.95		2.03	
Dynamic VID Slew-Rate Accuracy				10		15	mV/µs
Soft-Start/Soft-Shutdown Slew-Rate Accuracy				1.248		1.872	mV/µs
On-Time (Note 5)	t_{ON}	V_{IN} = 12V, V_{FB} = 1.2V	R_{TON} = 96.75kΩ	142		192	ns
			R_{TON} = 200kΩ	300		366	
			R_{TON} = 303.25kΩ	425		575	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH (Note 5)				400	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, SKIP = 5V, FB forced above the regulation point				3	mA

1-Phase Quick-PWM NVIDIA CPU Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to unloaded output voltage		250		350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage, measured at FB		1.45		1.55	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		-450		-350	mV
PWRGD Startup Delay		Measured at startup from the time when $\overline{SHDN}$ goes high		3		8	ms
PWRGD Threshold		Measured at FB with respect to unloaded output voltage; 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	mV
PWRGD Output Low Voltage		I_{SINK} = 3mA				0.4	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV typical hysteresis, controller disabled below this level		4.0		4.5	V
THERMAL COMPARATOR AND PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge; typical hysteresis = 100mV		29.2		30.8	%
$\overline{VRHOT}$ Output On-Resistance	$R_{\overline{VRHOT}}$	Low state				8	Ω
VALLEY CURRENT LIMIT AND DROOP							
Current-Limit Threshold Voltage (Positive Adjustable)	V_{LIMIT}	V_{CSP} - V_{CSN}	V_{REF} - V_{ILIM} = 100mV	7		13	mV
			V_{REF} - V_{ILIM} = 500mV	45		55	
Current-Limit Threshold Voltage (Positive Default)		ILIM = V_{CC}, V_{CSP} - V_{CSN}		20		25	mV
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	V_{CSP} - V_{CSN}, nominally -125% of V_{LIMIT}		-5		+5	mV
CSP, CSN Common-Mode Input Range				0		1.9	V
Droop Amplifier GMD) Offset		(V_{CSP} - V_{CSN}) at I_{FB} = 0		-1.0		+1.0	mV
Droop Amplifier (GMD) Transconductance		$\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; FB = CSN = 0.45V to 2.0V, and (V_{CSP} - V_{CSN}) = -15.0mV to +15.0mV		588		612	µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SHDN}$ = ILIM = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.05V; G5–G0 set for 1.05V (G0–G5 = 100110); **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.7	
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V				20	Ω
CURRENT MONITOR							
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta(V_{CSP} - V_{CSN})$ V_{CSN} = 0.5V to 1.0V		4.9		5.1	mS
Current-Monitor Offset Referred to V(CSP,CSN)		I_{IMON} = 0		-1.0		+1.0	mV
IMON Clamp Voltage	V_{IMON}	I_{IMON} = -1.0mA		1.05		1.15	V
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, SKIP		2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, SKIP				1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	G0–G5		0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	G0–G5				0.33	V

Note 3: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

Note 4: The equation for the target voltage V_{TARGET} is:
V_{TARGET} = the slew-rate-controlled version of V_{DAC}, where V_{DAC} = 0 for shutdown, V_{DAC} = V_{VID} otherwise (the V_{VID} voltages for all possible VID codes are given in Table 4).
In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

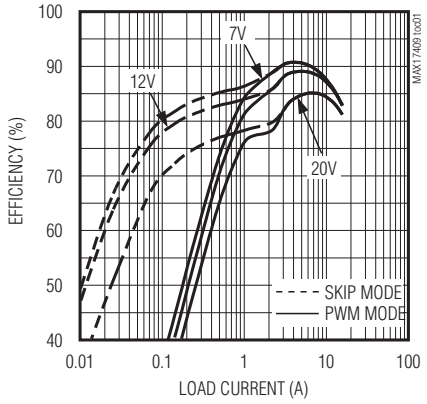
Note 5: On-time and minimum off-time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0V, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

1-Phase Quick-PWM NVIDIA CPU Controller

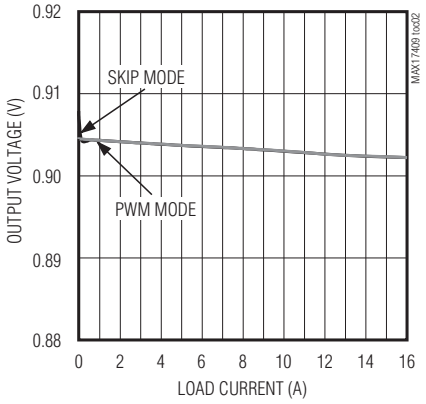
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, G0–G5 set for 1.05V (G0–G5 = 100110), T_A = +25°C, unless otherwise specified.)

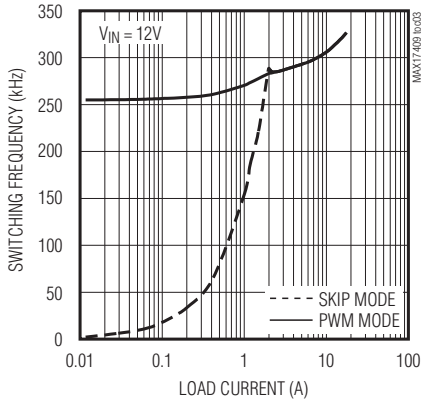
0.9V OUTPUT EFFICIENCY vs. LOAD CURRENT



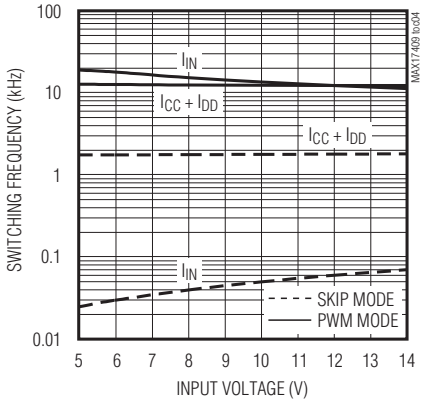
0.9V OUTPUT VOLTAGE vs. LOAD CURRENT



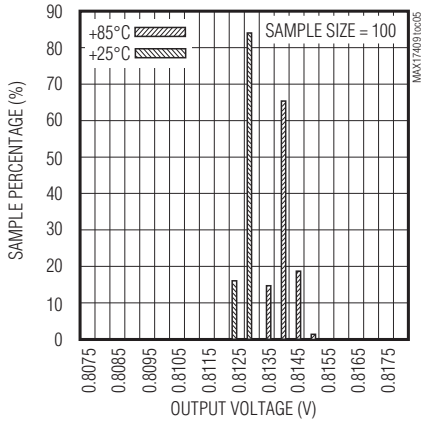
SWITCHING FREQUENCY vs. LOAD CURRENT



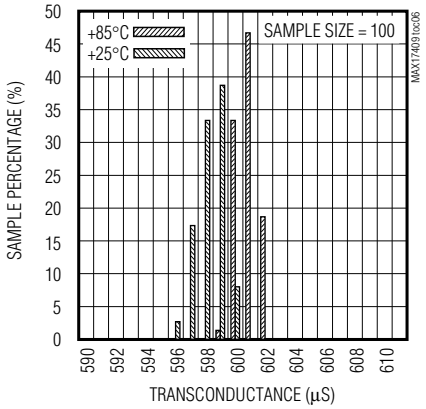
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



0.8125V OUTPUT VOLTAGE DISTRIBUTION



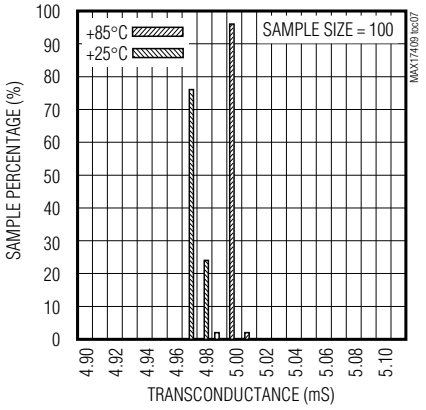
Gm(FB) TRANSCONDUCTANCE DISTRIBUTION



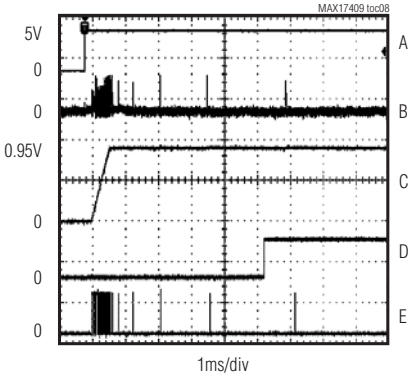
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, G0–G5 set for 1.05V (G0–G5 = 100110), T_A = +25°C, unless otherwise specified.)

Gm(IMON) TRANSCONDUCTANCE DISTRIBUTION

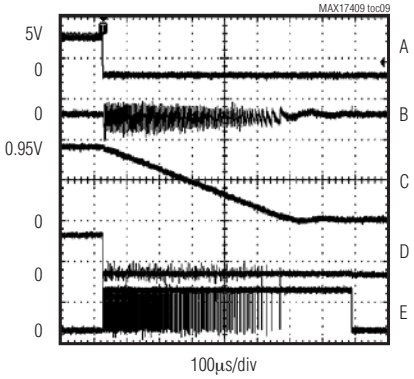


SOFT-START WAVEFORM



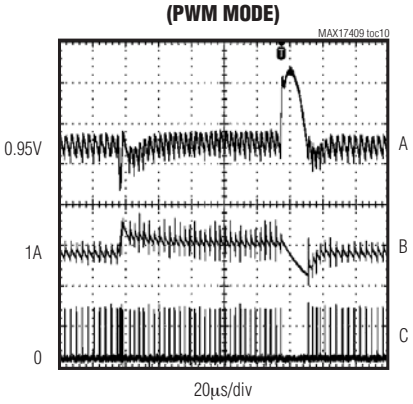
A. $\overline{SHDN}$, 5V/div
B. I_{LX}, 10A/div
C. V_{OUT}, 500mV/div
D. PWRGD, 5V/div
E. DL, 5V/div
I_{OUT} = 0A, SKIP MODE

SOFT-SHUTDOWN WAVEFORM



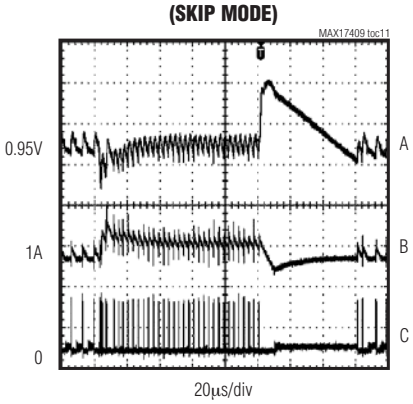
A. $\overline{SHDN}$, 5V/div
B. I_{LX}, 10A/div
C. V_{OUT}, 500mV/div
D. PWRGD, 5V/div
E. DL, 5V/div
I_{OUT} = 0A, SKIP MODE

LOAD-TRANSIENT RESPONSE (PWM MODE)



A. V_{OUT}, 50mV/div
B. I_{LX}, 20A/div
C. LX, 10V/div
I_{OUT} = 1A - 11A

LOAD-TRANSIENT RESPONSE (SKIP MODE)



A. V_{OUT}, 50mV/div
B. I_{LX}, 20A/div
C. LX, 10V/div
I_{OUT} = 1A - 11A

1-Phase Quick-PWM NVIDIA CPU Controller

Pin Description

PIN	NAME	FUNCTION
1	IMON	Current Monitor Output. The MAX17409 IMON output sources a current that is directly proportional to the current-sense voltage as defined by: $I_{IMON} = G_{m(IMON)} \times (V_{CSP} - V_{CSN})$ where $G_{m(IMON)}$ = 5mS (typ). The IMON current is unidirectional (sources current out of IMON only) for positive current-sense values. For negative current-sense voltages, the IMON current is zero. Connect an external resistor between IMON and GNDS to create the desired IMON gain based on the following equation: $R_{IMON} = 1.0V/(I_{LOAD(MAX)} \times R_{SENSE} \times G_{m(IMON)})$ where $I_{LOAD(MAX)}$ is the maximum load current, and R_{SENSE} is the current-sense voltage. The IMON voltage is internally clamped to 1.1V. The transconductance amplifier and voltage clamp are internally compensated, so IMON cannot drive large external capacitance values. To filter the IMON signal, use an RC filter as shown in Figure 1.
2	GNDS/OFSP	Remote Ground-Sense Input/Positive Offset Input. Connect directly to the ground-sense pin or ground connection of the load. GNDS internally connects to a transconductance amplifier that adjusts the feedback voltage—compensating for voltage drops between the regulator's ground and the processor's ground.
3	FB	Remote-Sense Feedback Input and Voltage-Positioning Transconductance Amplifier Output. Connect resistor R_{FB} between FB and the output remote-sense pin (or Kelvin-sensed to the supply pin of the load) for best accuracy and to set the steady-state droop based on the voltage-positioning gain requirement: $R_{FB} = R_{DROOP}/(R_{SENSE} \times G_{MD})$ where R_{DROOP_DC} is the desired voltage-positioning slope, G_{MD} = 600µS (typ), and R_{SENSE} is the current-sense resistance with respect to CSP to CSN current-sense inputs. See the *Current Sense* section for details on designing with sense resistors or inductor DCR sensing. Shorting FB directly to the output effectively disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FB enters a high-impedance state in shutdown.
4	CSN	Negative Inductor Current-Sense Input. Connect CSN to the negative terminal of the inductor current-sensing resistor or directly to the negative terminal of the inductor if the lossless DCR sensing method is used (see Figure 3).
5	CSP	Positive Inductor Current-Sense Input. Connect CSP to the positive terminal of the inductor current-sensing resistor or directly to the positive terminal of the filtering capacitor used when the lossless DCR sensing method is used (see Figure 3).
6	SKIP	Pulse-Skipping Control Input. The SKIP signal indicates the power usage and sets the operating mode of the MAX17409. When the system forces SKIP high, the MAX17409 immediately enters automatic pulse-skipping mode. The controller returns to continuous forced-PWM mode when SKIP is pulled low **and** the output is in regulation. SKIP determines the operating mode and output-voltage transition slew rate as shown in the truth table below: SKIP — Functionality 0 — Normal slew rate, forced-PWM mode 1 — Normal slew rate, skip mode The SKIP state is ignored during soft-start and shutdown. The MAX17409 always uses pulse-skipping mode during startup to ensure a monotonic power-up. During shutdown, the controller always uses forced-PWM mode so the output can be actively discharged.

Pin Description (continued)

PIN	NAME	FUNCTION
7	THRM	Comparator Input for Thermal Protection. THRM connects to the positive input of an internal comparator. The comparator's negative input connects to an internal resistive voltage-divider that accurately sets the THRM threshold to 30% of the V_{CC} voltage. Connect the output of a resistor-divider and thermistor-divider (between V_{CC} and GND) to THRM with the values selected so the voltage at THRM falls below 30% of V_{CC} (1.5V when V_{CC} = 5V) at the desired high temperature.
8	TON	Switching Frequency-Setting Input. An external resistor (R_{TON}) between the input power source and TON sets the switching frequency ($f_{SW} = 1/t_{SW}$) according to the following equation used to determine the nominal switching period: $t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$ TON enters a high impedance in shutdown to reduce the input quiescent current. If the TON current is less than 10µA, the MAX17409 disables the controller, sets the TON OPEN fault latch, and pulls DH and DL low.
9	PWRGD	Open-Drain Power-Good Output. The MAX17409 forces PWRGD low when $\overline{SHDN}$ is pulled low. After the controller is properly powered up, PWRGD becomes a high-impedance output as long as the feedback voltage is in regulation and the startup blanking time has expired. PWRGD becomes active 5ms after the MAX17409 reaches the VID target. The MAX17409 pulls PWRGD low when shutdown ($\overline{SHDN}$ = GND) is pulled low, during startup, and during shutdown transitions. The PWRGD upper threshold is blanked during any downward output-voltage transition that occurs when the MAX17409 is in skip mode (SKIP = V_{CC}). PWRGD remains blanked until the transition-related PWRGD blanking period expires **and** the controller detects the output is in regulation (error-amplifier edge occurs). **Note:** The pullup resistance on PWRGD causes additional shutdown current.
10	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the controller into the low-power 1µA (max) shutdown state. During startup, the controller ramps up the output voltage with a 1.56mV/µs slew rate to the selected target voltage. During the shutdown transition, the MAX17409 softly ramps down the output voltage with a 1.56mV/µs slew rate. Forcing $\overline{SHDN}$ to 11V ~ 13V disables overvoltage protection, undervoltage protection, and thermal shutdown, and clears the fault latches.
11–16	G0–G5	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The G0–G5 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the µP. The output voltage is set by the DAC code indicated by the logic-level voltages on G0–G5.
17	PGND	Power Ground. Ground connection for the DL driver.
18	DL	Low-Side Gate-Driver Output. DL swings from V_{DD} to PGND. DL is forced low in shutdown. DL is also forced low when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL is forced low in skip mode after detecting an inductor current zero crossing.
19	V_{DD}	Driver-Supply Voltage Input. V_{DD} supplies power to the low-side gate driver (DL) and to the internal BST switch used to refresh the BST capacitor. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to PGND with a 1µF or greater ceramic capacitor.
20	BST	Boost Flying Capacitor Connection. BST provides the upper supply rail for the DH high-side gate driver. An internal switch between V_{DD} and BST charges the flying capacitor while the low-side MOSFET is on (DL pulled high and LX pulled to ground).
21	LX	Inductor Connection. LX serves as the lower supply rail for the DH high-side gate driver. The MAX17409 also uses LX as the input to the zero-crossing comparator.

1-Phase Quick-PWM NVIDIA CPU Controller

Pin Description (continued)

PIN	NAME	FUNCTION
22	DH	High-Side Gate-Driver Output. DH swings from LX to BST. The controller pulls DH low in shutdown.
23	GND	Analog Ground. Internally connected to GND.
24	$\overline{VRHOT}$	Thermal Comparator's Open-Drain Output. The comparator pulls $\overline{VRHOT}$ low when the voltage at THRM drops below 30% of V_{CC} (1.5V with 5V V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.
25	REF	Buffered 2V Reference Output. Bypass REF with a 100pF to 1000pF capacitor. Do not exceed 1000pF.
26	ILIM	Valley Current-Limit Adjustment Input. The valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential REF to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). The negative current-limit threshold is nominally -125% of the corresponding valley current-limit threshold. Connect ILIM directly to V_{CC} to set the default 22.5mV current-limit threshold setting.
27	V_{CC}	Analog Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with a 1µF minimum capacitor.
28	CCV	Integrator Capacitor Connection. Connect a capacitor (C_{CCV}) from CCV to GND to set the integration time constant. Choose the capacitor value according to: $16\pi \times [C_{CCV}/G_{m(CCV)}] \times f_{SW} >> 1$ where $G_{m(CCV)}$ = 320µS (max) is the integrator's transconductance and f_{SW} is the switching frequency set by the R_{TON} resistance. The integrator is internally disabled during any downward output-voltage transition that occurs in pulse-skipping mode, and remains disabled until the transition blanking period expires **and** the output reaches regulation (error-amplifier transition detected).
—	EP	Exposed Pad (Backside). Internally connected to the substrate. Connect to the ground plane through a thermally enhanced via.

1-Phase Quick-PWM NVIDIA CPU Controller

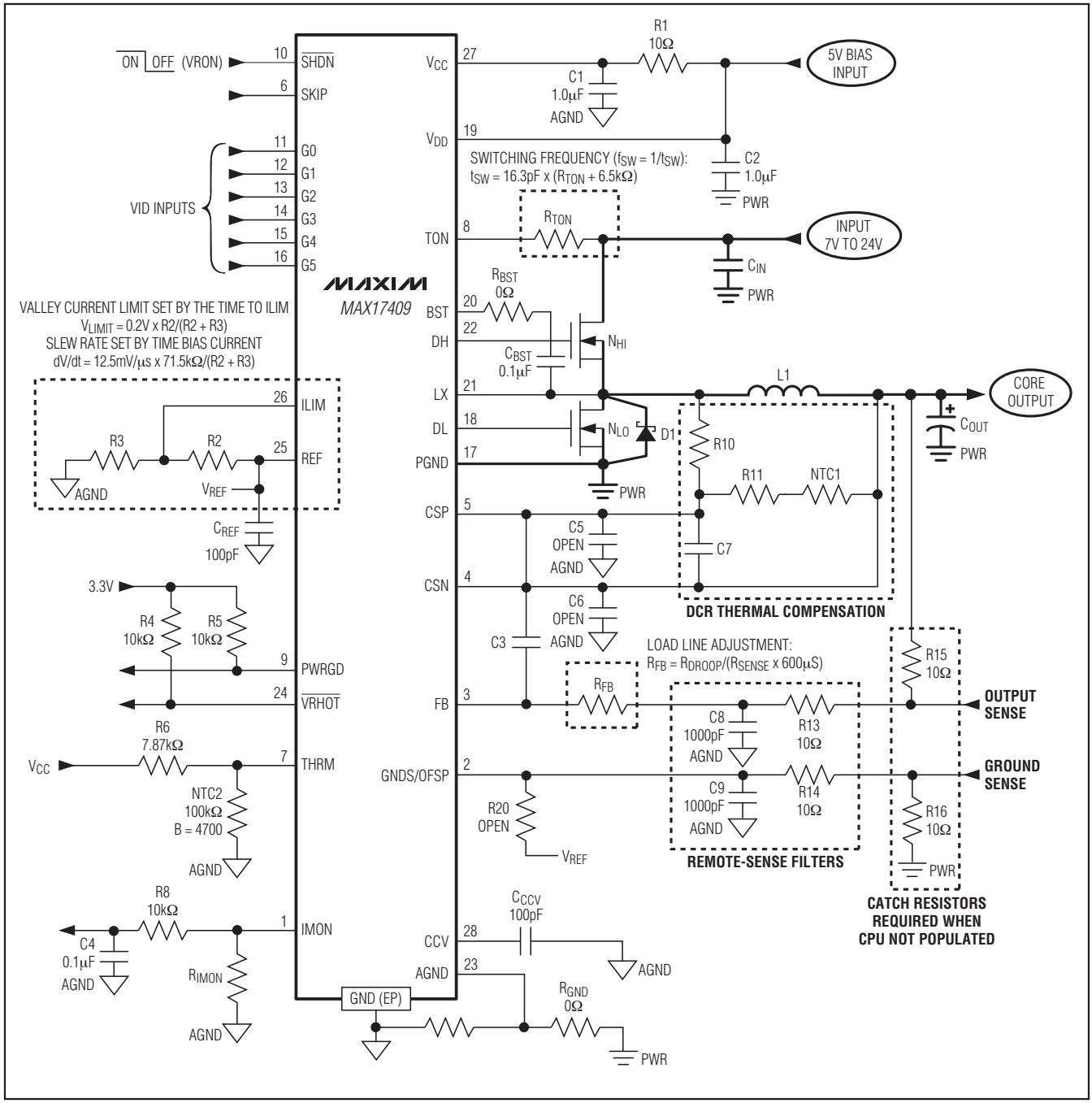


Figure 1. MAX17409 Application Circuit

1-Phase Quick-PWM NVIDIA CPU Controller

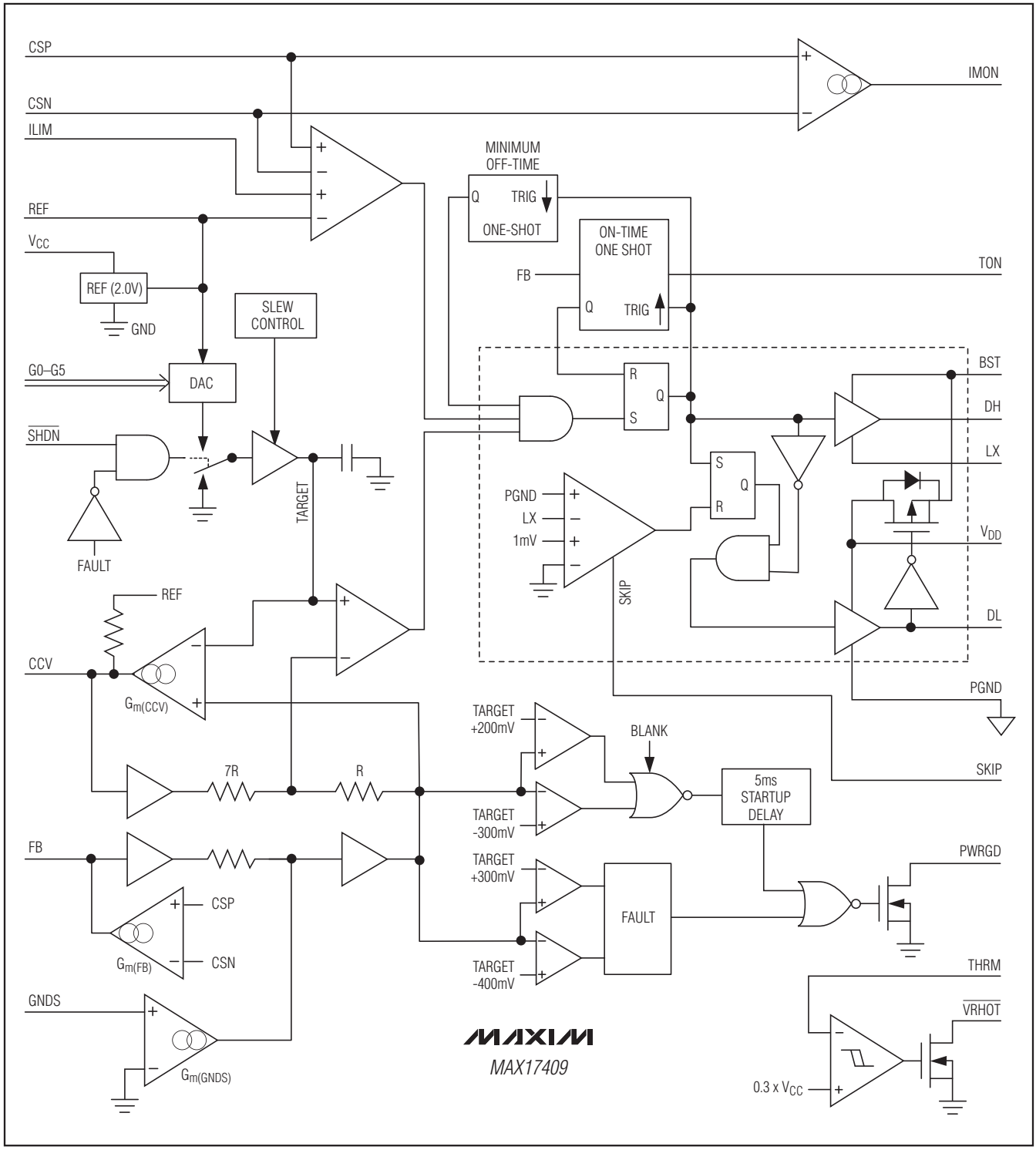


Figure 2. Functional Diagram

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	14A DESIGN	9A DESIGN	5A DESIGN
Input Voltage Range	8V to 20V	8V to 20V	8V to 20V
Maximum Load Current	14A	9A	5A
Transient Load Current	10A	7A	4A
COMPONENTS			
TON Resistance (R_{TON})	200kΩ (f_{SW} = 300kHz)	170kΩ (f_{SW} = 350kHz)	150kΩ (f_{SW} = 390kHz)
Inductance (L1)	0.6µH, 17A, 2.3mΩ NEC-TOKIN MPC0750LR60C	0.75µH, 10.7A, 6.2mΩ TOKO FDVE0630-R75M	1.50µH, 8A, 12.1mΩ TOKO FDVE0630-1R5M
High-Side MOSFET (N_{HI})	9.4mΩ/12.0mΩ (typ/max) Fairchild FDS6298	11mΩ/13.75mΩ (typ/max) Vishay Si7392DP	14.5mΩ/20.5mΩ (typ/max) International Rectifier IRF7904
Low-Side MOSFET (N_{LO})	4.2mΩ/5.0mΩ (typ/max) Fairchild FDS8670	5mΩ/6.5mΩ (typ/max) International Rectifier IRF7822	10mΩ/13mΩ (typ/max) International Rectifier IRF7904
Output Capacitors (C_{OUT})	1x 470µF, 6mΩ, 2V SANYO 2TPE470M6	1x 330µF, 6mΩ, 2V SANYO 2TPE330M6	1x 220µF, 6mΩ, 2V SANYO 2TPE220M6
Input Capacitors (C_{IN})	2x 10µF, 25V ceramic (1210)	1x 10µF, 25V ceramic (1210)	1x 10µF, 25V ceramic (1210)
REF/ILIM Resistance (R2)	10kΩ	17.8kΩ	20kΩ
ILIM/GND Resistance (R3)	63.4kΩ	60.4kΩ	54.9kΩ
FB Resistance (R_{FB})	100Ω	100Ω	100Ω
Feedforward Capacitance (C3)	0.22µF	0.15µF	0.1µF
LX/CSP Resistance (R10)	1.3kΩ	1.3kΩ	1.3kΩ
CSP/CSN Series Resistance (R11 + NTC1)	2kΩ + 10kΩ NTC (B = 3380)	2kΩ + 10kΩ NTC (B = 3380)	2kΩ + 10Ω NTC (B = 3380)
DCR Sense Capacitance (C7)	0.22µF, 6V ceramic (0603)	0.1µF, 6V ceramic (0603)	0.1µF, 6V ceramic (0603)
IMON Resistance (R_{IMON})	6.81kΩ	3.92kΩ	3.24kΩ

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corporation	www.avxcorp.com
Fairchild Semiconductor	www.fairchildsemi.com
NEC-TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
SANYO Electric Co., Ltd.	www.sanyodevice.com

MANUFACTURER	WEBSITE
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec
Vishay	www.vishay.com

1-Phase Quick-PWM NVIDIA CPU Controller

Detailed Description

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current is below the valley current-limit threshold, and the minimum off-time one-shot times out.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period ($t_{SW} = 1/f_{SW}$):

$$t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively.

High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

On-Time One-Shot

The core contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the R_{TON} input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{t_{SW}\left(V_{FB} + 0.075V\right)}{V_{IN}}$$

where the switching period ($t_{SW} = 1/f_{SW}$) is set by the resistor at the TON pin and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

This algorithm results in a nearly constant switching frequency and balanced inductor currents despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output-voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PCB copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output-voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the

on-time by a period equal to the DH rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The output current is differentially sensed by the high-impedance current-sense inputs (CSP and CSN). Low-offset amplifiers are used for voltage-positioning gain, current-limit protection, and power monitoring. Sensing the current at the output offers advantages, including less noise sensitivity and the flexibility to use either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the inductor (see Figure 3). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements, and the time constant of the RC network should match the inductor's time constant (L/R_{CS}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current (I_{CSP} and I_{CSN}), choose R1//R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 3). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method above, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, C_{EQ} and R1 are the time-constant matching components.

Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that uses current-sense inputs (CSP to CSN) as the current-sensing elements. If the current-sense signal exceeds the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current drops below the valley current-limit threshold.

Since only the valley current level is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

The positive current-limit threshold is fixed internally at 22.5mV (typ). There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is 130% of the nominal valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP, CSN).

1-Phase Quick-PWM NVIDIA CPU Controller

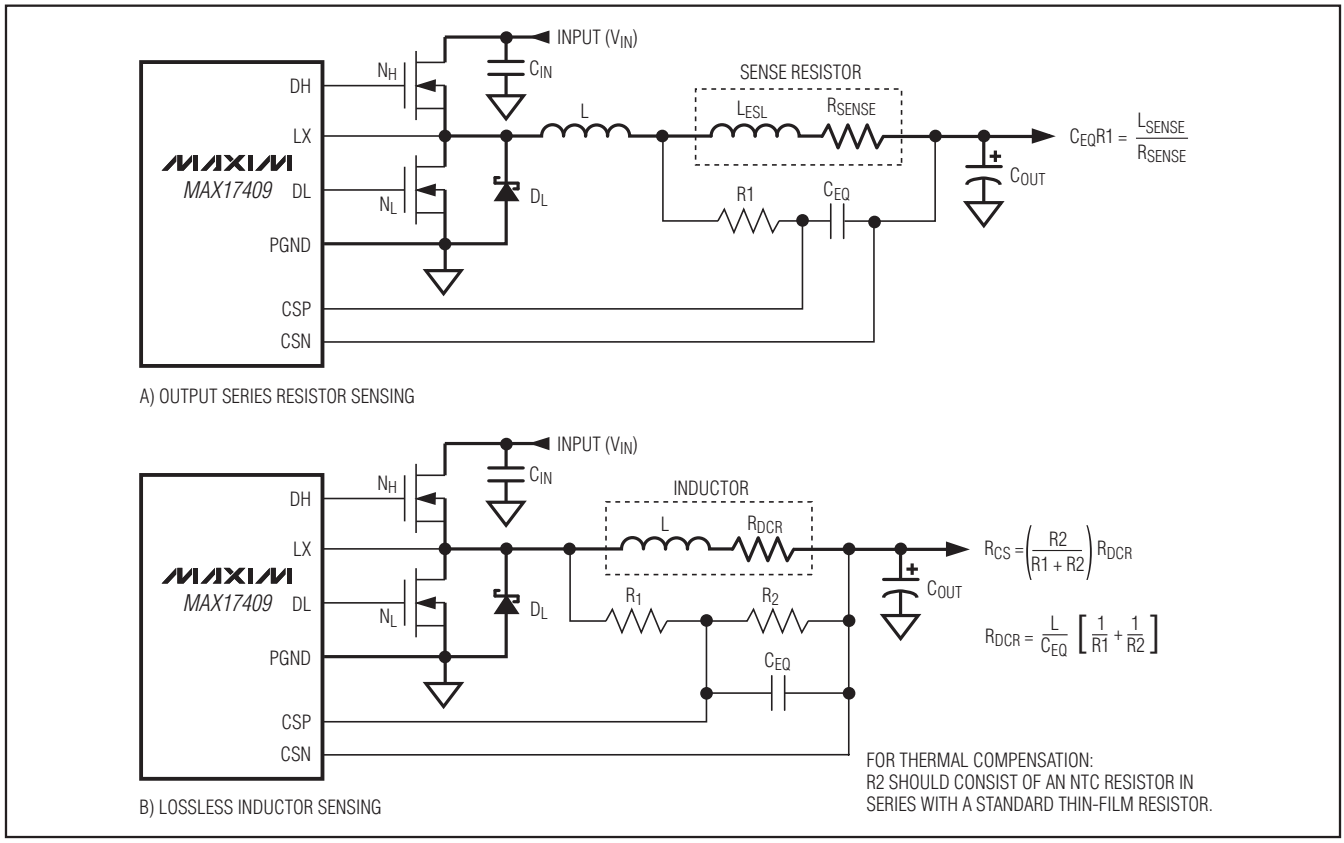


Figure 3. Current-Sense Methods

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State DC Droop)

The MAX17409 includes a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by the differential current-sense inputs, which sense the inductor current by measuring the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the current-sense voltages:

$$I_{FB} = G_{m(FB)} \times (V_{CSP} - V_{CSN})$$

where $V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 600µS, as defined in the *Electrical Characteristics* table.

Differential Remote Sense

The MAX17409 includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}) and ground-sense (GNDS) input directly to the processor's remote-sense outputs as shown in Figure 1.

Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage

(Figure 2), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±80mV (typ). The differential input voltage range is at least ±60mV total, including DC offset and AC ripple. The integration time constant can be set easily with an external compensation capacitor between CCV and analog ground, with the minimum recommended CCV capacitor value determined by:

$$C_{CCV} >> \frac{G_{m(CCV)}}{16\pi \times f_{SW}}$$

where $G_{m(CCV)}$ is the integrator's maximum transconductance (320µs) and f_{SW} is the switching frequency set by the TON resistance.

The MAX17409 disables the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (SKIP = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Nominal Output-Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX17409 slews the target voltage from ground to the selected VID voltage.

DAC Inputs (G0–G5)

The digital-to-analog converter (DAC) programs the output voltage using the G0–G5 inputs. G0–G5 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave G0–G5 unconnected. Changing G0–G5 initiates a transition to a new output-voltage level. Change G0–G5 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings could cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time (Table 4).

Table 3. MAX17409 Operating Mode Truth Table

$\overline{SHDN}$	SKIP	OPERATING MODE	DESCRIPTION
GND	X	DISABLED	Low-Power Shutdown Mode. DL forced low, and the controller is disabled. The supply current drops to 10µA (max).
Rising	X	Pulse-Skipping 1.56mV/µs Slew Rate	Startup. When $\overline{SHDN}$ is pulled high, the MAX17409 begins the startup sequence. The controller enables the PWM controller and ramps the output voltage up to the selected VID voltage.
High	Low	Forced-PWM 12.5mV/µs Slew Rate	Full Power. The no-load output voltage is determined by the selected VID DAC code (G0–G5, Table 4).
High	High	Pulse-Skipping 12.5mV/µs Slew Rate	Suspend Mode. The no-load output voltage is determined by the selected VID DAC code (G0–G5, Table 4). When SKIP is pulled high, the MAX17409 immediately enters pulse-skipping operation, allowing automatic PWM/PFM switchover under light loads. The PWRGD upper threshold is blanked during the transition.
Falling	X	Forced-PWM 1.56mV/µs Slew Rate	Shutdown. When $\overline{SHDN}$ is pulled low, the MAX17409 immediately pulls PWRGD low, and the output voltage is ramped down to ground. Once the output reaches 0V, the controller enters the low-power shutdown state.
High	X	DISABLED	Fault Mode. The fault latch has been set by the MAX17409 UVP or thermal-shutdown protection, or by the OVP protection. The controller remains in fault mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

1-Phase Quick-PWM NVIDIA CPU Controller

Table 4. Output Voltage VID DAC Codes

G5	G4	G3	G2	G1	G0	OUTPUT VOLTAGE (V)
1	0	0	0	0	0	1.1250
1	0	0	0	0	1	1.1125
1	0	0	0	1	0	1.1000
1	0	0	0	1	1	1.0875
1	0	0	1	0	0	1.0750
1	0	0	1	0	1	1.0675
1	0	0	1	1	0	1.0500
1	0	0	1	1	1	1.0375
1	0	1	0	0	0	1.0250
1	0	1	0	0	1	1.0125
1	0	1	0	1	0	1.0000
1	0	1	0	1	1	0.9875
1	0	1	1	0	0	0.9750
1	0	1	1	0	1	0.9625
1	0	1	1	1	0	0.9500
1	0	1	1	1	1	0.9275
1	1	0	0	0	0	0.9250
1	1	0	0	0	1	0.9125
1	1	0	0	1	0	0.9000
1	1	0	0	1	1	0.8875
1	1	0	1	0	0	0.8750
1	1	0	1	0	1	0.8625
1	1	0	1	1	0	0.8500
1	1	0	1	1	1	0.8375
1	1	1	0	0	0	0.8250
1	1	1	0	0	1	0.8125
1	1	1	0	1	0	0.8000
1	1	1	0	1	1	0.7875
1	1	1	1	0	0	0.7750
1	1	1	1	0	1	0.7625
1	1	1	1	1	0	0.7500
1	1	1	1	1	1	0.7375

G5	G4	G3	G2	G1	G0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	0.7250
0	0	0	0	0	1	0.7125
0	0	0	0	1	0	0.7000
0	0	0	0	1	1	0.6875
0	0	0	1	0	0	0.6750
0	0	0	1	0	1	0.6625
0	0	0	1	1	0	0.6500
0	0	0	1	1	1	0.6275
0	0	1	0	0	0	0.6250
0	0	1	0	0	1	0.6125
0	0	1	0	1	0	0.6000
0	0	1	0	1	1	0.5875
0	0	1	1	0	0	0.5750
0	0	1	1	0	1	0.5625
0	0	1	1	1	0	0.5500
0	0	1	1	1	1	0.5275
0	1	0	0	0	0	0.5250
0	1	0	0	0	1	0.5125
0	1	0	0	1	0	0.5000
0	1	0	0	1	1	0.4875
0	1	0	1	0	0	0.4750
0	1	0	1	0	1	0.4625
0	1	0	1	1	0	0.4500
0	1	0	1	1	1	0.4275
0	1	1	0	0	0	0.4250
0	1	1	0	0	1	0.4125
0	1	1	0	1	0	0.4000
0	1	1	0	1	1	0.3875
0	1	1	1	0	0	0.3750
0	1	1	1	0	1	0.3625
0	1	1	1	1	0	0.3500
0	1	1	1	1	1	0.3375

Output-Voltage Transition Timing

The MAX17409 performs mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output-voltage transition, the MAX17409 blanks both PWRGD thresholds, preventing the PWRGD open-drain output from changing states during the transition. The controller enables the PWRGD thresholds approximately 20µs after the slew-rate controller reaches the target output voltage. The slew rate is set to 12.5mV/µs to ensure that the transition can be completed within a reasonable time period.

The MAX17409 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current source to transition the target voltage. The total transition time depends on the 12.5mV/µs slew rate, the voltage difference, and the accuracy of the slew-rate controller, C_{SLEW}, accuracy).

The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For all dynamic VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{12.5mV/\mu s}$$

where V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See Slew-Rate Accuracy in the *Electrical Characteristics* for slew-rate limits. For soft-start and shutdown, the controller automatically reduces the slew rate to 1.56mV/µs (1/8 of the nominal slew rate).

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times 12.5mV/\mu s$$

where C_{OUT} is the total output capacitance.

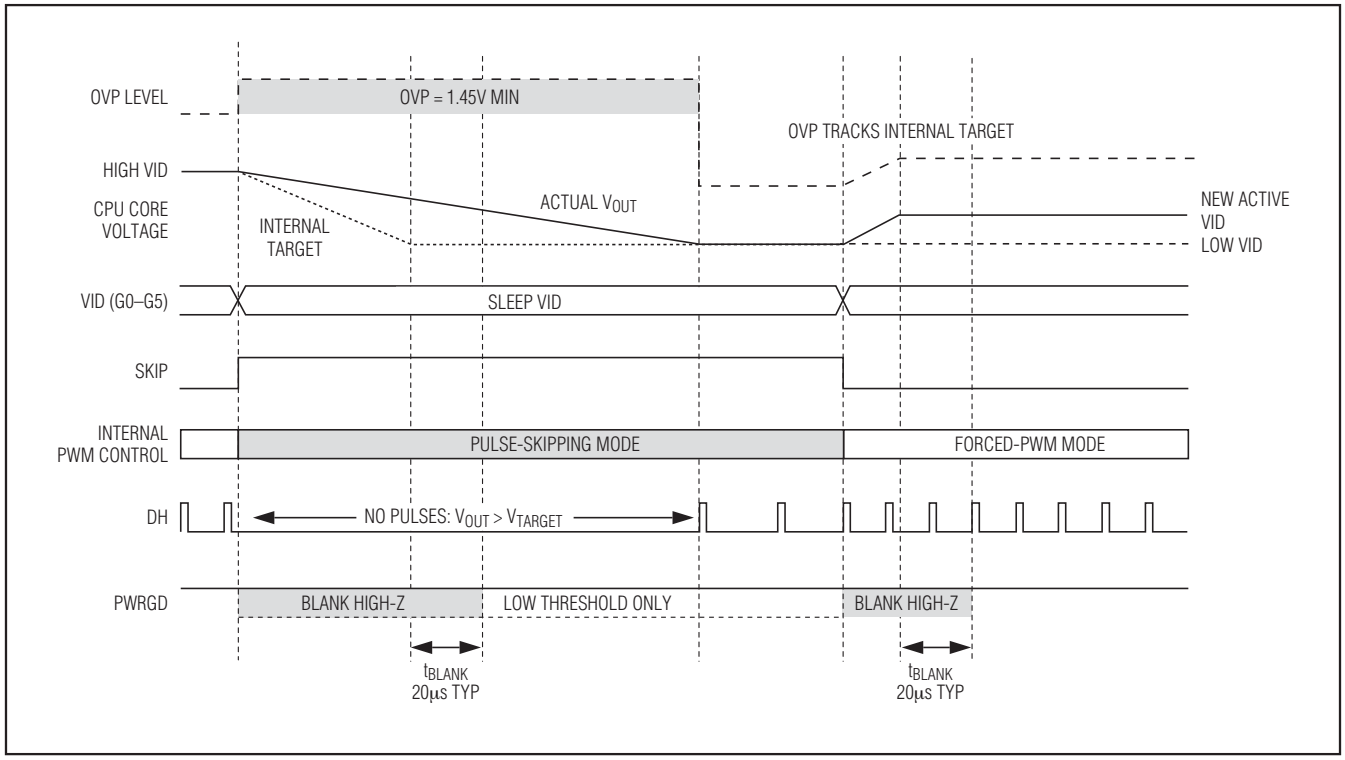


Figure 4. VID Transition

1-Phase Quick-PWM NVIDIA CPU Controller

Forced-PWM Operation (Normal Mode)

During soft-shutdown and normal operation—when the CPU is actively running (SKIP = low, Table 3)—the MAX17409 operates with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative-output-voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the processor might switch the controller to a low-power pulse-skipping control scheme after entering suspend mode. The MAX17409 automatically uses pulse-skipping operation during soft-start, regardless of the SKIP configuration.

Light-Load Pulse-Skipping Operation

During soft-start and sleep states—SKIP is pulled high—the MAX17409 operates in pulse-skipping mode. The pulse-skipping mode enables the driver's zero-crossing comparator, so the controller pulls DL low when its current-sense inputs detect "zero" inductor current. This keeps the inductor from sinking current and discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output.

Upon entering pulse-skipping operation, the controller temporarily blanks the upper PWRGD thresholds, and sets the OVP threshold to 1.80V to prevent false OVP faults when the transition to pulse-skipping operation coincides with a VID DAC code. The MAX17409 automatically uses forced-PWM operation during soft-shutdown, regardless of the SKIP configuration.

Automatic Pulse-Skipping Switchover

In skip mode (SKIP = high), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFETs. Once V_{LX} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics* table), the comparator forces DL low (Figure 2). This mechanism causes the threshold between pulse-skipping PFM and nonskipping-PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 5). For a 7V to 20V battery input range, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \frac{1}{2}\left(\frac{t_{SW}V_{OUT}}{L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The switching waveforms might appear noisy and asynchronous when light loading activates pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs between PFM noise and light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input-voltage levels.

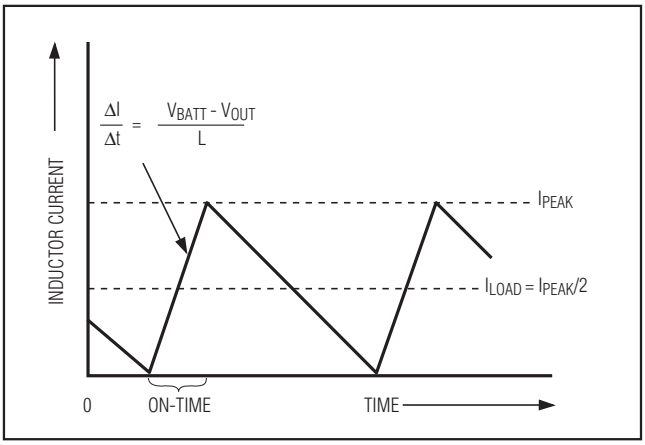


Figure 5. Pulse-Skipping/Discontinuous Crossover Point

Power-Up Sequence (POR, UVLO)

The MAX17409 is enabled when $\overline{SHDN}$ is driven high (Figure 6). The reference powers up first. Once the reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 150µs one-shot delay. The PWM controller then begins switching.

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} is above 4.25V, and $\overline{SHDN}$ is driven high. With the reference in regulation, the controller ramps the output voltage to the selected VID voltage with a 1.56mV/µs slew rate:

$$t_{TRAN(START)} = \frac{V_{BOOT}}{(1.56mV/\mu s)}$$

where V_{BOOT} is the initial VID target. The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PWRGD becomes high impedance approximately 5ms after the target output voltage is reached. The MAX17409 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown, regardless of the SKIP configuration.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high-impedance output (DL and DH pulled low).

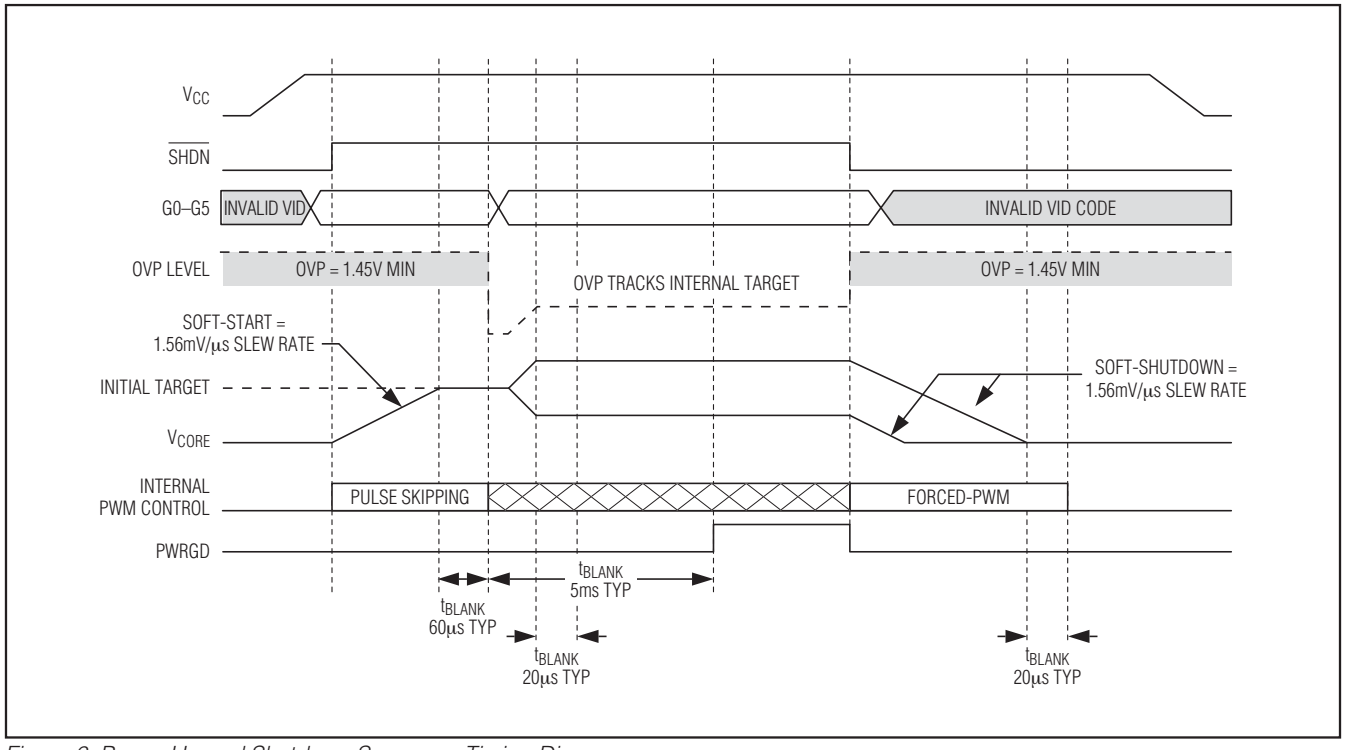


Figure 6. Power-Up and Shutdown Sequence Timing Diagram

1-Phase Quick-PWM NVIDIA CPU Controller

Shutdown

When $\overline{SHDN}$ goes low, the MAX17409 enters low-power shutdown mode. PWRGD is pulled low immediately, and the output voltage ramps down with a 1.56mV/µs slew rate:

$$t_{TRAN(SHDN)} = \frac{V_{OUT}}{(1.56mV/\mu s)}$$

Slowly discharging the output capacitors by slewing the output over a long period of time keeps the average negative inductor current low (damped response), thereby eliminating the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX17409 shuts down completely—the drivers are disabled (DL driven high, DH pulled low)—the reference turns off, and the supply currents drop to approximately 1µA (max).

When a fault condition—output UVLO or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 0.5V typ.

Temperature Comparator ($\overline{VRHOT}$)

The MAX17409 also features an independent comparator with an accurate threshold (V_{HOT}) that tracks the analog supply voltage ($V_{HOT} = 0.3V_{CC}$). This makes the thermal trip threshold independent of the V_{CC} supply voltage tolerance. Use a resistor- and thermistor-divider between V_{CC} and GND to generate a voltage-regulator overtemperature monitor. Place the thermistor as close to the MOSFETs and inductors as possible.

Fault Protection (Latched)

Output Overvoltage (OVP) Protection

The OVP circuit is designed to protect the processor against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17409 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the set VID DAC voltage by more than 300mV, subject to a minimum OVP threshold of 0.8V. During pulse-skipping operation (SKIP = high), the controller initially sets the OVP threshold to a fixed 1.8V threshold. Once the output is in regulation (the first on-time is triggered) and the PWRGD blanking time expires, the controller tightens the OVP threshold, tracking the OVP threshold by 300mV, subject to a minimum OVP threshold of 0.8V. The controller also uses the fixed 1.8V OVP threshold during soft-start and soft-shutdown.

When the OVP circuit detects an overvoltage fault, the MAX17409 immediately forces DL high and pulls DH low. This action turns on the synchronous-rectifier MOSFETs with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

OVP protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Output Undervoltage Protection (UVP)

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX17409 output voltage is 400mV below the target voltage, the controller activates the shutdown sequence and sets the fault latch. Once the controller ramps down to zero, it forces the DL high, and pulls DH low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

UVP protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Thermal-Fault Protection

The MAX17409 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, an internal thermal sensor sets the fault latch and forces the DL high and the DH low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C. Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched fault protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a “no-fault” test mode is provided to disable the fault protection—overvoltage protection, undervoltage protection, and thermal shutdown. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 11V to 13V on $\overline{SHDN}$.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH) source and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17409 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.25Ω (typ) on-resistance. This helps DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces might require that rising LX edges do not pull up the low-side MOSFETs' gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 7), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents could be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 7). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

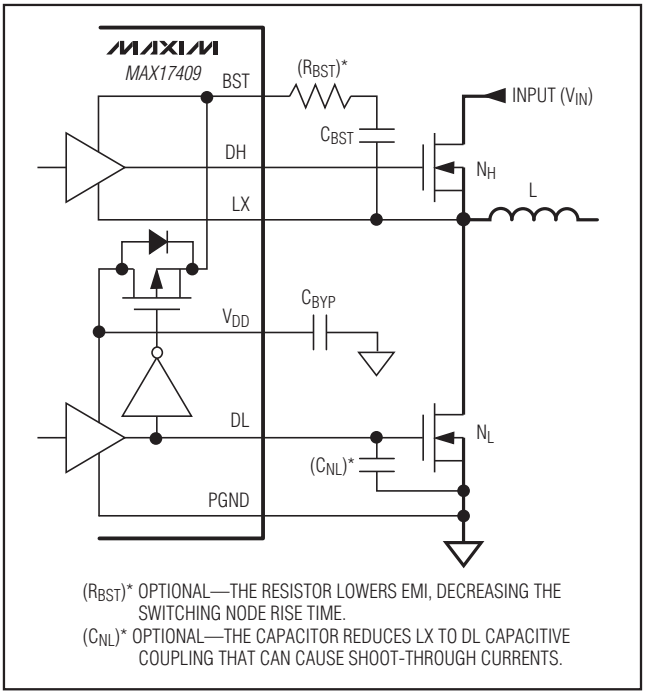


Figure 7. Gate-Drive Circuit

Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output

1-Phase Quick-PWM NVIDIA CPU Controller

capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite and molded iron cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(1 + \frac{LIR}{2}\right)$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low $V_{IN} - V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. The worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2 \left[\left(\frac{V_{OUT} t_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT} V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT}) t_{SW}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT} V_{OUT}}$$

Current-Limit Control (ILIM)

REF and ILIM are used to set the current limit. REF regulates to a fixed 2.0V and the REF-to-ILIM voltage determines the valley current-sense threshold. When ILIM = V_{CC}, the controller uses the preset 22.5mV current-limit threshold. In an adjustable design, ILIM is connected to a resistive voltage-divider connected between REF and ground. The differential voltage between REF and ILIM sets the current-limit threshold (V_{LIMIT}), so the valley current-sense threshold is:

$$V_{LIMIT} = \frac{V_{REF} - V_{ILIM}}{10}$$

This allows design flexibility since the DCR sense circuit or sense resistor does not have to be adjusted to meet the current limit as long as the current-sense voltage never exceeds 50mV. Keeping V_{LIMIT} between 20mV to 40mV leaves room for future current-limit adjustment.

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)}\left(1 - \frac{LIR}{2}\right)$$

where:

$$I_{VALLEY} = \frac{V_{LIMIT}}{R_{SENSE}} = \frac{V_{LIMIT}}{DCR \times \frac{R_{CSP\text{-}CSN}}{R_{LX\text{-}CSN}}}$$

where R_{SENSE} is the sensing resistor and $R_{CSP\text{-}CSN}/R_{LX\text{-}CSN}$ is the ratio of resistor-divider with DCR-sensing approach.

Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power dissipation requirements. The controller uses a transconductance amplifier to set the transient and DC output voltage droop (Figure 2) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor (R_{FB}) between FB and V_{OUT} to set the DC steady-state droop (load line) based on the required voltage positioning slope (R_{DROOP}):

$$R_{FB} = \frac{R_{DROOP}}{R_{SENSE} G_{m(FB)}}$$

where the effective current-sense resistance (R_{SENSE}) depends on the current-sense method (see the *Current Sense* section), and the voltage-positioning amplifier's transconductance ($G_{m(FB)}$) is typically 600µS as defined in the *Electrical Characteristics* table. When the inductors' DCR is used as the current-sense element ($R_{SENSE} = R_{DCR}$), each current-sense input should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

Output Capacitor Selection

The output filter capacitor must have low enough effective equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In processor core supplies and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In nonprocessor applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. The maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT}) V_{OUT}} \right] V_{RIPPLE}$$

where f_{SW} is the switching frequency. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF} C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{DROOP(AC)} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total ESR, R_{SENSE} is the current-sense resistance ($R_{CM} = R_{CS}$), $R_{DROOP(AC)}$ is the AC component of the droop, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors.

1-Phase Quick-PWM NVIDIA CPU Controller

In applications that require DC droop, $R_{DROOP(AC)}$ is the same as the DC droop setting ($R_{DROOP(AC)}$ = $R_{DROOP(DC)}$). In applications that do not require DC droop, this AC signal is generated by capacitively coupling the inductor ripple current signal to the FB pin. In this case, $R_{DROOP(AC)}$ = R_{SENSE}, where R_{SENSE} is the effective sense resistance seen at the CSP-CSN pins.

In Figure 1, C3 couples the inductor ripple current signal to the FB pin. C3 can be connected to the CSN pin or the CSP pin. Connecting to the CSN pin only couples the output capacitor ESR to the FB pin. Connecting to the CSP pin adds the R_{SENSE} component to the effective resistance in addition to the output capacitor ESR. This is useful for applications using all ceramic output capacitors.

Keep the C3 x R_{FB} time constant between 3x and 5x of the switching period. Practical values for C3 range from 0.1µF to 1µF. Calculate R_{FB} after selecting C3. Keeping R_{FB} below 100Ω minimizes any residual DC droop.

In the standard application circuit (Figure 1), the effective resistance for stability is the sum of the ~ 2mΩ DCR and the 6mΩ ESR of the 470µF output capacitor. The ESR zero frequency is 42kHz, well within the requirement of f_{SW}/π.

Ceramic capacitors have a high-ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. Do not put high-value ceramic capacitors directly across the output without verifying that the circuit contains enough voltage positioning and series PCB resistance to ensure stability. When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency) to minimize the energy transferred from inductor to capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{V_{IN}} \right) \sqrt{V_{OUT} \left(V_{IN} - V_{OUT} \right)}$$

The worst-case RMS current requirement occurs when operating with V_{IN} = $2V_{OUT}$. At this point, the above equation simplifies to I_{RMS} = 0.5 x I_{LOAD}.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DL gate

driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems could occur (see the *MOSFET Gate Drivers* section).

MOSFET Power Dissipation

Worst-case conduction losses occur in the high-side MOSFET (N_H) is a function of the duty factor, with the worst-case power dissipation occurring at the minimum input voltage:

$$PD\ (NH\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{LOAD}{}^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the switching losses in a high-side MOSFET (N_H) is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (NH\ Switching) = V_{IN} I_{LOAD} f_{SW} \left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}{}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.2A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the C x $V_{IN}{}^2$ x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (NL\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] (I_{LOAD})^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit can be overdesigned to tolerate:

$$I_{LOAD} = \left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right) = I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current during the dead times. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate charging requirements of the high-side MOSFETs. However, high-current applications driving large high-side MOSFETS require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

1-Phase Quick-PWM NVIDIA CPU Controller

Applications Information

Positive Offset

Some applications require a positive offset to shift the output voltage to a different level. This might be necessary to obtain a voltage not supported by the VID code, or to allow a shift in the VID code mapping.

A positive offset is generated by raising the voltage at the GNDS/OFSP pin using a resistor-divider from REF. Refer to R14 and R20 in Figure 1. The voltage at the GNDS/OFSP pin relative to the analog ground of the IC sets the offset voltage that is added to the programmed VID voltage:

$$V_{GNDS} = V_{OFFSET} = \left(\frac{R14}{R20 + R14}\right)V_{REF}$$

and:

$$V_{TARGET} = V_{DAC} + V_{OFFSET}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 8). If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow the MAX17409 Evaluation Kit layout and use the following guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, REF, GNDS bypass capacitors, and compensation (CCV) components.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- CSP and CSN connections for current limiting and voltage positioning must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes away from sensitive analog areas (CCV, FB, CSP, CSN, etc.).

Layout Procedures

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50mils to 100mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST capacitors, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; the master's analog ground plane where sensitive analog components go, the master's GND pin and V_{CC} bypass capacitor go; and the slave's analog ground plane where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the PGND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the PGND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

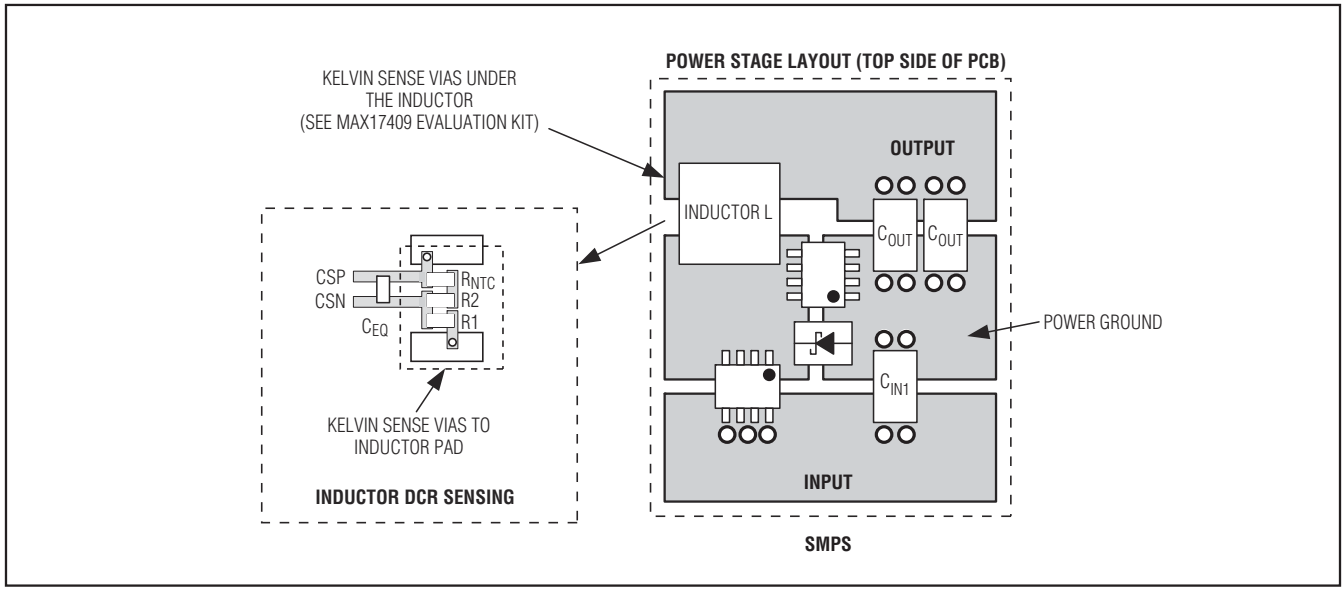


Figure 8. PCB Layout Example

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN	T2844-1	**21-0139**