- — 2.7V or 3.3V V_{CC}
- — 2.7V, 3.3V or 5V V_{PP}

■ Common Flash Interface (CFI)
   — Universal & Upgradable Interface

■ Scalable Command Set (SCS)

■ High Speed Write Performance
   — 32 Bytes x 2 plane Page Buffer
   — 2.7 µS/Byte Write Transfer Rate

■ High Speed Read Performance
   — 100/130ns(3.3V±0.3V), 120/150ns(2.7V-3.6V)

■ Enhanced Automated Suspend Options
   — Write Suspend to Read
   — Block Erase Suspend to Write
   — Block Erase Suspend to Read

■ Industry-Standard Packaging
   — 56-Lead TSOP
   — 56-Lead SSOP
   — 64-Lead SDIP

■ Chip Size Packaging
   — 64-Lead CSP

■ SRAM-Compatible Write Interface

■ High-Density Symmetrically-Blocked Architecture
   — Thirty-two 64-Kbyte Erasable Block

■ Enhanced Data Protection Features
   — Absolute Protection with V_{PP}=GND
   — Flexible Block Locking
   — Erase/Write Lockout during Power Transitions

■ Extended Cycling Capability
   — 100,000 Block Erase Cycles
   — 3.2 Million Block Erase Cycles/Chip

■ Low Power Management
   — Deep Power-Down Mode
   — Automatic Power Savings Mode Decreases I_{CC} in Static Mode

■ Automated Write and Erase
   — Command User Interface
   — Status Register

■ ETOX^{TM*} V Nonvolatile Flash Technology

■ Not designed or rated as radiation hardened

SHARP's LH28F160S3-L10/13 Flash memory with Smart 3 technology is a high-density, low-cost, nonvolatile read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160S3-L10/13 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designer ultimate control of their code security needs.

The LH28F160S3-L10/13 is conformed to the flash Scalable Command Set (SCS) and the Common Flash Interface (CFI) specification which enable universal and upgradable interface, enable the highest system/device data transfer rates and minimize device and system-level implementation costs.

The LH28F160S3-L10/13 is manufactured on SHARP's 0.4µm ETOX^{TM*} V process technology. It comes in industry-standard package: the 56-Lead TSOP, 56-Lead SSOP, 64-Lead SDIP or Chip size package: the 64-Lead CSP, ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment,etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

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1.1 Product Overview

The LH28F160S3-L10/13 is a high-performance 16-Mbit Smart 3 Flash memory organized as 2MBx8/1MBx16. The 2MB of data is arranged in thirty-two 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 7.

Smart 3 technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 2.7V V_{CC} consumes approximately one-fifth the power of 5V V_{CC}. V_{PP} at 2.7V and 3.3V eliminates the need for a separate 12V converter. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by Smart 3 Technology

V_{CC} Voltage	V_{PP} Voltage
2.7V	2.7V, 3.3V, 5V
3.3V	3.3V, 5V

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 0.41 second (3.3V

A word/byte write is performed in byte increments typically within 12.95 µs (3.3V V_{CC}, 5V V_{PP}). A multi word/byte write has high speed write performance of 2.7 µs/byte (3.3V V_{CC}, 5V V_{PP}). (Multi) Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits and WP#, Thirty-two block lock-bits, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and cleared block lock-bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

The STS output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using STS minimizes both CPU overhead and system power consumption. STS pin can be configured to different states using the Configuration command. The STS pin defaults to RY/BY# operation. When low, STS indicates that the WSM is performing a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration. STS-High Z indicates that the WSM is ready for a new command, block erase is suspended and (multi) word/byte write are inactive, (multi) word/byte write are suspended, or the device is in deep power-down mode. The other 3 alternate configurations are all pulse mode for use as a system interrupt.

is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 3 mA at 3.3V V_{CC}.

When either CE_0# or CE_1#, and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time

Outline Package, 1.2 mm thick), 56-Lead SSOP (Shrink Small Outline Package), 64-Lead SDIP (Shrink Dual Inline Package) and 64-Lead CSP (Chip Size Package). Pinout is shown in Figure 2,3,4,5 and 6.
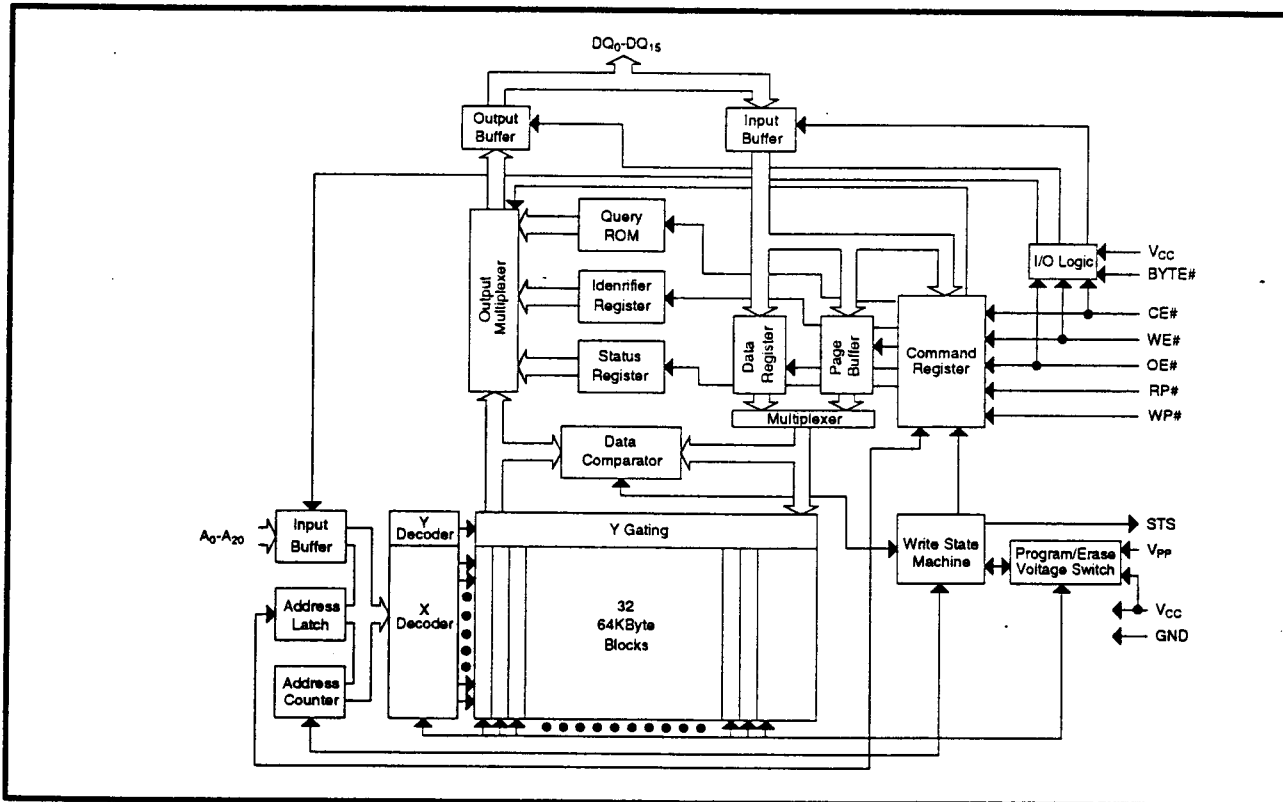

Figure 1. Block Diagram

		A16–A20 : Block Address.
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS:** DQ_0–DQ_7:Inputs data and commands during CUI write cycles; outputs data during memory array, status register, query, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8–DQ_{15}:Inputs data during CUI write cycles in x16 mode; outputs data during memory array read cycles in x16 mode; not used for status register, query and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in x8 mode(Byte#=V_{IL}). Data is internally latched during a write cycle.
CE_0#, CE_1#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers decoders, and sense amplifiers. Either CE_0# or CE_1# V_{IH} deselects the device and reduces power consumption to standby levels. Both CE_0# and CE_1# must be V_{IL} to select the devices.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP# V_{IH} enables normal operation. When driven V_{IL}, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	**STS (RY/BY#):** Indicates the status of the internal WSM. When configured in level mode (default mode), it acts as a RY/BY# pin. When low, the WSM is performing an internal operation (block erase, full chip erase, (multi) word/byte write or block lock-bit configuration). STS High Z indicates that the WSM is ready for new commands, block erase is suspended, and (multi) word/byte write is inactive, (multi) word/byte write is suspended or the device is in deep power-down mode. For alternate configurations of the STATUS pin, see the Configuration command.
WP#	INPUT	**WRITE PROTECT:** Master control for block locking. When V_{IL}, Locked blocks can not be erased and programmed, and block lock-bits can not be set and reset.
BYTE#	INPUT	**BYTE ENABLE:** BYTE# V_{IL} places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. BYTE# V_{IH} places the device in x16 mode , and turns off the A_0 input buffer.
V_{PP}	SUPPLY	**BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE, BLOCK LOCK-BIT CONFIGURATION POWER SUPPLY:** For erasing array blocks, writing bytes or configuring block lock-bits. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection configures the device for 2.7V or 3.3V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internal connected; it may be driven or floated.

Figure 2 (Normal Bend) — left side pins

Pin	Signal
8	A16
9	Vcc
10	A15
11	A14
12	A13
13	A12
14	CE0#
15	Vpp
16	RP#
17	A11
18	A10
19	A9
20	A8
21	GND
22	A7
23	A6
24	A5
25	A4
26	A3
27	A2
28	A1

56 LEAD TSOP
STANDARD PINOUT
14mm x 20mm
TOP VIEW

Figure 2 (Normal Bend) — right side pins

Pin	Signal
49	DQ6
48	GND
47	DQ13
46	DQ5
45	DQ12
44	DQ4
43	Vcc
42	GND
41	DQ11
40	DQ3
39	DQ10
38	DQ2
37	Vcc
36	DQ9
35	DQ1
34	DQ8
33	DQ0
32	A0
31	BYTE#
30	NC
29	NC

Figure 2. TSOP 56-Lead Pinout (Normal Bend)

Figure 3 (Reverse Bend) — left side pins

Signal	Pin
WP#	56
WE#	55
OE#	54
STS	53
DQ15	52
DQ7	51
DQ14	50
DQ6	49
GND	48
DQ13	47
DQ5	46
DQ12	45
DQ4	44
Vcc	43
GND	42
DQ11	41
DQ3	40
DQ10	39
DQ2	38
Vcc	37
DQ9	36
DQ1	35
DQ8	34
DQ0	33
A0	32
BYTE#	31
NC	30
NC	29

56 LEAD TSOP
STANDARD PINOUT
14mm x 20mm
TOP VIEW

Figure 3 (Reverse Bend) — right side pins

Pin	Signal
1	NC
2	CE1#
3	NC
4	A20
5	A19
6	A18
7	A17
8	A16
9	Vcc
10	A15
11	A14
12	A13
13	A12
14	CE0#
15	Vpp
16	RP#
17	A11
18	A10
19	A9
20	A8
21	GND
22	A7
23	A6
24	A5
25	A4
26	A3
27	A2
28	A1

Figure 3. TSOP 56-Lead Pinout (Reverse Bend)

CE1# 7
NC 8
A20 9
A19 10
A18 11
A17 12
A16 13
VCC 14
GND 15
DQ6 16
DQ14 17
DQ7 18
DQ15 19
STS 20
OE# 21
WE# 22
WP# 23
DQ13 24
DQ5 25
DQ12 26
DQ4 27
VCC 28

50 A2
49 A3
48 A4
47 A5
46 A6
45 A7
44 GND
43 A8
42 VCC
41 DQ9
40 DQ1
39 DQ8
38 DQ0
37 A0
36 BYTE#
35 NC
34 NC
33 DQ2
32 DQ10
31 DQ3
30 DQ11
29 GND

56 LEAD SSOP
STANDARD PINOUT
1.8mm x 16mm x 23.7mm
TOP VIEW

Figure 4. SSOP 56-Lead Pinout

	1	2	3	4	5	6	7	8
A	NC	A20	NC	NC	WP#	OE#	STS	NC
B	A17	A18	A19	CE1#	WE#	DQ15	DQ7	DQ14
C	A15	VCC	A14	A16	DQ6	DQ5	GND	DQ13
D	A12	CE0#	A13	NC	NC	DQ12	VCC	DQ4
E	RP#	VPP	A11	NC	NC	DQ3	GND	DQ11
F	A9	A8	A10	GND	DQ9	DQ10	VCC	DQ2
G	A7	A6	A5	A2	NC	DQ0	DQ8	DQ1
H	NC	A4	A3	A1	NC	BYTE#	A0	NC

64-LEAD CSP
STANDARD PINOUT
8mm X 11mm
TOP VIEW

Figure 5. CSP 64-Lead Pinout

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```
GND          7              58    A₁₆
A₇    ☐ 8              57    A₁₇
A₆    ☐ 9              56    A₁₈
A₅    ☐ 10             55    A₁₉
A₄    ☐ 11             54    A₂₀
A₃    ☐ 12             53    NC
A₂    ☐ 13             52    CE₁#
A₁    ☐ 14    64 LEAD SDIP        51    NC
NC    ☐ 15    STANDARD PINOUT     50    NC
NC    ☐ 16    17mm X 58mm         49    NC
NC    ☐ 17    TOP VIEW            48    NC
NC    ☐ 18                        47    WP#
NC    ☐ 19                        46    WE#
NC    ☐ 20                        45    OE#
NC    ☐ 21                        44    STS
BYTE# ☐ 22                        43    DQ₁₅
A₀    ☐ 23                        42    DQ₇
DQ₀   ☐ 24                        41    DQ₁₄
DQ₈   ☐ 25                        40    DQ₆
DQ₁   ☐ 26                        39    GND
DQ₉   ☐ 27                        38    DQ₁₃
Vcc   ☐ 28                        37    DQ₅
DQ₂   ☐ 29                        36    DQ₁₂
DQ₁₀  ☐ 30                        35    DQ₄
DQ₃   ☐ 31                        34    Vcc
DQ₁₁  ☐ 32                        33    GND
```
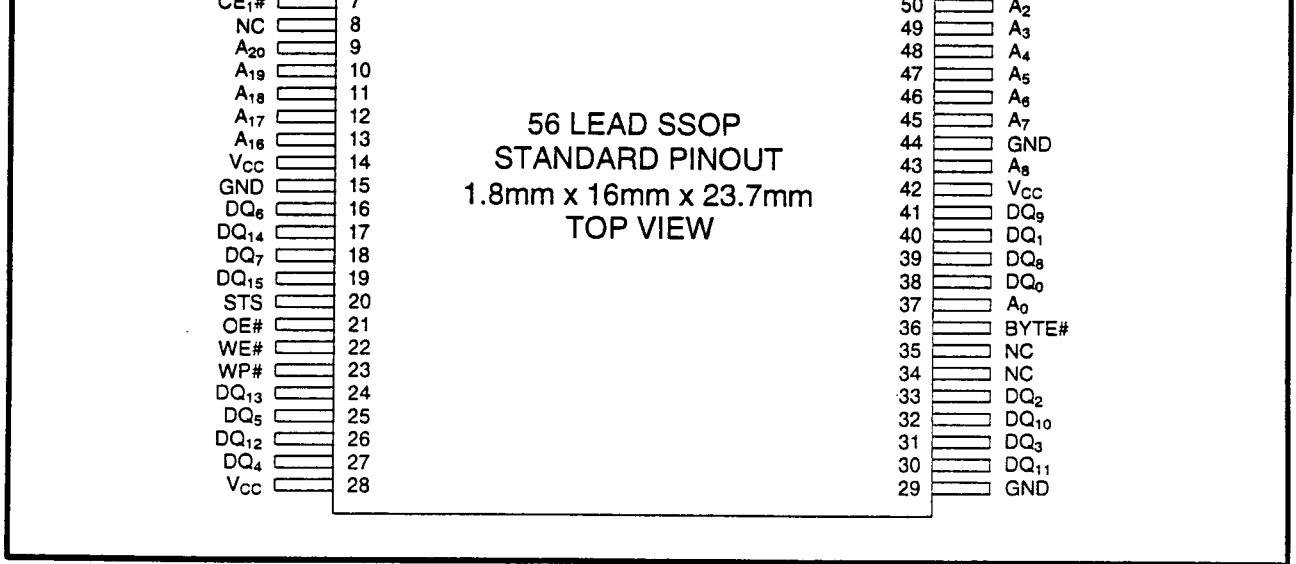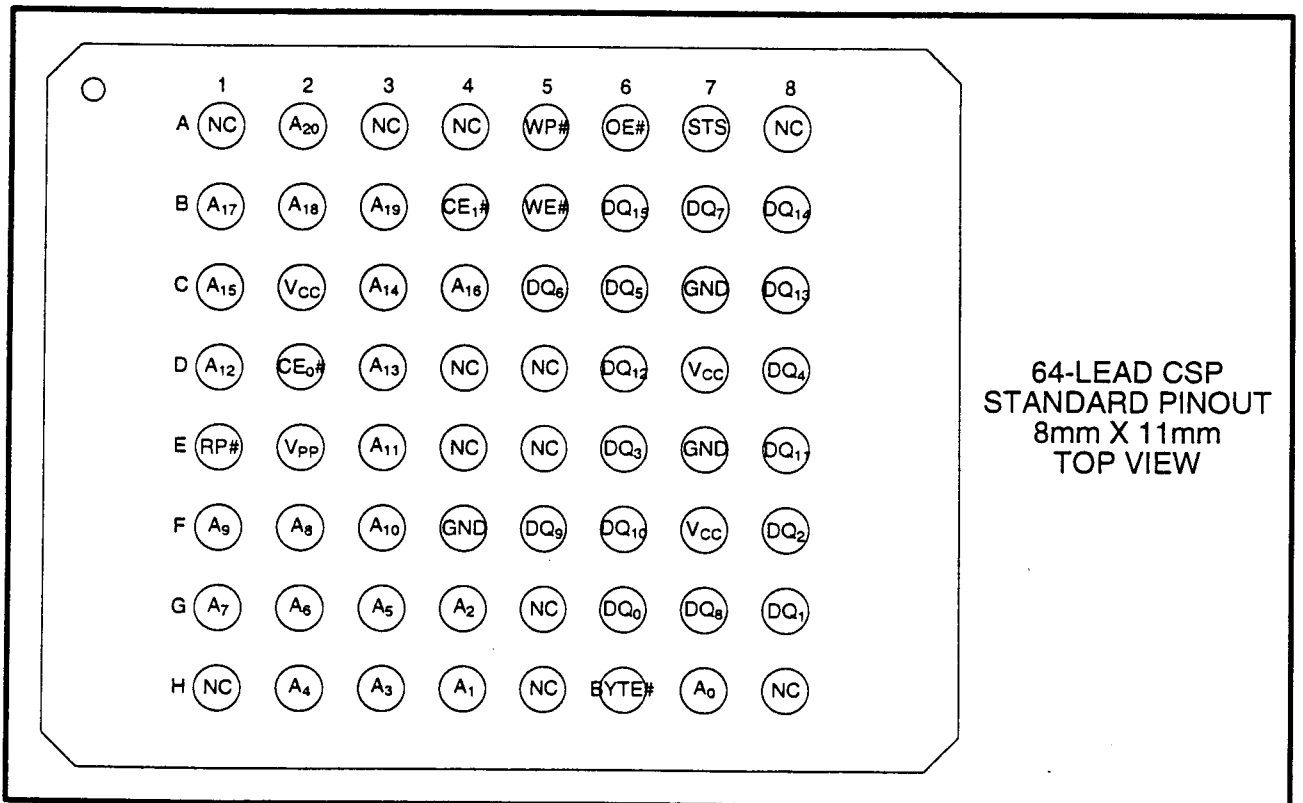
Figure 6. SDIP 64-Lead Pinout

erase, full chip erase, (multi) word/byte write and block lock-bit configuration, and minimal processor overhead with RAM-Like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register, query structure and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. All functions associated with altering memory contents—block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, status, query and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, outputs query structure or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, (multi) word/byte write and block lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Write suspend allows system software to suspend a (multi) word/byte write to read data from any other flash memory array location.

Address	64-Kbyte Block	#
1C0000 / 1BFFFF	64-Kbyte Block	27
1B0000 / 1AFFFF	64-Kbyte Block	26
1A0000 / 19FFFF	64-Kbyte Block	25
190000 / 18FFFF	64-Kbyte Block	24
180000 / 17FFFF	64-Kbyte Block	23
170000 / 16FFFF	64-Kbyte Block	22
160000 / 15FFFF	64-Kbyte Block	21
150000 / 14FFFF	64-Kbyte Block	20
140000 / 13FFFF	64-Kbyte Block	19
130000 / 12FFFF	64-Kbyte Block	18
120000 / 11FFFF	64-Kbyte Block	17
110000 / 10FFFF	64-Kbyte Block	16
100000 / 0FFFFF	64-Kbyte Block	15
0F0000 / 0EFFFF	64-Kbyte Block	14
0E0000 / 0DFFFF	64-Kbyte Block	13
0D0000 / 0CFFFF	64-Kbyte Block	12
0C0000 / 0BFFFF	64-Kbyte Block	11
0B0000 / 0AFFFF	64-Kbyte Block	10
0A0000 / 09FFFF	64-Kbyte Block	9
090000 / 08FFFF	64-Kbyte Block	8
080000 / 07FFFF	64-Kbyte Block	7
070000 / 06FFFF	64-Kbyte Block	6
060000 / 05FFFF	64-Kbyte Block	5
050000 / 04FFFF	64-Kbyte Block	4
040000 / 03FFFF	64-Kbyte Block	3
030000 / 02FFFF	64-Kbyte Block	2
020000 / 01FFFF	64-Kbyte Block	1
010000 / 00FFFF	64-Kbyte Block	0
000000		

Figure 7. Memory Map

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The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with multi-step block erase, full chip erase, (multi) word/byte write and block lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and (multi) word/byte write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, query structure, or status register independent of the V_{PP} voltage. RP# must be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE# (CE$_0$#, CE$_1$#), OE#, WE#, RP# and WP#. CE$_0$#, CE$_1$# and OE# must be driven active to obtain data at the outputs. CE$_0$#, CE$_1$# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ$_0$-DQ$_{15}$) control and when active drives the selected memory data onto the I/O bus. WE# and RP# must be at V_{IH}. Figure 21, 22 illustrates a read cycle.

Either CE$_0$# or CE$_1$# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ$_0$-DQ$_{15}$ outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, (multi) word/byte write or block lock-bit configuration modes, RP#-low will abort the operation. STS remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

block status codes identify locked or unlocked block setting and erase completed or erase uncompleted condition.

Figure 8. Device Identifier Code Memory Map

Query structure are always presented on the lowest-order data output (DQ_0-DQ_7) only.

3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$, the CUI additionally controls block erase, full chip erase, (multi) word/byte write and block lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/byte Write command requires the command and address of the location to be written. Set Block Lock-Bit command requires the command and block address within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 23 and 24 illustrate WE# and CE#-controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK}$, Read operations from the status register, identifier codes, query, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.
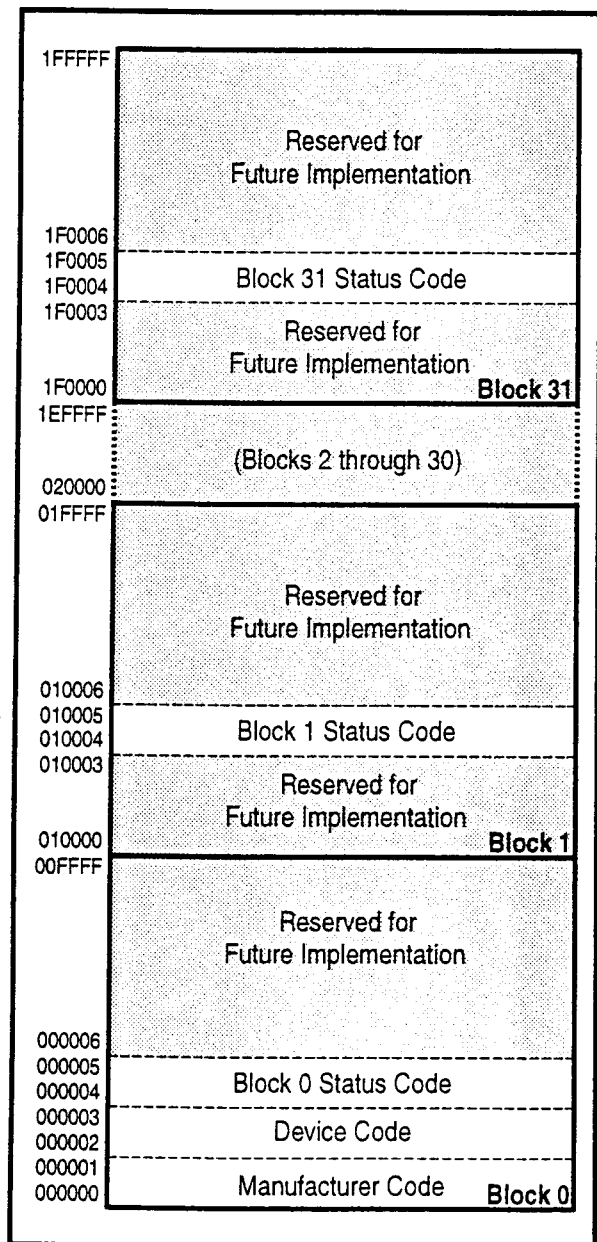
Mode	Notes	RP#	CE$_0$#	CE$_1$#	OE#	WE#	Address	V$_{PP}$	DQ$_{0-7}$	STS
Deep Power-Down	4	V$_{IL}$	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes		V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	See Figure 8	X	Note 5	High Z
Query		V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	See Table 7~11	X	Note 6	High Z
Write	3,7,8,9	V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IL}$	X	X	D$_{IN}$	X

Table 3.1. Bus Operations(BYTE#=V$_{IL}$)

Mode	Notes	RP#	CE$_0$#	CE$_1$#	OE#	WE#	Address	V$_{PP}$	DQ$_{0-7}$	STS
Read	1,2,3,9	V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	X	X	D$_{OUT}$	X
Output Disable	3	V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IH}$	X	X	High Z	X
Standby	3	V$_{IH}$	V$_{IH}$ / V$_{IH}$ / V$_{IL}$	V$_{IH}$ / V$_{IL}$ / V$_{IH}$	X	X	X	X	High Z	X
Deep Power-Down	4	V$_{IL}$	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes		V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	See Figure 8	X	Note 5	High Z
Query		V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	See Table 7~11	X	Note 6	High Z
Write	3,7,8,9	V$_{IH}$	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IL}$	X	X	D$_{IN}$	X

NOTES:
1. Refer to DC Characteristics. When V$_{PP} \leq$ V$_{PPLK}$, memory contents can be read, but not altered.
2. X can be V$_{IL}$ or V$_{IH}$ for control pins and addresses, and V$_{PPLK}$ or V$_{PPH1/2/3}$ for V$_{PP}$. See DC Characteristics for V$_{PPLK}$ and V$_{PPH1/2/3}$ voltages.
3. STS is V$_{OL}$ (if configured to RY/BY# mode) when the WSM is executing internal block erase, full chip erase, (multi) word/byte write or block lock-bit configuration algorithms. It is floated during when the WSM is not busy, in block erase suspend mode with (multi) word/byte write inactive, (multi) word/byte write suspend mode, or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. See Section 4.5 for query data.
7. Command writes involving block erase, full chip erase, (multi) word/byte write or block lock-bit configuration are reliably executed when V$_{PP}$=V$_{PPH1/2/3}$ and V$_{CC}$=V$_{CC1/2}$.
8. Refer to Table 4 for valid D$_{IN}$ during a write operation.
9. Don't use the timing both OE# and WE# are V$_{IL}$.

Command		Notes	Oper	Addr	Data	Oper	Addr	Data
Clear Status Register	1		Write	X	50H	Read	X	SRD
Block Erase Setup/Confirm	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase Setup/Confirm	2		Write	X	30H	Write	X	D0H
Word/Byte Write Setup/Write	2	5,6	Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write Setup/Write	2	5,6	Write	WA	10H	Write	WA	WD
Multi Word/Byte Write Setup/Confirm	≥4	9	Write	WA	E8H	Write	WA	N
Block Erase and (Multi) Word/byte Write Suspend	1	5	Write	X	B0H			
Confirm and Block Erase and (Multi) Word/byte Write Resume	1	5	Write	X	D0H			
Block Lock-Bit Set Setup/Confirm	2	7	Write	BA	60H	Write	BA	01H
Block Lock-Bit Reset Setup/Confirm	2	8	Write	X	60H	Write	X	D0H
STS Configuration Level-Mode for Erase and Write (RY/BY# Mode)	2		Write	X	B8H	Write	X	00H
STS Configuration Pulse-Mode for Erase	2		Write	X	B8H	Write	X	01H
STS Configuration Pulse-Mode for Write	2		Write	X	B8H	Write	X	02H
STS Configuration Pulse-Mode for Erase and Write	2		Write	X	B8H	Write	X	03H

NOTES:

1. BUS operations are defined in Table 3 and Table 3.1.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 8.
   QA=Query Offset Address.
   BA=Address within the block being erased or locked.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 14 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID=Data read from identifier codes.
   QD=Data read from query database.
4. Following the Read Identifier Codes command, read operations access manufacturer, device and block status codes. See Section 4.2 for read identifier code data.
5. If the block is locked, WP# must be at V_{IH} to enable block erase or (multi) word/byte write operations. Attempts to issue a block erase or (multi) word/byte write to a locked block while RP# is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the byte write setup.
7. A block lock-bit can be set while WP# is V_{IH}.
8. WP# must be at V_{IH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
9. Following the Third Bus Cycle, inputs the write address and write data of 'N'+1 times. Finally, input the confirm command 'D0H'.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

internal WSM has started a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend and (Multi) Word/byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# must be V_{IH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 8 retrieve the manufacturer, device, block lock configuration and block erase status (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# must be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address	Data
Manufacture Code	00000 00001	B0
Device Code	00002 00003	D0
Block Status Code	X0004[1] X0005[1]	
•Block is Unlocked		$DQ_0=0$
•Block is Locked		$DQ_0=1$
•Last erase operation completed successfully		$DQ_1=0$
•Last erase operation did not completed successfully		$DQ_1=1$
•Reserved for Future Use		DQ_{2-7}

NOTE:
1. X selects the specific block status code to be read. See Figure 8 for the device identifier code memory map.

Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#(Either CE_0# or CE_1#), whichever occurs. OE# or CE#(Either CE_0# or CE_1#) must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# must be V_{IH}.

The extended status register may be read to determine multi byte write availability(see Table 14.1). The extended status register may be read at any time by writing the Multi Byte Write command. After writing this command, all subsequent read operations output data from the extended status register, until another valid command is written. The contents of the extended status register are latched on the falling edge of OE# or CE#(Either CE_0#- or CE_1#), whichever occurs last in the read cycle. Multi Byte Write command must be re-issued to update the extended status register latch.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 14). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. RP# must be V_{IH}. This command is not functional during block erase, full chip erase, (multi) word/byte write block lock-bit configuration, block erase suspend or (multi) word/byte write suspend modes.

address is ignored when X8 mode (BYTE#=V_{IL}).

Query data are always presented on the low-byte data output (DQ_0-DQ_7). In x16 mode, high-byte (DQ_8-DQ_{15}) outputs 00H. The bytes not assigned to any information or reserved for future use are set to "0". This command functions independently of the V_{PP} voltage. RP# must be V_{IH}.

	1 , 0 , 0 , 0 , 1 , 1 (23H)	High-Z	"R"
X16 mode	A_5, A_4, A_3, A_2, A_1		
	1 , 0 , 0 , 0 , 0 (10H)	00H	"Q"
	1 , 0 , 0 , 0 , 1 (11H)	00H	"R"

4.5.1 Block Status Register

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregulary, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid.

Table 7. Query Block Status Register

Offset (Word Address)	Length	Description
(BA+2)H	01H	Block Status Register bit0　Block Lock Configuration 　　　0=Block is unlocked 　　　1=Block is Locked bit1　Block Erase Status 　　　0=Last erase operation completed successfully 　　　1=Last erase operation not completed successfully bit2-7　reserved for future use

Note:
1. BA=The beginning of a Block Address.

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Table 8. CFI Query Identification String

Offset (Word Address)	Length	Description
10H,11H,12H	03H	Query Unique ASCII string "QRY" 51H,52H,59H
13H,14H	02H	Primary Vendor Command Set and Control Interface ID Code 01H,00H (SCS ID Code)
15H,16H	02H	Address for Primary Algorithm Extended Query Table 31H,00H (SCS Extended Query Table Offset)
17H,18H	02H	Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists)
19H,1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

4.5.3 System Interface Information

The following device information can be useful in optimizing system interface software.

Table 9. System Information String

Offset (Word Address)	Length	Description
1BH	01H	V_{CC} Logic Supply Minimum Write/Erase voltage 27H (2.7V)
1CH	01H	V_{CC} Logic Supply Maximum Write/Erase voltage 55H (5.5V)
1DH	01H	V_{PP} Programming Supply Minimum Write/Erase voltage 27H (2.7V)
1EH	01H	V_{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V)
1FH	01H	Typical Timeout per Single Byte/Word Write 03H (2^3=8 µsec)
20H	01H	Typical Timeout for Maximum Size Buffer Write (32 Bytes) 06H (2^6=64 µsec)
21H	01H	Typical Timeout per Individual Block Erase 0AH (0AH=10, 2^{10}=1024 msec)
22H	01H	Typical Timeout for Full Chip Erase 0FH (0FH=15, 2^{15}=32768 msec)
23H	01H	Maximum Timeout per Single Byte/Word Write, 2^N times of typical. 04H (2^4=16, 8 µsecx16=512 µsec)
24H	01H	Maximum Timeout Maximum Size Buffer Write, 2^N times of typical. 04H (2^4=16, 64 µsecx16=4096 µsec)
25H	01H	Maximum Timeout per Individual Block Erase, 2^N times of typical. 04H (2^4=16, 1024 msecx16=16384 msec)
26H	01H	Maximum Timeout for Full Chip Erase, 2^N times of typical. 04H (2^4=16, 32768msecx16=524288 msec)

27H	01H	Device Size 15H (15H=21, 2^{21}=2097152=2M Bytes)
28H,29H	02H	Flash Device Interface description 02H,00H (x8/x16 supports x8 and x16 via BYTE#)
2AH,2BH	02H	Maximum Number of Bytes in Multi word/byte write 05H,00H (2^5=32 Bytes)
2CH	01H	Number of Erase Block Regions within device 01H (symmetrically blocked)
2DH,2EH	02H	The Number of Erase Blocks 1FH,00H (1FH=31 ==> 31+1=32 Blocks)
2FH,30H	02H	The Number of "256 Bytes" cluster in a Erase block 00H,01H (0100H=256 ==>256 Bytes x 256= 64K Bytes in a Erase Block)

4.5.5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 11. SCS OEM Specific Extended Query Table

Offset (Word Address)	Length	Description
31H,32H,33H	03H	PRI 50H,52H,49H
34H	01H	31H (1) Major Version Number , ASCII
35H	01H	30H (0) Minor Version Number, ASCII

36H,37H,
38H,39H
	04H	0FH,00H,00H,00H
		Optional Command Support
		    bit0=1 : Chip Erase Supported
		    bit1=1 : Suspend Erase Supported
		    bit2=1 : Suspend Write Supported
		    bit3=1 : Lock/Unlock Supported
		    bit4=0 : Queued Erase Not Supported
		    bit5-31=0 : reserved for future use

3AH	01H	01H
		Supported Functions after Suspend
		    bit0=1 : Write Supported after Erase Suspend
		    bit1-7=0 : reserved for future use

3BH,3CH	02H	03H,00H
		Block Status Register Mask
		    bit0=1 : Block Status Register Lock Bit [BSR.0] active
		    bit1=1 : Block Status Register Valid Bit [BSR.1] active
		    bit2-15=0 : reserved for future use

3DH	01H	V_{CC} Logic Supply Optimum Write/Erase voltage(highest performance) 50H(5.0V)
3EH	01H	V_{PP} Programming Supply Optimum Write/Erase voltage(highest performance) 50H(5.0V)
3FH	reserved	Reserved for future versions of the SCS Specification

block to be erased (erase changes all block data to FFH). Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect block erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or if set, that WP#=V_{IH}. If block erase is attempted when the corresponding block lock-bit is set and WP#=V_{IL}, SR.1 and SR.5 will be set to "1".

4.7 Full Chip Erase Command

This command followed by a confirm command (D0H) erases all of the unlocked blocks. A full chip

the two-cycle full chip erase sequence is written, the device automatically outputs status register dat when read (see Figure 10). The CPU can detect fu chip erase completion by analyzing the output data o the STS pin or status register bit SR.7.

When the full chip erase is complete, status registe bit SR.5 should be checked. If erase error i detected, the status register should be cleared befor system software attempts corrective actions. The CU remains in read status register mode until a nev command is issued. If error is detected on a bloc during full chip erase operation, WSM stops erasinç Reading the block valid status by issuing Read IC Codes command or Query command informs whic blocks failed to its erase.

This two-step command sequence of set-up followe by execution ensures that block contents are no accidentally erased. An invalid Full Chip Eras command sequence will result in both status registe bits SR.4 and SR.5 being set to "1". Also, reliable fu chip erasure can only occur when $V_{CC}=V_{CC1/2}$ anc $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage block contents are protected against erasure. If ful chip erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 anc SR.5 will be set to "1". When WP#=V_{IH}, all blocks are erased independent of block lock-bits status. Wher WP#=V_{IL}, only unlocked blocks are erased. In this case, SR.1 and SR.4 will not be set to "1". Full chip erase can not be suspended.

controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect the completion of the word/byte write event by analyzing the STS pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires that the corresponding block lock-bit be cleared or, if set, that $WP\#=V_{IH}$. If word/byte write is attempted when the corresponding block lock-bit is set and $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1". Word/byte write operations with $V_{IL}<WP\#<V_{IH}$ produce spurious results and should not be attempted.

4.9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes in x8 mode (16 words in x16 mode) can be loaded into the buffer and written to the Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read (see Figure 12,13). If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry,

count (N) must be less than or equal to 1FH in x8 mode (0FH in x16 mode). On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH28F160S3-L10/13 has two buffers. If an error occurs while writing, the device will stop writing and flush next multi word/byte write command loaded in multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a multi word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

Reliable multi byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against multi word/byte writes. If multi word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful multi word/byte write requires that the corresponding block lock-bit be cleared or, if set, that $WP\#=V_{IH}$. If multi byte write is attempted when the corresponding block lock-bit is set and $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1".

the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). STS will also transition to High-Z. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Multi) Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the (Multi) Word/Byte Write Suspend command (see Section 4.11), a (multi) word/byte write operation can also be suspended. During a (multi) word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the STS (if set to RY/BY#) output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 14). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH}. Block erase cannot resume

allows (multi) word/byte write interruption to read data in other flash memory locations. Once the (multi) word/byte write process starts, writing the (Multi) Word/Byte Write Suspend command requests that the WSM suspend the (multi) word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the (Multi) Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the (multi) word/byte write operation has been suspended (both will be set to "1"). STS will also transition to High-Z. Specification t_{WHRH1} defines the (multi) word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while (multi) word/byte write is suspended are Read Status Register and (Multi) Word/Byte Write Resume. After (Multi) Word/Byte Write Resume command is written to the flash memory, the WSM will continue the (multi) word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and STS will return to V_{OL}. After the (Multi) Word/Byte Write command is written, the device automatically outputs status register data when read (see Figure 15). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for (multi) word/byte write) while in (multi) word/byte write suspend mode. WP# must also remain at V_{IH} or V_{IL}.

summary of hardware and software write protection options.

Set block lock-bit is executed by a two-cycle command sequence. The set block lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set block lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 16). The CPU can detect the completion of the set block lock-bit event by analyzing the STS pin output or status register bit SR.7.

When the set block lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires $WP\#=V_{IH}$. If it is attempted with $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations with $WP\#<V_{IH}$ produce spurious results and should not be attempted.

4.13 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With $WP\#=V_{IH}$,

setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 17). The CPU can detect completion of the clear block lock-bits event by analyzing the STS Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. If a clear block lock-bits operation is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires $WP\#=V_{IH}$. If it is attempted with $WP\#=V_{IL}$, SR.1 and SR.5 will be set to "1" and the operation will fail. Clear block lock-bits operations with $V_{IH}<RP\#$ produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

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V_{IL}. Upon initial device power-up and after exit from deep power-down mode, the STS pin defaults to RY/BY# operation where STS low indicates that the WSM is busy. STS High Z indicates that the WSM is ready for a new operation.

To reconfigure the STS pin to other modes, the STS Configuration is issued followed by the appropriate configuration code. The three alternate configurations are all pulse mode for use as a system interrupt. The STS Configuration command functions independently of the V_{PP} voltage and RP# must be V_{IH}.

	Set STS pin to pulsed output signal for specific erase operation. In this mode, STS provides low pulse at the completion of BLock Erase, Full Chip Erase and Clear Block Lock-bits operations.
01H	
02H	Set STS pin to pulsed output signal for a specific write operation. In this mode, STS provides low pulse at the completion of (Multi) Byte Write and Set Block Lock-bit operation.
03H	Set STS pin to pulsed output signal for specific write and erase operation. STS provides low pulse at the completion of Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-bit Configuration operations.

Table 13. Write Protection Alternatives

Operation	Block Lock-Bit	WP#	Effect
Block Erase, (Multi) Word/Byte Write	0	V_{IL} or V_{IH}	Block Erase and (Multi) Word/Byte Write Enabled
	1	V_{IL}	Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled
		V_{IH}	Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled
Full Chip Erase	0,1	V_{IL}	All unlocked blocks are erased, locked blocks are not erased
	X	V_{IH}	All blocks are erased
Set Block Lock-Bit	X	V_{IL}	Set Block Lock-Bit Disabled
		V_{IH}	Set Block Lock-Bit Enabled
Clear Block Lock-Bits	X	V_{IL}	Clear Block Lock-Bits Disabled
		V_{IH}	Clear Block Lock-Bits Enabled

0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS
    1 = Block Erase Suspended
    0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS
       STATUS
    1 = Error in Erase or Clear Blocl Lock-Bits
    0 = Successful Erase or Clear Block Lock-Bits

SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS
    1 = Error in Write or Set Block Lock-Bit
    0 = Successful Write or Set Block Lock-Bit

SR.3 = V_{PP} STATUS
    1 = V_{PP} Low Detect, Operation Abort
    0 = V_{PP} OK

SR.2 = WRITE SUSPEND STATUS
    1 = Write Suspended
    0 = Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
    1 = Block Lock-Bit and/or WP# Lock Detected,
        Operation Abort
    0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

erase, (multi) word/byte write or block lock-bit configuration completion.
SR.6-0 are invalid while SR.7="0".

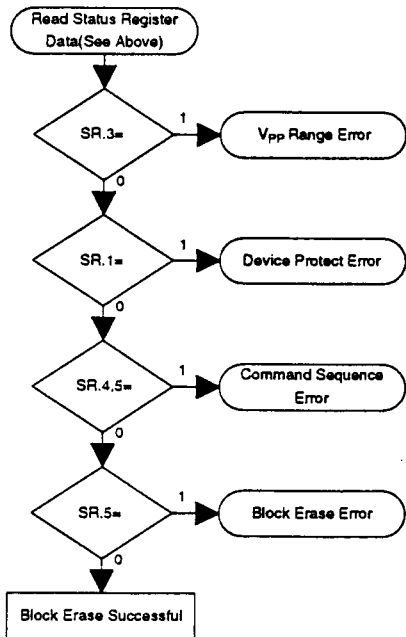If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2/3}$.

SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lock-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

Table 14.1. Extended Status Register Definition

SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

	NOTES:

XSR.7 = STATE MACHINE STATUS
    1 = Multi Word/Byte Write available
    0 = Multi Word/Byte Write not available
 	
XSR.6-0=RESERVED FOR FUTURE ENHANCEMENTS
	After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available.
	
	XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.
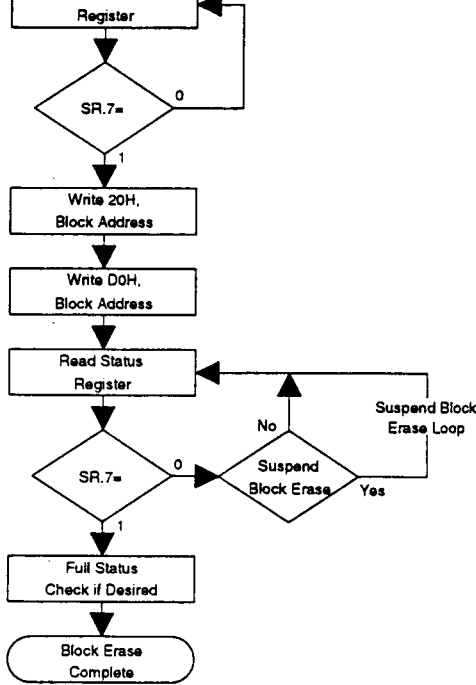
Flowchart (left side)

- Register
- SR.7= → 0 (loops back)
- ↓ 1
- Write 20H, Block Address
- Write D0H, Block Address
- Read Status Register
- SR.7= → 0 → Suspend Block Erase → No (Suspend Block Erase Loop) / Yes
- ↓ 1
- Full Status Check if Desired
- Block Erase Complete

FULL STATUS CHECK PROCEDURE

- Read Status Register Data(See Above)
- SR.3= → 1 → V$_{PP}$ Range Error
- ↓ 0
- SR.1= → 1 → Device Protect Error
- ↓ 0
- SR.4,5= → 1 → Command Sequence Error
- ↓ 0
- SR.5= → 1 → Block Erase Error
- ↓ 0
- Block Erase Successful

Table (upper right)

Bus Operation	Command	Comments
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

Table (lower right)

Bus Operation	Command	Comments
Standby		Check SR.3 1=V$_{PP}$ Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V$_{IL}$,Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 9. Automated Block Erase Flowchart

Bus Operation	Command	Comments
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Full Chip Erase Setup	Data=30H Addr=X
Write	Full Chip Erase Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Full status check can be done after each full chip erase.
Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

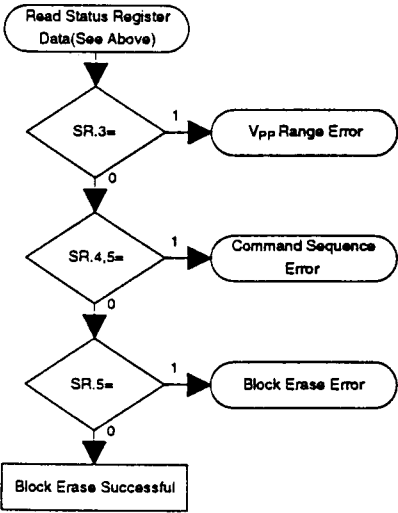| Bus Operation	Command	Comments
Standby		Check SR.3 1=Vpp Error Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status
  Register Command in cases where multiple blocks are erased
  before full status is checked.
If error is detected, clear the Status Register before attempting
  retry or other error recovery.

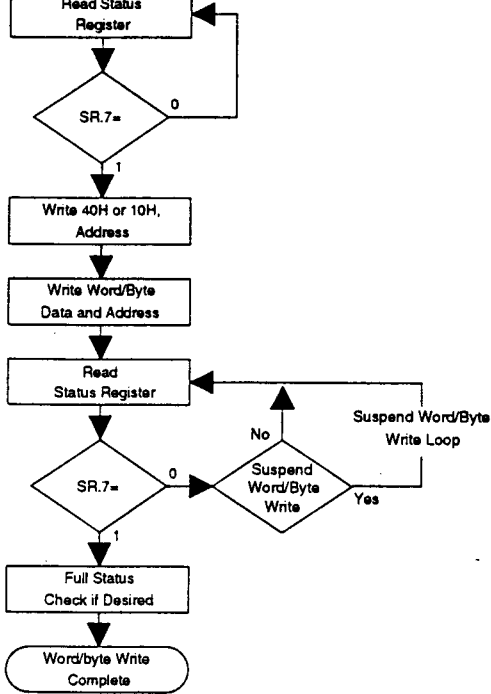Figure 10. Automated Full Chip Erase Flowchart

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Figure 11. Automated Word/byte Write Flowchart

Read Status Register

SR.7 = 0 (loop back), 1

Write 40H or 10H, Address

Write Word/Byte Data and Address

Read Status Register

SR.7 = 0 → Suspend Word/Byte Write? → Yes → Suspend Word/Byte Write Loop; No → loop back to Read Status Register

SR.7 = 1

Full Status Check if Desired

Word/byte Write Complete

FULL STATUS CHECK PROCEDURE

Read Status Register Data(See Above)

SR.3 = 1 → Vpp Range Error; 0 ↓

SR.1 = 1 → Device Protect Error; 0 ↓

SR.4 = 1 → Word/byte Write Error; 0 ↓

Word/Byte Write Successful

Bus Operation	Command	Comments
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup Word/Byte Write	Data=40H or 10H Addr=Location to Be Written
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent word/byte writes.
SR full status check can be done after each word/byte write, or after a sequence of word/byte writes.
Write FFH after the last word/byte write operation to place device in read array mode.

Bus Operation	Command	Comments
Standby		Check SR.3 1=Vpp Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=VIL,Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1=Data Write Error

SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
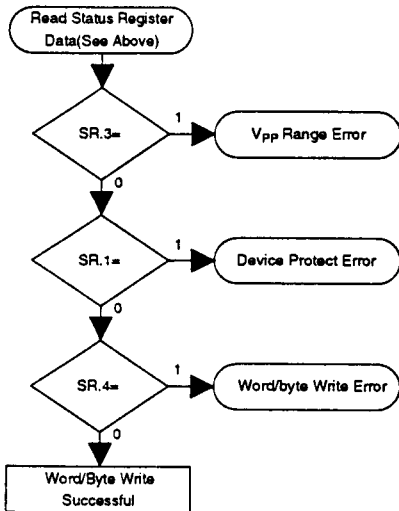If error is detected, clear the Status Register before attempting retry or other error recovery.

Read Status Register

XSR.7 = 0 → Write Buffer Time Out — No / Yes

XSR.7 = 1

Write Word or Byte Count (N-1), Start Address

Write Buffer Data, Start Address

X=0

Abort Buffer Write Command? — Yes → Write Another Block Address → Multi Word/Byte Write Abort

No

Write Buffer Data, Device Address

X = N — Yes / No

X=X+1

Write D0H

Another Buffer Write? — Yes / No

Read Status Register

SR.7 = 0 → Suspend Multi Word/Byte Write — No (Suspend Multi Word/Byte Write Loop) / Yes

SR.7 = 1

Full Status Check if Desired

Multi Word/Byte Write Complete

Command		
Write	Setup Multi Word/Byte Write	Data=E8H Addr=Start Address
Read		Extended Status Register Data
Standby		Check XSR.7 1=Multi Word/Byte Write Ready 0=Multi Word/Byte Write Busy
Write (Note2)		Data=Word or Byte Count (N-1) Addr=Start Address
Write (Note2,3)		Data=Buffer Data Addr=Start Address
Write (Note4,5)		Data=Buffer Data Addr=Device Address
Write		Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

1. Byte or word count values on DQ_{0-7} are loaded into the count register.
2. Write Buffer contents will be programmed at the start address.
3. Align the start address on a Write Buffer boundary for maximum programming performance.
4. The device aborts the Multi Word/Byte Write command if the current address is outside of the original block address.
5. The Status Register indicates an "improper command sequence" if the Multi Word/Byte command is aborted. Follow this with a Clear Status Register command. SR full status check can be done after each multi word/byte write, or after a sequence of multi word/byte writes.
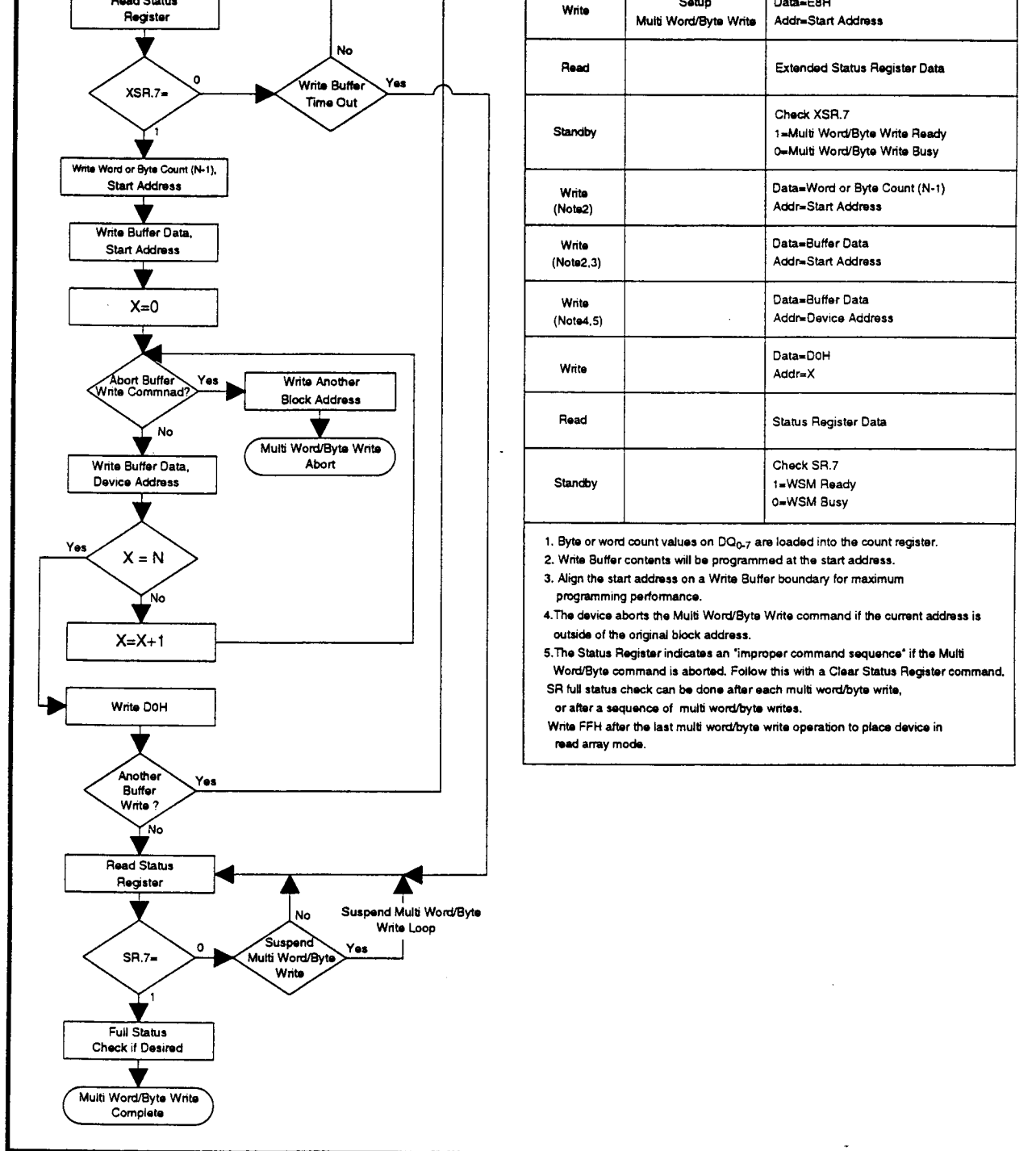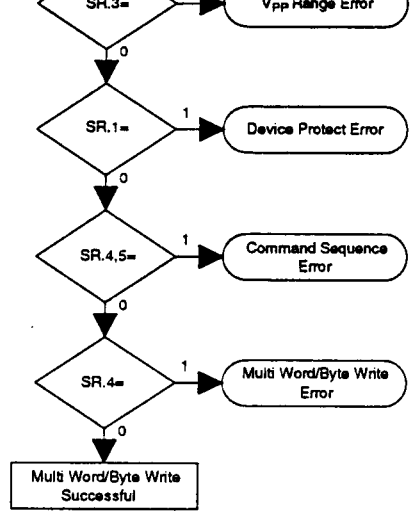Write FFH after the last multi word/byte write operation to place device in read array mode.

Figure 12. Automated Multi Word/Byte Write Flowchart

Figure 13. Full Status Check Procedure for Automated Multi Word/Byte Write

Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL},Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Data Write Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register
  command in cases where multiple locations are written before
  full status is checked.
If error is detected, clear the Status Register before attempting
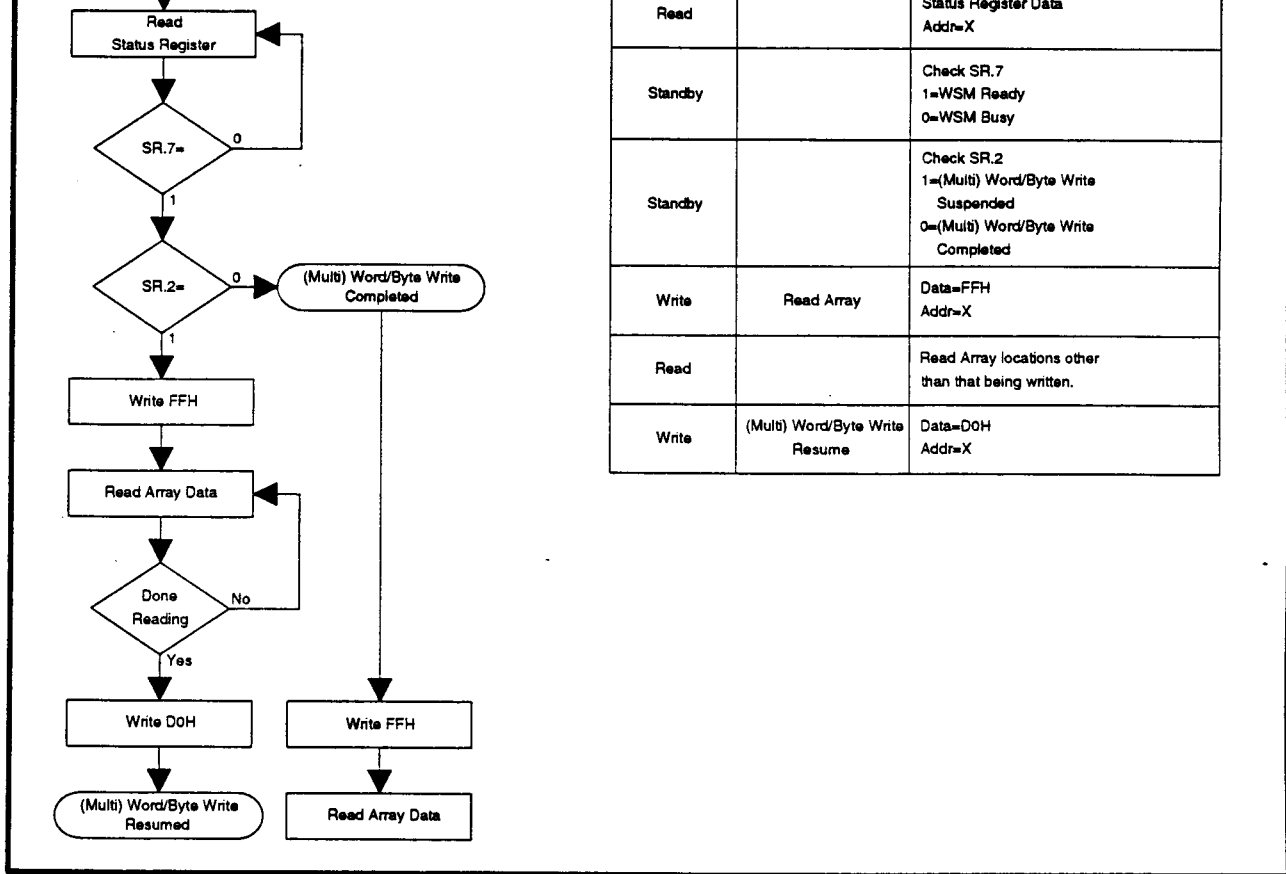 retry or other error recovery.

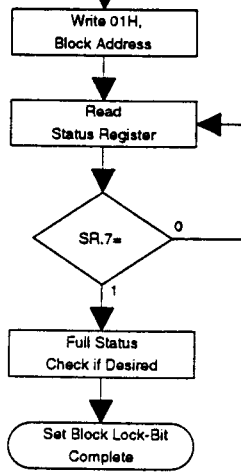|		
Read		Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Flowchart:

Read Status Register →
SR.7= : 0 (loops back to Read Status Register), 1 ↓
SR.6= : 0 → Block Erase Completed, 1 ↓
Read or Write? : Read → Read Array Data; (Multi) Word/Byte Write → (Multi) Word/Byte Write Loop
Done? : No (loops back up), Yes ↓
Write D0H → Block Erase Resumed

Block Erase Completed → Write FFH → Read Array Data

Figure 14. Block Erase Suspend/Resume Flowchart

Read Status Register

SR.7= 0 →

SR.7= 1 ↓

SR.2= 0 → (Multi) Word/Byte Write Completed

SR.2= 1 ↓

Write FFH

Read Array Data

Done Reading — No

Done Reading — Yes ↓

Write D0H

(Multi) Word/Byte Write Resumed

Write FFH

Read Array Data

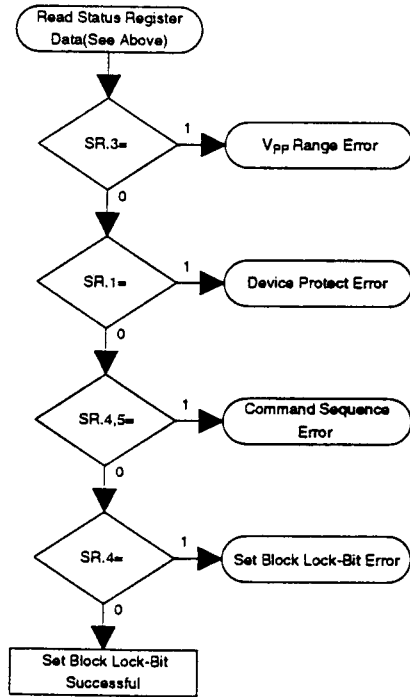|		
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=(Multi) Word/Byte Write Suspended 0=(Multi) Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	(Multi) Word/Byte Write Resume	Data=D0H Addr=X

Figure 15. (Multi) Word/Byte Write Suspend/Resume Flowchart

Figure 16. Set Block Lock-Bit Flowchart
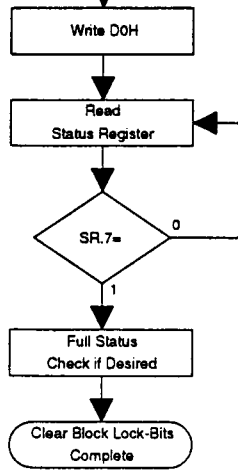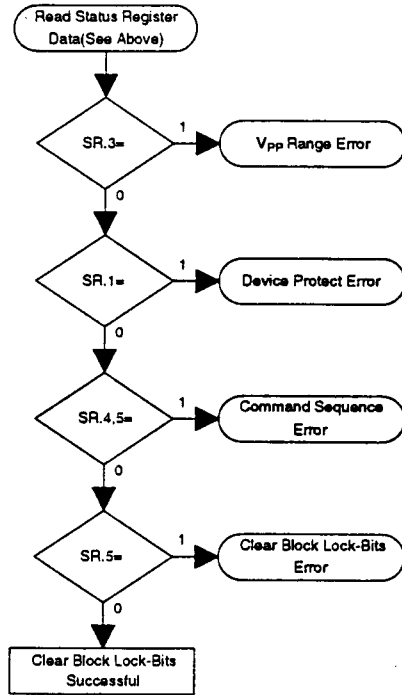
Write		Lock-Bits Confirm	Addr=X
Read			Status Register Data
Standby			Check SR.7 1=WSM Ready 0=WSM Busy

Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.

Bus Operation	Command	Comments
Standby		Check SR.3 1=V$_{PP}$ Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V$_{IL}$
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Clear Block Lock-Bits Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 17. Clear Block Lock-Bits Flowchart

Line control provides for:

    a. Lowest possible memory power dissipation.

    b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 STS and Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Polling

STS is an open drain output that should be connected to V_{CC} by a pullup resistor to provide a hardware method of detecting block erase, full chip erase, (multi) word/byte write and block lock-bit configuration completion. In default mode, it transitions low after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see the Configuration command.

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times.

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

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along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, STS(if set to RY/BY# mode) will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block and full chip erasure, (multi) word/byte writing or block lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC})

The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics— Read Only and Write Operations and Figures 21, 22, 23, 24 for more information.

Temperature under Bias .... -10°C to +80°C

Storage Temperature .... -65°C to +125°C

Voltage On Any Pin
(except V_{CC}, V_{PP}) .... -0.5V to V_{CC}+0.5V[2]

V_{CC} Supply Voltage .... -0.2V to +7.0V[2]

V_{PP} Update Voltage during
Erase, Write and
Block Lock-Bit Configuration .... -0.2V to +7.0V[2]

Output Short Circuit Current .... 100mA[3]

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	0	+70	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3V±0.3V)	3.0	3.6	V	

6.2.1 CAPACITANCE[1]

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 18. Transient Input/Output Reference Waveform for V$_{CC}$=2.7V-3.6V

3.0

INPUT ╳ 1.5 ◄──────── TEST POINTS ──────► ╳ 1.5   OUTPUT

0.0

AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

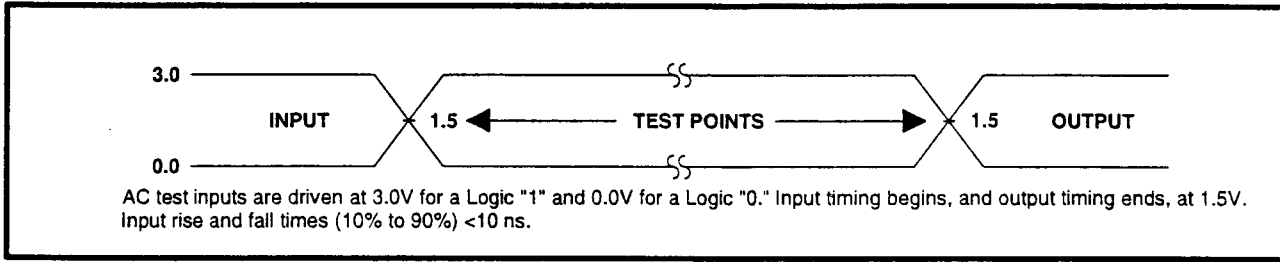**Figure 19. Transient Input/Output Reference Waveform for V$_{CC}$=3.3V±0.3V**

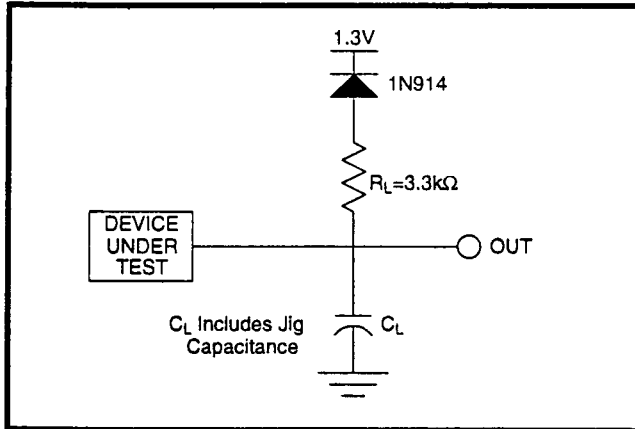**Figure 20. Transient Equivalent Testing Load Circuit**

Test Configuration Capacitance Loading Value

Test Configuration	C$_L$ (pF)
V$_{CC}$=3.3V±0.3V, 2.7V-3.6V	50

Symbol	Parameter	Notes					Unit	Test Conditions
I_{LO}	Output Leakage Current	1		±0.5		±0.5	μA	$V_{CC}=V_{CC}$Max $V_{OUT}=V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	20	100	20	100	μA	CMOS Inputs $V_{CC}=V_{CC}$Max CE#=RP#=V_{CC}±0.2V
			1	4	1	4	mA	TTL Inputs $V_{CC}=V_{CC}$Max CE#=RP#=V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1		15		15	μA	RP#=GND±0.2V I_{OUT}(STS)=0mA
I_{CCR}	V_{CC} Read Current	1,5,6		25		25	mA	CMOS Inputs $V_{CC}=V_{CC}$Max, CE#=GND f=5MHz, I_{OUT}=0mA
				30		30	mA	TTL Inputs $V_{CC}=V_{CC}$Max, CE#=V_{IL} f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Write Current ((Multi) W/B Write or Set Block Lock Bit)	1,7		17	—	—	mA	V_{PP}=2.7V-3.6V
				17		17	mA	V_{PP}=3.3V±0.3V
				17		17	mA	V_{PP}=5.0V±10%
I_{CCE}	V_{CC} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits)	1,7		17	—	—	mA	V_{PP}=2.7V-3.6V
				17		17	mA	V_{PP}=3.3V±0.3V
				17		17	mA	V_{PP}=5.0V±10%
I_{CCWS} I_{CCES}	V_{CC} Write or Block Erase Suspend Current	1,2	1	6	1	6	mA	CE#=V_{IH}
I_{PPS}	V_{PP} Standby Current	1	±2	±15	±2	±15	μA	$V_{PP} \leq V_{CC}$
I_{PPR}	V_{PP} Read Current	1	10	200	10	200	μA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	0.1	5	μA	RP#=GND±0.2V
I_{PPW}	V_{PP} Write Current ((Multi) W/B Write or Set Block Lock Bit)	1,7		80	—	—	mA	V_{PP}=2.7V-3.6V
				80		80	mA	V_{PP}=3.3V±0.3V
				80		80	mA	V_{PP}=5.0V±10%
I_{PPE}	V_{PP} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits)	1,7		40	—	—	mA	V_{PP}=2.7V-3.6V
				40		40	mA	V_{PP}=3.3V±0.3V
				40		40	mA	V_{PP}=5.0V±10%
I_{PPWS} I_{PPES}	V_{PP} Write or Block Erase Suspend Current	1	10	200	10	200	μA	$V_{PP}=V_{PPH1/2/3}$

Symbol	Parameter	Notes	Min	Max	Min	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	3,7		0.4		0.4	V	$V_{CC}=V_{CC}Min$ $I_{OL}=2mA$
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		2.4		V	$V_{CC}=V_{CC}Min$ $I_{OH}=-2.5mA$
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		0.85 V_{CC}		V	$V_{CC}=V_{CC}Min$ $I_{OH}=-2.5\mu A$
			V_{CC} -0.4		V_{CC} -0.4		V	$V_{CC}=V_{CC}Min$ $I_{OH}=-100\mu A$
V_{PPLK}	V_{PP} Lockout Voltage during Normal Operations	4,7		1.5		1.5	V	
V_{PPH1}	V_{PP} Voltage during Write or Erase Operations		2.7	3.6	—	—	V	
V_{PPH2}	V_{PP} Voltage during Write or Erase Operations		3.0	3.6	3.0	3.6	V	
V_{PPH3}	V_{PP} Voltage during Write or Erase Operations		4.5	5.5	4.5	5.5	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes STS.
4. Block erases, full chip erases, (multi) word/byte writes and block lock-bit configurations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), between V_{PPH2}(max) and V_{PPH3}(min) and above V_{PPH3}(max).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA at 2.7V and 3.3V V_{CC} in static operation.
6. CMOS inputs are either $V_{CC}\pm0.2V$ or GND$\pm0.2V$. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.

Sym.	Parameter	Notes		Max.		Max.	Unit
t_{ELQV}	CE# to Output Delay	2		120		150	ns
t_{PHQV}	RP# High to Output Delay			600		600	ns
t_{GLQV}	OE# to Output Delay	2		50		55	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		50		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20		25	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		120		150	ns
t_{FLQZ}	BYTE# to Output in High Z	3		30		40	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		5	ns

NOTE:
See 3.3V V_{CC} Read-Only Operations for notes 1 through 4.

$V_{CC}=3.3V\pm0.3V$, $T_A=0°C$ to $+70°C$

Versions[4]			LH28F160S3-L100		LH28F160S3-L130		
Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		100		130		ns
t_{AVQV}	Address to Output Delay			100		130	ns
t_{ELQV}	CE# to Output Delay	2		100		130	ns
t_{PHQV}	RP# High to Output Delay			600		600	ns
t_{GLQV}	OE# to Output Delay	2		45		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		50		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20		25	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		100		130	ns
t_{FLQZ}	BYTE# to Output in High Z	3		30		40	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		5	ns

NOTES:
1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).

NOTE: CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.
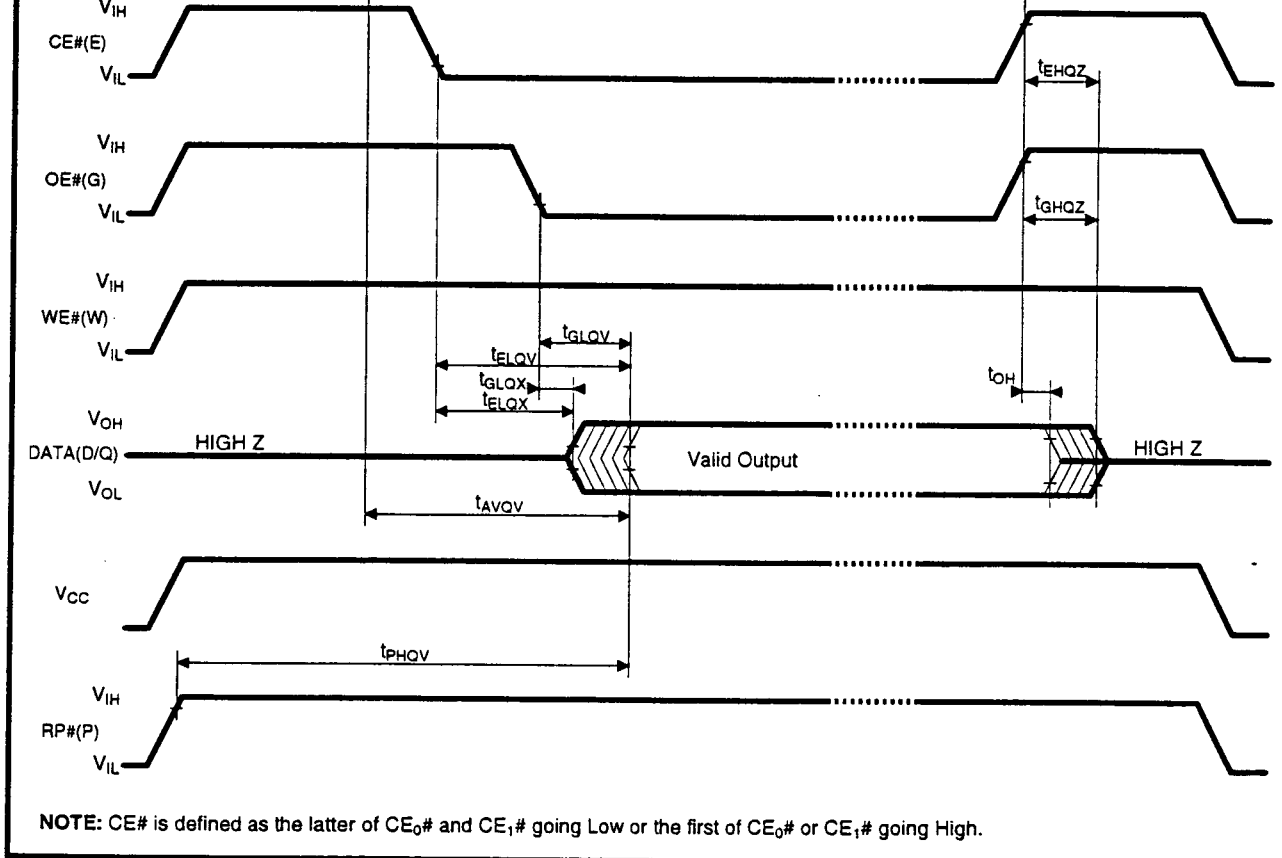
Figure 21. AC Waveform for Read Operations
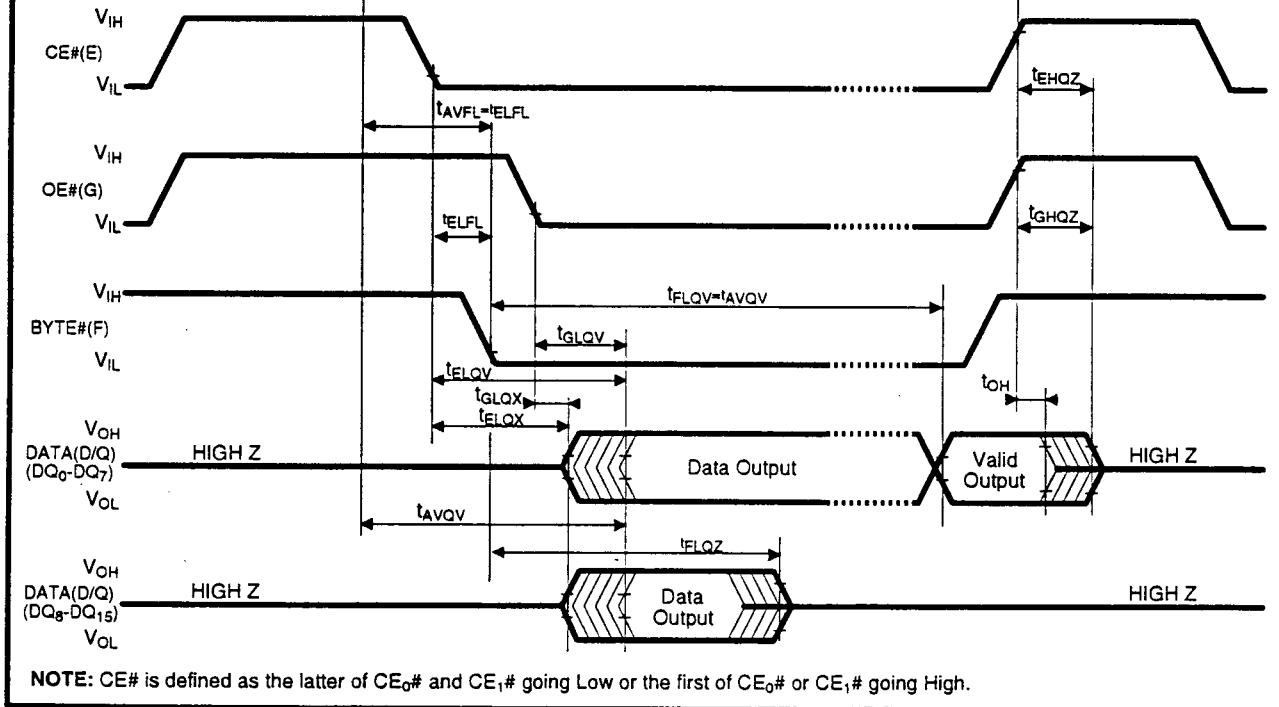
Figure 22. BYTE# Timing Waveforms

NOTE: CE# is defined as the latter of CE$_0$# and CE$_1$# going Low or the first of CE$_0$# or CE$_1$# going High.

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Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
	Low						µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		50		ns
t_{WHDX}	Data Hold from WE# High		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHBL}	WE# High to STS Going Low			100		100	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		0		ns

NOTE:

See 3.3V V_{CC} WE#-Controlled Writes for notes 1 through 5.

$V_{CC}=3.3V\pm0.3V$, $T_A=0°C$ to $+70°C$

Versions[5]			LH28F160S3-L100		LH28F160S3-L130		
Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		130		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	WE# Pulse Width		50		50		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		50		ns
t_{WHDX}	Data Hold from WE# High		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHBL}	WE# High to STS Going Low			100		100	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		0		ns

NOTES:

1. Read timing characteristics during block erase, full chip erase, (multi) wrod/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
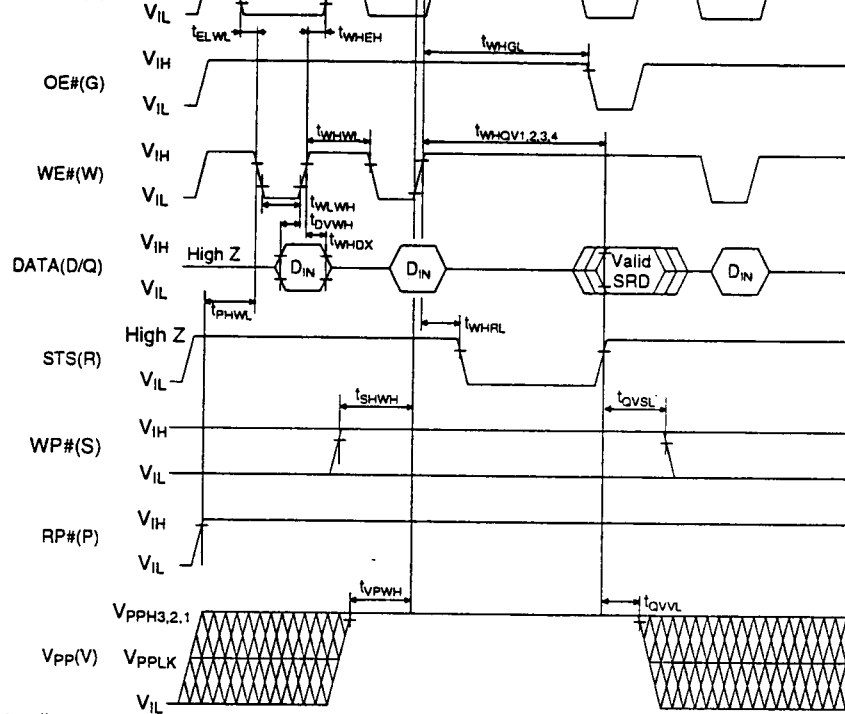
NOTES:
1. V_{CC} power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.
7. CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 23. AC Waveform for WE#-Controlled Write Operations

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t_{PHEL}	RP# High Recovery to CE# Going Low	2	1			1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0			0		ns
t_{ELEH}	CE# Pulse Width		70			70		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100			100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100			100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50			50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50			50		ns
t_{EHDX}	Data Hold from CE# High		5			5		ns
t_{EHAX}	Address Hold from CE# High		5			5		ns
t_{EHWH}	WE# Hold from CE# High		0			0		ns
t_{EHEL}	CE# Pulse Width High		25			25		ns
t_{EHRL}	CE# High to STS Going Low			100			100	ns
t_{EHGL}	Write Recovery before Read		0			0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0			0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0			0		ns

NOTE:

See 3.3V V_{CC} Alternative CE#-Controlled Writes for notes 1 through 5.

$$V_{CC}=3.3V\pm0.3V,\ T_A=0°C\ to\ +70°C$$

	Versions[5]			LH28F160S3-L100		LH28F160S3-L130		
Sym.	**Parameter**	**Notes**	**Min.**	**Max.**	**Min.**	**Max.**		**Unit**
t_{AVAV}	Write Cycle Time		100		130			ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		1			µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0			ns
t_{ELEH}	CE# Pulse Width		70		70			ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		100			ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100			ns
t_{AVEH}	Address Setup to CE# Going High	3	50		50			ns
t_{DVEH}	Data Setup to CE# Going High	3	50		50			ns
t_{EHDX}	Data Hold from CE# High		5		5			ns
t_{EHAX}	Address Hold from CE# High		5		5			ns
t_{EHWH}	WE# Hold from CE# High		0		0			ns
t_{EHEL}	CE# Pulse Width High		25		25			ns
t_{EHRL}	CE# High to STS Going Low			100		100		ns
t_{EHGL}	Write Recovery before Read		0		0			ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		0			ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		0			ns

NOTES:

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
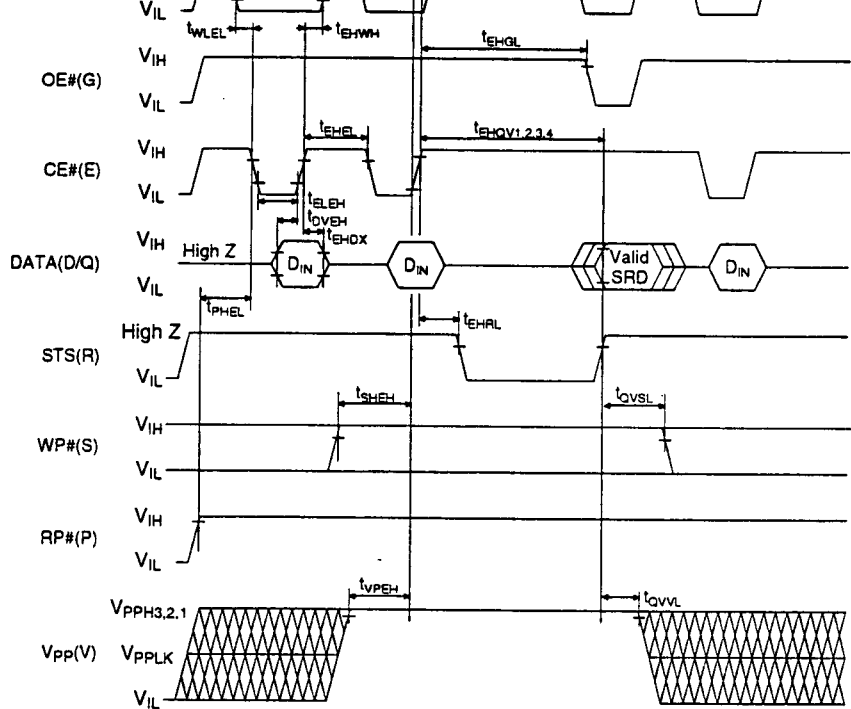
NOTES:
1. V_{CC} power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.
7. CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

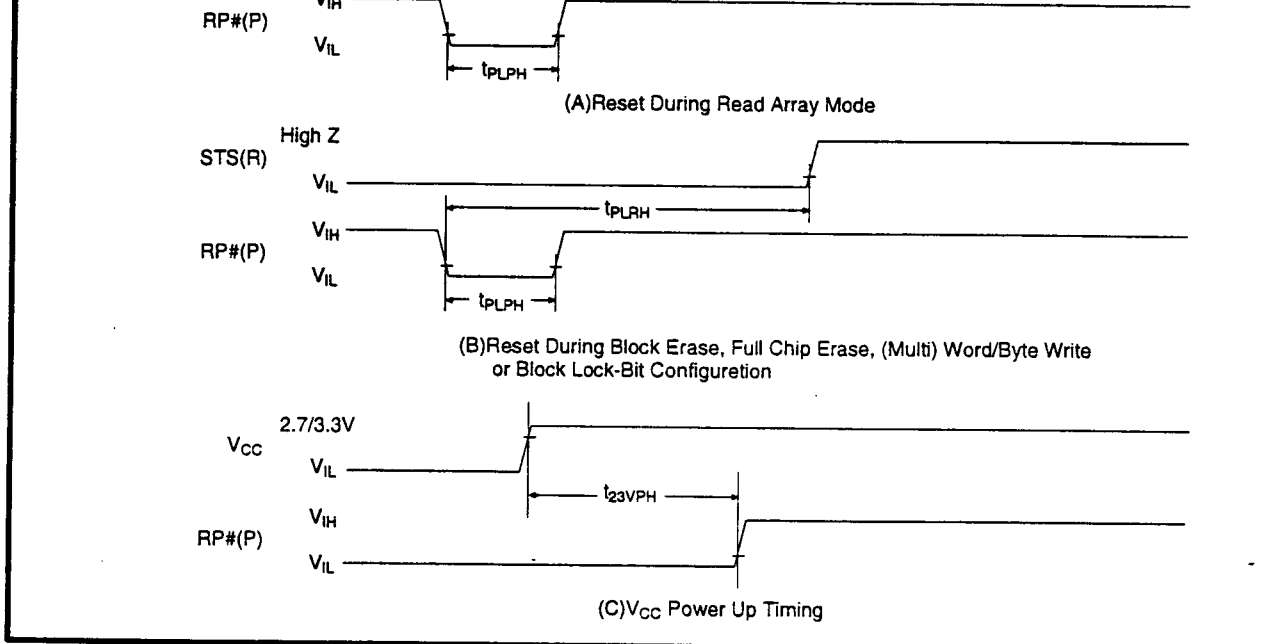**Figure 24. Alternate AC Waveform for CE#-Controlled Write Operations**

(A)Reset During Read Array Mode

(B)Reset During Block Erase, Full Chip Erase, (Multi) Word/Byte Write
or Block Lock-Bit Configuretion

(C)V$_{CC}$ Power Up Timing

Figure 25. AC Waveform for Reset Operation

Reset AC Specifications[1]

Symbol	Parameter	Notes	V$_{CC}$=2.7V		V$_{CC}$=3.3V		Unit
			Min.	Max.	Min.	Max.	
t$_{PLPH}$	RP# Pulse Low Time (If RP# is tied to V$_{CC}$, this specification is not applicable)		100		100		ns
t$_{PLRH}$	RP# Low to Reset during Block Erase, Full Chip Erase, (Multi) Word/Byte Write or Block Lock-Bit Configuration	2,3		20		20	µs
t$_{23VPH}$	V$_{CC}$ at 2.7V to RP# High V$_{CC}$ at 3.0V to RP# High	4		50		50	µs

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is not executing, the reset will complete within 100ns.
3. A reset time, t$_{PHQV}$, is required from the latter of STS going High Z or RP# going high until outputs are valid.
4. When the device power-up, holding RP# low minimum 100ns is required after V$_{CC}$ has been in predefined range and also has been in stable there.

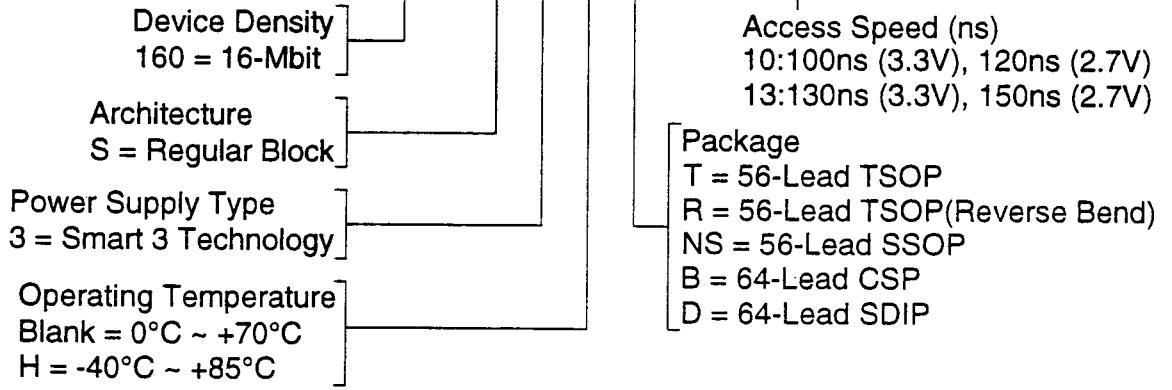| Symbol	Parameter	Note		Min	Max		Min	Max		Min	Max	Unit
t$_{WHQV1}$ t$_{EHQV1}$	(using W/B write, in word mode)	2		22.17	TBD		22.17	TBD		13.2	TBD	µs
t$_{WHQV1}$ t$_{EHQV1}$	Word/Byte Write Time (using W/B write, in byte mode)	2		19.89	TBD		19.89	TBD		13.2	TBD	µs
	Word/Byte Write Time (using multi word/byte write)	2		5.76	TBD		5.76	TBD		2.76	TBD	µs
	Block Write Time (using W/B write, in word mode)	2		0.91	TBD		0.91	TBD		0.44	TBD	sec
	Block Write Time (using W/B write, in byte mode)	2		1.63	TBD		1.63	TBD		0.87	TBD	sec
	Block Write Time (using multi word/byte write)	2		0.37	TBD		0.37	TBD		0.18	TBD	sec
t$_{WHQV2}$ t$_{EHQV2}$	Block Erase Time	2		0.56	TBD		0.56	TBD		0.42	TBD	sec
	Full Chip Erase Time			17.9	TBD		17.9	TBD		13.3	TBD	sec
t$_{WHQV3}$ t$_{EHQV3}$	Set Block Lock-Bit Time	2		22.17	TBD		22.17	TBD		13.2	TBD	µs
t$_{WHQV4}$ t$_{EHQV4}$	Clear Block Lock-Bits Time	2		0.56	TBD		0.56	TBD		0.42	TBD	sec
t$_{WHRH1}$ t$_{EHRH1}$	Write Suspend Latency Time to Read			7.24	10.2		7.24	10.2		6.73	9.48	µs
t$_{WHRH2}$ t$_{EHRH2}$	Erase Suspend Latency Time to Read			15.5	21.5		15.5	21.5		12.54	17.54	µs

NOTE:

See 3.3V V$_{CC}$ Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Performance for notes 1 through 4.

				Min	Max		Min	Max	Unit
	Word/Byte Write Time (using multi word/byte write)	2		5.66	TBD		2.7	TBD	µs
	Block Write Time (using W/B write, in word mode)	2		0.89	TBD		0.43	TBD	sec
	Block Write Time (using W/B write, in byte mode)	2		1.6	TBD		0.85	TBD	sec
	Block Write Time (using multi word/byte write)	2		0.36	TBD		0.18	TBD	sec
t_{WHQV2} t_{EHQV2}	Block Erase Time	2		0.55	TBD		0.41	TBD	sec
	Full Chip Erase Time			17.6	TBD		13.1	TBD	sec
t_{WHQV3} t_{EHQV3}	Set Block Lock-Bit Time	2		21.75	TBD		12.95	TBD	µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2		0.55	TBD		0.41	TBD	sec
t_{WHRH1} t_{EHRH1}	Write Suspend Latency Time to Read			7.1	10		6.6	9.3	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			15.2	21.1		12.3	17.2	µs

NOTES:

1. Typical values measured at T_A=+25°C and nominal voltages. Assumes corresponding block lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

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| | | LH | 28 | F | 1 | 6 | 0 | S | 3 | (H) | T | - | L | 1 | 0 |

Device Density
160 = 16-Mbit

Architecture
S = Regular Block

Power Supply Type
3 = Smart 3 Technology

Operating Temperature
Blank = 0°C ~ +70°C
H = -40°C ~ +85°C

Access Speed (ns)
10:100ns (3.3V), 120ns (2.7V)
13:130ns (3.3V), 150ns (2.7V)

Package
T = 56-Lead TSOP
R = 56-Lead TSOP(Reverse Bend)
NS = 56-Lead SSOP
B = 64-Lead CSP
D = 64-Lead SDIP

		Valid Operational Combinations	
		V_{CC}=2.7-3.6V 50pF load, 1.35V I/O Levels	V_{CC}=3.3±0.3V 50pF load, 1.5V I/O Levels
Option	Order Code		
1	LH28F160S3XX-L10	LH28F160S3-L120	LH28F160S3-L100
2	LH28F160S3XX-L13	LH28F160S3-L150	LH28F160S3-L130

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LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX LH28F160S3-L 16M(2Mx8/1Mx16) Smart3 Voltage