18Mb NtRAM™ Specification

100TQFP/165FBGA with Pb/Pb-Free
(RoHS compliant)

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Document Title

512Kx36 & 1Mx18-Bit Flow Through N*t*RAM™

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	Mar. 23. 2004	Advance
0.1	1. Update the DC current spec(I_{CC}, I_{SB})	May. 21. 2004	Preliminary
0.2	1. Change the ISB,ISB1,ISB2 - ISB ; from 120mA to 170mA - ISB1 ; from 80mA to 150mA - ISB2 ; from 80mA to 130mA	Sep. 21. 2004	Preliminary
0.3	1. Remove the 1.8V Vdd voltage level	Oct. 18. 2004	Preliminary
0.4	1. Remove the -75 speed bin	Jan. 04. 2004	Preliminary
1.0	1. Finalize the datasheet	July 18. 2005	Final
2.0	1. Add the overshoot timing	Feb. 16. 2006	Final
3.0	1. Change ordering information	Apr. 04. 2006	Final

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18Mb NtRAM (Flow Through) Ordering Information

Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
1Mx18	3.3/2.5	7.5	6.5	K7M161835B-P(Q)[1]C(I)[2]65	√
512Kx36	3.3/2.5	7.5	6.5	K7M163635B-P(Q)[1]C(I)[2]65	√

Note 1. P(Q) [Package type] : P-Pb Free, Q-Pb
    2. C(I)   [Operating Temperature] : C-Commercial, I-Industrial

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512Kx36 & 1Mx18-Bit Flow Through N*t*RAM™

FEATURES

- V$_{DD}$= 2.5 or 3.3V +/- 5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A (Lead and Lead free package)
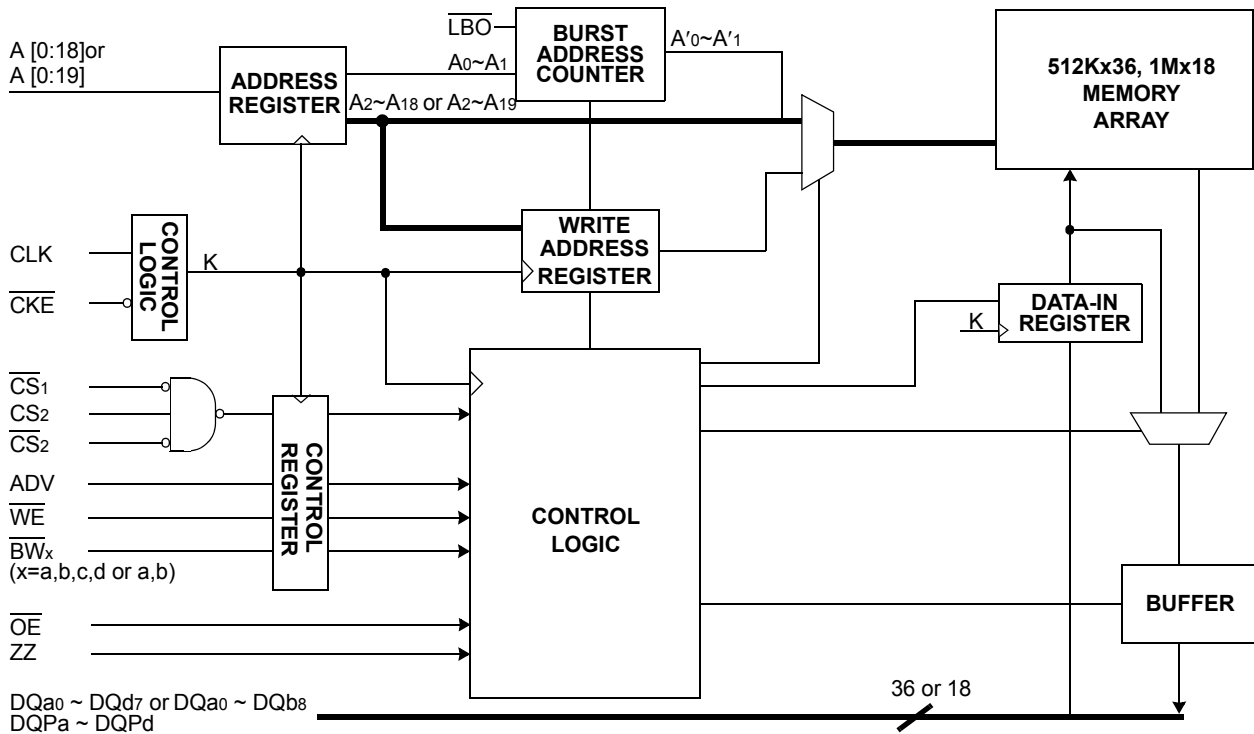- Operating in commeical and industrial temperature range.

GENERAL DESCRIPTION

The K7M163635B and K7M161835B are 18,874,368-bits Synchronous Static SRAMs.

The N*t*RAM™, or No Turnaround Random Access Memory utilizes all bandwidth in any combination of operating cycles.

Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ).

Output Enable controls the outputs at any given time.

Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation

and provides increased timing flexibility for incoming signals.

For read cycles, Flow-Through SRAM allows output data to simply flow freely from the memory array.

The K7M163635B and K7M161835B are implemented with SAMSUNG′s high performance CMOS technology and is available in 100pin TQFP packages. Multiple power and ground pins minimize ground bounce.

FAST ACCESS TIMES

Parameter	Sym.	-65	Unit
Cycle Time	t$_{CYC}$	7.5	ns
Clock Access Time	t$_{CD}$	6.5	ns
Output Enable Access Time	t$_{OE}$	3.5	ns

LOGIC BLOCK DIAGRAM

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PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP

(20mm x 14mm)

K7M163635B(512Kx36)
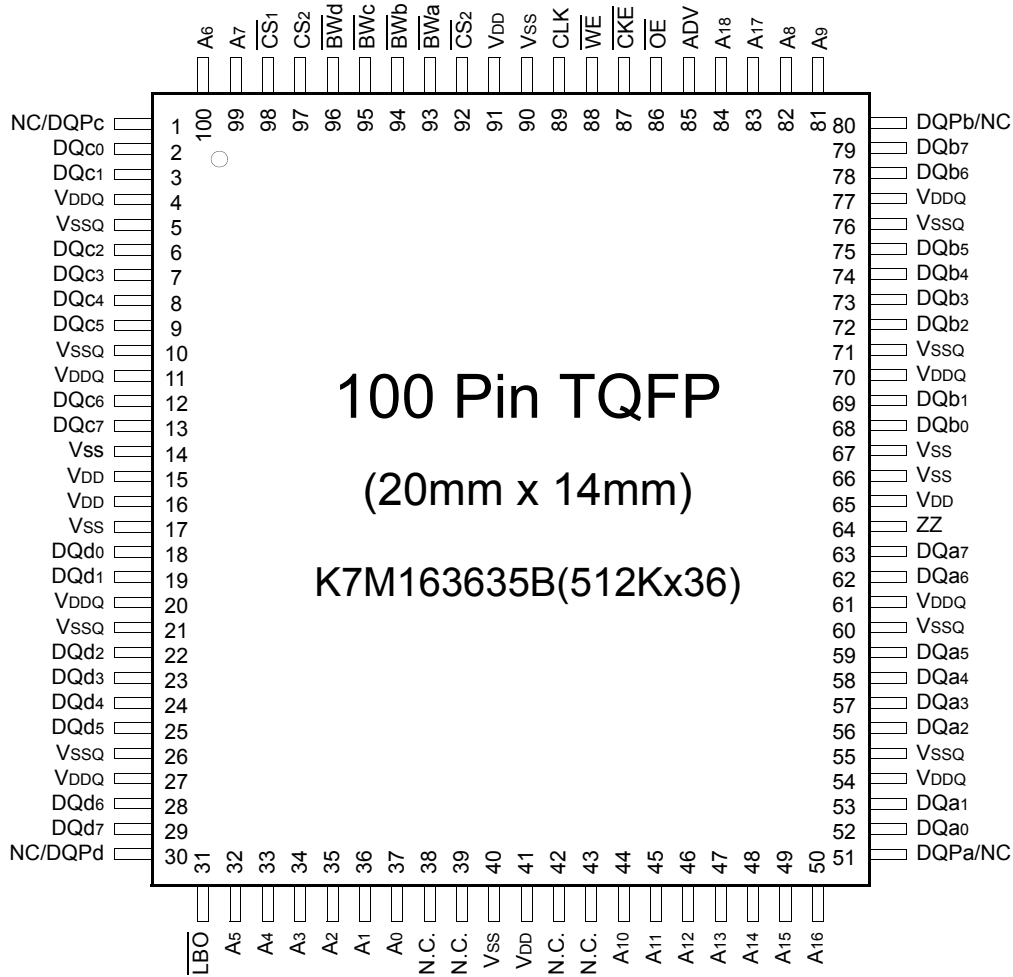
PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{18}	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,81 82,83,84,99,100	V_{DD} V_{SS}	Power Supply(+3.3V) Ground	15,16,41,65,91 14,17,40,66,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	38,39,42,43
$\overline{WE}$	Read/Write Control Input	88			
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{CKE}$	Clock Enable	87	DQb0~b7	Data Inputs/Outputs	68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	DQc0~c7	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS_2	Chip Select	97	DQd0~d7	Data Inputs/Outputs	18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	DQPa~Pd	Data Inputs/Outputs	51,80,1,30
$\overline{BWx}$(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	or NC		
$\overline{OE}$	Output Enable	86			
ZZ	Power Sleep Mode	64	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{LBO}$	Burst Mode Control	31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP

(20mm x 14mm)

K7M161835B(1Mx18)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,80 81,82,83,84,99,100	V_{DD} V_{SS}	Power Supply(+3.3V) Ground	15,16,41,65,91 14,17,40,66,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,25,28,29,30,
$\overline{WE}$	Read/Write Control Input	88			38,39,42,43,51,52,53,
CLK	Clock	89			56,57,75,78,79,95,96
$\overline{CKE}$	Clock Enable	87			
$\overline{CS_1}$	Chip Select	98	$DQa_0{\sim}a_8$	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CS_2	Chip Select	97	$DQb_0{\sim}b_8$	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
$\overline{CS_2}$	Chip Select	92			
$\overline{BWx}(x{=}a,b)$	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{ZZ}$	Power Sleep Mode	64			
$\overline{LBO}$	Burst Mode Control	31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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FUNCTION DESCRIPTION

The K7M163635B and K7M161835B are N*t*RAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

N*t*RAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS}_1$, CS_2, $\overline{CS}_2$) are active .
Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS}_1$, CS_2, $\overline{CS}_2$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. Data appears at the outputs within the same clock cycle as the address for the data. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The Flow Through N*t*RAM™ uses a late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required one cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.
The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.
And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$=High)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$=Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

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STATE DIAGRAM FOR N*t*RAM™
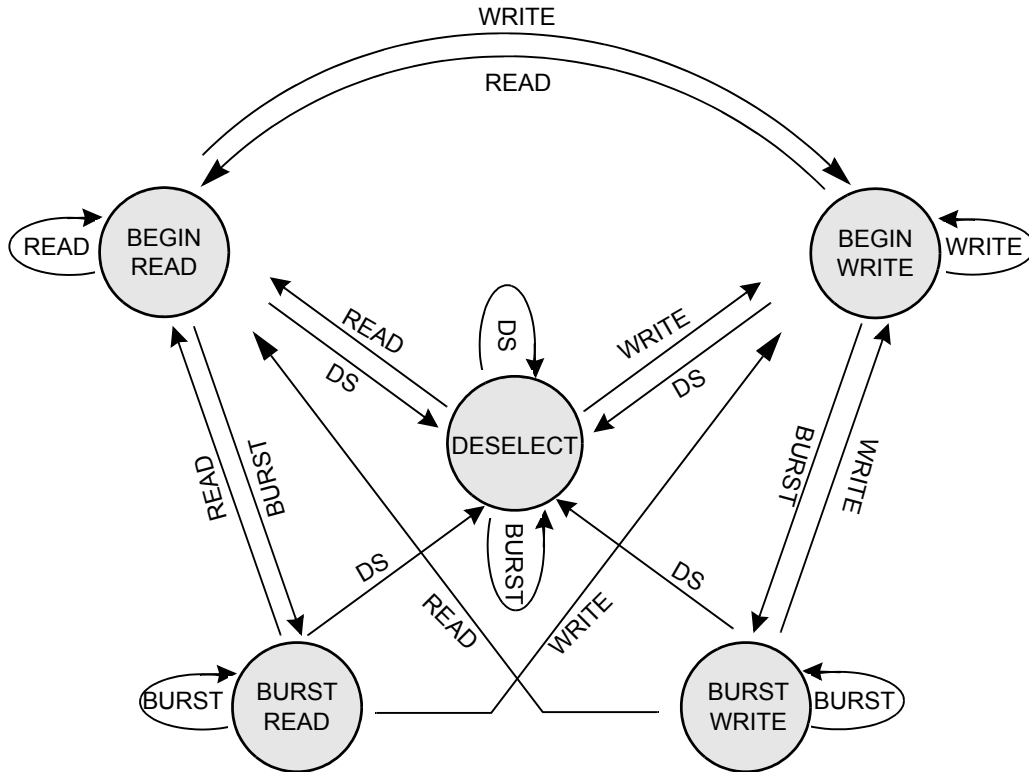
COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown is the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don't Care".   2. The rising edge of clock is symbolized by (↑).

3. A continue deselect cycle can only be enterd if a deselect cycle is executed first.

4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTEs
L	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
Read	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
Operating Temperature	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS $(0°C \leq T_A \leq 70°C)$

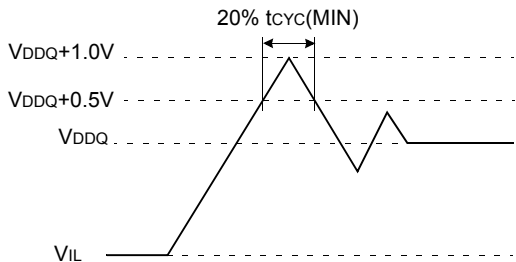| PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD1}	2.375	2.5	2.625	V
Supply Voltage	V_{DDQ1}	2.375	2.5	2.625	V
Supply Voltage	V_{DD2}	3.135	3.3	3.465	V
Supply Voltage	V_{DDQ2}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$
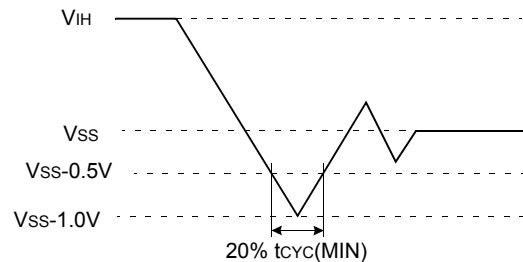
CAPACITANCE*$(T_A=25°C, f=1MHz)$

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	6	pF

*Note : Sampled not 100% tested.

Overshoot Timing

Undershoot Timing

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, $ZZ{\leq}V_{IL}$, Cycle Time $\geq$ t_{CYC} Min	-65	-	300	mA	1,2
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, $ZZ{\leq}V_{IL}$, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-65	-	170	mA	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	150	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	130	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
      2. Reference AC Operating Conditions and Characteristics for input and timing.
      3. Data states are all zero.
      4. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.

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Output Load(A)

Output Load(B),
(for t$_{LZC}$, t$_{LZOE}$, t$_{HZOE}$ & t$_{HZC}$)

+3.3V for 3.3V I/O
/+2.5V for 2.5V I/O

Dout

RL=50Ω

VL=1.5V for 3.3V I/O
V$_{DDQ}$/2 for 2.5V I/O

Zo=50Ω

Dout

319Ω / 1667Ω

353Ω / 1538Ω

5pF*
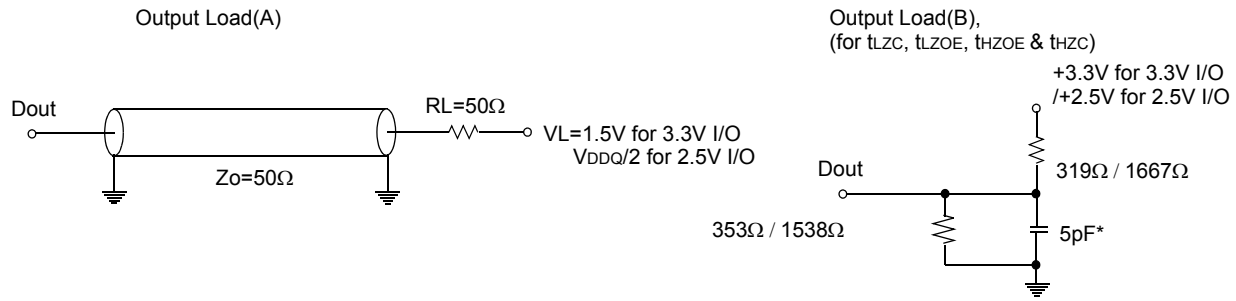
* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-65		UNIT
		MIN	MAX	
Cycle Time	t$_{CYC}$	7.5	-	ns
Clock Access Time	t$_{CD}$	-	6.5	ns
Output Enable to Data Valid	t$_{OE}$	-	3.5	ns
Clock High to Output Low-Z	t$_{LZC}$	2.5	-	ns
Output Hold from Clock High	t$_{OH}$	2.5	-	ns
Output Enable Low to Output Low-Z	t$_{LZOE}$	0	-	ns
Output Enable High to Output High-Z	t$_{HZOE}$	-	3.5	ns
Clock High to Output High-Z	t$_{HZC}$	-	3.8	ns
Clock High Pulse Width	t$_{CH}$	2.5	-	ns
Clock Low Pulse Width	t$_{CL}$	2.5	-	ns
Address Setup to Clock High	t$_{AS}$	1.5	-	ns
$\overline{CKE}$ Setup to Clock High	t$_{CES}$	1.5	-	ns
Data Setup to Clock High	t$_{DS}$	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x)	t$_{WS}$	1.5	-	ns
Address Advance Setup to Clock High	t$_{ADVS}$	1.5	-	ns
Chip Select Setup to Clock High	t$_{CSS}$	1.5	-	ns
Address Hold from Clock High	t$_{AH}$	0.5	-	ns
$\overline{CKE}$ Hold from Clock High	t$_{CEH}$	0.5	-	ns
Data Hold from Clock High	t$_{DH}$	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BW}$x)	t$_{WH}$	0.5	-	ns
Address Advance Hold from Clock High	t$_{ADVH}$	0.5	-	ns
Chip Select Hold from Clock High	t$_{CSH}$	0.5	-	ns
ZZ High to Power Down	t$_{PDS}$	2	-	cycle
ZZ Low to Power Up	t$_{PUS}$	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
4. A write cycle is defined by $\overline{WE}$ low having been registerd into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
5. To avoid bus contention, At a given vlotage and temperature t$_{LZC}$ is more than t$_{HZC}$.
The soecs as shown do not imply bus contention because t$_{LZC}$ is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than t$_{HZC}$, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperatue.

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SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SLEEP MODE during t_{PUS}, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.
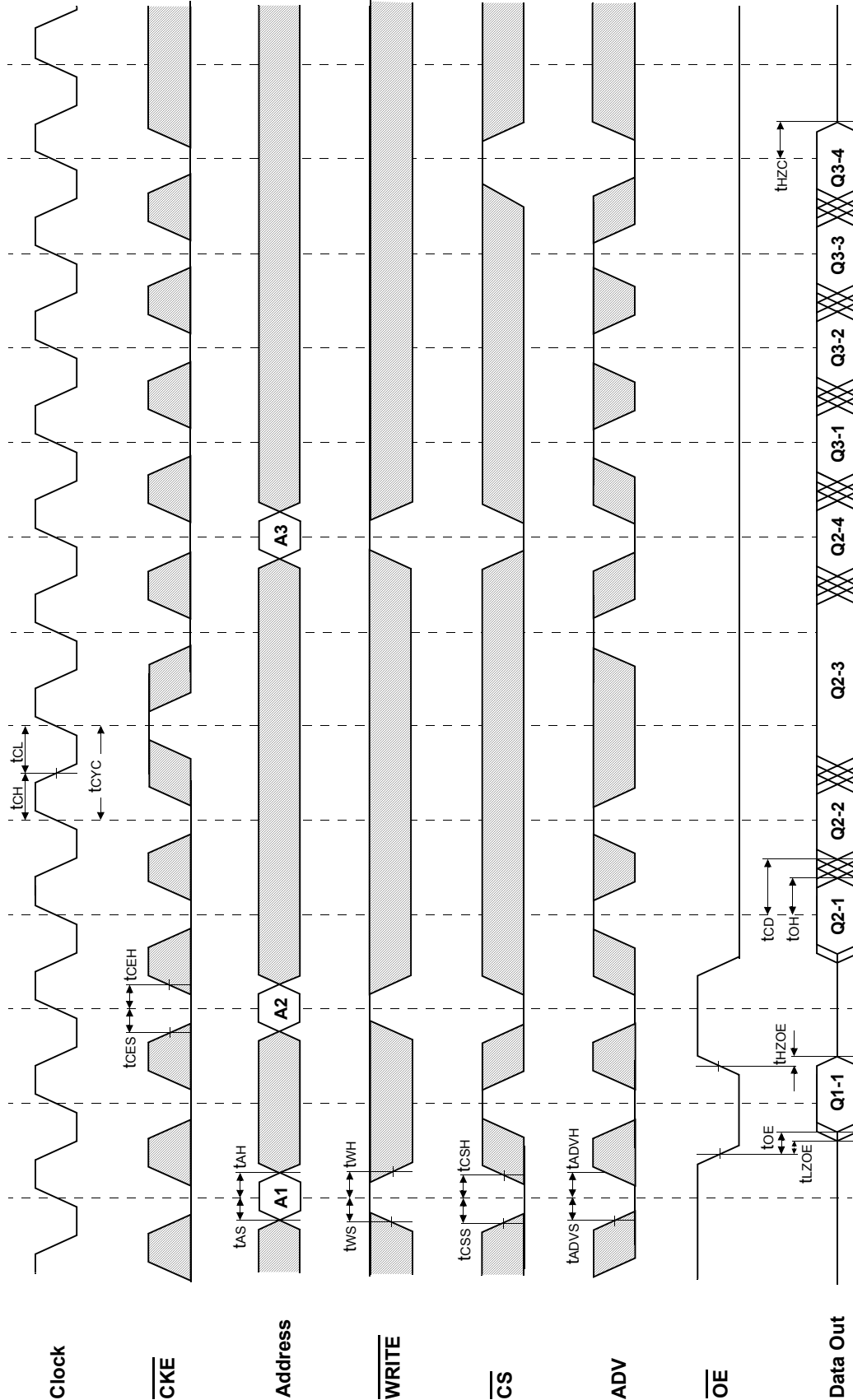
SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	ZZ ≥ V$_{IH}$	I$_{SB2}$		130	mA
ZZ active to input ignored		t$_{PDS}$	2		cycle
ZZ inactive to input sampled		t$_{PUS}$	2		cycle
ZZ active to SLEEP current		t$_{ZZI}$		2	cycle
ZZ inactive to exit SLEEP current		t$_{RZZI}$	0		

SLEEP MODE WAVEFORM

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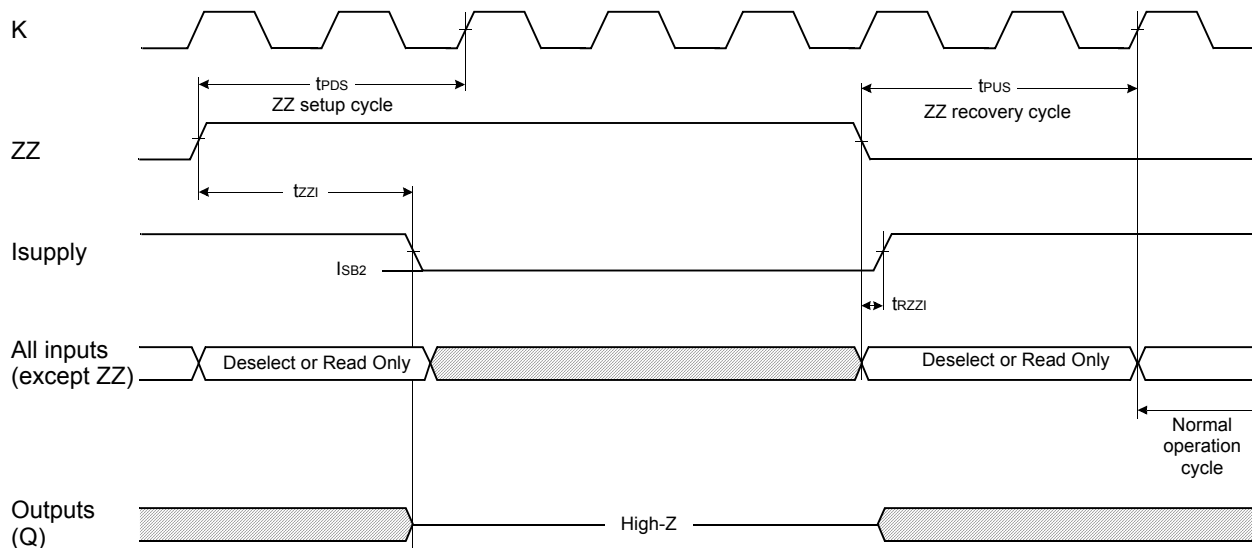
TIMING WAVEFORM OF READ CYCLE

NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS₁ = L, CS₂ = H and CS₂ = L
CS = L means CS₁ = L, CS₂ = H and CS₂ = L
CS = H means CS₁ = H, or CS₁ = L and CS₂ = H, or CS₁ = L, and CS₂ = L

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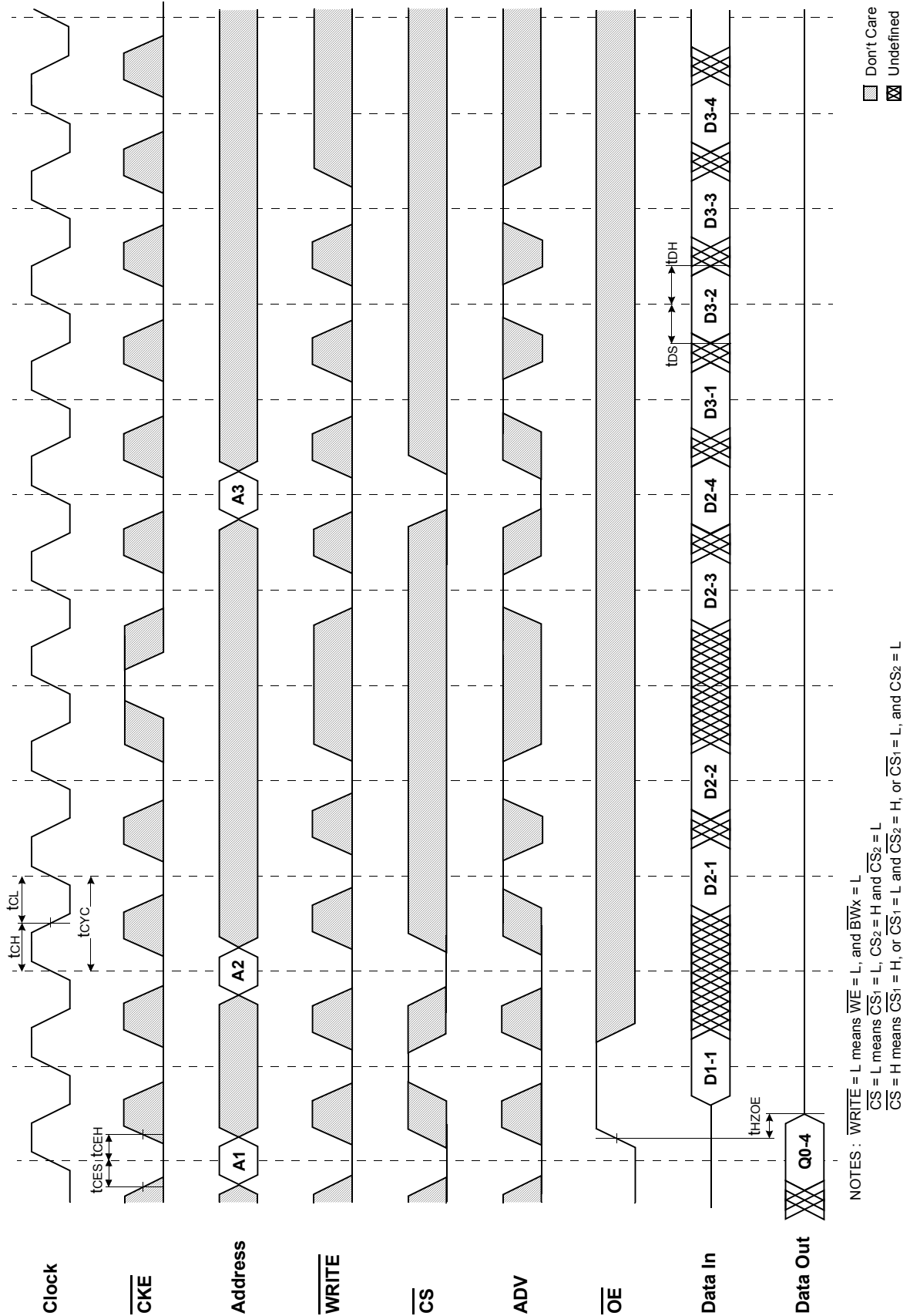**TIMING WAVEFORM OF WRTE CYCLE**
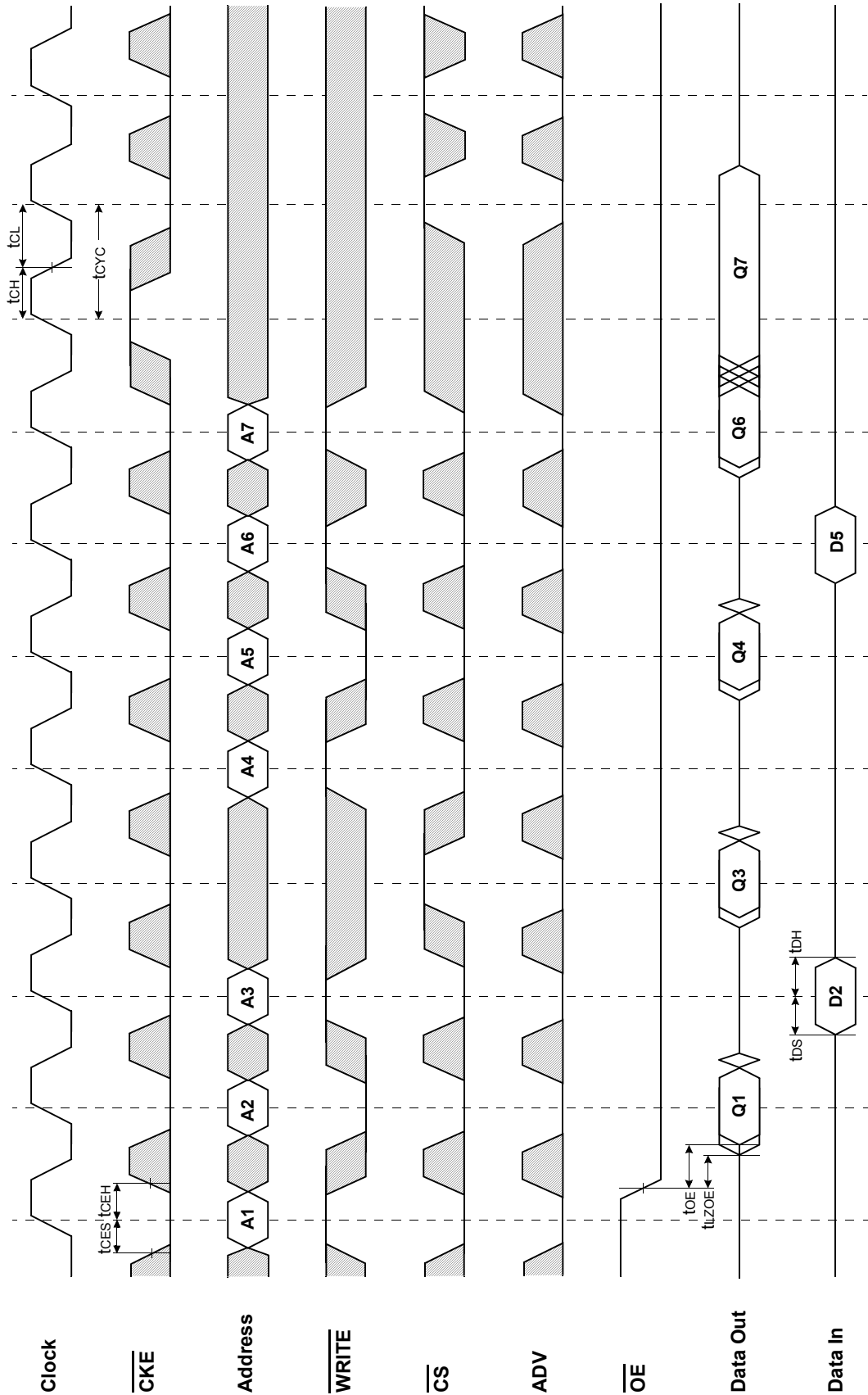

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BW}x$ = L
$\overline{CS}$ = L means $\overline{CS}_1$ = L, CS_2 = H and $\overline{CS}_2$ = L
$\overline{CS}$ = H means $\overline{CS}_1$ = H, or $\overline{CS}_1$ = L and CS_2 = H, or $\overline{CS}_1$ = L, and CS_2 = L

Clock

$\overline{CKE}$

Address

$\overline{WRITE}$

$\overline{CS}$

ADV

$\overline{OE}$

Data In

Data Out

TIMING WAVEFORM OF SINGLE READ/WRITE

Don't Care

Undefined

Clock

$\overline{CKE}$

Address

$\overline{WRITE}$

$\overline{CS}$

ADV

$\overline{OE}$

Data Out

Data In

t_{CES} t_{CEH}

t_{CH} t_{CL} t_{CYC}

A1 A2 A3 A4 A5 A6 A7

Q1 Q3 Q4 Q6 Q7

t_{OE} t_{LZOE}

t_{DS} t_{DH}

D2 D5

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and CS_2 = H, or $\overline{CS_1}$ = L, and CS_2 = L

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TIMING WAVEFORM OF CKE OPERATION

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BW}$x = L

$\overline{CS}$ = L means $\overline{CS}_1$ = L, CS_2 = H and $\overline{CS}_2$ = L

$\overline{CS}$ = H means $\overline{CS}_1$ = H, or CS_2 = L and $\overline{CS}_2$ = H, or $\overline{CS}_1$ = L, and CS_2 = L

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TIMING WAVEFORM OF C̅S̅ OPERATION

Clock

C̅K̅E̅

Address

W̅R̅I̅T̅E̅

C̅S̅

ADV

O̅E̅

Data Out

Data In
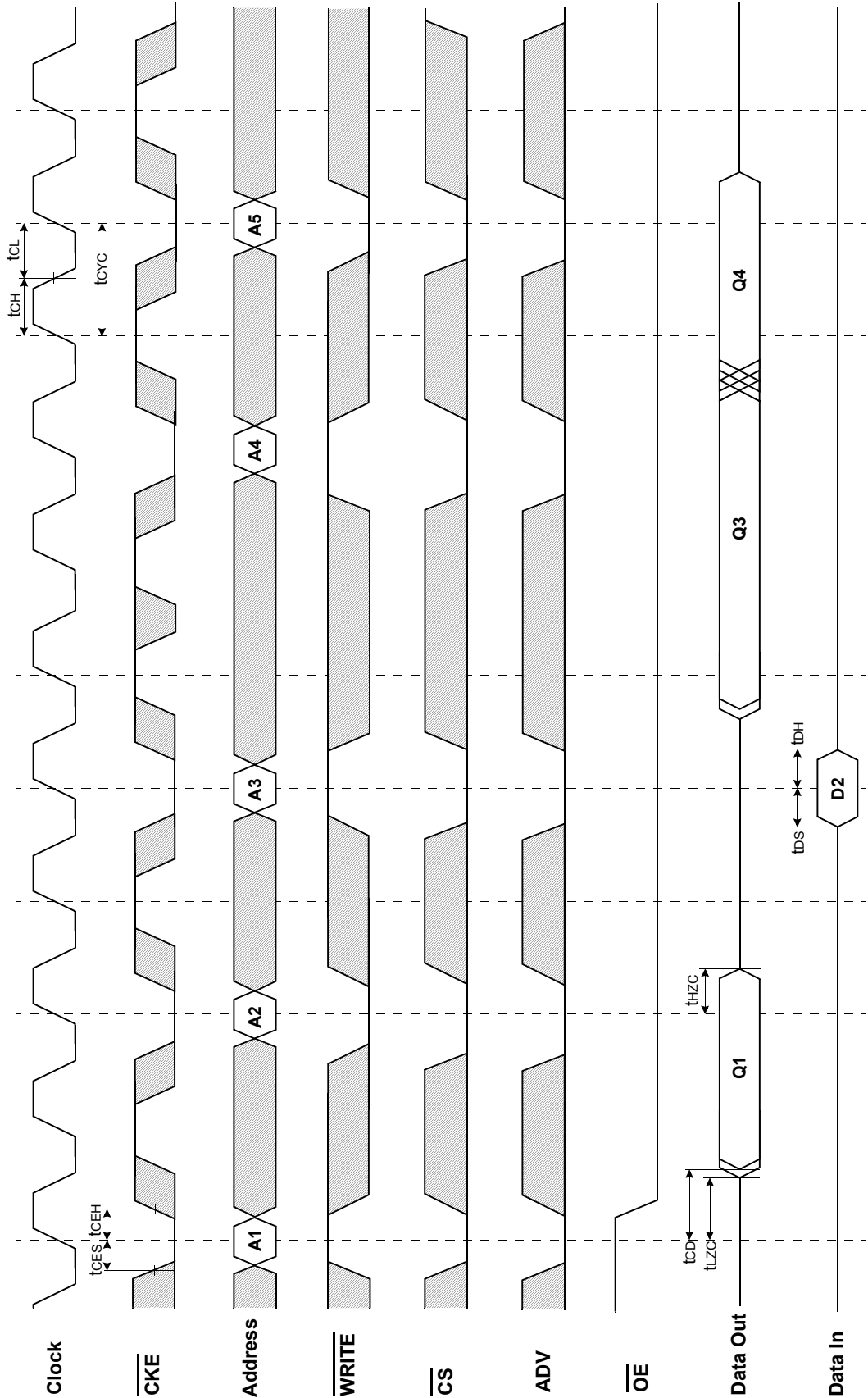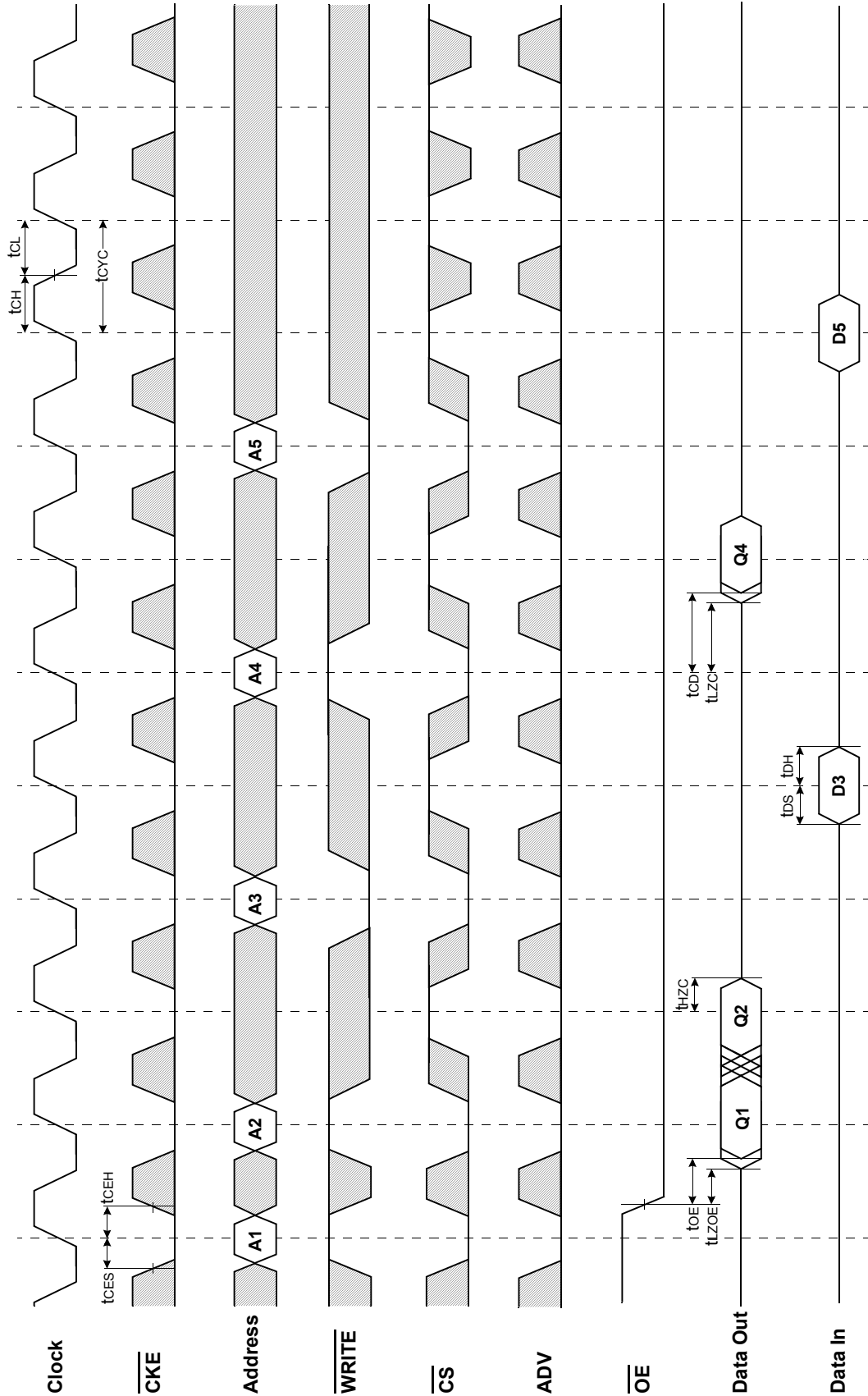
☐ Don't Care
☒ Undefined

NOTES : W̅R̅I̅T̅E̅ = L means W̅E̅ = L, and B̅W̅x = L
C̅S̅ = L means C̅S̅₁ = L, CS₂ = H and C̅S̅₂ = L
C̅S̅ = H means C̅S̅₁ = H, or C̅S̅₁ = L and C̅S̅₂ = H, or C̅S̅₁ = L, and CS₂ = L

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PACKAGE DIMENSIONS

100-TQFP-1420A (Lead and Lead free package)   Units ; millimeters/Inches

22.00 ±0.30
20.00 ±0.20

16.00 ±0.30
14.00 ±0.20

(0.83)

#1   0.65   0.30 ±0.10   (0.58)
0.10 MAX

0~8°
0.127 +0.10 -0.05

0.10 MAX

0.50 ±0.10

1.40 ±0.10   1.60 MAX
0.05 MIN
0.50 ±0.10

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