ICM7243

8-Character, Microprocessor-Compatible, LED Display Decoder Driver

August 1997

Features

- **14-Segment and 16-Segment Fonts with Decimal Point**
- **Mask Programmable for Other Font-Sets Up to 64 Characters**
- **Microprocessor Compatible**
- **Directly Drives LED Common Cathode Displays**
- **Cascadable Without Additional Hardware**
- **Standby Feature Turns Display Off; Puts Chip in Low Power Mode**
- **Sequential Entry or Random Entry of Data Into Display**
- **Single +5V Operation**
- **Character and Segment Drivers, All MUX Scan Circuitry, 8 x 6 Static Memory and 64-Character ASCII Font Generator Included On-Chip**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7243AIJL	-25^{o}C to 85^{o}C	40 Ld CERPDIP	F40.6
ICM7243AIPL	-25^{o}C to 85^{o}C	40 Ld PDIP	E40.6
ICM7243BIJL	-25^{o}C to 85^{o}C	40 Ld CERPDIP	F40.6
ICM7243BIPL	-25^{o}C to 85^{o}C	40 Ld PDIP	E40.6

Description

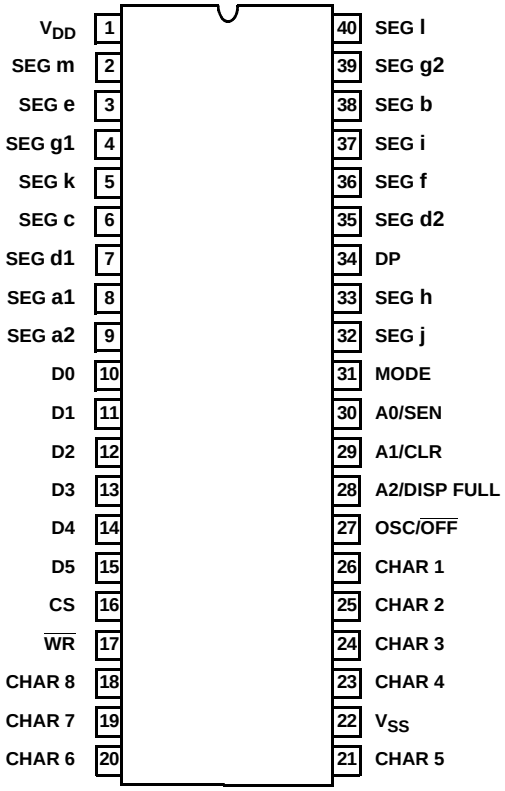
The ICM7243 is an 8-character, alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14-segment or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8 x 6 memory, high power character and segment drivers, and the multiplex scan circuitry.

6-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Sequential** (MODE = 1) or **Random** access mode (MODE = 0). In the **Sequential Access** mode the first entry is stored in the lowest location and displayed in the “left-most” character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate “right” of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading devices together. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

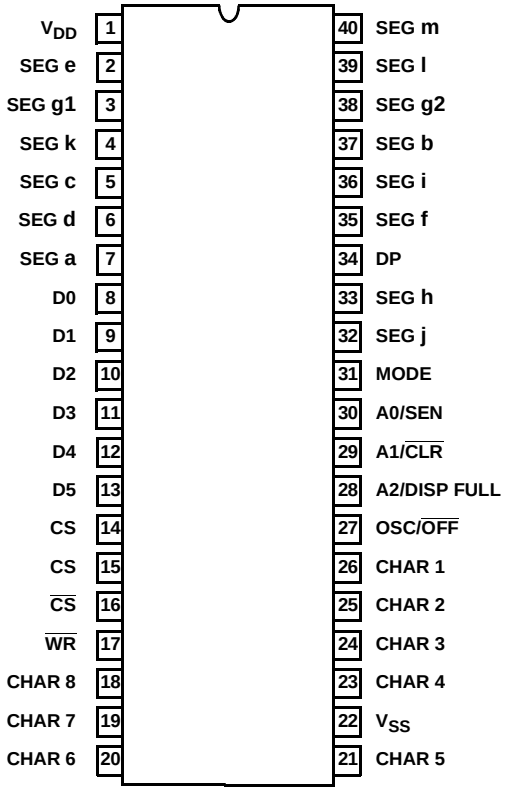
The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

Pinouts

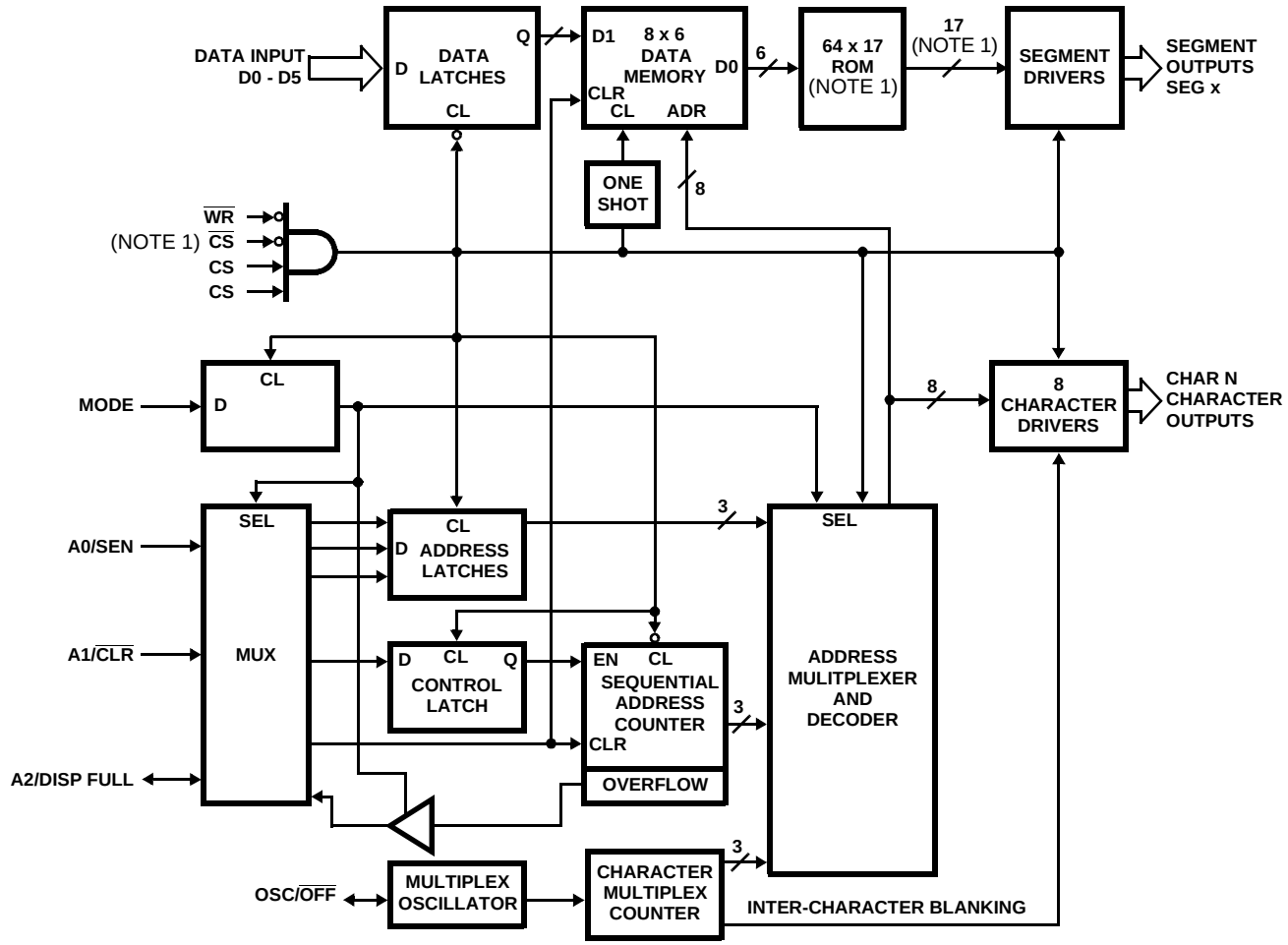
ICM7243A (16-SEGMENT CHARACTER)
(PDIP, CERDIP)
TOP VIEW



ICM7243B (14-SEGMENT CHARACTER)
(PDIP, CERDIP)
TOP VIEW



Functional Block Diagram



NOTE:

1. ICM7243A has only one CS and no $\overline{CS}$.
   ICM7243B has 15 Segments.

Absolute Maximum Ratings

Supply Voltage V_{DD} - V_{SS} . . . . . +6.0V
Input Voltage (Any Terminal) . . . . . V_{DD} +0.3V to V_{SS} -0.3V
CHARacter Output Current. 300mA
SEGment Output Current 30mA

Operating Conditions

Temperature Range . . . . . -25°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	55	N/A
CERDIP Package	50	10

Maximum Junction Temperature
CERDIP Package . . . . . 175°C
PDIP Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = 25×°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Supply Voltage (V_{DD} - V_{SS}), V_{SUPP}		4.75	5.0	5.25	V
Operating Supply Current, I_{DD}	V_{SUPP} = 5.25V, 10 Segments ON, All 8 Characters	-	180	-	mA
Quiescent Supply Current, I_{STBY}	V_{SUPP} = 5.25V, OSC/$\overline{OFF}$ Pin < 0.5V, CS = V_{SS}	-	30	250	µA
Input High Voltage, V_{IH}		2	-	-	V
Input Low Voltage, V_{IL}		-	-	0.8	V
Input Current, I_{IN}		-10	-	+10	µA
CHARacter Drive Current, I_{CHAR}	V_{SUPP} = 5V, V_{OUT} = 1V	140	190	-	mA
CHARacter Leakage Current, I_{CHLK}		-	-	100	µA
SEGment Drive Current, I_{SEG}	V_{SUPP} = 5V, V_{OUT} = 2.5V	14	19	-	mA
SEGment Leakage Current, I_{SLK}		-	0.01	10	µA
DISPlay FULL Output Low, V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V
DISPlay FULL Output High, V_{OH}	I_{IH} = 100µA	2.4	-	-	V
Display Scan Rate, f_{DS}		-	400	-	Hz

Electrical Specifications

Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. V_{DD} = 5V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS					
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low, t_{WPl}		300	250	-	ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High (Note 1), t_{WPH}		-	250	-	ns
Data Hold Time, t_{DH}		0	-100	-	ns
Data Setup Time, t_{DS}		250	150	-	ns
Address Hold Time, t_{AH}		125	-	-	ns
Address Setup Time, t_{AS}		40	15	-	ns
CS, $\overline{CS}$ Setup Time, t_{CS}		0	-	-	ns
Pulse Transition Time, t_T		-	-	100	ns
SEN Setup Time, t_{SEN}		0	-25	-	ns
Display Full Delay, t_{WDF}		700	480	-	ns

Capacitance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance, C_{IN}	(Note 2)	-	5	-	pF
Output Capacitance, C_O	(Note 2)	-	5	-	pF

NOTES:
1. In Sequential mode $\overline{WR}$ high must be ≥ T_{SEN} +T_{WDF}.
2. For design reference only, not tested.

Timing Waveforms

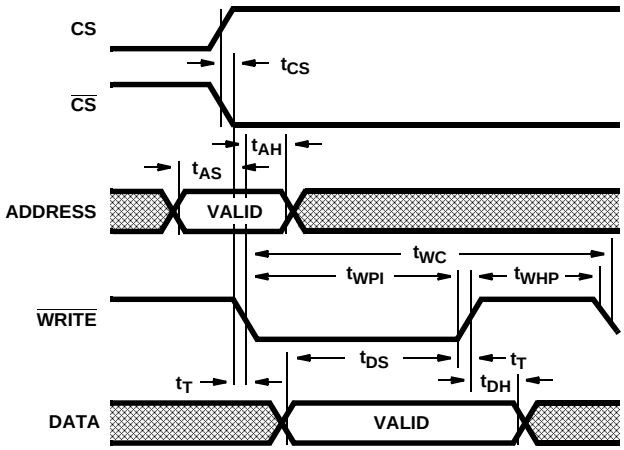


FIGURE 1. RANDOM ACCESS TIMING

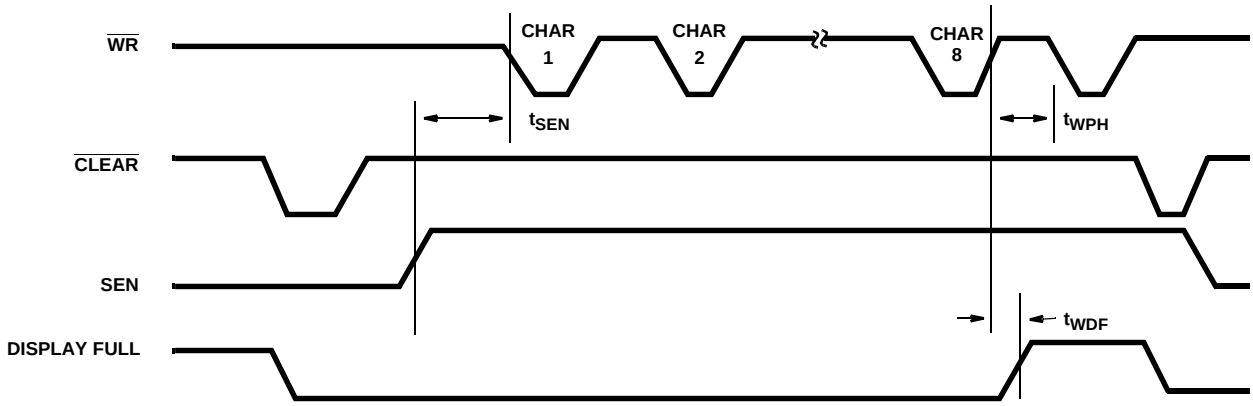


FIGURE 2. SEQUENTIAL ACCESS MODE TIMING (MODE = 1)

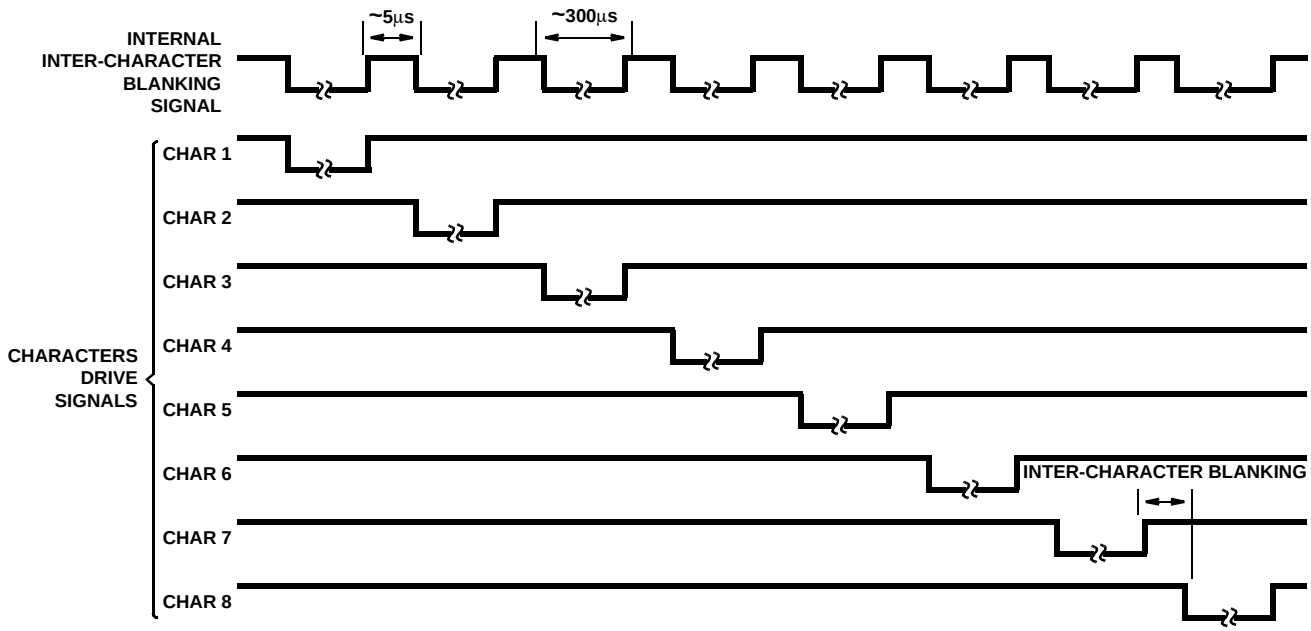


FIGURE 3. DISPLAY CHARACTERS MULTIPLEX TIMING DIAGRAM

Performance Curves

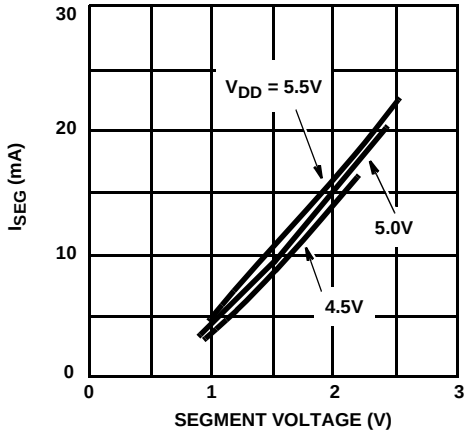


FIGURE 4. SEGMENT CURRENT vs OUTPUT VOLTAGE

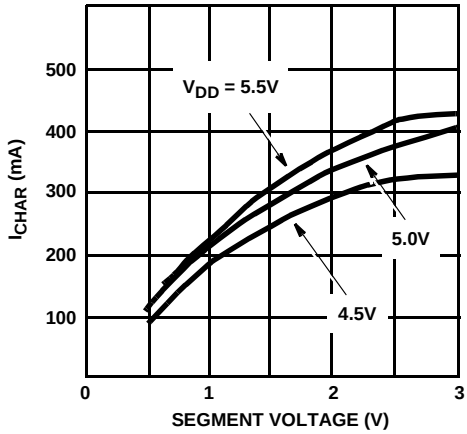


FIGURE 5. CHARACTER CURRENT VS OUPUT VOLTAGE

Pin Descriptions

SIGNAL	PIN	FUNCTION
ICM7243A(B)		
D0 - D5	10 - 15 (8 - 13)	Six-Bit ASCll Data input pins (active high).
CS, $\overline{CS}$	16 (14 - 16)	Chip Select from μP address decoder, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Sequential Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via A0 - A2 Address pins.
A0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading devices for displays of more than 8 characters (active high enables device controller).
A1/$\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V_{DD} will lower the internal oscillator frequency. An external oscillator can be applied to this pin. A low at this input sets the device into a (shutdown) mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG a - SEG m, DP	2 - 9, 32 - 40 (2 - 7), (32 - 40)	SEGment driver outputs.
CHARacter 1 - 8	18 - 21, 23 - 26	CHARacter driver outputs.

Test Circuit

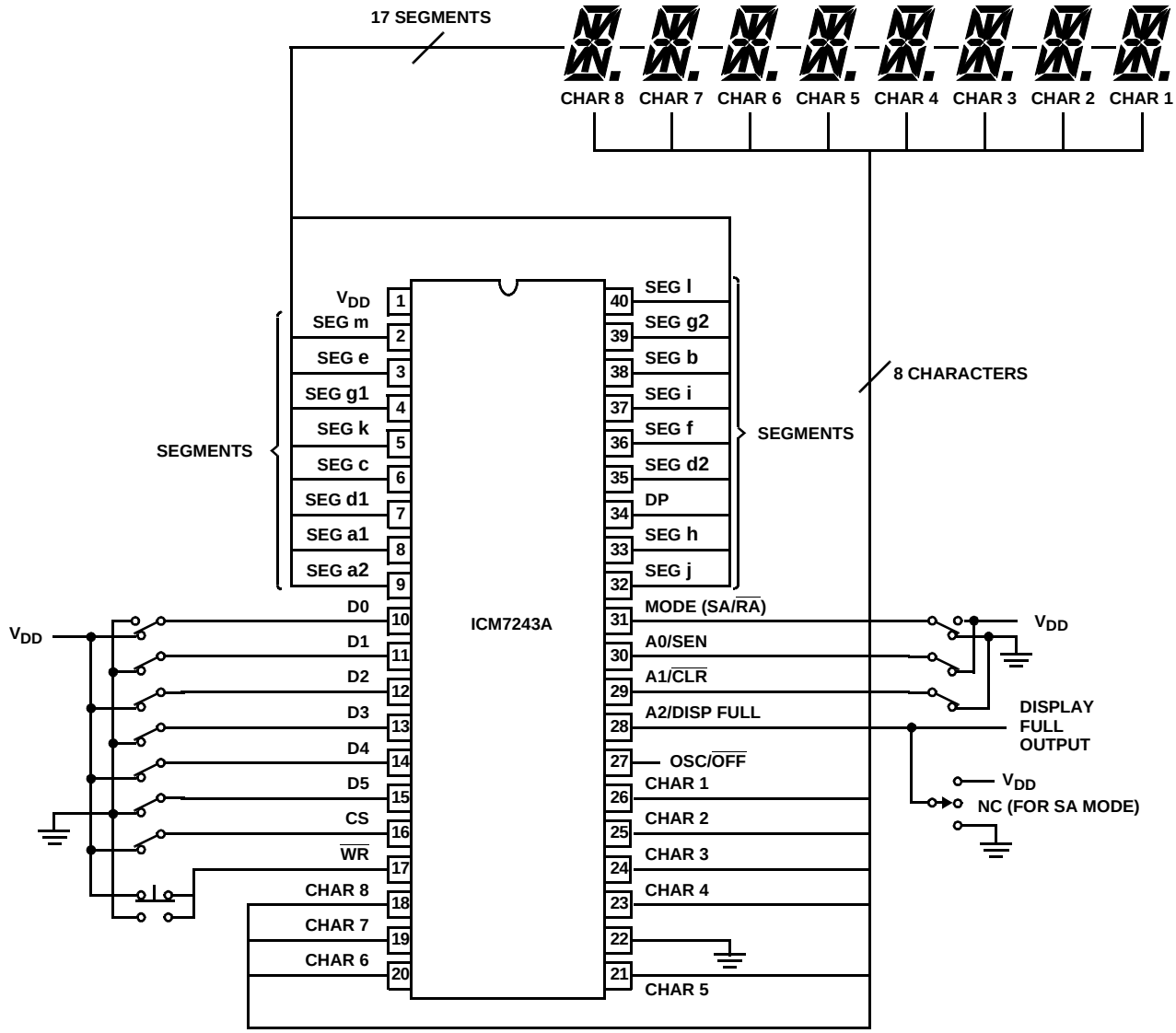


FIGURE 6.

Typical Applications

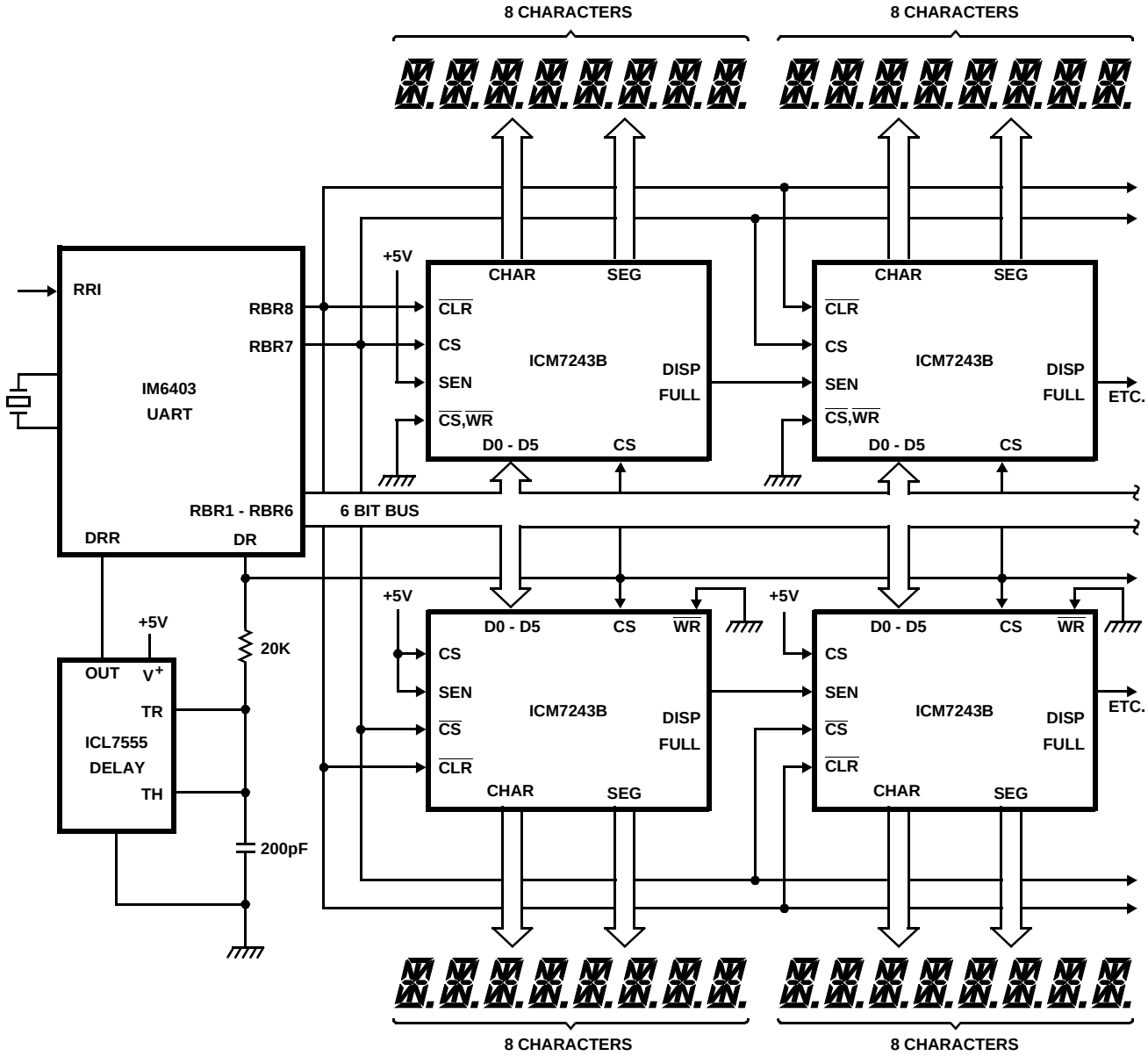
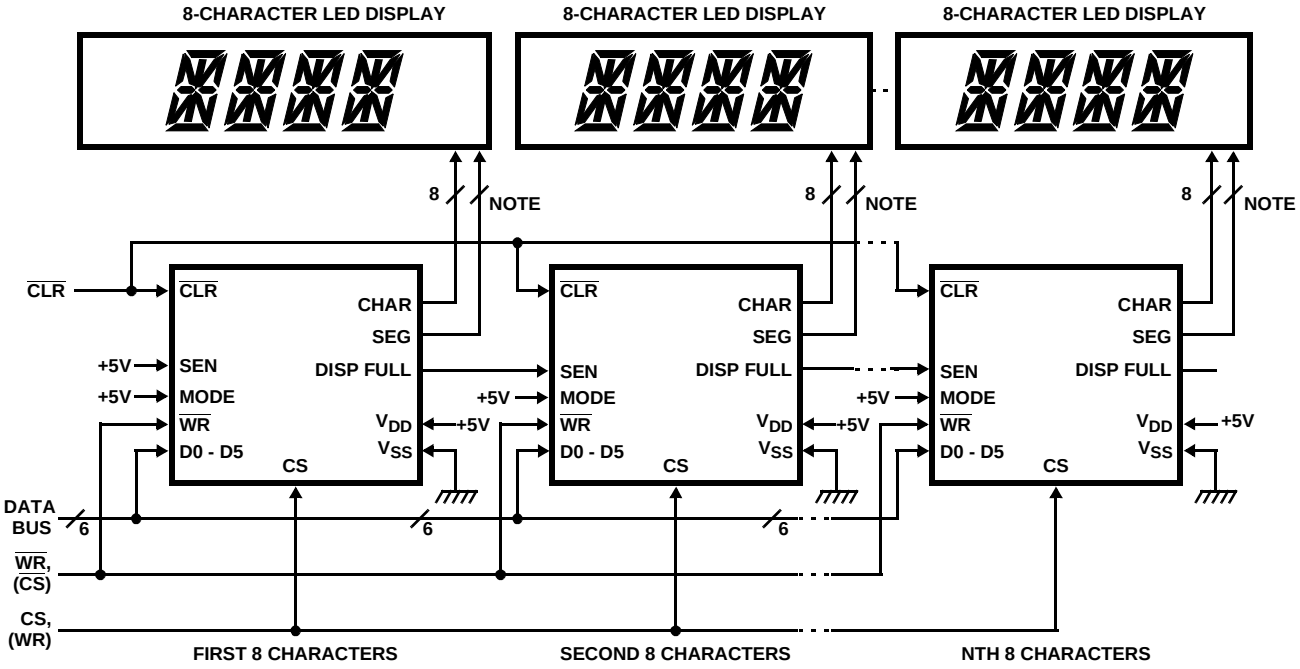


FIGURE 7. DRIVING TWO ROWS OF CHARACTERS FROM A SERIAL INPUT

Typical Applications (Continued)



NOTE: 17 for ICM7243A, 15 for ICM7243B.

FIGURE 8. MULTICHARACTER DISPLAY USING SEQUENTIAL ACCESS MODE

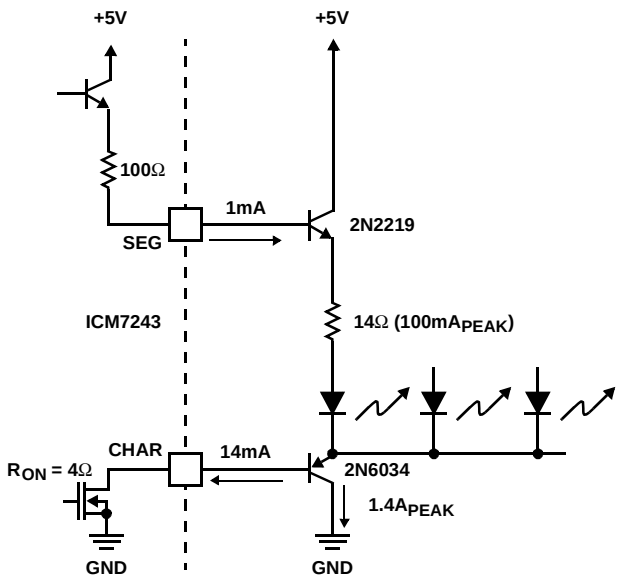


FIGURE 9A. COMMON CATHODE DISPLAY

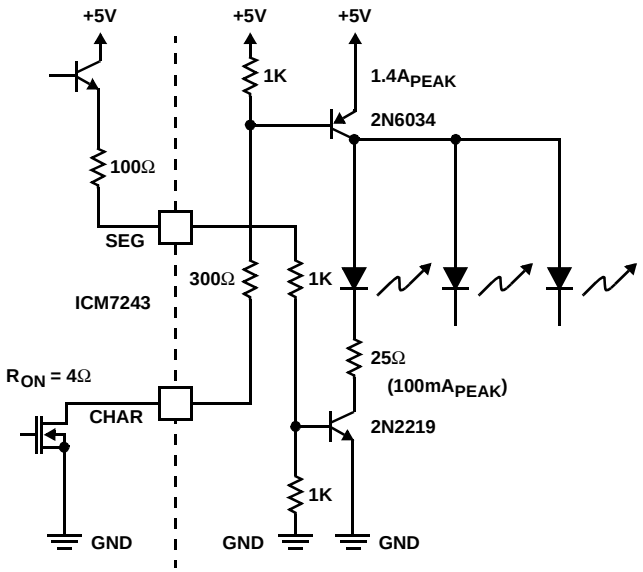


FIGURE 9B. COMMON ANODE DISPLAY

FIGURE 9. DRIVING LARGE DISPLAYS

Typical Applications (Continued)

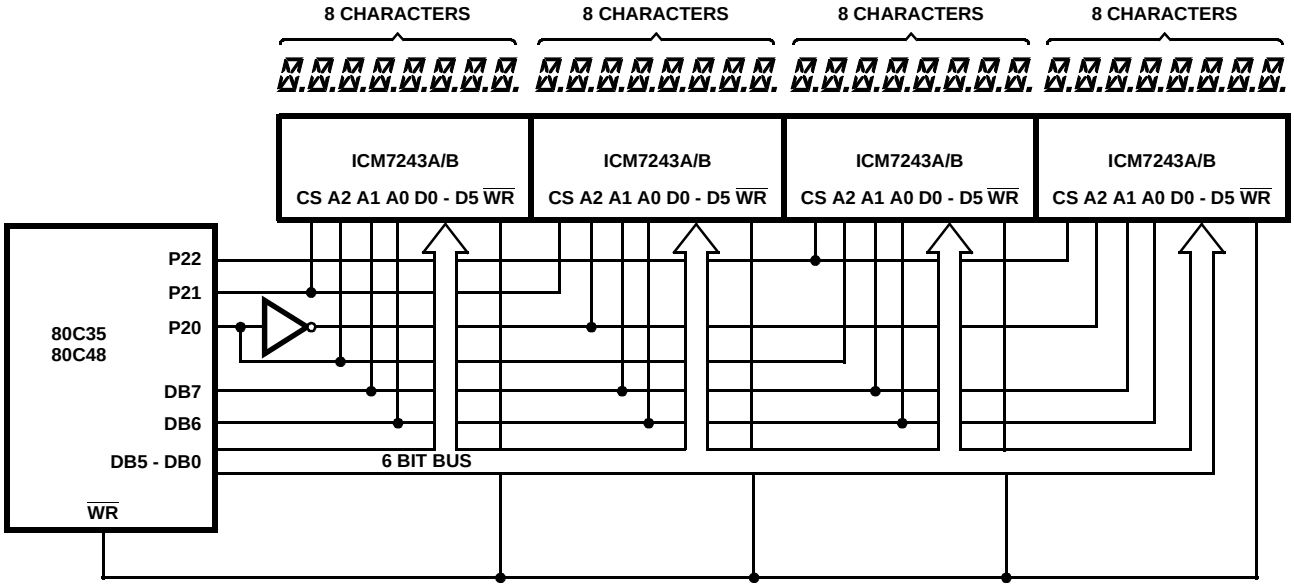
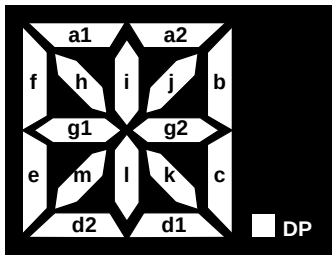


FIGURE 10. RANDOM ACCESS 32-CHARACTER DISPLAY IN A 80C48 SYSTEM

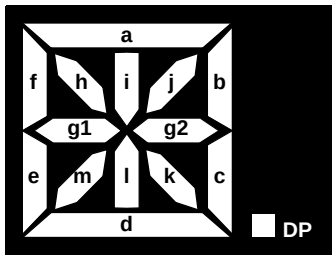
Display Font and Segment Assignments



D5, D4	0	0	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	0	1	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	_
	1	0		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	1	1	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
		D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

FIGURE 11. ICM7232A 16-SEGMENT CHARACTER FONT WITH DECIMAL POINT

Display Font and Segment Assignments (Continued)



D5, D4	0	0	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	0	1	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	_
	1	0		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	1	1	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
		D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

FIGURE 12. ICM7243B 14-SEGMENT CHARACTER FONT WITH DECIMAL POINT

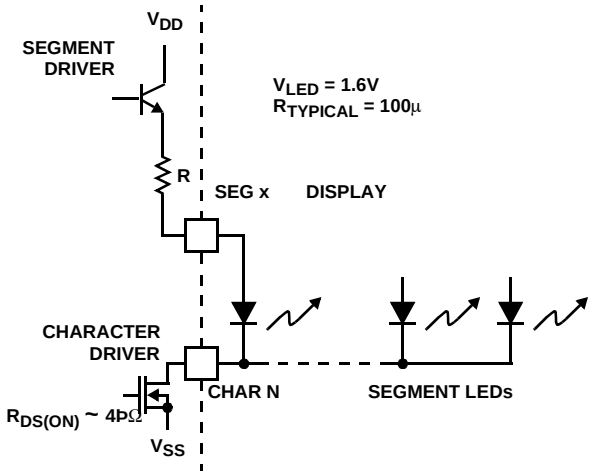


FIGURE 13. SEGMENT AND CHARACTER DRIVERS OUTPUT CIRCUIT

Detailed Description

$\overline{WR}$, $\overline{CS}$, CS - These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE - The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location (in Data Memory) where incoming data will be placed is determined either from the Address pins or the Sequential Address Counter. This is controlled by MODE input. MODE also controls the function of A0/SEN, A1/$\overline{CLR}$, and A2/DISPlay FULL lines.

Random Access Mode - When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A0, A1 and A2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Sequential Access Mode - If the internal latch is set for **Sequential Access (SA)**, (MODE latched high), the Serial ENable input or SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Sequential Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output will be active in **SA** mode to indicate the overflow status of the Sequential Address Counter. If this output is low, and SEN is (latched) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy “daisy-chaining” of display drivers for multiple character displays in a **Sequential Access** mode.

Changing Modes - Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of WR (or its equivalent). When changing mode from **Sequential Access** to **Random Access**, note that A2/DISPlay FULL will be an output until WR has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Sequential Access**, A1/CLR should be high to avoid inadvertent clearing of the Data Memory and Sequential Address Counter. DISPlay FULL will become active immediately after the rising edge of WR.

Data Entry - The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/OFF - The device includes a relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter drive lines (see Figure 3). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output - The output of the Multiplex Counter is decoded and multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in Sequential Access mode, with SEN high and DISPlay FULL low), when it scans through the display data. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5μs). Each CHARacter output lasts nominally about 300μs, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL Low for **Sequential Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.