Features

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual In-line Memory Module with 8 Byte busses
- 8Mx64 Extended Data Out SO DIMM
- Performance:

		-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	13ns	15ns
t_{AA}	Access Time From Address	25ns	30ns
t_{RC}	Cycle Time	84ns	104ns
t_{HPC}	EDO Mode Cycle Time	20ns	25ns

- All inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Au contacts
- Optimized for byte-write non-parity applications
- System Performance Benefits:
  - Reduced noise (18 V_{SS}/18V_{CC} pins)
  - Byte write, byte read accesses
  - Serial PDs
- Extended Data Out (EDO) Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only, CBR Hidden Refresh, and Self Refresh
- 4096 refresh cycles distributed across 128ms
- 12/11 addressing (Row/Column)
- Card size: 2.66" x 1.0" x 0.149"
- DRAMS in TSOP Package

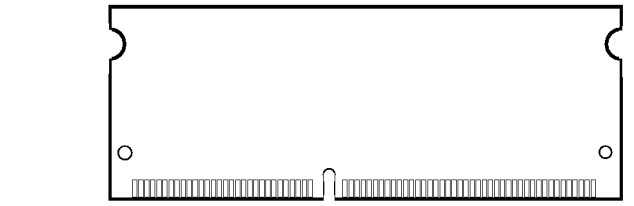
Description

IBM11T8645HP is an industry standard 144-pin 8-byte Small Outline Dual In-line Memory Module (SO DIMM) which is organized as an 8Mx64 high speed memory array designed for use in non-parity applications. The SO DIMM uses 8 8Mx8 EDO DRAMs in TSOP packages. The use of EDO DRAMs allows for a reduction in Page Mode Cycle time from 40ns (Fast Page) to 15ns for 60ns EDO modules.

This card uses Serial Presence Detects (SPDs) implemented via a serial EEPROM using the two pin I^2C Protocol. This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example, the System Microprocessor) and the slave EEPROM device. The device address for the EEPROM is set to zero at the card. The first 128 bytes are utilized by the SO DIMM manufacturer, and the second 128 bytes are available to the end user.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.66" long space-saving footprint. Related products are the 1Mx64, 2Mx64, 4Mx64 and the x72 (ECC) SO DIMMs.

Card Outline



Pin Description

$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A11	Address Inputs
DQ0 - DQ63	Data Input/Output
V_{CC}	Power (3.3V)
V_{SS}	Ground
NC	No Connect
SCL	Serial Presence Detect Clock Input
SDA	Serial Presence Detect Data Input
$\overline{RAS0}$	Row Address Strobe

Pinout

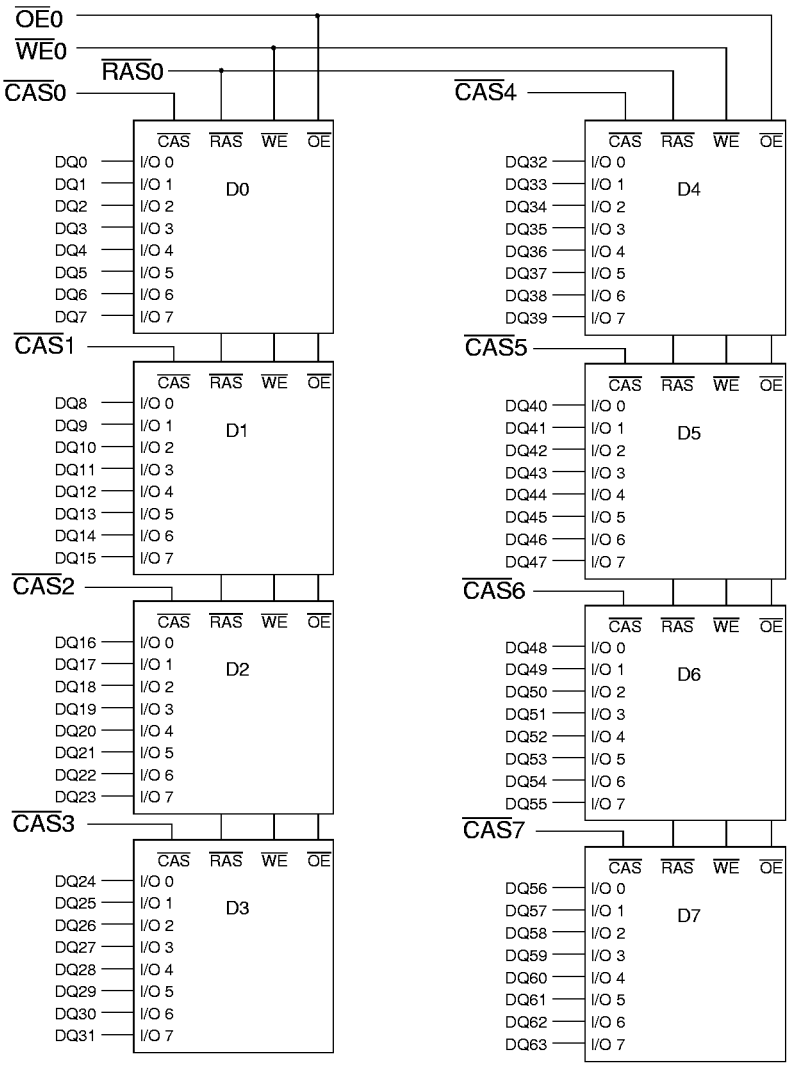
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	2	V_{SS}	73	$\overline{OE}$	74	NC
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{CC}	82	V_{CC}
11	V_{CC}	12	V_{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	$\overline{CAS0}$	24	$\overline{CAS4}$	95	DQ21	96	DQ53
25	$\overline{CAS1}$	26	$\overline{CAS5}$	97	DQ22	98	DQ54
27	V_{CC}	28	V_{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{CC}	102	V_{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	A11
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	A12
39	DQ9	40	DQ41	111	A10	112	A13
41	DQ10	42	DQ42	113	V_{CC}	114	V_{CC}
43	DQ11	44	DQ43	115	$\overline{CAS2}$	116	$\overline{CAS6}$
45	V_{CC}	46	V_{CC}	117	$\overline{CAS3}$	118	$\overline{CAS7}$
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ28	132	DQ60
VOLTAGE KEY				133	DQ29	134	DQ61
61	DU	62	DU	135	DQ30	136	DQ62
63	V_{CC}	64	V_{CC}	137	DQ31	138	DQ63
65	DU	66	DU	139	V_{SS}	140	V_{SS}
67	$\overline{WE}$	68	NC	141	SDA	142	SCL
69	$\overline{RAS0}$	70	NC	143	V_{CC}	144	V_{CC}
71	NC	72	NC				

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Leads	Dimension	Power
IBM11T8645HP-50T	8Mx64	50ns	Au	2.66"x1.0"x 0.149"	3.3V
IBM11T8645HP-60T	8Mx64	60ns	Au	2.66"x1.0"x 0.149	3.3V

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	DQx
Standby		H	X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	Valid Data Out
Early-Write		L	L	L	X	Row	Col	Valid Data In
Late-Write		L	L	H→L	H	Row	Col	Valid Data In
RMW		L	L	H→L	L→H	Row	Col	Valid Data In/Out
EDO Page Mode - Read 1st Cycle		L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	L	N/A	Col	Valid Data Out
EDO Page Mode - Write 1st Cycle		L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	X	N/A	Col	Valid Data In
EDO Page Mode - RMW 1st Cycle		L	H→L	H→L	L→H	Row	Col	Valid Data In/Out
Subsequent Cycles		L	H→L	H→L	L→H	N/A	Col	Valid Data In/Out
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	H	X	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	X	High Impedance

Serial Presence Detect

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	EDO	02	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	11	0B	
5	Number of DIMM Banks	1	01	
6 - 7	Data Width of Assembly	x64	4000	
8	Voltage Interface Level of this Assembly	LVTTL	01	
9	$\overline{RAS}$ Access	50ns	32	
		60ns	3C	
10	$\overline{CAS}$ Access	13ns	0D	
		15ns	0F	
11	DIMM Configuration Type	Non-Parity	00	
12	Refresh Rate/Type	SR/2 (31.2 us)	83	
13	Primary DRAM Data Width	x8	08	
14	Error Checking DRAM Data Width	N/A	00	
15 - 62	Reserved	Undefined	00	
63	Checksum for bytes 0 - 62	Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	ASCII '11T8645HP"R"-50T'	313154383634354850r r2D35305420202020	2, 3
		ASCII '11T8645HP"R"-60T'	313154383634354850r r2D36305420202020	
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number	Serial Number	ssssssss	6
99 - 127	Reserved	Undefined	00	
128 - 255	Open for Customer Use	Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
$V_{IN/OUT(SPD)}$	Input Voltage(Serial PD Device)	-0.3 to 6.5	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	4.1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1, 2
$V_{IH(SPD)}$	Input High Voltage(Serial PD Device)	V_{CC} x 0.7	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2
$V_{IL(SPD)}$	Input Low Voltage(Serial PD Device)	-0.3	—	V_{CC} x 0.3	V	1, 2
$V_{OL(SPD)}$	Output Low Voltage(Serial PD Device) I_{OL} = 3ma	—	—	0.4	V	

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns . Additionally, V_{IL} may undershoot to -1.2V for pulse widths ≤ 4.0ns. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Max	Units
C_{I1}	Input Capacitance (A0-A9)	55	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	68	pF
C_{I3}	Input Capacitance ($\overline{CAS}$)	12	pF
C_{I4}	Input Capacitance ($\overline{SCL}$)	9	pF
C_{IO1}	Input/Output Capacitance (DQ0-63)	10	pF
C_{IO2}	Input/Output Capacitance (SDA)	10	pF

DC Electrical Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter		8M x 64 Min.	8M x 64 Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	-50	—	1120	mA	1, 2, 3
		-60	—	920		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	16.1	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50	—	1040	mA	1, 3, 4
		-60	—	880		
I_{CC4}	EDO Page Mode Current Average Power Supply Current, EDO Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-50	—	800	mA	1, 2, 3
		-60	—	640		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	1.7	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	1120	mA	1, 3, 4
		-60	—	920		
I_{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min); $\overline{CAS}$ held low; $\overline{WE}$ = V_{CC} -0.2V; Addresses and D_{IN} = V_{CC} -0.2V OR 0.2.		—	3.3	mA	4
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V x=y	$\overline{RAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{ADD}$	-16	+16	µA	
		$\overline{CAS}$	-2	+2		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-2	+2	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +4.2mA)		0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.
4. Refresh current is specified for one bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

1. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Valid column addresses are only A0 through A10.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	—	104	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	100k	60	100k	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	100k	10	100k	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	7	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	7	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	37	14	45	ns	1
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time	9	25	12	30	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	8	—	10	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	—	50	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	13	—	15	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time From D_{IN}	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time From D_{IN}	0	—	0	—	ns	4
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	

1. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
3. Either t_{CDD} or t_{OED} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.

Write Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	7	—	10	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	8	—	10	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8	—	10	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	7	—	10	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

Read Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 3
t_{AA}	Access Time from Address	—	25	—	30	ns	1, 3
t_{OEA}	Access Time From $\overline{OE}$	—	13	—	15	ns	3
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	3
t_{OEZ}	Output Buffer Turn-Off Delay From $\overline{OE}$	0	13	0	15	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	ns	6
t_{OFF}	Output Buffer Turn-Off Delay	0	13	0	15	ns	5
t_{OES}	$\overline{OE}$ Setup Time Prior to $\overline{CAS}$	5	—	5	—	ns	
t_{ORD}	$\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	ns	

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{CDD} or t_{OED} must be satisfied

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	109	—	135	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	—	79	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	28	—	34	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	40	—	49	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	10	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

EDO Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (Hyper Page Mode)	8	100K	10	10K	ns	
t_{HPC}	Hyper Page Mode Cycle Time (Read/Write)	20	—	25	—	ns	
t_{HPRWC}	Hyper Page Mode Read Modify Write Cycle Time	54	—	66	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	27	—	35	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	27	—	35	ns	1
t_{RASP}	Hyper Page Mode $\overline{RAS}$ Pulse Width	50	200K	60	200K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	5	—	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—	10	—	ns	

1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	—	5	—	5	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	—	5	—	10	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	—	5	—	10	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	—	5	—	10	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	—	5	—	5	ns	
t_{REF}	Refresh Period	—	128	—	128	ms	1

1. 4096 refreshes are required every 128ms.

Self Refresh Cycle

Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	84	—	104	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1

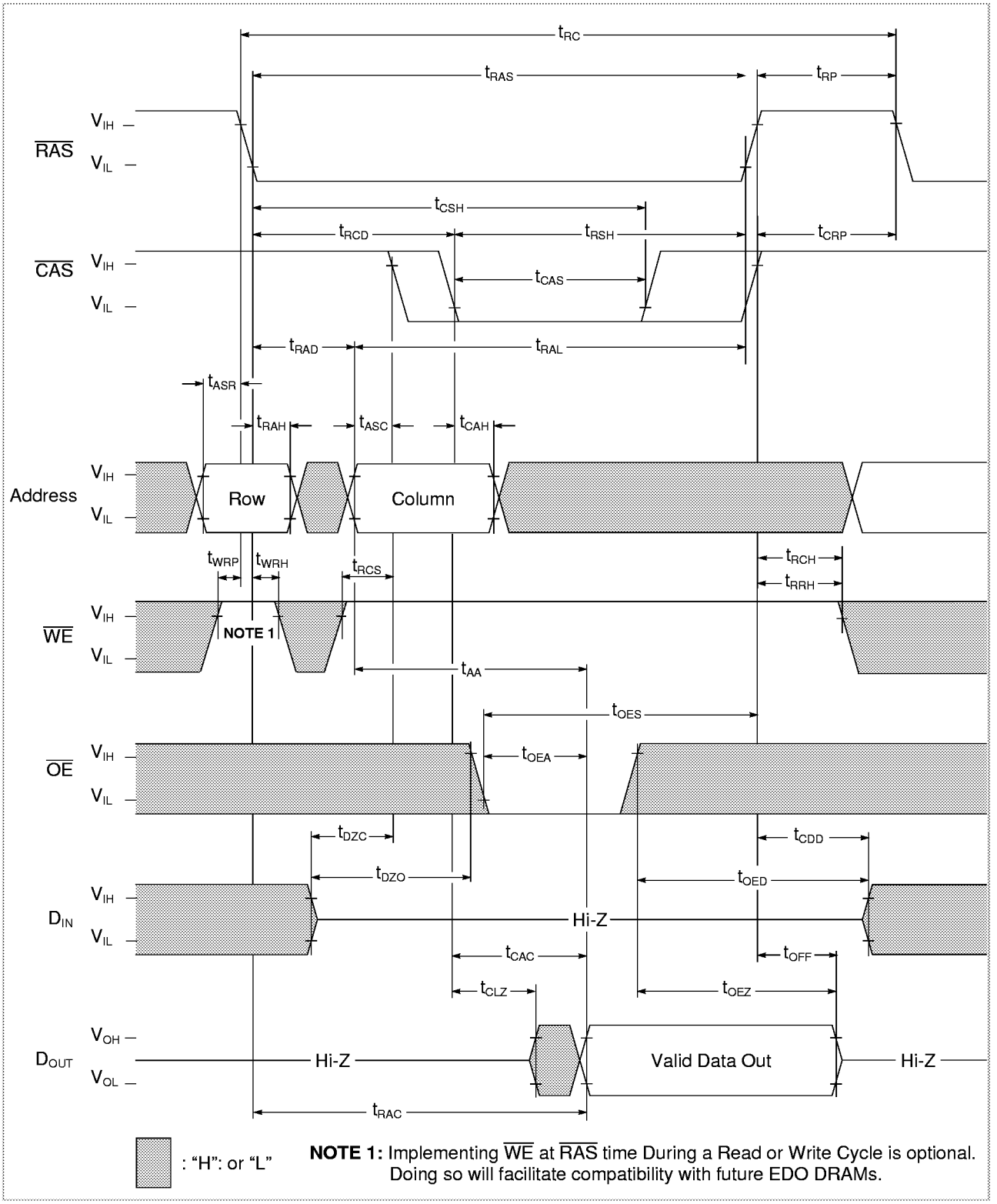
1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

Presence Detect Read and Write Cycle

Symbol	Parameter	-70		Unit	Notes
		Min	Max		
f_{SCL}	SCL Clock Frequency		80	kHZ	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.5		µs	
t_{LOW}	Clock Low Period	6.7		µs	
t_{HIGH}	Clock High Period	4.5		µs	
$t_{SU:STA}$	Start Condition Setup Time(for a Repeated Start Condition)	6.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	500		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	6.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

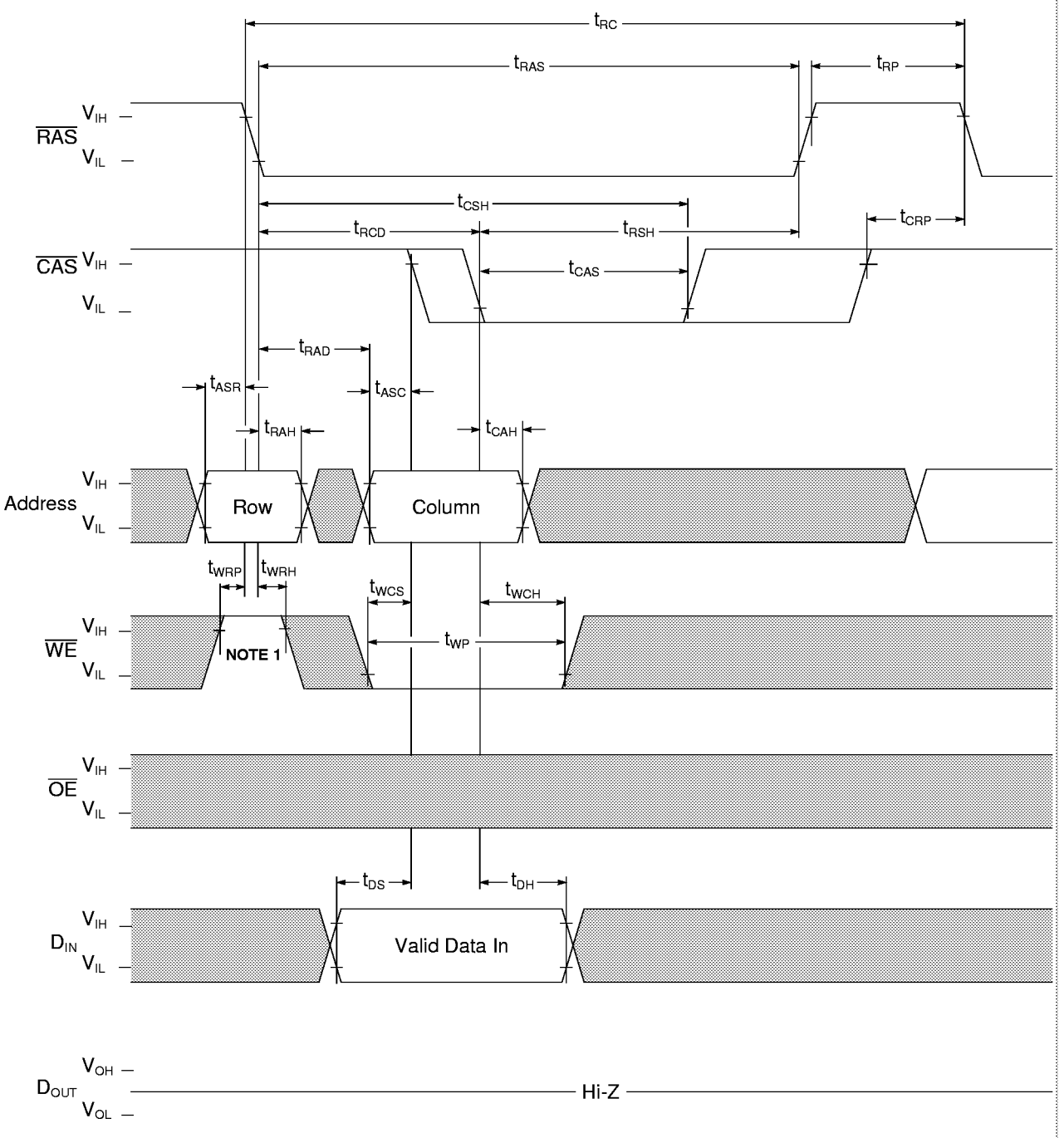
1. The write cycle time(t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Read Cycle



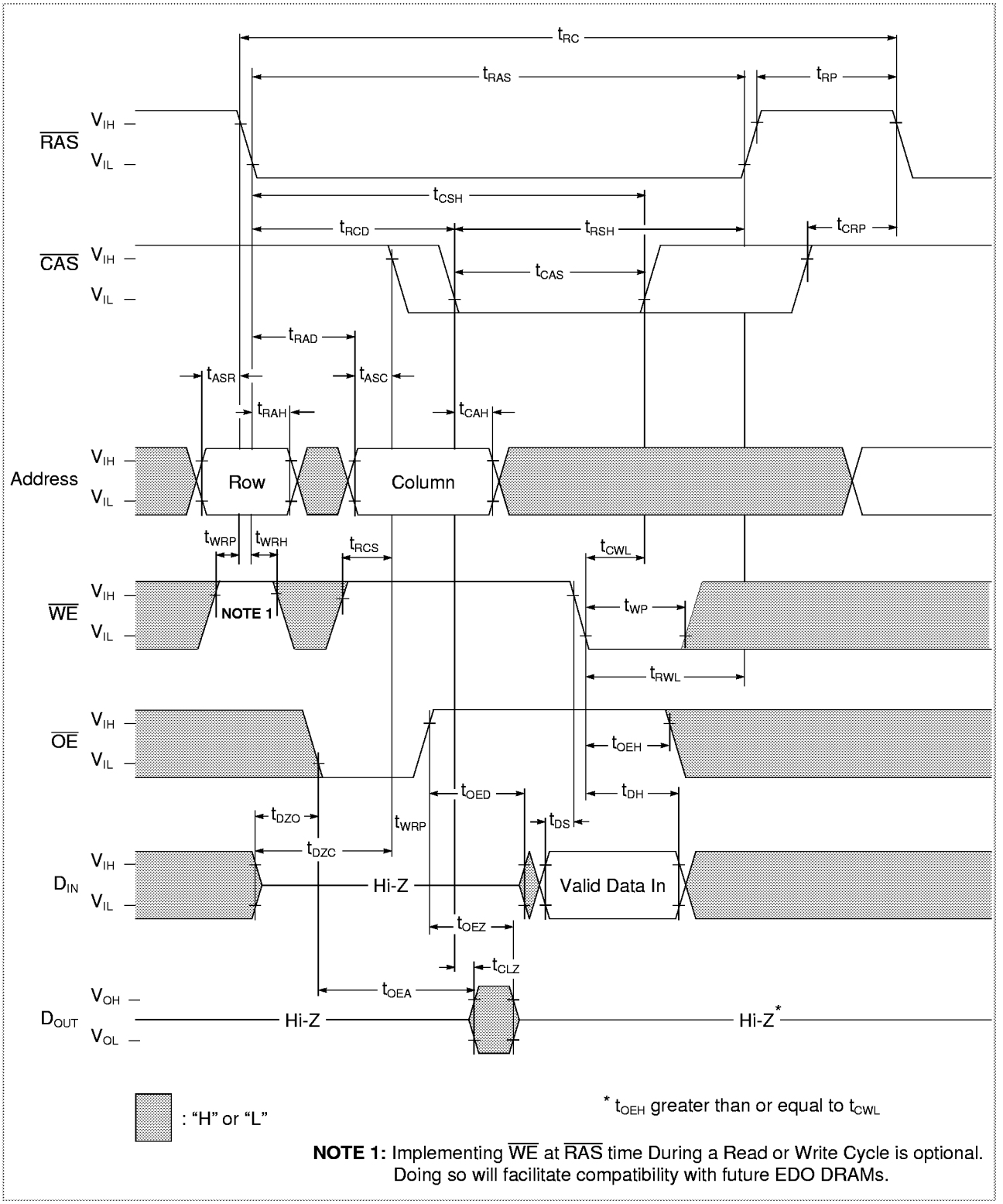
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Early Write)



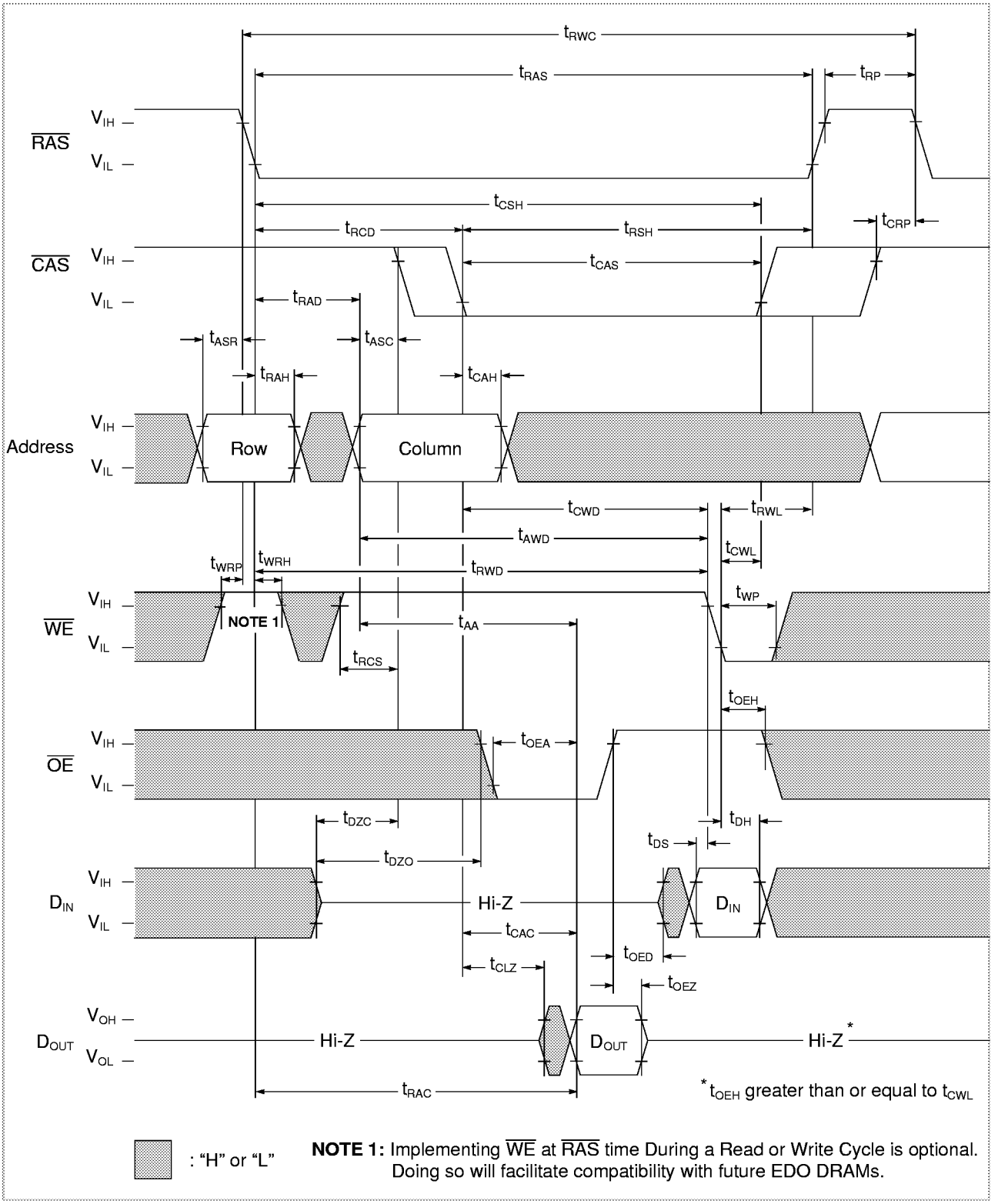
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Late Write)

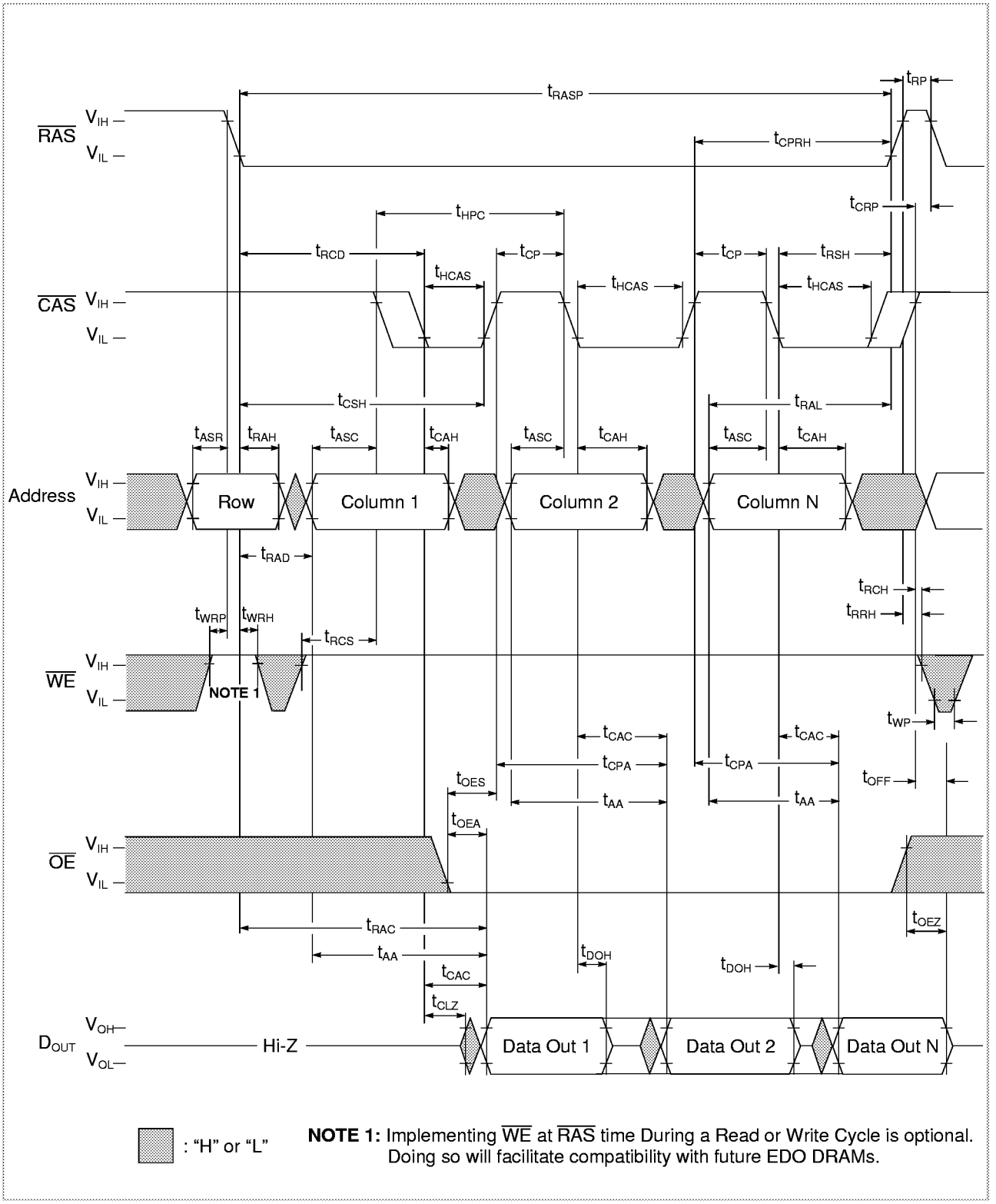


NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

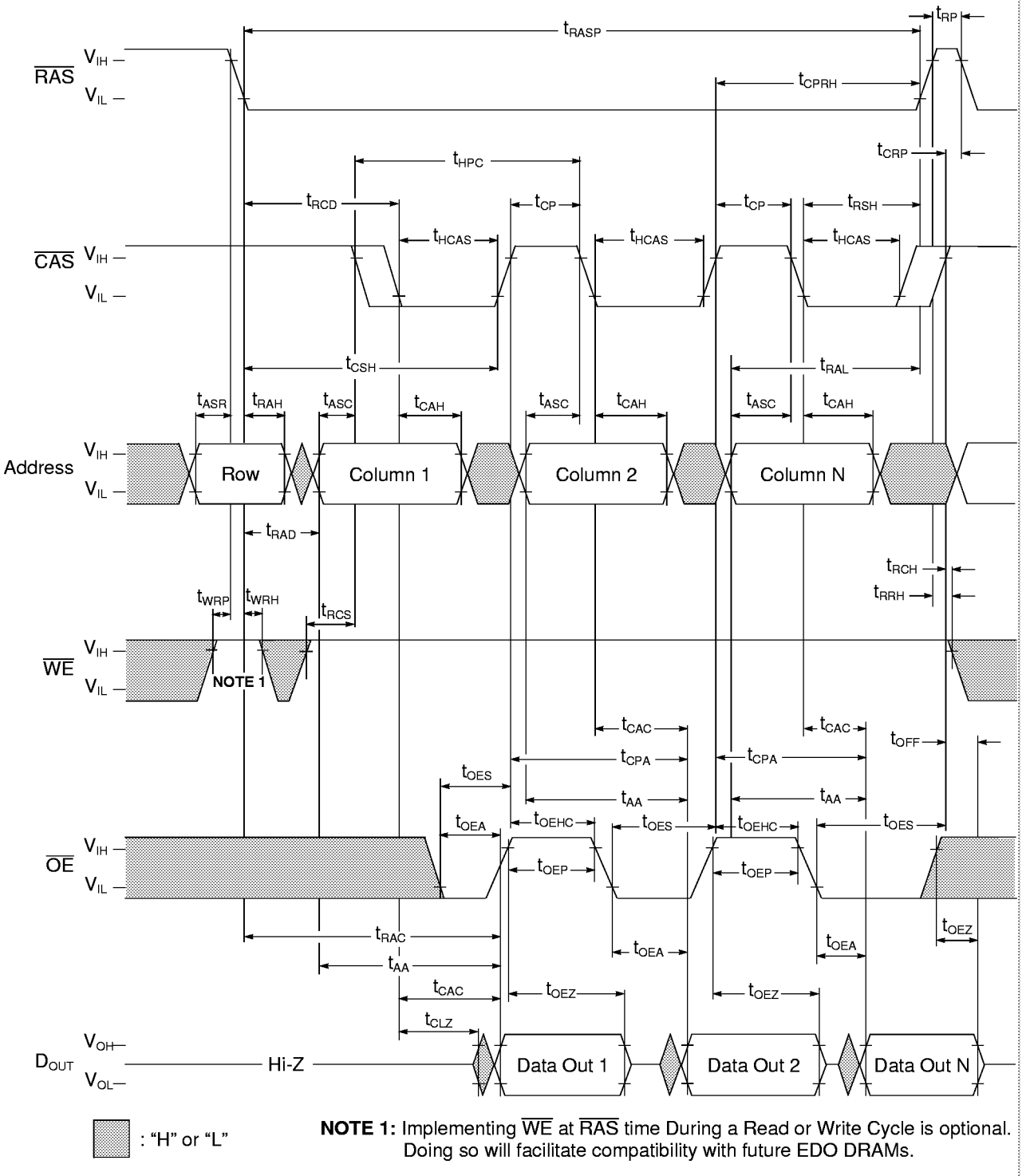
Read-Modify-Write-Cycle



EDO Page Mode Read Cycle

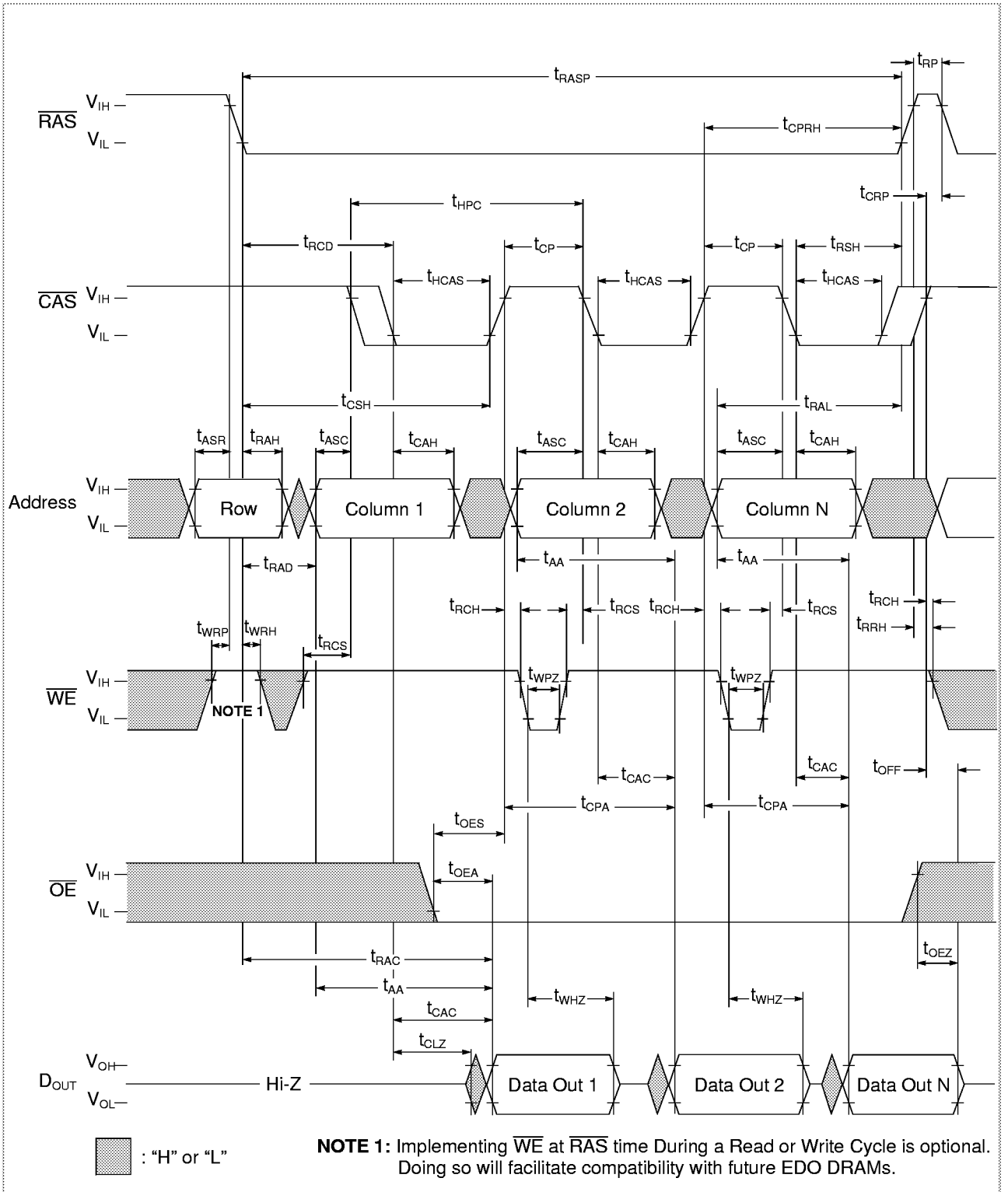


EDO Page Mode Read Cycle ($\overline{OE}$ Control)



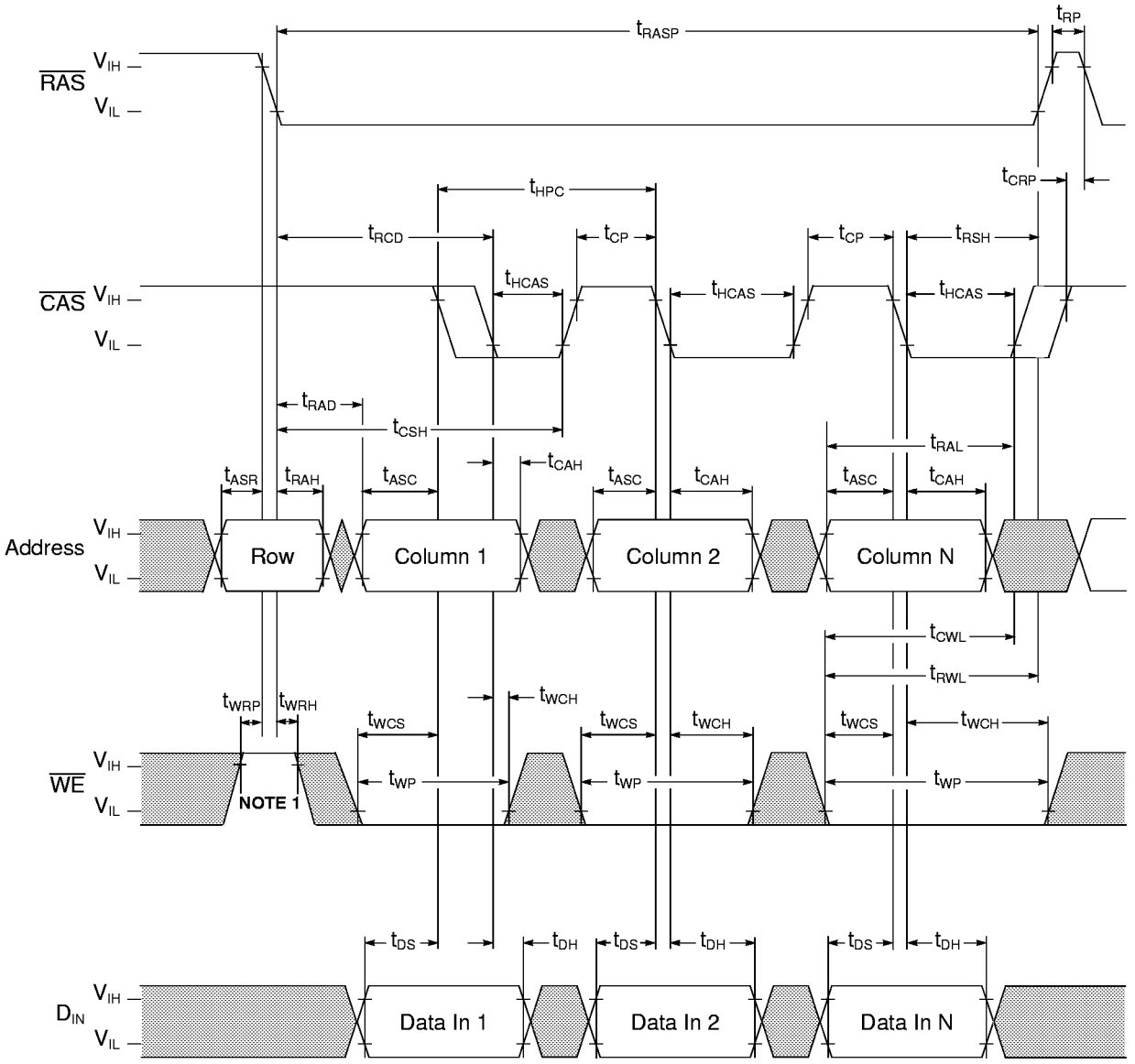
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Read Cycle ($\overline{WE}$ Control)



NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Early Write Cycle

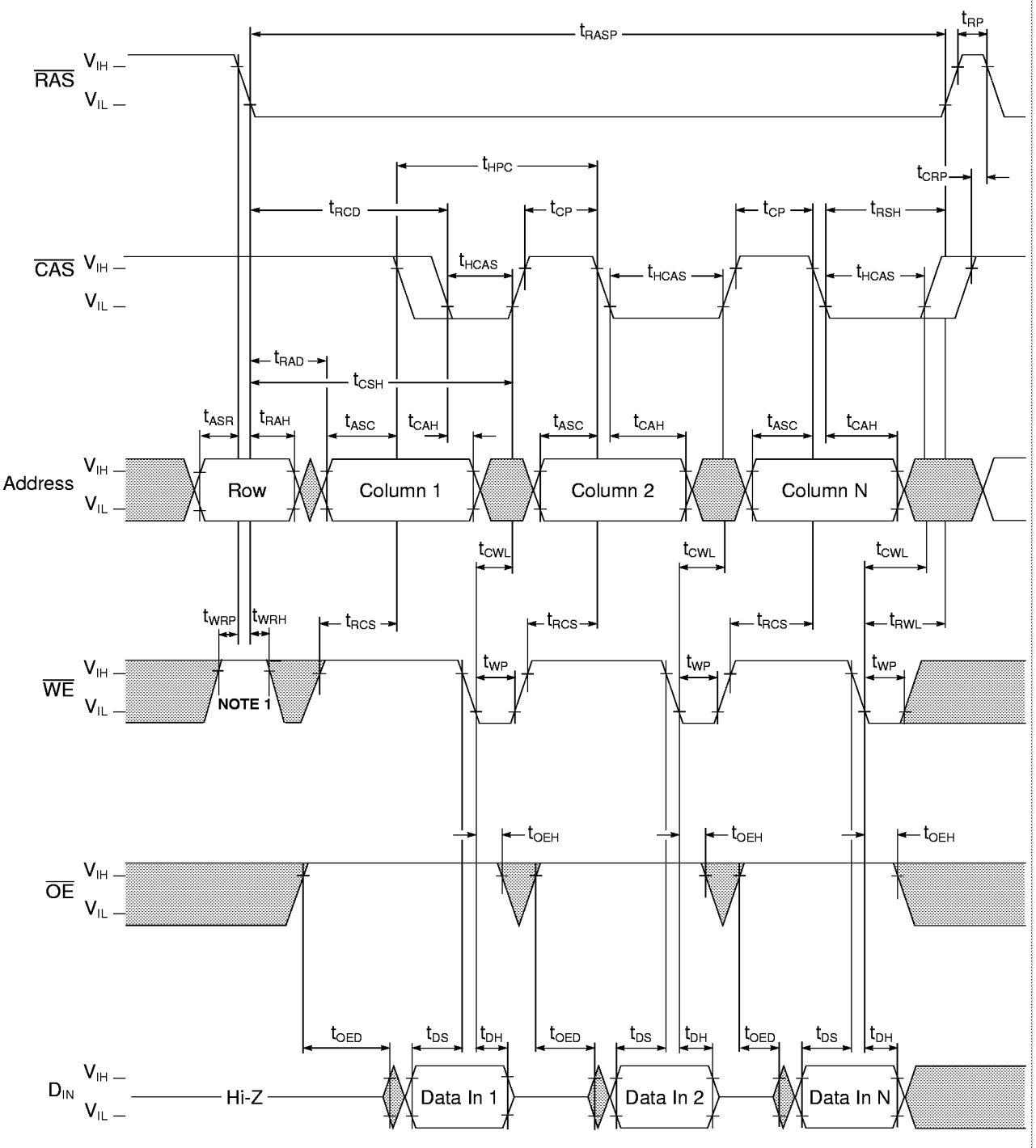


: "H" or "L"

$\overline{OE}$ = Don't care

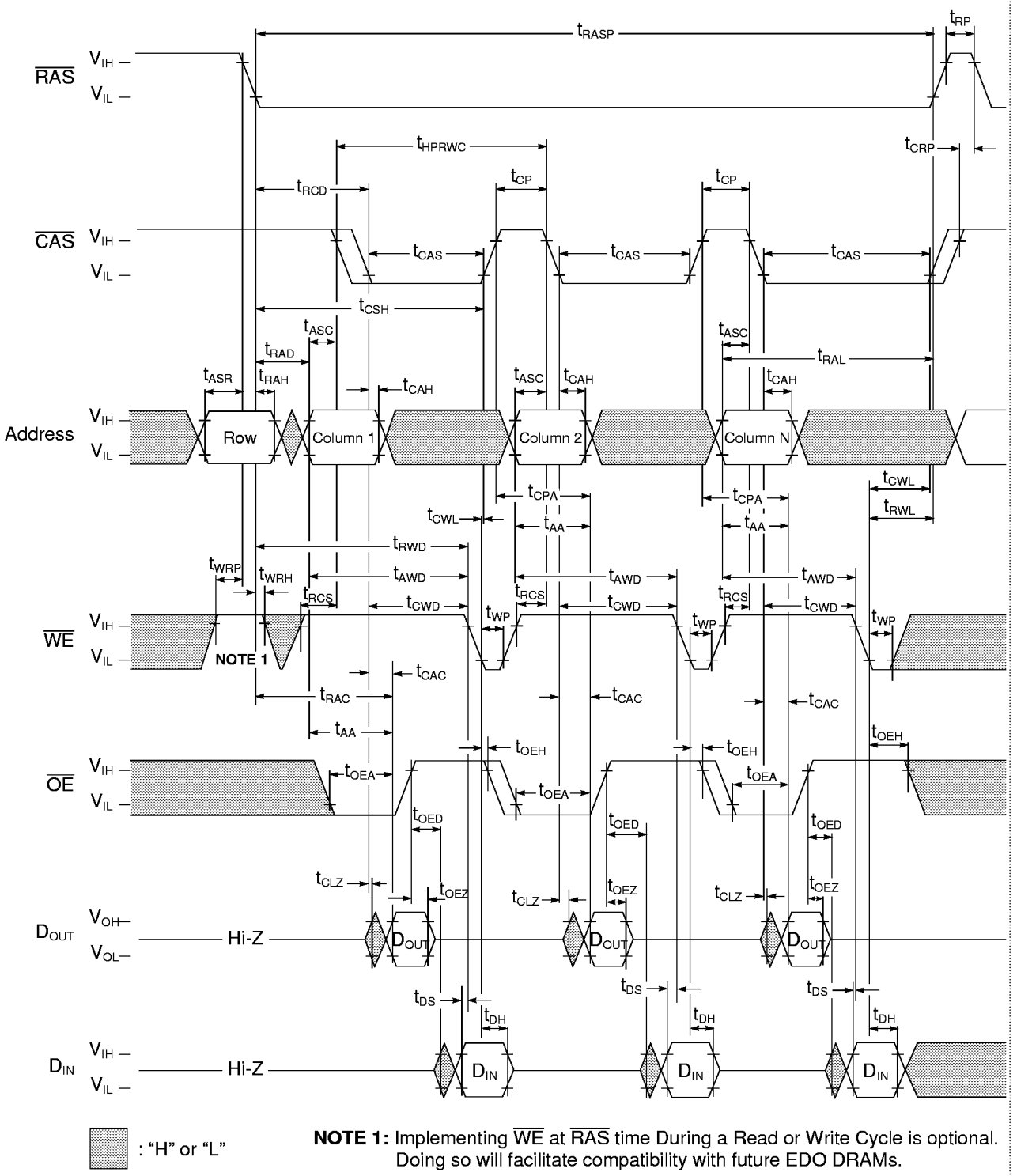
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Late Write Cycle



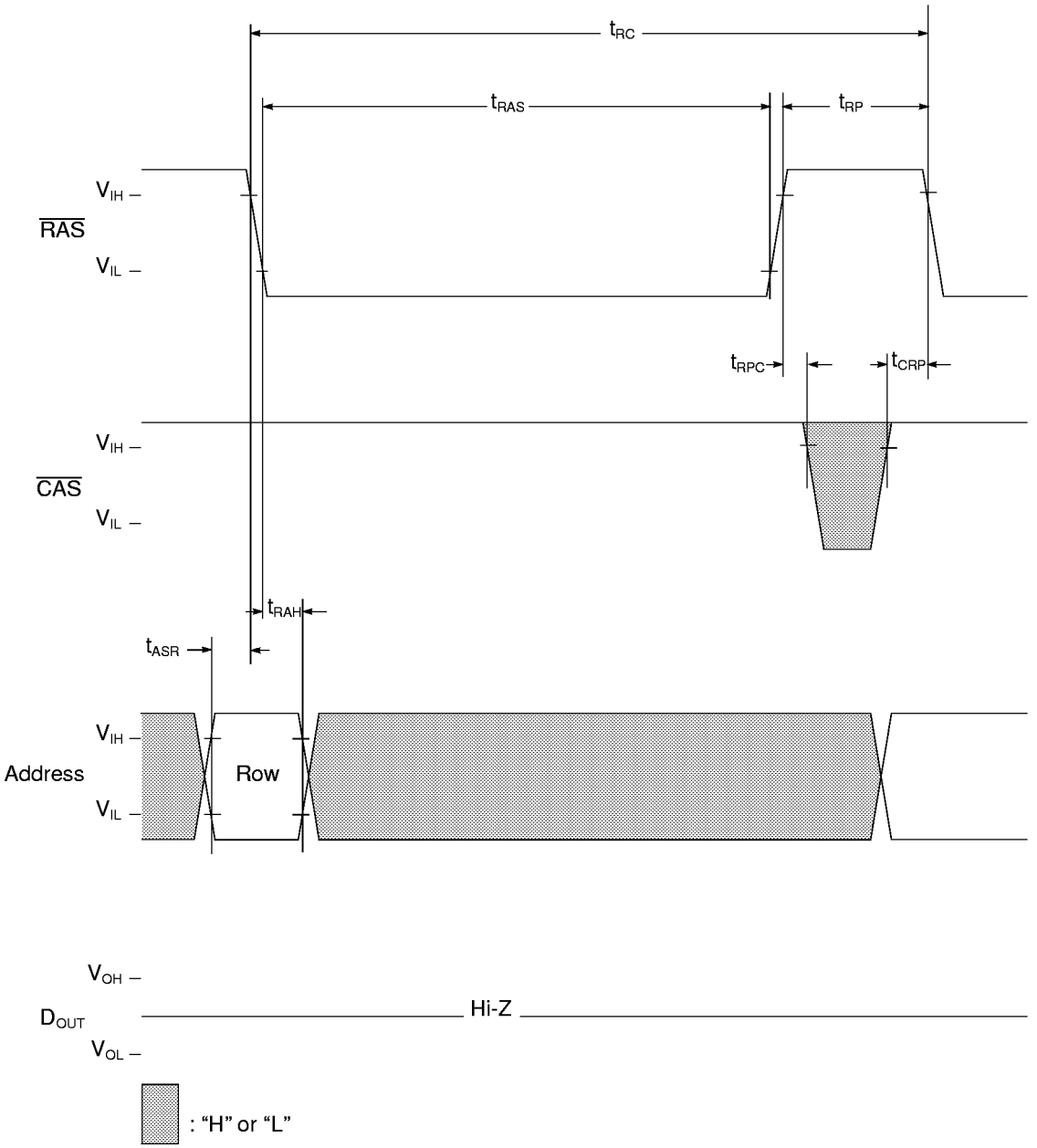
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO Page Mode Read Modify Write Cycle



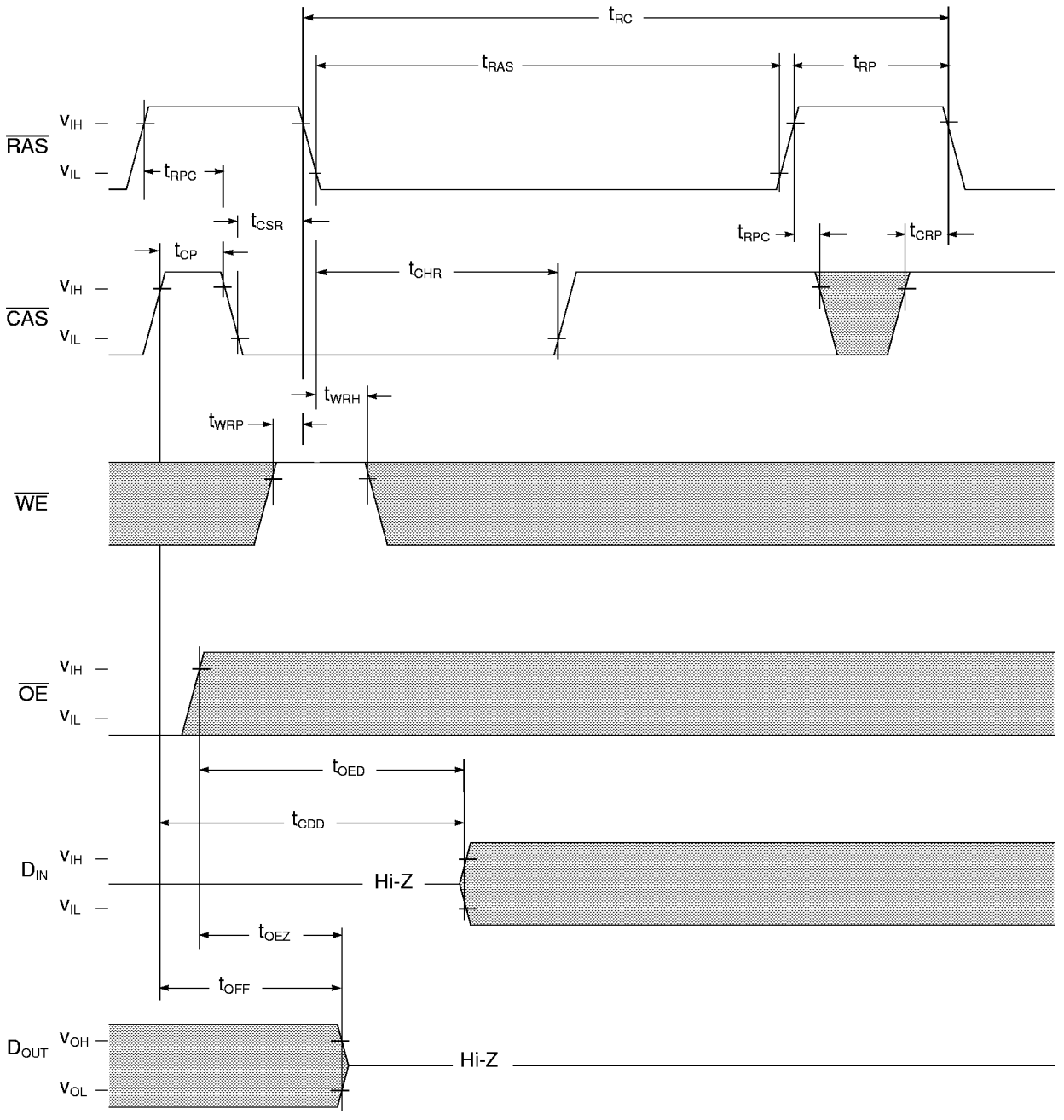
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{RAS}$ Only Refresh Cycle



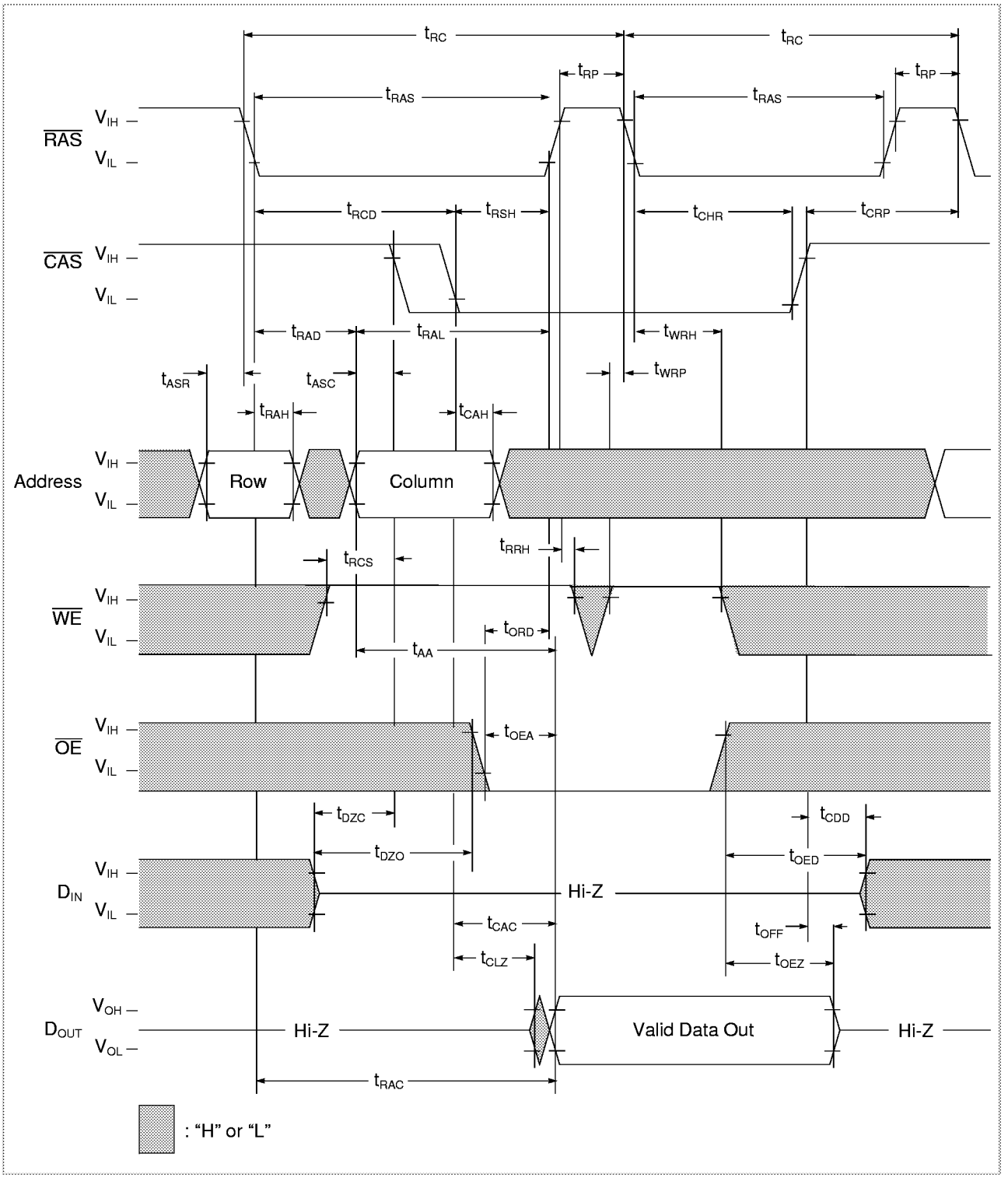
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

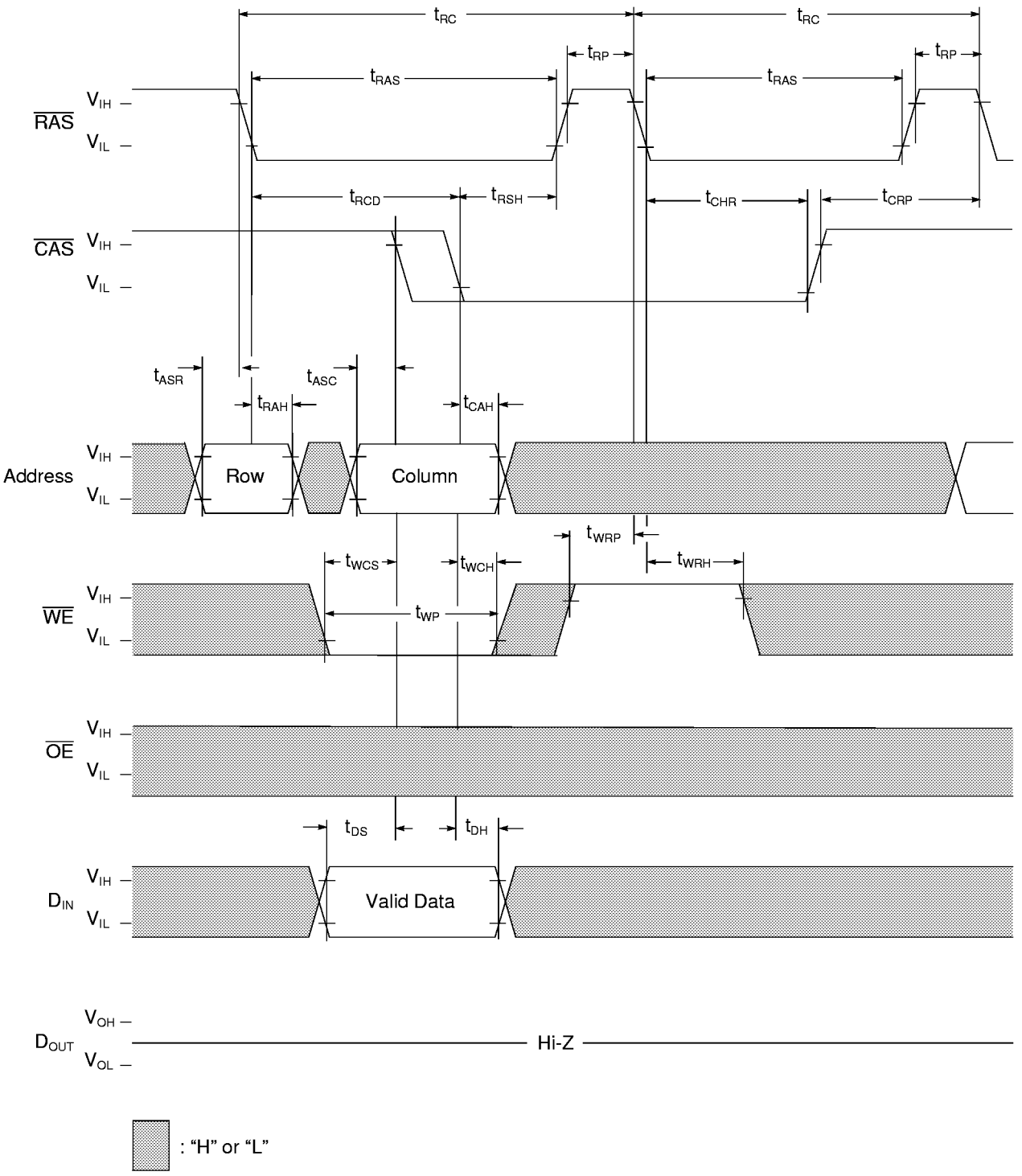


Note: Addresses are "H" or "L"

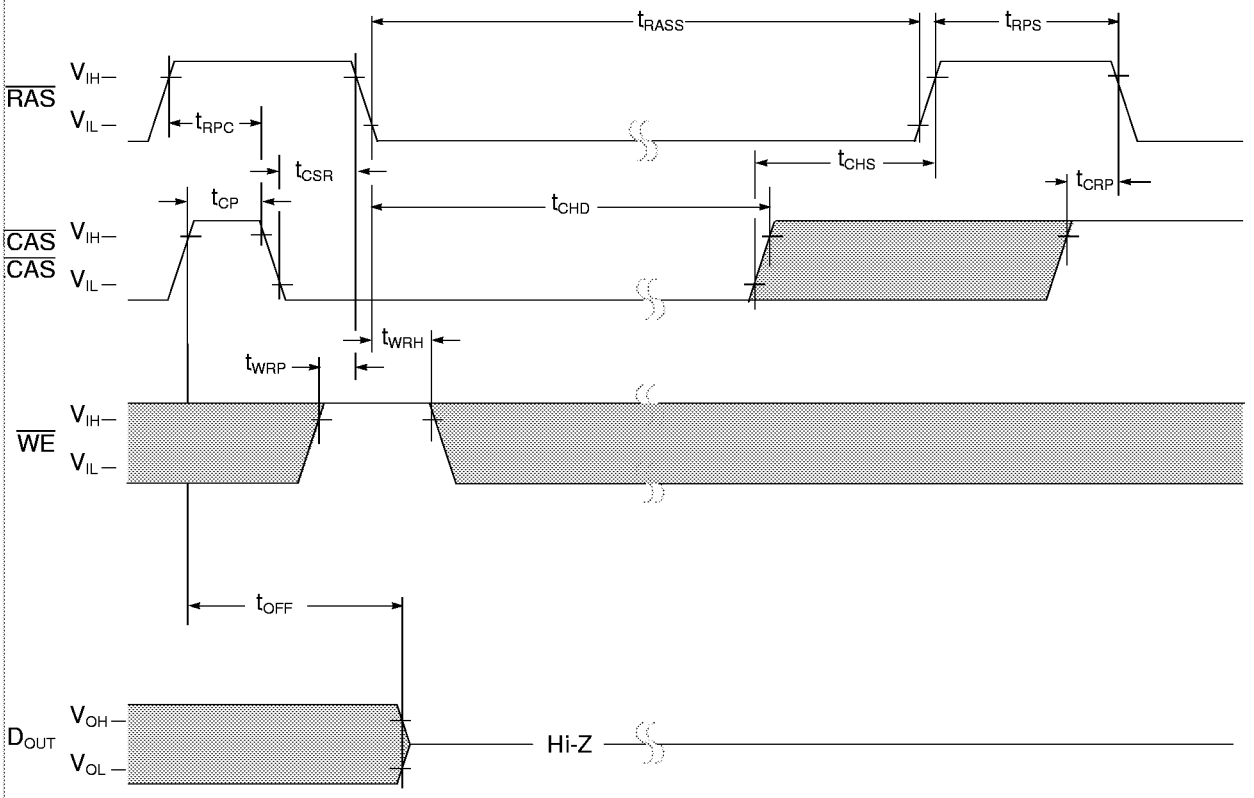
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode)

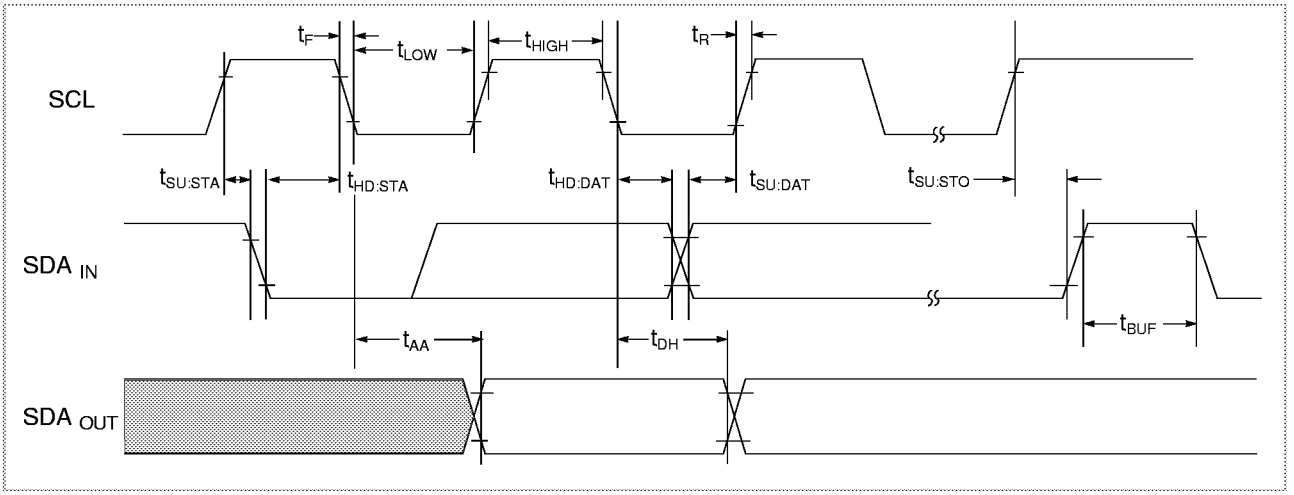


: "H" or "L"

NOTES:

1. Address and $\overline{OE}$ are "H" or "L"
2. Once $\overline{RAS}$ (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies.

Presence Detect (EEPROM) Bus Timing



Presence Detect Operation

Clock and Data Conventions: Data states on the SDA line can change only during SCL low. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 1 & Figure 2).

Start Condition: All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is high. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition: All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the serial PD device into standby power mode.

Acknowledge: Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, The PD device, will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 1. Data Window

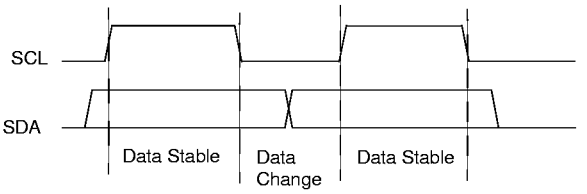


Figure 2. Definition of Start & Stop

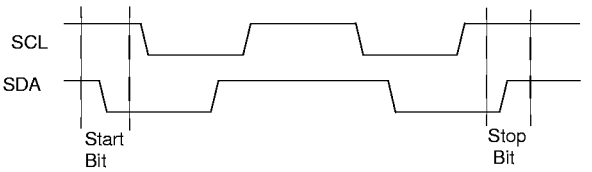
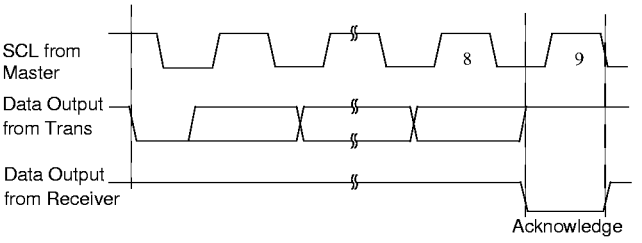
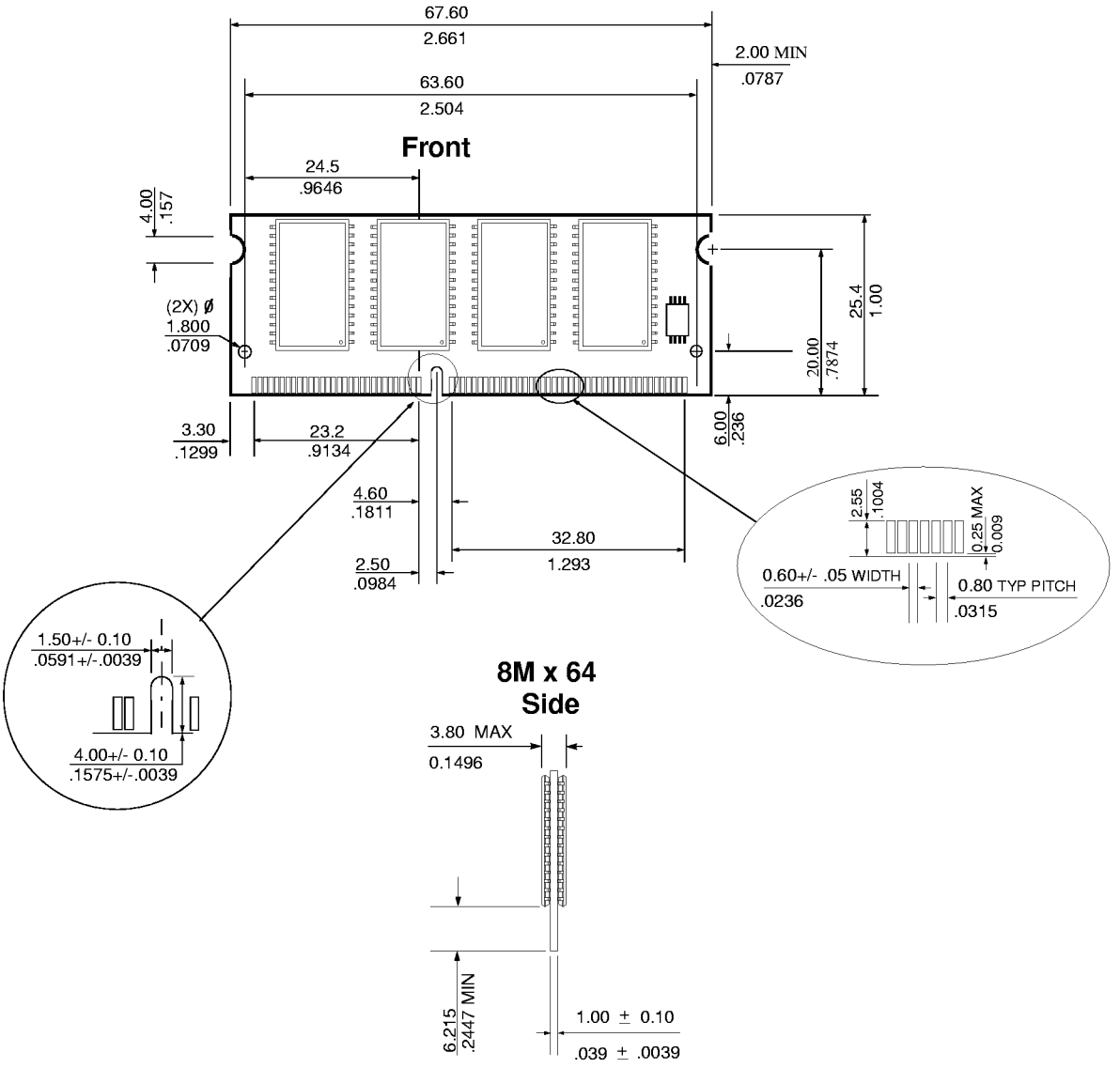


Figure 3. Acknowledge Response From Receiver



Layout Drawing



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
1/97	Initial Release.
4/97	Update Serial Presence Detect table Update power
11/97	Update Refresh Rate

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