Military & Space Products

# 5 MEGABIT MEMORY MODULE

# HX84050

RADIATION

- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.75 µm Process ($L_{eff}$ = 0.6 µm)
- Total Dose Hardness through $1x10^6$ rad ($SiO_2$)
- Neutron Hardness through $1x10^{14}$ $cm^{-2}$
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad (Si)/s
- Dose Rate Survivability through $1x10^{11}$ rad(Si)/s
- Soft Error Rate of $<1x10^{-10}$ Upsets/bit-day in Geosynchronous Orbit
- No Latchup

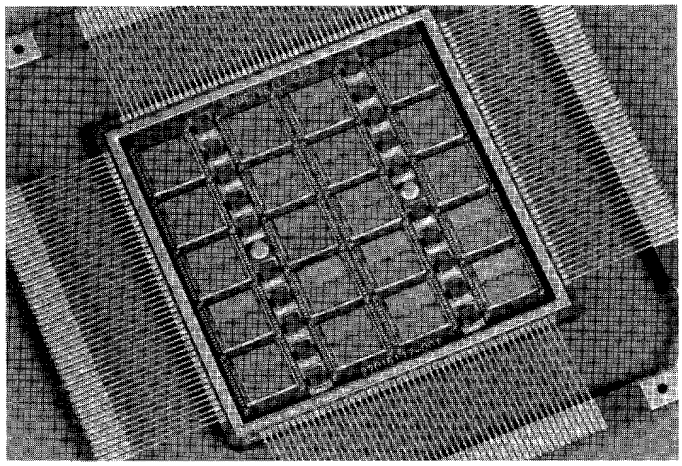
OTHER

- Listed on SMD #5962-96840
- Read/Write Cycle Times
  ≤ 20 ns (Typical)
  ≤ 30 ns (-55 to 125°C)
- Asynchronous Operation
- CMOS Compatible I/O
- Single 5 V ± 10% Power Supply
- Low Operating Power
- 200-Lead Quad Flat Pack (2.1 in. x 2.1 in.)

## GENERAL DESCRIPTION

A major emphasis in Honeywell's packaging program is the use of multichip modules (MCMs). Use of multichip modules will result in higher density packaging of integrated circuits (ICs) and components, lower weight and volume associated with size reduction, higher performance due to a decrease in interconnect length, and additional improvement with new material systems. Honeywell has had a leading role in the development and application of space qualified multichip modules for the last 14 years. In conjunction with the basic technology, we have also developed the necessary tools and methodology for the design of MCMs, Known Good Die (KGD) testing, materials/processes for assembly of MCMs, and test capability for MIL STD and QML screening.

The 5M Memory Module is organized into two separate 64K x 40 memory banks. Each memory bank contains two 32K x 40 blocks, using five SRAMs each. The two banks of memory are connected to different busses, making them logically and physically separate within each bank. Only one block is enabled and consuming power at any given time. The die are packaged in a 200-pin 2.1" x 2.1" co-fired substrate ceramic flat package.





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## FUNCTIONAL DIAGRAMS

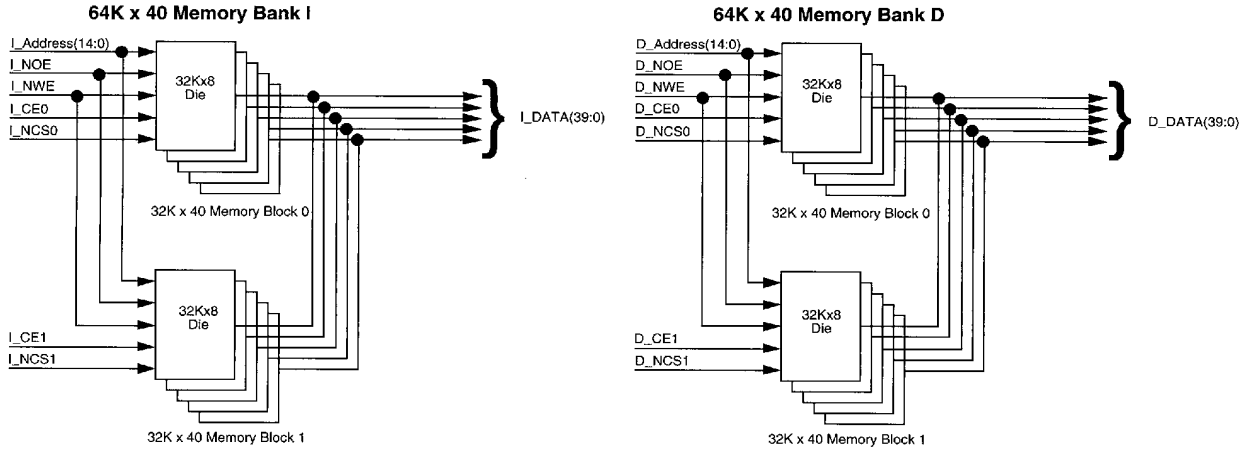



**Figure 1. 2 x 64K x 40 (Top Level Diagram)**

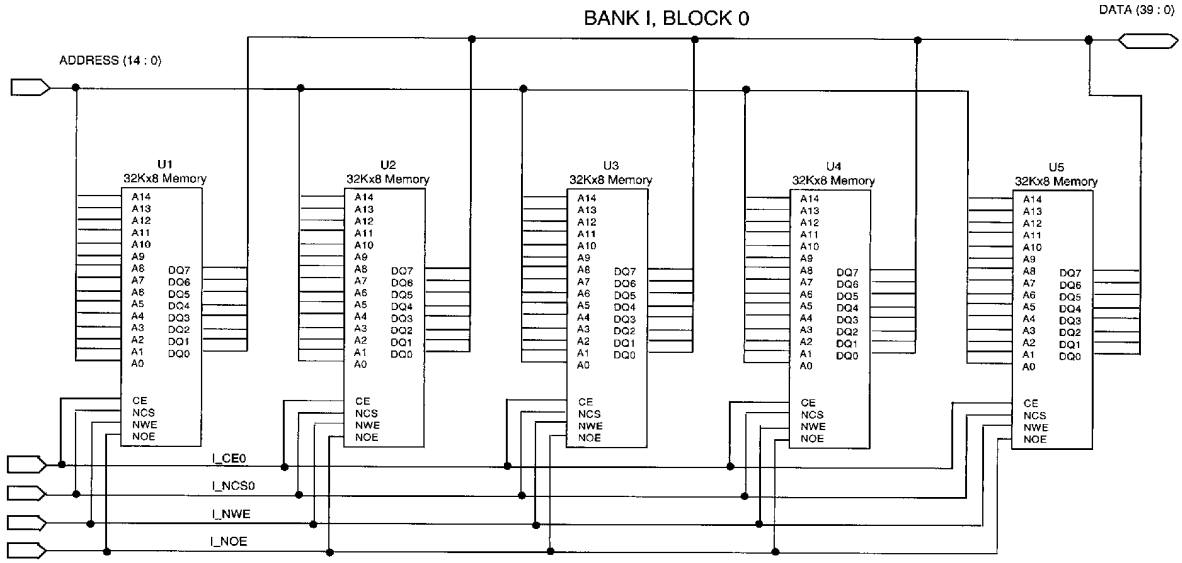



**Figure 2. 32K x 40 Memory Block Functional Diagram**

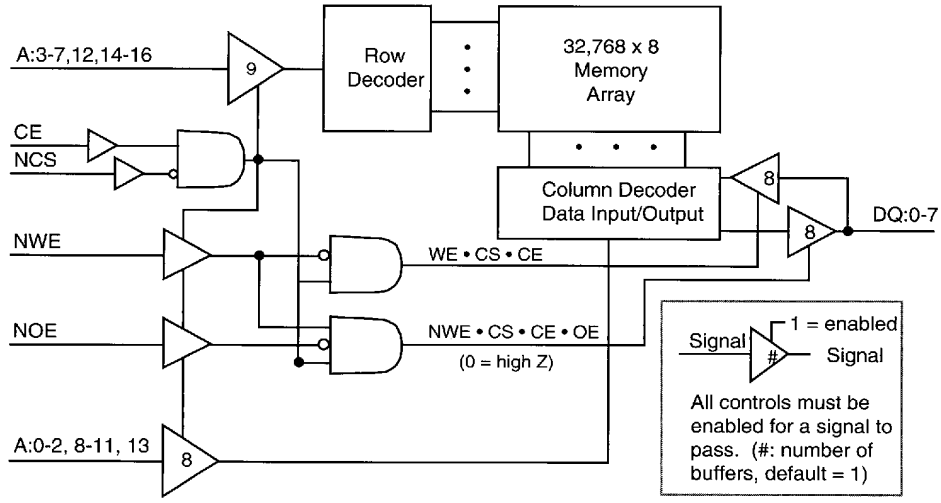



**Figure 3. 32K x 8 SRAM Functional Diagram**

## SIGNAL DEFINITIONS

Signal definitions for an individual SRAM within the five chip 32K x 40 memory block are shown below.

A: 0 - 14 Address input pins (A) which select a particular eight bit word within the memory array.

A: 0-3 (Column Select)
A: 4-11 (Row Select)
A: 12-14 (Block Select)

DQ: 0 - 7 Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS Negative chip select, when at a low level, allows normal read or write operation. When at a high level it defaults the SRAM to a pre-charge condition and holds the data output drivers in a high impedance state. All input signals except NCS and CE are disabled. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or at VDD or VSS is eliminated. If the NCS signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level it allows normal read operation.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If the NOE signal is not used it must be connected to VSS.

CE Chip enable, when at a high level, allows normal operation. When at a low level it forces the array to a pre-charge condition, holds the data output drivers in a high impedance state and disables all the input buffers except CE and NCS. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or not at VDD or VSS levels is eliminated. If the CE signal is not used it must be connected to VDD.

## TRUTH TABLE

| CE | NCS | NWE | NOE | MODE | DQ |
|---|---|---|---|---|---|
| H | L | H | L | Read | Data Out |
| H | L | L | X | Write | Data In |
| X | H | XX | XX | Deselected | High Z |
| L | X | XX | XX | Disabled | High Z |

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

## RADIATION CHARACTERISTICS

### Total Ionizing Radiation Dose

The memory module will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad($SiO_2$)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

### Transient Pulse Ionizing Radiation

The memory module is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the transient dose rate upset specification, when applied under recommended operating conditions.

The memory module will meet any functional or electrical specification after exposure to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

### Neutron Radiation

The memory module will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

### Soft Error Rate

The memory module is immune to Single Event Upsets (SEU) to the specified Soft Error Rate (SER), under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

### Latchup

The memory module will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

## RADIATION HARDNESS RATINGS (1)

| Parameter | Limits (2) | Units | Test Conditions |
|---|---|---|---|
| Total Dose | $\geq 1x10^6$ | rad($SiO_2$) | $T_A$=25°C, VDD=5.5V. X-ray or Co60 |
| Transient Dose Rate Upset | $\geq 1x10^9$ | rad(Si)/s | Pulse width ≤1 µs |
| Transient Dose Rate Survivability | $\geq 1x10^{11}$ | rad(Si)/s | Pulse width ≤50 ns, X-ray, VDD=6.0 V, $T_A$=25°C |
| Soft Error Rate | $<1x10^{-10}$ | upsets/bit-day | Adams 90% worst case environment, VDD=4.5V |
| Neutron Fluence | $\geq 1x10^{14}$ | N/cm² | 1 MeV equivalent energy, Unbiased, $T_A$=25°C |

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Parameter | Rating | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| VDD | Supply Voltage Range (2) | -0.5 | 6.5 | V |
| VPIN | Voltage on Any Pin (2) | -0.5 | VDD+0.5 | V |
| VOZ | Output Voltage Applied to High Z State (VIN and VOUT) | -0.3 | VDD+0.3 | V |
| TSTORE | Storage Temperature (Zero Bias) | -65 | 150 | °C |
| TSOLDER | Soldering Temperature (10 sec) | | +288 | °C |
| PD | Maximum Power Dissipation (3) | | 5.6 | W |
| IOUT | DC or Average Output Current | | 25 | mA |
| VPROT | ESD Input Protection Voltage | 2000 | | V |
| ΘJC | Thermal Resistance (Jct-to-Case) (4) | | 4.0 | °C/W |
| TJ | Junction Temperature | | 175 | °C |

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) All voltages are referenced to VSS (VSS = ground) unless otherwise specified.
(3) Maximum power dissipation with 20 chips utilized at 50 percent (each bank is maximally utilized, alternating between blocks).
(4) Assumes a uniform temperature on the bottom surface of the package, and a uniform power distribution over the top surface of the die and all die at equal power level.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Description | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| VDD | Supply Voltage (referenced to VSS) | 4.5 | 5.0 | 5.5 | V |
| TAC | Case Operating Temperature | -55 | 25 | 125 | °C |
| VPIN | Voltage on Any Pin (referenced to VSS) | -0.3 | | VDD+0.3 | V |

## CAPACITANCE (1)

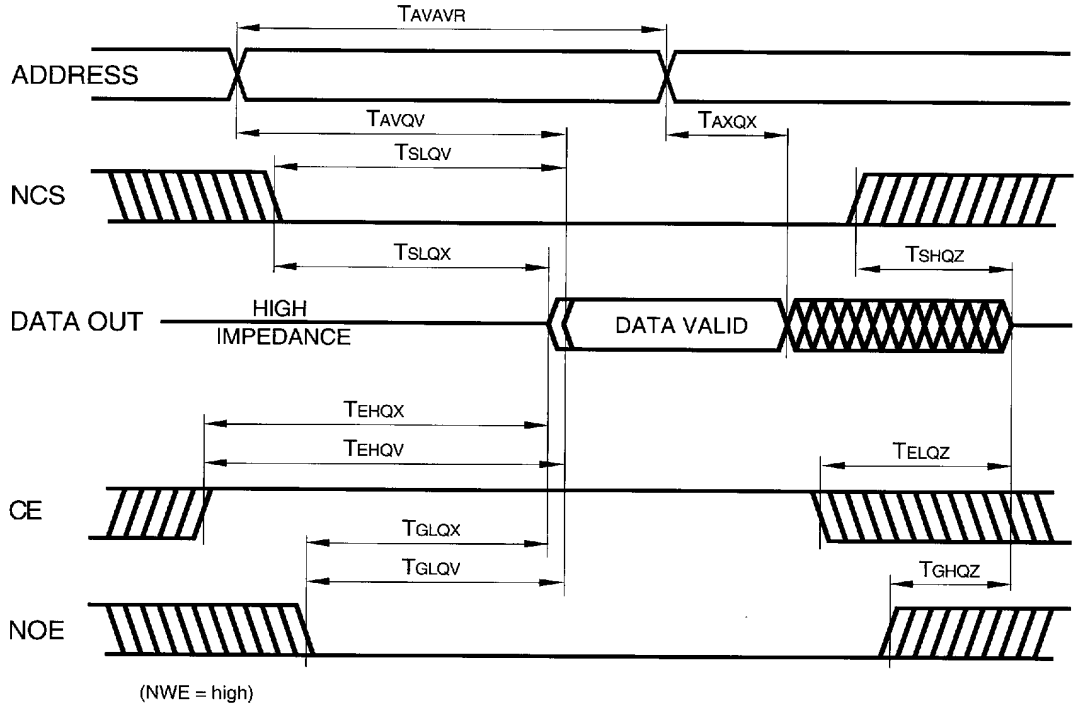
| Symbol | Parameter | Worst Case | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| CIN1 | Input Capacitance for CE and NCS Inputs | | 50 | pF | VIN=VDD or VSS, f=1 MHz |
| CIN2 | Input Capacitance for Address NOE and NWE Inputs | | 70 | pF | VIN=VDD or VSS, f=1 MHz |
| COUT | Output Capacitance | | 26 | pF | VIN=VDD or VSS, f=1 MHz |

(1) This parameter is tested during initial design characterization only.
(2) Worst case operating conditions: TA= -55°C to +125°C, past total dose at 25°C.

## READ CYCLE AC TIMING CHARACTERISTICS (1)

| Symbol (1) | Parameter | Typical (2) | Worst Case (3) -55 to 125°C Min | Worst Case (3) -55 to 125°C Max | Units |
|---|---|---|---|---|---|
| TAVAVR | Address Read Cycle Time | 20 | 30 | | ns |
| TAVQV | Address Access Time | 17 | | 26 | ns |
| TAVQX | Address Change to Output Invalid Time | | 3 | | ns |
| TSLQV | Chip Select Access Time | | | 30 | ns |
| TSLQX | Chip Select Output Enable Time | | 5 | | ns |
| TSHQZ | Chip Select Output Disable Time | | | 16 | ns |
| TEHQV | Chip Enable Access Time | | | 30 | ns |
| TEHQX | Chip Enable Output Enable Time | | 5 | | ns |
| TELQZ | Chip Enable Output Disable Time | | | 16 | ns |
| TGLQV | Output Enable Access Time | | | 13 | ns |
| TGLQX | Output Enable Output Enable Time | | 0 | | ns |
| TGHQZ | Output Enable Output Disable Time | | | 16 | ns |

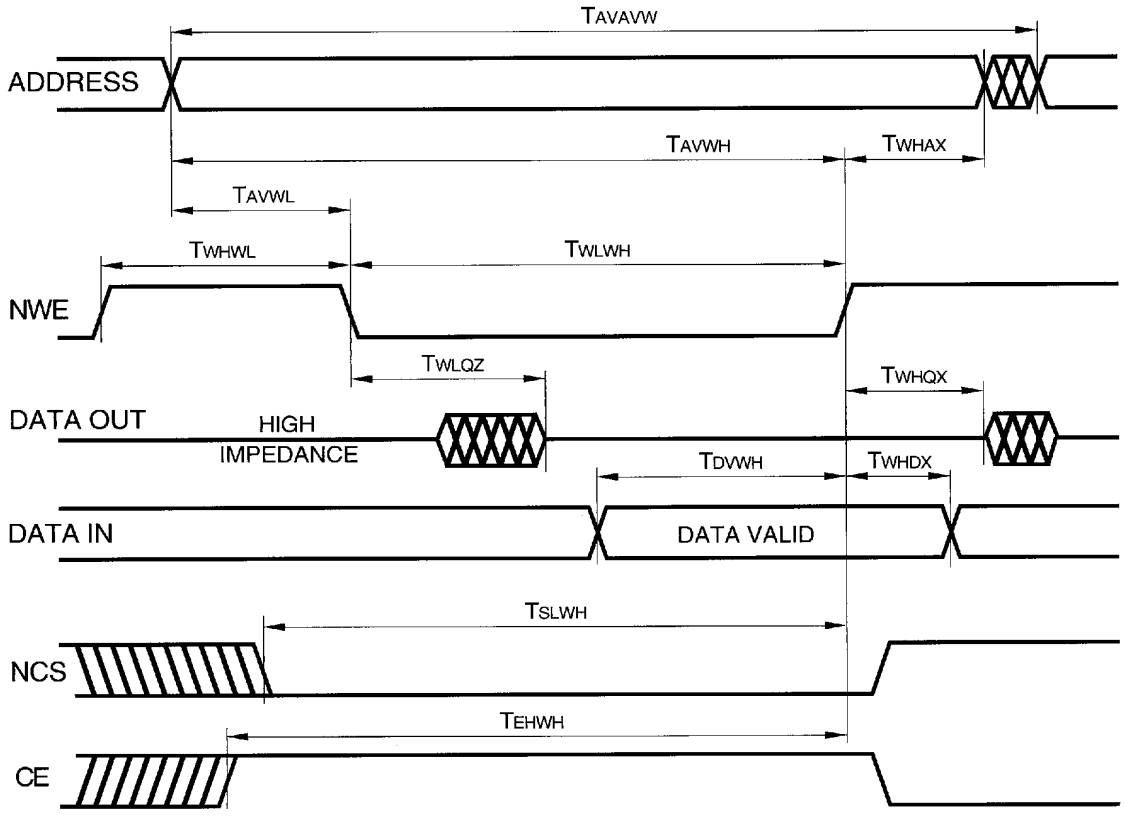
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading $C_L$=5 pF for TSHQZ, TELQZ TGHQZ. For $C_L$ >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, post total dose at 25°C.



## WRITE CYCLE AC TIMING CHARACTERISTICS (1)

| Symbol (1) | Parameter | Typical (2) | Worst Case (3) -55 to 125°C Min | Worst Case (3) -55 to 125°C Max | Units |
|---|---|---|---|---|---|
| TAVAVW | Write Cycle Time | 20 | 30 | | ns |
| TWLWH | Write Enable Write Pulse Width | 12 | 20 | | ns |
| TSLWH | Chip Select to End of Write Time | | 25 | | ns |
| TDVWH | Data Valid to End of Write Time | | 20 | | ns |
| TAVWH | Address Valid to End of Write Time | | 25 | | ns |
| TWHDX | Data Hold Time after End of Write Time | | 1 | | ns |
| TAVWL | Address Valid Setup to Start of Write Time | | 5 | | ns |
| TWHAX | Address Valid Hold after End of Write Time | | 0 | | ns |
| TWLQZ | Write Enable to Output Disable Time | | | 16 | ns |
| TWHQX | Write Disable to Output Enable Time | | 5 | | ns |
| TWHWL | Write Disable to Write Enable Pulse Width | | 6 | | ns |
| TEHWH | Chip Enable to End of Write Time | | 25 | | ns |

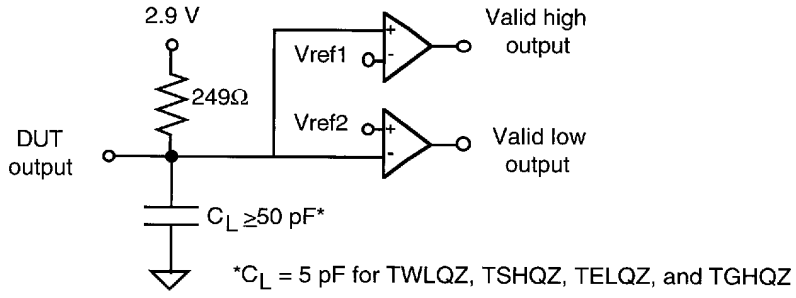
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading ≥50 pF, or equivalent capacitive load of 5 pF for TWLQZ.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, post total dose at 25°C.



## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Typical (1) | Worst Case (2) Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| ICC1 | Operating Supply Current | 250 | | 525 | mA | VDD=CE=5.5V, NCS=NOE=NWE=0V, f=20 MHz |
| ICC2 | Supply Current (Deselected) | 2 | | 30 | mA | VDD=NCS=NOE=CE=NWE=5.5V, f=20 MHz |
| ICC3 | Supply Current (Standby) | 2 | | 30 | mA | VDD=NCS=CE=5.5V, f=0.0 MHz |
| ICC4 | Supply Current (Disabled) | 2 | | 30 | mA | VDD=5.5V, NCS=CE=0V, f=20 MHz |
| ICC5 | Supply Current (Disabled, Idle) | 2 | | 30 | mA | VDD=5.5V, NCS=CE=0V, f=0.0 MHz |
| ICC6 | Data Retention Current | | | 10 | mA | VDD=NCS=NOE=CE=NWE=2.5V |
| IIL | Input Current, Low | | -50 | +50 | µA | VDD=NOE=CE=NWE=5.5V, NCS=VIL=0V |
| IIH | Input Current, High | | -50 | +50 | µA | VDD=CE=VIH=5.5V, NCS=NOE=NWE=0V |
| IOZL | Output Leakage Current, Low | | -50 | +50 | µA | VDD=NOE=CE=NWE=5.5V NCS=VOH=0V |
| IOZH | Output Leakage Current, High | | -50 | +50 | µA | VDD=NOE=CE=VOH=5.5V, NCS=NWE=0 |
| VIL | Low Level Input Voltage Range (CMOS) | | -0.3 | 0.3xVDD | V | VDD=4.5V (3) |
| VIH | High Level Input Voltage Range (CMOS) | | 0.7xVDD | VDD+0.3 | V | VDD=5.5V (3) |
| VOL | Output Low Volatage | | | 0.4 | V | VDD=CE=NWE=4.5V, NCS=NOE=0, IOL=10mA |
| VOH | Output High Voltage | | 4.2 | | V | VDD=CE=NWE=4.5V, NCS=NOE=0, IOH=-5mA |

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.
(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, post total dose at 25°C.
(3) Tested at die level test, not in MCM.




**Tester Equivalent Load Circuit**

## DYNAMIC ELECTRICAL CHARACTERISTICS

### Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

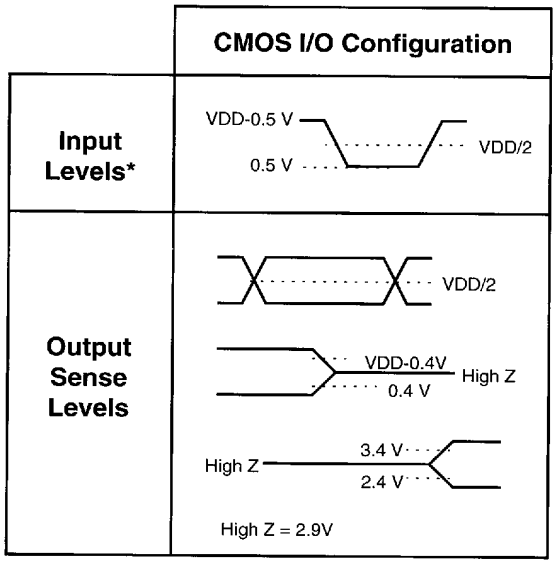
### Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. NCS differs from CE in that it does not disable the input buffers; however, both CE and NCS fully disable the RAM decode logic for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity; however, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

## TESTER AC TIMING CHARACTERISTICS




* Input rise and fall times <1 ns/V

## QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," a computer data base process performance tracking system, and a radiation hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

## SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. "Engineering Devices" are available with varying degrees of limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Microcircuits Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

## RELIABILITY

Honeywell understands the stringent reliability requirements that space and defense systems require and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer's requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

## PACKAGING

The memory MCM is offered in a custom 200-lead ceramic quad flat pack. The package is constructed of multilayer ceramic ($Al_2O_3$) and features internal power and ground planes.

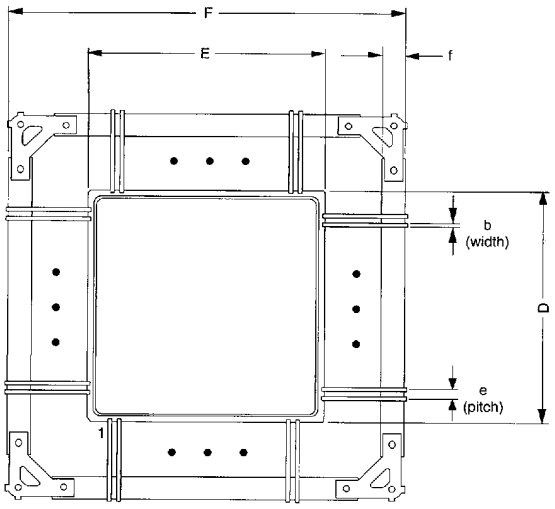
Ceramic chip capacitors (20) are mounted inside the package to maximize supply noise decoupling and avoid ground bounce. These capacitors effectively attach to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment.

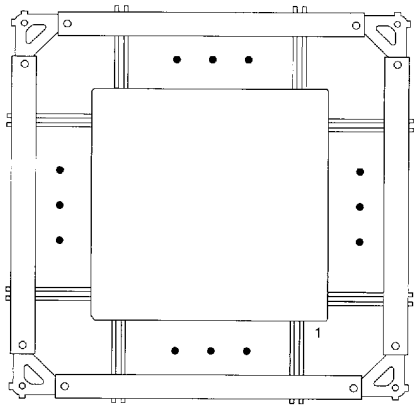
## 200-LEAD QUAD FLAT PACK PIN LIST

| Pin | Signal Name | Pin Type | Pin | Signal Name | Pin Type | Pin | Signal Name | Pin Type | Pin | Signal Name | Pin Type | Pin | Signal Name | Pin Type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VSS | Pwr/Gnd | 41 | D_DATA(08) | Tri-State | 81 | D_DATA(22) | Tri-State | 121 | D_DATA(38) | Tri-State | 161 | I_DATA(27) | Tri-State |
| 2 | I_ADRS(04) | Input | 42 | D_DATA(09) | Tri-State | 82 | VSS | Pwr/Gnd | 122 | D_DATA(39) | Tri-State | 162 | VDD | Pwr/Gnd |
| 3 | I_ADRS(03) | Input | 43 | D_ADRS(00) | Input | 83 | VDD | Pwr/Gnd | 123 | D_NCS0 | Input | 163 | VSS | Pwr/Gnd |
| 4 | I_ADRS(02) | Input | 44 | VSS | Pwr/Gnd | 84 | D_DATA(23) | Tri-State | 124 | VDD | Pwr/Gnd | 164 | I_DATA(26) | Tri-State |
| 5 | I_ADRS(01) | Input | 45 | VDD | Pwr/Gnd | 85 | D_DATA(24) | Tri-State | 125 | VSS | Pwr/Gnd | 165 | I_DATA(25) | Tri-State |
| 6 | VDD | Pwr/Gnd | 46 | D_ADRS(01) | Input | 86 | D_DATA(25) | Tri-State | 126 | VSS | Pwr/Gnd | 166 | I_DATA(24) | Tri-State |
| 7 | VSS | Pwr/Gnd | 47 | D_ADRS(02) | Input | 87 | D_DATA(26) | Tri-State | 127 | VDD | Pwr/Gnd | 167 | I_DATA(23) | Tri-State |
| 8 | I_ADRS(00) | Input | 48 | D_ADRS(03) | Input | 88 | VSS | Pwr/Gnd | 128 | D_NCS0 | Input | 168 | VDD | Pwr/Gnd |
| 9 | I_DATA(09) | Tri-State | 49 | D_ADRS(04) | Input | 89 | VDD | Pwr/Gnd | 129 | I_DATA(39) | Tri-State | 169 | VSS | Pwr/Gnd |
| 10 | I_DATA(08) | Tri-State | 50 | VSS | Pwr/Gnd | 90 | D_DATA(27) | Tri-State | 130 | I_DATA(38) | Tri-State | 170 | I_DATA(22) | Tri-State |
| 11 | I_DATA(07) | Tri-State | 51 | VSS | Pwr/Gnd | 91 | D_DATA(28) | Tri-State | 131 | I_DATA(37) | Tri-State | 171 | I_DATA(21) | Tri-State |
| 12 | VDD | Pwr/Gnd | 52 | VDD | Pwr/Gnd | 92 | D_DATA(29) | Tri-State | 132 | VSS | Pwr/Gnd | 172 | I_DATA(20) | Tri-State |
| 13 | VSS | Pwr/Gnd | 53 | D_ADRS(05) | Input | 93 | D_ADRS(09) | Input | 133 | VDD | Pwr/Gnd | 173 | I_NOE | Input |
| 14 | I_DATA(06) | Tri-State | 54 | D_ADRS(06) | Input | 94 | VSS | Pwr/Gnd | 134 | I_DATA(36) | Tri-State | 174 | VDD | Pwr/Gnd |
| 15 | I_DATA(05) | Tri-State | 55 | D_ADRS(07) | Input | 95 | VDD | Pwr/Gnd | 135 | I_DATA(35) | Tri-State | 175 | VSS | Pwr/Gnd |
| 16 | I_DATA(04) | Tri-State | 56 | VDD | Pwr/Gnd | 96 | D_ADRS(10) | Input | 136 | I_DATA(34) | Tri-State | 176 | VSS | Pwr/Gnd |
| 17 | I_DATA(03) | Tri-State | 57 | VSS | Pwr/Gnd | 97 | D_ADRS(11) | Input | 137 | I_DATA(33) | Tri-State | 177 | VDD | Pwr/Gnd |
| 18 | VDD | Pwr/Gnd | 58 | D_ADRS(08) | Input | 98 | D_ADRS(12) | Input | 138 | VSS | Pwr/Gnd | 178 | I_NWE | Input |
| 19 | VSS | Pwr/Gnd | 59 | D_DATA(10) | Tri-State | 99 | VDD | Pwr/Gnd | 139 | VDD | Pwr/Gnd | 179 | I_DATA(19) | Tri-State |
| 20 | I_DATA(02) | Tri-State | 60 | D_DATA(11) | Tri-State | 100 | VSS | Pwr/Gnd | 140 | I_DATA(32) | Tri-State | 180 | I_DATA(18) | Tri-State |
| 21 | I_DATA(01) | Tri-State | 61 | D_DATA(12) | Tri-State | 101 | VSS | Pwr/Gnd | 141 | I_DATA(31) | Tri-State | 181 | I_DATA(17) | Tri-State |
| 22 | I_DATA(00) | Tri-State | 62 | VDD | Pwr/Gnd | 102 | VDD | Pwr/Gnd | 142 | I_DATA(30) | Tri-State | 182 | VSS | Pwr/Gnd |
| 23 | I_NCS1 | Input | 63 | VSS | Pwr/Gnd | 103 | D_CE0 | Input | 143 | I_ADRS(14) | Input | 183 | VDD | Pwr/Gnd |
| 24 | VDD | Pwr/Gnd | 64 | D_DATA(13) | Tri-State | 104 | D_CE1 | Input | 144 | VSS | Pwr/Gnd | 184 | I_DATA(16) | Tri-State |
| 25 | VSS | Pwr/Gnd | 65 | D_DATA(14) | Tri-State | 105 | D_ADRS(13) | Input | 145 | VDD | Pwr/Gnd | 185 | I_DATA(15) | Tri-State |
| 26 | VSS | Pwr/Gnd | 66 | D_DATA(15) | Tri-State | 106 | VDD | Pwr/Gnd | 146 | I_ADRS(13) | Input | 186 | I_DATA(14) | Tri-State |
| 27 | VDD | Pwr/Gnd | 67 | D_DATA(16) | Tri-State | 107 | VSS | Pwr/Gnd | 147 | I_CE1 | Input | 187 | I_DATA(13) | Tri-State |
| 28 | D_NCS1 | Input | 68 | VDD | Pwr/Gnd | 108 | D_ADRS(14) | Input | 148 | I_CE0 | Input | 188 | VSS | Pwr/Gnd |
| 29 | D_DATA(00) | Tri-State | 69 | VSS | Pwr/Gnd | 109 | D_DATA(30) | Tri-State | 149 | VDD | Pwr/Gnd | 189 | VDD | Pwr/Gnd |
| 30 | D_DATA(01) | Tri-State | 70 | D_DATA(17) | Tri-State | 110 | D_DATA(31) | Tri-State | 150 | VSS | Pwr/Gnd | 190 | I_DATA(12) | Tri-State |
| 31 | D_DATA(02) | Tri-State | 71 | D_DATA(18) | Tri-State | 111 | D_DATA(32) | Tri-State | 151 | VSS | Pwr/Gnd | 191 | I_DATA(11) | Tri-State |
| 32 | VSS | Pwr/Gnd | 72 | D_DATA(19) | Tri-State | 112 | VDD | Pwr/Gnd | 152 | VDD | Pwr/Gnd | 192 | I_DATA(10) | Tri-State |
| 33 | VDD | Pwr/Gnd | 73 | D_NWE | Input | 113 | VSS | Pwr/Gnd | 153 | I_ADRS(12) | Input | 193 | I_ADRS(08) | Input |
| 34 | D_DATA(03) | Tri-State | 74 | VDD | Pwr/Gnd | 114 | D_DATA(33) | Tri-State | 154 | I_ADRS(11) | Input | 194 | VSS | Pwr/Gnd |
| 35 | D_DATA(04) | Tri-State | 75 | VSS | Pwr/Gnd | 115 | D_DATA(34) | Tri-State | 155 | I_ADRS(10) | Input | 195 | VDD | Pwr/Gnd |
| 36 | D_DATA(05) | Tri-State | 76 | VSS | Pwr/Gnd | 116 | D_DATA(35) | Tri-State | 156 | VDD | Pwr/Gnd | 196 | I_ADRS(07) | Input |
| 37 | D_DATA(06) | Tri-State | 77 | VDD | Pwr/Gnd | 117 | D_DATA(36) | Tri-State | 157 | VSS | Pwr/Gnd | 197 | I_ADRS(06) | Input |
| 38 | VSS | Pwr/Gnd | 78 | D_NOE | Input | 118 | VDD | Pwr/Gnd | 158 | I_ADRS(09) | Input | 198 | I_ADRS(05) | Input |
| 39 | VDD | Pwr/Gnd | 79 | D_DATA(20) | Tri-State | 119 | VSS | Pwr/Gnd | 159 | I_DATA(29) | Tri-State | 199 | VDD | Pwr/Gnd |
| 40 | D_DATA(07) | Tri-State | 80 | D_DATA(21) | Tri-State | 120 | D_DATA(37) | Tri-State | 160 | I_DATA(28) | Tri-State | 200 | VSS | Pwr/Gnd |

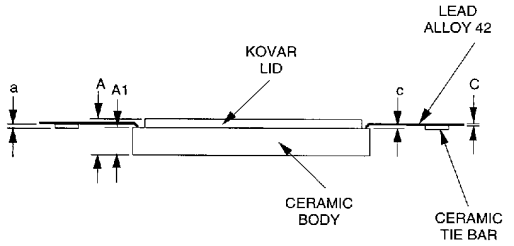
# HX84050

## 200-LEAD QUAD FLAT PACK




| Dimensions in inches | |
|---|---|
| A | 0.203 max |
| A1 | 0.149±.015 |
| a | 0.035±.005 |
| b | 0.010 +.002 - 0.001 |
| C | 0.006 +.002 -0.001 |
| c | 0.008 REF |
| D | 2.100±.021 |
| E | 2.100±.021 |
| e | 0.035 |
| F | 3.500±.035 |
| f | 0.200±.005 |




## ORDERING INFORMATION (1)

| H | X | 84050 | S | R |
|---|---|---|---|---|
| **SOURCE**<br>H=HONEYWELL | **PROCESS**<br>X=SOI | **PART NUMBER** | **SCREEN LEVEL**<br>V=QML Class V<br>Q=QML Class Q<br>S=Class S<br>B=Class B<br>E=Engr Device (2) | **TOTAL DOSE HARDNESS**<br>R=1x10$^5$ rad(SiO$_2$)<br>F=3x10$^5$ rad(SiO$_2$)<br>H=1x10$^6$ rad(SiO$_2$)<br>N=No Level Guaranteed |

(1) Orders may be faxed to 612-954-2051. For technical assistance, contact our Customer Service Department at 612-954-2888.
(2) Engineering device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed.
Contact Factory with other needs.

**To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com**



**Honeywell**

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