HM65V8512 Series

3.0 V & 3.3 V Supply

524288-Word × 8-Bit High Speed Pseudo Static RAM

Description

HM65V8512 is a pseudo-static RAM organized as 524,288-word × 8-bit. HM65V8512 realized low power consumption by employing 0.8 μm CMOS process technology.

Power supply voltage if 3 V ± 10% and all inputs and outputs are CMOS compatible. The low power version dissipates only 60 μW (typ) in self refresh mode, so it retains the data with battery.

The HM65V8512 is pin-compatible with 4-Mbit static RAM and with 4-Mbits 5 V operation Pseudo Static RAM.

Features

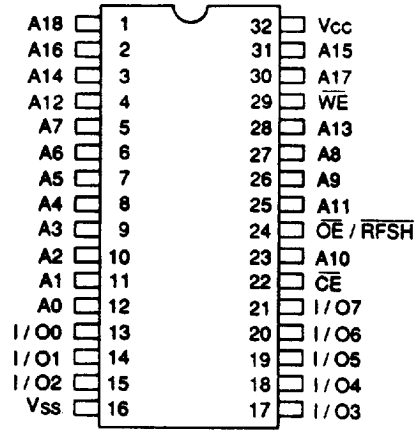
- Single 3 V (±10%)
- High speed
  - —Access time
    $\overline{CE}$ access time: 120 ns/150 ns (max)
  - —Cycle time
    Random read.write cycle time:
    190 ns/230 ns (min)
- Low power
  - —75 mW typ active
  - —60 μW typ standby
- All inputs and outputs CMOS compatible
- Package
  - —32-pin SOP package
  - —32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions:
  - —L/LV-version: Address refresh
    Automatic refresh
    Self refresh
  - —D-version: Address refresh
    Automatic refresh

Ordering Information

Type No.	Access time	Package
HM65V8512DFP-12	120 ns	32-pin plastic SOP (FP-32D)
HM65V8512DFP-15	150 ns	
HM65V8512LFP-12	120 ns	
HM65V8512LFP-15	150 ns	
HM65V8512LFP-12V	120 ns	
HM65V8512LFP-15V	150 ns	
HM65V8512DTT-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP (TTP-32D)
HM65V8512DTT-15	150 ns	
HM65V8512LTT-12	120 ns	
HM65V8512LTT-15	150 ns	
HM65V8512LTT-12V	120 ns	
HM65V8512LTT-15V	150 ns	
HM65V8512DRR-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TTP-32DR)
HM65V8512DRR-15	150 ns	
HM65V8512LRR-12	120 ns	
HM65V8512LRR-15	150 ns	
HM65V8512LRR-12V	120 ns	
HM65V8512LRR-15V	150 ns	

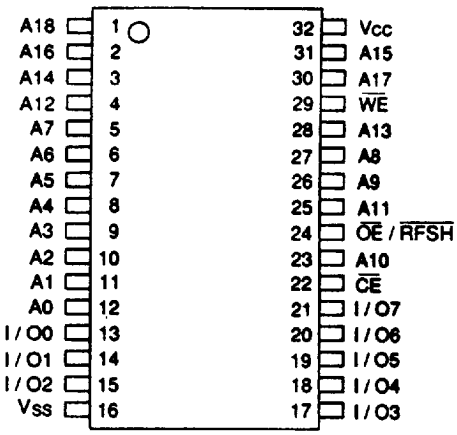
Pin Arrangement

HM65V8512FP Series



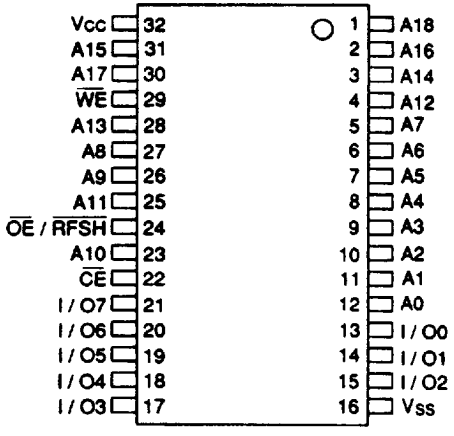
(Top View)

HM65V8512TT Series



(Top View)

HM65V8512RR Series



(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/RFSH	Output enable/refresh
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

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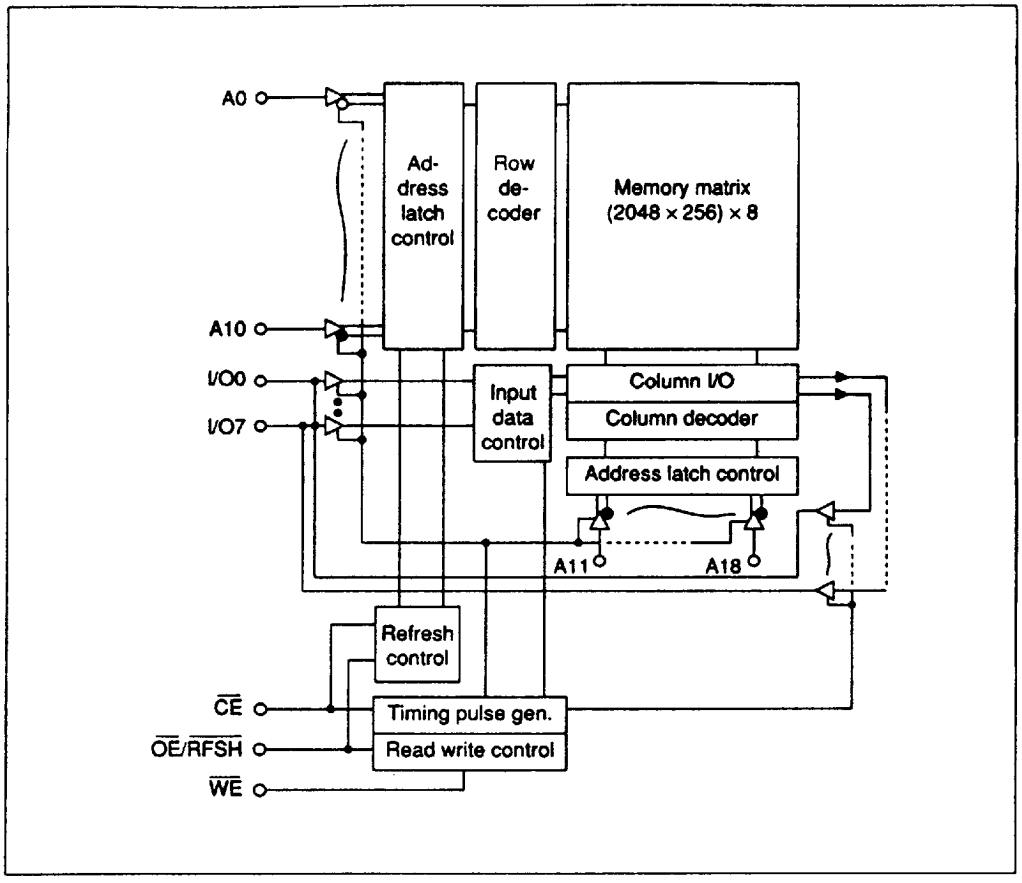
Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LV-version.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	−0.5 to +6.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.1	—	6.0	V
	V_{IL}	−0.5 *1	—	0.7	V

Note: 1. V_{IL} min = −1.2 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	25	40	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	—	0.5	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/RFSH = V_{IH}
	I_{SB2}	—	8	20	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V, Vin ≥ 0 V $\overline{OE}$/RFSH ≥ V_{CC} − 0.2 V
Operating power supply current in self refresh mode	I_{CC2}	—	—	0.5 *1	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/RFSH = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	20 *1	40 *1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V $\overline{OE}$/RFSH ≤ 0.2 V Vin ≥ 0 V
Input leakage current	I_{LI}	−5	—	5	µA	V_{CC} = 3.3 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version and LV-version.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	−5	—	5	µA	$\overline{OE}/RFSH$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA
	V_{OH}	2.6	—	—	V	I_{OH} = −100 µA

Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.6 V
Input rise and fall times: 5 ns
Timing measurement level: 1.5 V
Reference level: V_{OH} = 2.1 V, V_{OL} = 0.9 V
Output load: 50 pF

		HM65V8512-12		HM65V8512-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	190	—	230	—	ns	
Chip enable access time	t_{CEA}	—	120	—	150	ns	
Read-modify-write cycle time	t_{RWC}	250	—	290	—	ns	
Output enable access time	t_{OEA}	—	60	—	80	ns	
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	ns	1, 2
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	ns	2
Output disable to output in high-Z	t_{OHZ}	—	30	—	30	ns	1, 2
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns	2

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%) (cont)

Parameter	Symbol	HM65V8512-12 Min	HM65V8512-12 Max	HM65V8512-15 Min	HM65V8512-15 Max	Unit	Notes
Chip enable pulse width	t_{CE}	120 ns	10 µs	150 ns	10 µs		
Chip enable precharge time	t_P	70	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address hold time	t_{AH}	30	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	
Write command pulse width	t_{WP}	35	—	35	—	ns	
Chip enable to end of write	t_{CW}	120	—	150	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	ns	
Data in to end of write	t_{DW}	30	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	30	—	30	ns	1, 2
Transition time (rise and fall)	t_T	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	70	—	80	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs		
Automatic refresh cycle time	t_{FC}	190	—	230	—	ns	
Refresh command pulse width for self refresh	t_{FAS}*9	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}*9	600	_	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	ms	2048 cycle

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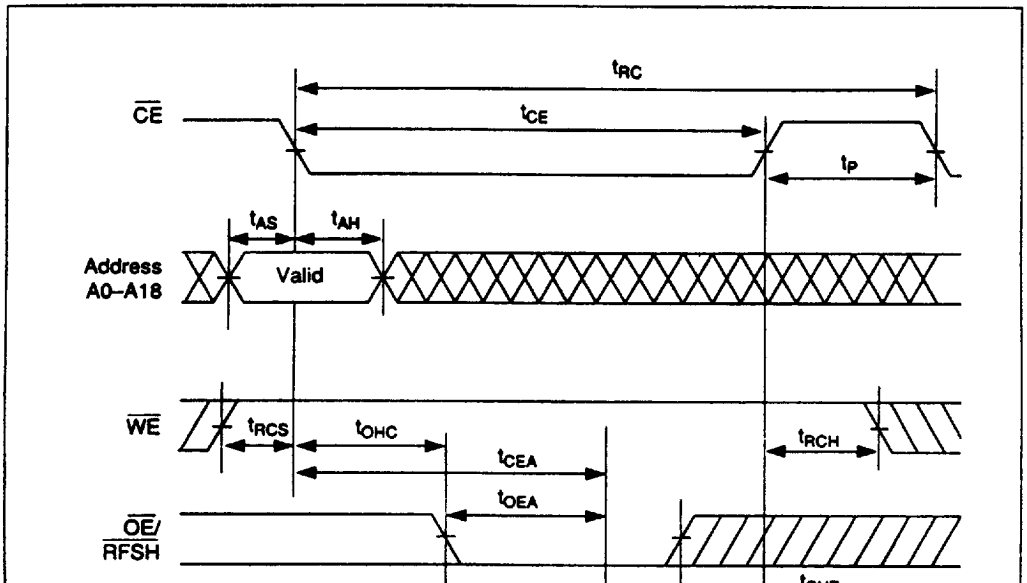
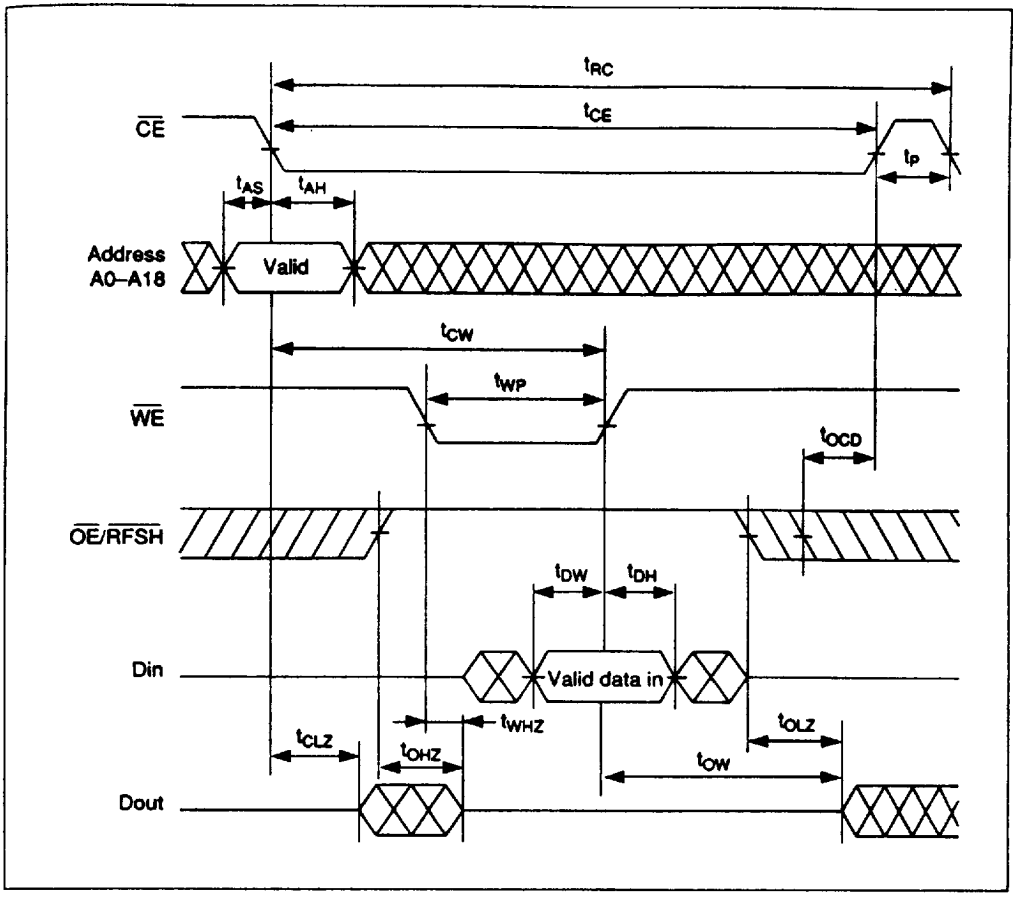
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ}, t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LV-version.
10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{OE}$/RFSH must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}$/RFSH at the beginning of auto refresh must not occur during t_{RFS} period.

Timing Waveforms

Read Cycle



Write Cycle (1) ($\overline{OE}$ High)



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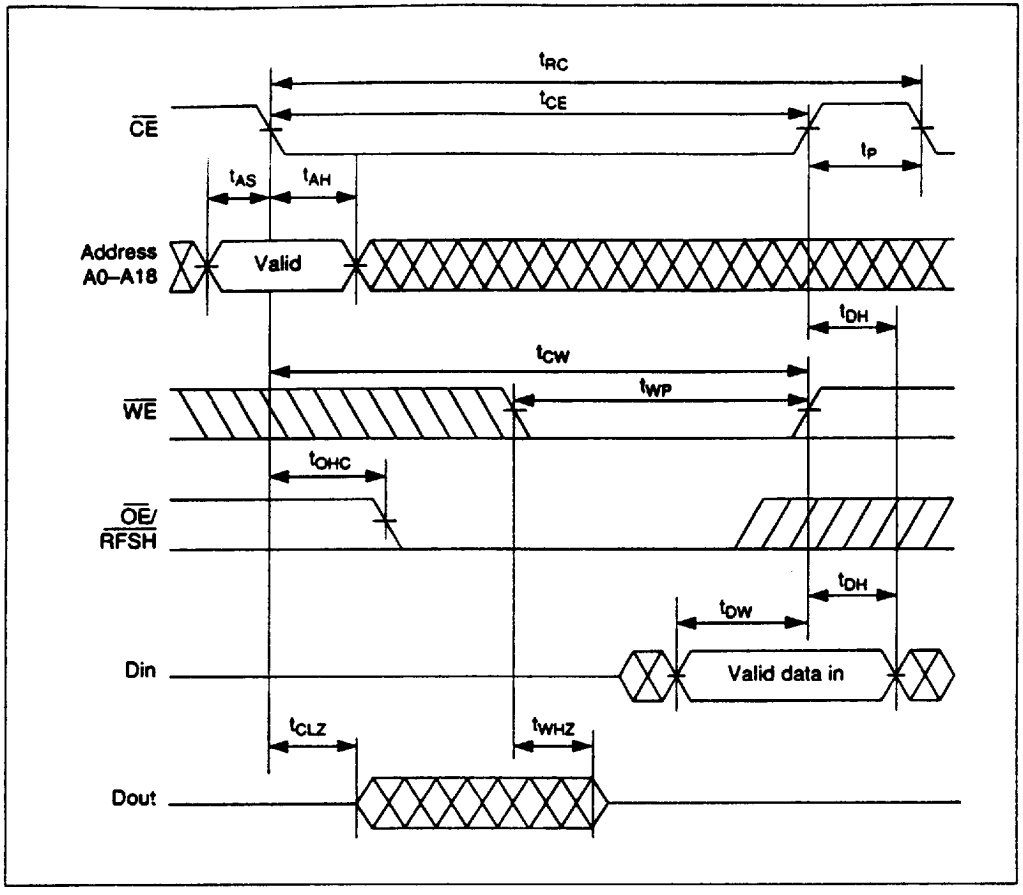
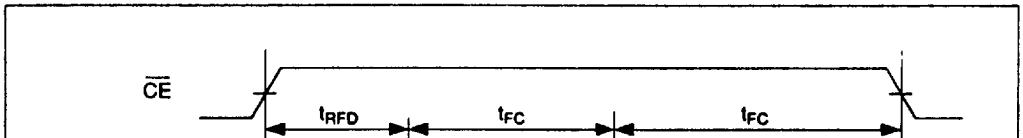
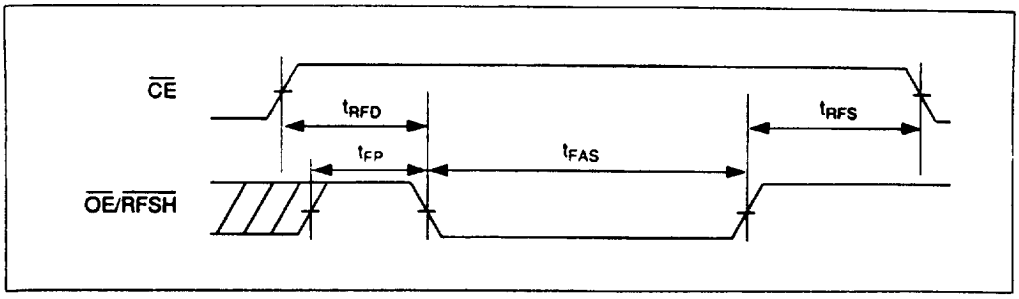
Write Cycle (2) ($\overline{OE}$ Low)



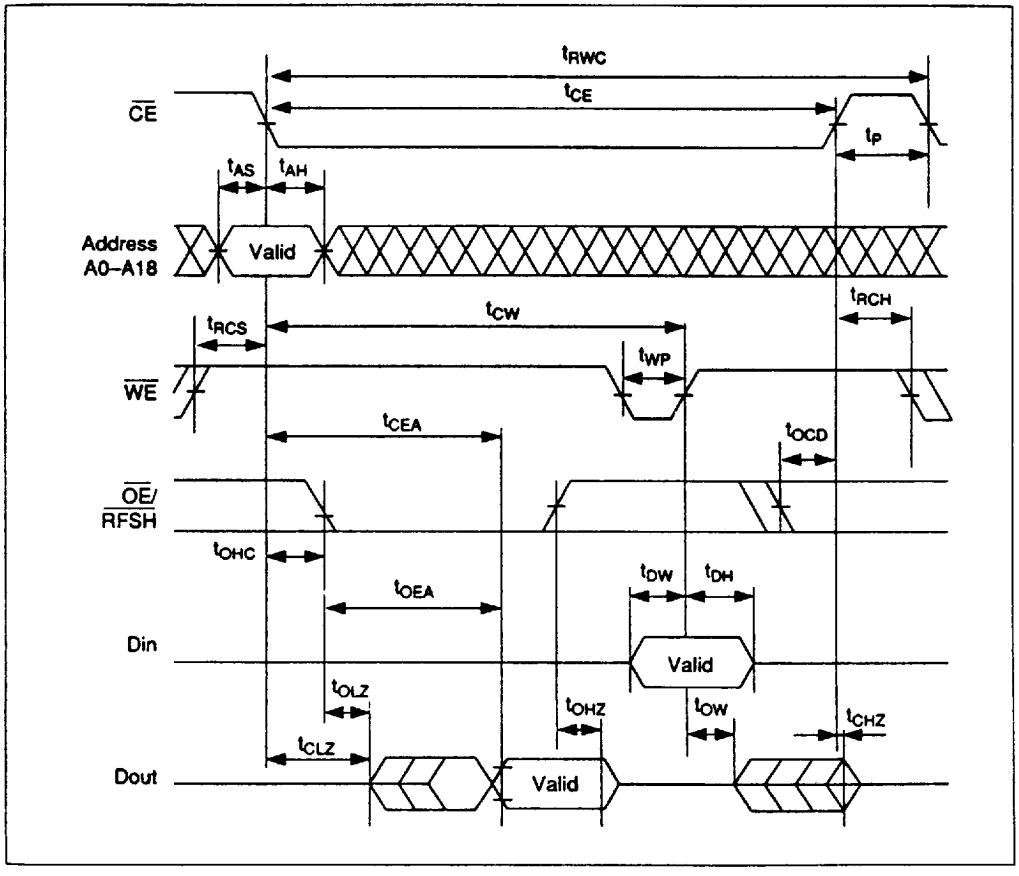
Automatic Refresh Cycle



Self Refresh Cycle



Read-Modify-Write Cycle



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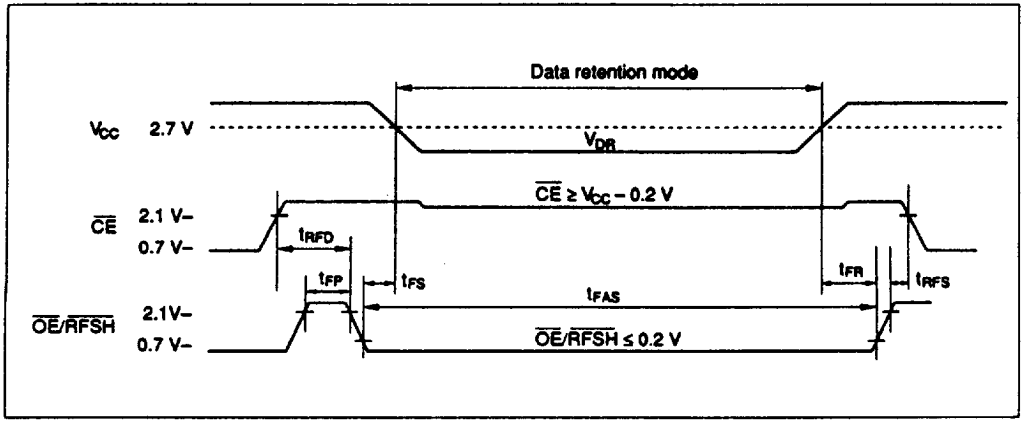
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	3.3	V	
Self refresh current	I_{CCDR}	—	—	25	µA	V_{CC} = 2.0 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
		—	—	40	µA	V_{CC} = 3.3 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
Refresh to data retention time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

Note: This characteristics is guaranteed only for LV-version.

Low V_{CC} Data Retention Timing Waveform



Notes: 1. t_R, t_F of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC} - 0.2$ V during data retention mode.
3. Regarding t_{RFS}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.