HD64400 GDP
Graphic Data Processor

Description

The HD64400 is a graphic data processing chip with high-speed drawing functions and an extensive set of display functions.

It can control a wide range of raster-scan CRT displays, ranging from low to high resolution, and can display up to four overlapping hardware windows.

Drawing commands include commands for drawing high-speed graphics, for text drawing on bit-mapped displays, for high-speed bit block transfers (BitBlt), and for enlarging, shrinking, and rotating images by arbitrary amounts.

Features

Display Functions

- Hardware windowing: up to four overlapping windows, one of which can be superimposed
- Multiport DRAM interface functions, supporting realtime read transfer
- Smooth scrolling, with independent vertical and horizontal direction
- Graphic cursor and cross-hair cursor
- Two memory access modes: single access and dual access
- Three scan modes: noninterlace, interlace sync, interlace sync & video
- External synchronization: master/slave, or TV sync
- Laser printer interface

Drawing Functions

- High-speed drawing. Speeds of representative commands at 4 bits/pixel are listed below (frame buffer data bus width—32 bits; clock rate—20 MHz):
  - — Line: 200 ns/pixel (any direction)
  - — Fill: 25 ns/pixel (single color)
  - — Text: 37.5 ns/pixel
  - — Copy (BitBlt): 75 ns/pixel (copy)
- Drawing versatility
  - — Thick lines can be drawn using arbitrary pel shapes (up to 32 × 32 pixels).
  - — Line style information can be stored on-chip RAM (up to 1024 bits).
  - — Areas can be tiled with arbitrary (binary or color) patterns. Patterns can be stored in on-chip RAM (for fast access) or the frame buffer (for large patterns), or in both locations.
  - — Raster operations: 20 arithmetic and logic operations; 20 enable/disable conditions.
  - — Hardware converts between binary and color data.
  - — Drawing area control: area detect, clipping, picking.
- High-level command language
  - — The command language conforms to VDI (CGI: ISO TC97/SC21 N1179, May 1986) and provides 11 line drawing commands, 7 fill commands, 5 text commands, 3 image commands, 17 interface commands, and 7 auxiliary commands.
  - — Characters can be rotated, enlarged, or modified for proportional spacing, kerning, italics, etc.
  - — Image commands include enlargement and shrinking with interpolation to preserve true shapes.

System Interface Functions

- The MPU can access the frame buffer directly.
- The bus interface supports both 68000/68020 and 80286/80386 MPUs.
- Large frame buffer address space (maximum 512 Mbytes).
- The GDP can draw graphics in system memory.
- Fifteen interrupt factors; interrupt vector output; on-chip bus-error handling.
- Color plane features: read/write masks, plane-to-plane copy

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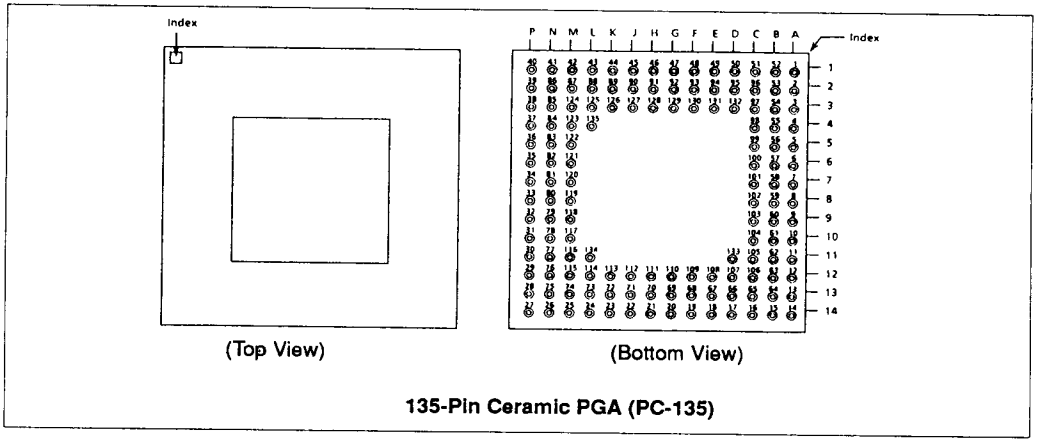
Pin Arrangement



135-Pin Ceramic PGA (PC-135)

Pin Configuration

Signal	Pin Code	Signal	Pin Code	Signal	Pin Code	Signal	Pin Code
D_0	D–2	$\overline{DREQ}$	G–1	MD_0	H–2	$\overline{AFBR}$	N–10
D_1	E–3	$\overline{DACK}$	H–1	MD_1	H–3	$\overline{HALT}$	P–11
D_2	B–1	$\overline{DONE}$	J–1	MD_2	J–2	$\overline{HALTA}$	N–11
D_3	A–1			MD_3	K–1	$\overline{SBREQ}$	M–11
D_4	C–2	MA_0	A–13	MD_4	K–2	$\overline{SBACK}$	P–12
D_5	B–2	MA_1	B–13	MD_5	L–1	$\overline{RETRY}$	N–12
D_6	A–2	MA_2	A–14	MD_6	L–2	$\overline{BERR}$	M–12
D_7	C–3	MA_3	D–12	MD_7	M–1		
D_8	B–3	MA_4	C–13	MD_8	N–1	CLKIN	B–9
D_9	A–3	MA_5	B–14	MD_9	M–2	SCLK	A–10
D_{10}	B–4	MA_6	D–13	MD_{10}	L–3	MCYC1	A–11
D_{11}	A–4	MA_7	C–14	MD_{11}	L–4	MCYC2	B–10
D_{12}	B–5	MA_8	F–12	MD_{12}	P–1		
D_{13}	A–5	MA_9	E–13	MD_{13}	N–2	$\overline{STB}$	A–9
D_{14}	C–6	MA_{10}	D–14	MD_{14}	P–2	FBS0	P–13
D_{15}	B–6	MA_{11}	F–13	MD_{15}	M–3	FBS1	N–13
		MA_{12}	E–14	MD_{16}	N–3	FBS2	P–14
$\overline{RES}$	A–8	MA_{13}	F–14	MD_{17}	P–3	FBS3	L–11
$\overline{CS}$	C–1	MA_{14}	G–13	MD_{18}	N–4		
RS1	E–2	MA_{15}	G–14	MD_{19}	P–4	$V_{CC}1$, $V_{CC}2$	F–3, C–4
$\overline{RS2}$	D–1	MA_{16}	H–14	MD_{20}	M–5	$V_{CC}3$, $V_{CC}4$	A–6, C–10
$\overline{R/W}$	F–2	MA_{17}	J–14	MD_{21}	N–5	$V_{CC}5$, $V_{CC}6$	E–12, J–12
$\overline{DTACK}$	F–1	MA_{18}	H–13	MD_{22}	P–5	$V_{CC}7$, $V_{CC}8$	L–12, P–10
$\overline{IRQ}$	E–1	MA_{19}	H–12	MD_{23}	M–6	$V_{CC}9$, $V_{CC}10$	M–7, K–3
$\overline{IACK}$	G–2	MA_{20}	J–13	MD_{24}	N–6	GND 1, GND 2	G–3, D–3
		MA_{21}	K–14	MD_{25}	P–6	GND 3, GND 4	C–5, A–7
$\overline{HSYNC}$/EXHSYNC	B–8	MA_{22}	K–13	MD_{26}	P–7	GND 5, GND 6	B–7, C–7
$\overline{VSYNC}$	B–11	MA_{23}	L–14	MD_{27}	N–7	GND 7, GND 8	C–9, C–11
$\overline{EXVSYNC}$/$\overline{ACT}$	C–8	MA_{24}	L–13	MD_{28}	P–8	GND 9, GND 10	D–11, G–12
$\overline{DISP1}$/EXDISP	C–12	MA_{25}	M–14	MD_{29}	N–8	GND 11, GND 12	K–12, M–10
$\overline{DISP2}$	B–12	MA_{26}	N–14	MD_{30}	P–9	GND 13, GND 14	M–9, M–8
$\overline{CUD}$	A–12	MA_{27}	M–13	MD_{31}	N–9	GND 15, GND 16	M–4, J–3

Pin Description

Type	Symbol	Pin Name	I/O	Function
Power	V_{CC}	Power Supply	—	+5 V power supply
	GND	Ground	—	Connected to system ground
Clock	CLKIN	Clock In	I	Max. 40 MHz clock input (50% duty ratio)
	SCLK	S Clock	O	Reference clock output
	MCYC1	Memory Cycle 1	O	Indicates frame buffer memory access timing
	MCYC2	Memory Cycle 2	O	90° phase delay with respect to MCYC1
MPU Bus Interface	$D_0 — D_{15}$	Data Bus	3-state I/O	Used for data transfer between the GDP and MPU
MPU Bus Control	$\overline{RES}$	Reset	I	External input that resets the GDP. (1) The entire internal state of the GDP is reset. Display and drawing operations both abort. (2) During $\overline{RES}$ input the GDP outputs DRAM refresh addresses at the MA pins specified in the refresh address output position (RAP) field. $\overline{HSYNC}$ remains low during this interval. (3) The following registers are affected by $\overline{RES}$ input.

Register	Effect of Reset
Address/Write FIFO Count Register (AWFCR)	WFC is reset to "100000," indicating write FIFO is empty.
Status Register (SR)	UDP, CED, WFR, and WFE are set to "1;" other bits are cleared to "0." SR value is H'8023.
FIFO	FIFO is entirely cleared. Commands, parameters, and data in write FIFO and data in read FIFO are all lost.
Command Control Registers (CCR0, CCR1)	SRES is set to "1;" all other bits are cleared to "0."
Interrupt Enable Register (IER)	All bits are cleared to "0."
Operation Mode Registers (OMR0, OMR1)	EXS is cleared to "00;" STR, LBP, and EXSP are cleared to "0." Other bits are not affected.
Display Control Registers (DCR0, DCR1)	DSPE is cleared to "0;" other bits are not affected.
Interrupt Vector Register (IVR)	Initialized to H'000F.

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
MPU Bus Control	$\overline{RES}$	Reset	I	(4) Registers other than those listed above are not affected by $\overline{RES}$ input.
	$\overline{CS}$	Chip Select	I	Used by the MPU and other system devices to select the GDP. The GDP's internal registers can be written and read only when $\overline{CS}$ is low.
	RS1, RS2	Register Select 1 & 2	I	Input signals that select internal registers in the GDP. Registers are accessed as indicated below.

RS2	RS1	R/$\overline{W}$	Register
L	L	L	Address register
L	L	H	Address/write FIFO counter register
L	H	L	Status register clear register
L	H	H	Status register
H	L	—	FIFO entry
H	H	—	Control registers

	R/$\overline{W}$	Read/Write	I	Indicates direction of data transfer between GDP and MPU. (1) Read: When R/$\overline{W}$ is high, GDP transfers data to MPU. (2) Write: When R/$\overline{W}$ is low, MPU transfers data to GDP.
	$\overline{DTACK}$	Data Transfer Acknowledge	3-state output	Indicates completion of data transfer. Used for data transfer control with HD68000 and other devices having an asynchronous bus interface.
	$\overline{IRQ}$	Interrupt Request	Open-drain output	Notifies MPU of command termination, undefined commands, etc.
	$\overline{IACK}$	Interrupt Acknowledge	I	Notifies GDP that current system bus cycle is an interrupt acknowledge cycle. When it receives this signal, the GDP sends its interrupt vector number to the MPU.
DMA Control	$\overline{DREQ}$	DMA Request	O	Requests a DMA controller to perform a DMA transfer of commands or data.
	$\overline{DACK}$	DMA Acknowledge	I	Reply from DMA controller to $\overline{DREQ}$
	$\overline{DONE}$	Done	Open-drain I/O	Indicates end of DMA transfer.

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
Display Control	$\overline{\text{HSYNC}}$ or $\overline{\text{EXHSYNC}}$	Horizontal Sync or External Horizontal Sync	I/O	Horizontal synchronization output signal (master or slave mode) Horizontal synchronization input signal (TV synchronization or laser printer mode)
	$\overline{\text{VSYNC}}$	Vertical Sync	O	Vertical synchronization signal
	$\overline{\text{EXVSYNC}}$ or $\overline{\text{ACT}}$	External Vertical Sync or Active	I/O	Vertical synchronization signal. When the GDP operates in master mode, $\overline{\text{EXVSYNC}}$ is an output pin. The shape of the $\overline{\text{EXVSYNC}}$ output depends on the scan mode as follows: (1) Non-interlace mode Same output waveform as $\overline{\text{VSYNC}}$. (2) Interlaced sync or interlaced sync and video mode Odd fields of $\overline{\text{VSYNC}}$, output separately. If the active (ACT) bit in command control register 0 (CCR0) is set to "1," this pin outputs a signal notifying external devices of the operating status of the drawing processor.
	$\overline{\text{DISP1}}$ or $\overline{\text{EXDISP}}$	Display Timing 1 or External Display Timing	I/O	In CRT display mode, an output signal indicating the display timing. In laser printer interface mode an input signal requesting display address output.
	$\overline{\text{DISP2}}$	Display Timing 2	O	Output during display of the superimpose window.
	$\overline{\text{CUD}}$	Cursor Display	O	Displays a cursor on the CRT.
Frame Buffer Control	MD_0 to MD_{31}	Frame Buffer Data Bus	3-state I/O	Data bus between GDP and frame buffer or system memory.
	MA_0 to MA_{27}	Frame Buffer Address Bus	3-state output	Address output for access from GDP to frame buffer.
Frame Buffer Bus Control	$\overline{\text{STB}}$	Strobe	O	Strobe for frame buffer address and status signals. Output even while the GDP is halted (while $\overline{\text{HALTA}}$ is asserted).

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Type	Symbol	Pin Name	I/O	Function
Frame Buffer Bus Control	FBS0 to FBS3	Frame Buffer Bus Status	3-state output	Output signals indicating frame buffer status in each cycle as follows:

FBS3	FBS2	FBS1	FBS0	Description
0	0	0	0	Not accessing frame buffer
0	0	0	1	Memory write with pixel address in write-only mode
0	0	1	0	Undefined
0	0	1	1	Executing ADOUT instruction
0	1	0	0	Drawing cycle: reading 16-bit word
0	1	0	1	Drawing cycle: writing 16-bit word
0	1	1	0	Drawing cycle: reading 32-bit longword
0	1	1	1	Drawing cycle: writing 32-bit longword
1	0	0	0	DRAM refresh address output
1	0	0	1	DRAM refresh output with common attribute output on MD pins
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Display address output for base window
1	1	0	1	Display address output for superimpose window
1	1	1	0	Undefined
1	1	1	1	Undefined

Bus Switching Control	$\overline{AFBR}$	Advanced Frame Buffer Request	O	Output signal notifying other devices of request for use of frame buffer bus.
	$\overline{HALT}$	Halt	I	Input signal that halts drawing and other operations by GDP.
	$\overline{HALTA}$	Halt Acknowledge	O	Output signal notifying bus requester that GDP has released frame buffer bus.
	$\overline{SBREQ}$	System Bus Request	O	Signal output by GDP to request use of bus for system memory access.
	$\overline{SBACK}$	System Bus Acknowledge	I	Input signal that notifies GDP when system bus is released.
	$\overline{RETRY}$	Retry	I	Input signal requesting repetition of drawing cycle when system memory access time is slower than GDP's memory cycle.
	$\overline{BERR}$	Bus Error	I	Input signal that notifies GDP of bus errors occurring during system memory access.

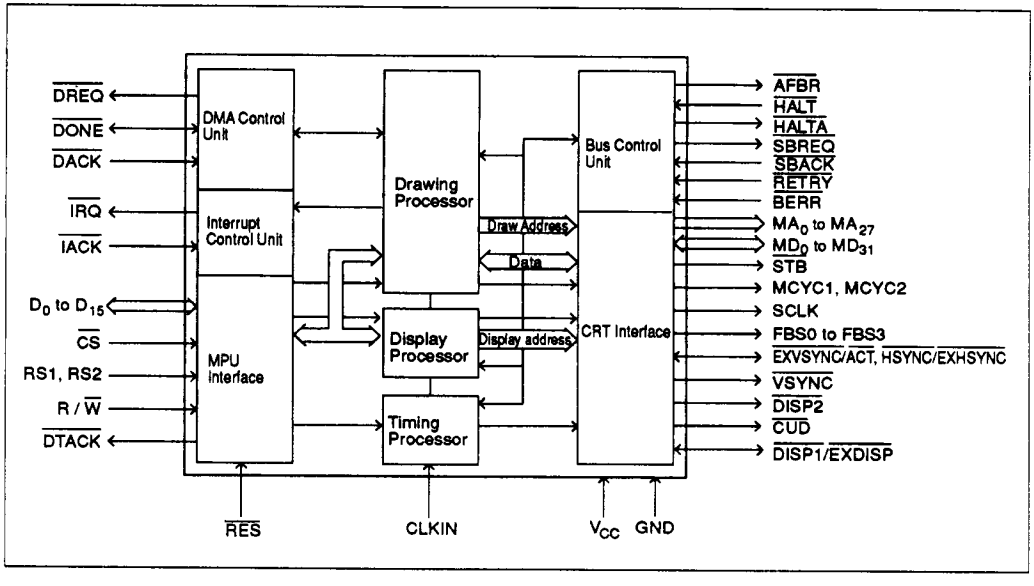
Functional Description

Item			Description	
Clock Frequency			20 MHz (max) or 16 MHz (max)	
Frame Buffer Space (full bit-mapped)			512 Mbytes (max)	
Display Functions	Hardware windows		Max. 4 overlapping windows (specified priorities), 1-window superimpose	
	Display control	Frame buffer access	Single access, dual access	
		Smooth scroll	Supported in any direction	
		Graphic cursor	Graphic or cross-hair cursor position signals	
		CRT scanning system	Non-interlace scan, interlace sync, interlace sync & video	
	Multiport DRAM interface		Realtime data transfer supported	
	DRAM refresh		10-bit address	
	External synchronization		Master-slave, TV sync	
	Laser printer interface		On-chip printer synchronization functions	
Drawing Functions	Command set	Line	11	Command set conform to GKS (GCI)
		Fill	7	
		Text	5	
		Image	3	
		Interface	17	
		Auxiliary	7	
	Drawing speed (Max.) (4 bits/pixel)	Line	200 ns/pixel (any direction)	
		Fill	25 ns/pixel (solid-color fill)	
		Text	37.5 ns/pixel	
		BitBit	75 ns/pixel (copy)	
	Coordinate systems		X-Y addresses (3 independent coordinate systems definable) and physical addresses	
	Color representation		Monochrome (binary) and color (1, 2, 4, 8, or 16 bits/pixel)	
Drawing Functions	Drawing modes	Mapping condition modes	8 modes (color→binary)	
		Color modes	4 modes (binary→color)	
		Operation modes	16 logic operations, +4 arithmetic operations	
		Color comparison modes	14 register comparisons, +6 transparent modes	
		Logical pel modes	2 modes, pel definable up to 32 × 32 pixels	
		Area modes	2 modes (graphic clipping, area detect)	
		Character area modes	3 modes (character clipping, area detect)	
		Pick mode	1 mode (picks graphics and text)	

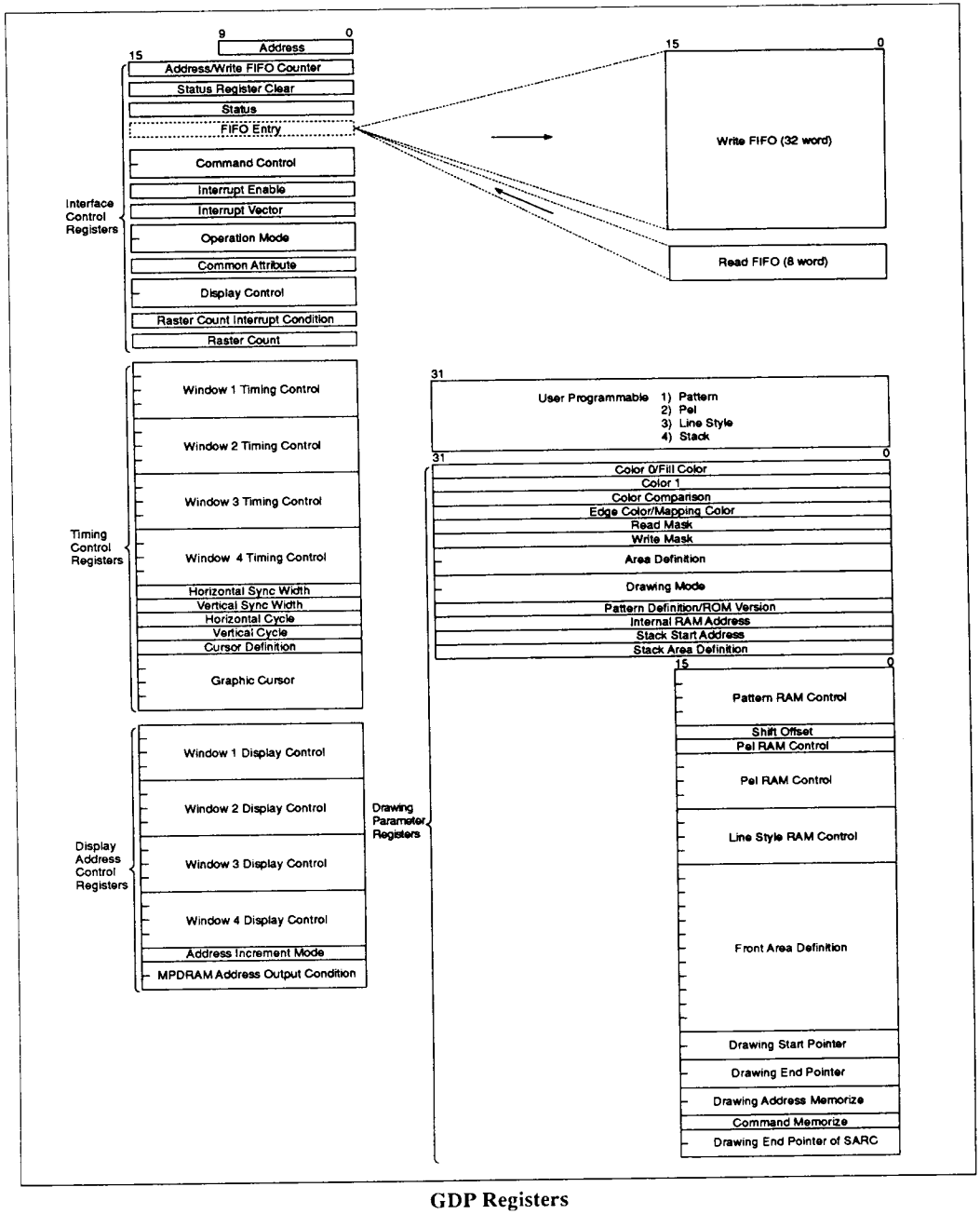
Functional Description (cont)

Item		Description
	Tiling	Tiling pattern can be stored in on-chip RAM or frame buffer
	Line style information	Up to 1024 bits specifiable in on-chip RAM
	Image operations	Enlargement and shrinking with any zoom ratio (with interpolation) rotation through any angle
	Character attribution	Proportional spacing, italic, enlargement, text path
System Interface	MPU interface (16-bit)	Supports H16/H32, 8086, and 68000 families
	MPU access to frame buffer	On-chip halt function
	GDP access to system memory	Font handling etc. (bus attribution functions)
	DMA transfer	PUT/GET commands
	Command transfer methods	3 methods (program I/O, DMA, batch transfer
	Interrupts	15 factors, generates interrupt vector
	Error handling	Saves address information and command code
	Color plane features	Read and write masks, plane-to-plane copy
Process		1.0μ CMOS
Supply Voltage		Single +5 V supply voltage
Package		135-pin PGA

Block Diagram



Registers



GDP Registers

Address Registers and Interface Control Registers

CS	RS2	RS1	R/W	No.	Name	Abbr.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	Setting LSP
1	–			–	–	–	–																	
0	0	0	0	AR	Address	AR							INC	ADDRESS								0	⊛	⊛
			1	AWFCR	Address/write FIFO counter	AWFCR	WFC						INC	ADDRESS									R	R
		1	0	SRCR	Status register clear	SRCR	UDCL	RCCL		WDCL	DECL	BECL	XECL	STCL	CECL	ARCL		FOCL					○	○
			1	SR	Status	SR	UDP	RCD		WDC	DER	BER	XER	STP	CER	ARD	CED	FOR	RFF	RFR	WFR	WFE	R	R
		0		FE	FIFO entry	FE	FE																⊛	⊛
				r002	Command control	CCR0	SRES	SHLT		ACT	IVM		GBM		WDM	WDRC			DDM	DDRC		DTSEL	⊛	⊛
				r004		CCR1								WTR		DTP		SMA	WTM		BSZ		⊛	⊛
				r006	Interrupt enable	IER	UDE	RCE		WDE	DEE	BEE	XEE	STE	CRE	ARE	CEE	FOE	RFE	RRE	WFE	WEE	○	○
				r008	Interrupt vector	IVR	IV																○	○
0	1	1	1/0	r00A	Operation mode	OMR0	STR	EXS		LBP	EXSP	ACP	CSK		DSK		RAM	MPM	ACM		RSM	VRP	○	○
				r00C		OMR1	RAP						RCYN		MATS	CATP	WATP						○	○
				r00E	Common attribute	CATRR	CATR																○	○
				r010	Display control	DCR0		PR4				PR3				PR2				PR1			○	×
				r012		DCR1	DSPE											SIE		SWD			○	×
				r014	Raster counter interrupt condition	RCCR			RCC														○	○
			1	r016	Raster count	RCR			RC														R	R
1	–			r018 to r0FE			Reserved																–	–

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)
2. Do not read or write registers r018 to r0FE. (These registers have undetermined values when read.)
3. Meaning of symbols:
⊛: Must always be set (although this does not mean the value is always necessary)
○: Must be set if the corresponding function is used.
×: The laser printer mode uses window 4, regardless of the setting.
R: Read-only

Timing Control Registers

CS	RS2	RS1	R/W	No.	Name		Abbr.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	Setting LSP
0	1	1	1/0	r100	Window 1	Horizontal display start 1	HDSR1												HDS1					○[1]	×
				r102		Horizontal display width 1	HDWR1												HDW1						
				r104		Vertical display start 1	VDSR1						VDS1												
				r106		Vertical display width 1	VDWR1						VDW1												
				r108	Window 2	Horizontal display start 2	HDSR2												HDS2					○[1]	×
				r10A		Horizontal display width 2	HDWR2												HDW2						
				r10C		Vertical display start 2	VDSR2						VDS2												
				r10E		Vertical display width 2	VDWR2						VDW2												
				r110	Window 3	Horizontal display start 3	HDSR3												HDS3					○[1]	×
				r112		Horizontal display width 3	HDWR3												HDW3						
				r114		Vertical display start 3	VDSR3						VDS3												
				r116		Vertical display width 3	VDWR3						VDW3												
				r118	Window 4	Horizontal display start 4	HDSR4												HDS4					○[1]	×
				r11A		Horizontal display width 4	HDWR4												HDW4						
				r11C		Vertical display start 4	VDSR4						VDS4												
				r11E		Vertical display width 4	VDWR4						VDW4												
1	–			r120 to r13E				Reserved																–	–
0	1	1	1/0	r140	Horizontal sync width		HSWR													HSW				⊛	×
				r142	Vertical sync width		VSWR													VSW					
				r144	Horizontal cycle		HCR													HC					○[2]
				r146	Vertical cycle		VCR													VC					
				r148	Cursor definition		CDR	CM	CCM				CDA						CON				COFF		×
				r14A	Graphic cursor		GCR													CXS				▲[1]	
				r14C																CXE					
				r14E																CYS					
				r150																CYE					
1	–			r152 to r17E				Reserved																–	–

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)
2. Do not read or write registers r120 to r13E or r152 to r17E. (These registers have undetermined values when read.)
3. Meaning of symbols:
⊛: Must always be set
×: Need not be set
▲[1]: Must be set if the cursor is used
○[1]: Need not be set for undisplayed windows (If there is no display, no settings are required.)
○[2]: Need not be set if static memory is used

Display Address Control Registers

CS	RS2	RS1	R/W	No.	Name		Abbr.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	Setting LBP
0	1	1	1/0	r180	Window 1	Window attribute control signal 1	WATRR1									WATR1								○[1]	×
				r182		Memory width 1	MWR1									MW1									
				r184		Start address 1	SAR1									SAH1									
				r186												SAL1									
				r188	Window 2	Window attribute control signal 2	WATRR2									WATR2								○[1]	×
				r18A		Memory width 2	MWR2									MW2									
				r18C		Start address 2	SAR2									SAH2									
				r18E												SAL2									
				r190	Window 3	Window attribute control signal 3	WATRR3									WATR3								○[1]	×
				r192		Memory width 3	MWR3									MW3									
				r194		Start address 3	SAR3									SAH3									
				r196												SAL3									
				r198	Window 4	Window attribute control signal 4	WATRR4									WATR4								○[1]	⊛
				r19A		Memory width 4	MWR4									MW4									
				r19C		Start address 4	SAR4									SAH4									
				r19E												SAL4									
1	–			r1A0 to r1BE	Reserved																			-	-
0	1	1	1/0	r1C0	Address increment mode		ADIR									SDA							DAI	⊛	⊛
				r1C2	MPDRAM display address output condition	Base window display address output condition	BDCR									BDC								▲[2]	×
				r1C4		Superimpose window display address output condition	SDCR									SDC								▲[3]	
1	–			r1C6 to r1FE	Reserved																			-	-

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write registers r1A0 to r1BE or r1C6 to r1FE. (These registers have undetermined values when read.)

3. Meaning of symbols:
   - ⊛ : Must always be set
   - × : Need not be set
   - ○[1]: Need not be set for undisplayed windows (If there is no display, no settings are required.)
   - ▲[2]: Must be set if multiport memory is used
   - ▲[3]: Must be set if multiport memory and superimpose window are used

Drawing Parameter Control Registers (1)

Register No.	Read/Write	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	R, W	Color 0/fill color	CLOR/FCLR	CL0H/FCLH															
01				CL0L/FCLL															
02	R, W	Color 1	CL1R	CL1H															
03				CL1L															
04	R, W	Color comparison	CCMPR	CCMPH															
05				CCMPL															
06	R, W	Edge color/mapping color	EDGR/MAPCLR	EDGH/MAPCLH															
07				EDGL/MAPCLL															
08	R, W	Read mask	RMASKR	RMASKH															
09				RMASKL															
0A	R, W	Write mask	WMASKR	WMASKH															
0B				WMASKL															
0C	R, W	Area definition	ADR	XMIN															
0D				YMIN															
0E				XMAX															
0F				YMAX															
10	R, W	Drawing mode	DMR	PICK		AREA		CAM							PEL			COL	
11				MAP			CCMPM									OPM			
12				DM	DMW														
13				SM	SMW														
14	R, W	Pattern definition	PDR	PM	PMW														
15	R	ROM version	RVR	RV															
16	R, W	Internal RAM address	IRAR	IRAH															
17				IRAL															
18	R, W	Stack: Start address	SSAR	SSAH															
19				SSAL															
1A		Stack: Area definition	SADR	SADH															
1B				SADL															
1C to 21	Reserved																		

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not write to register No. 15 (which is a read-only register). Do not read or write register Nos. 1C to 21. (These registers have undetermined values when read.)

Drawing Parameter Control Registers (2)

Register No.	Read/Write	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22	R, W	Pattern RAM control	PRCR	PSX															
23				PSY															
24				PEX															
25				PEY															
26	Reserved																		
27																			
28	R, W	Shift offset	SOFSR													SOFS			
29	Reserved																		
2A	R, W	Pel RAM address	PLAR						PLA									(PLD)	
2B	Reserved																		
2C	R, W	Pel RAM control	PLCR															PLX1	
2D																		PLX2	
2E																		PLY1	
2F																		PLY2	
30	R, W	Line style RAM control	LSCR													LSP			
31																LSS			
32																LSE			
33									LSZC									LSZ	
34	R, W	Font area definition	FADR	FSAH															
35				FSAL															
36																		FBNH	
37				FBNL															
38					FAMW														
39				IOFS															
3A																FSX			
3B																FSY			
3C				DX															
3D				DY															
3E																CSX			
3F																CSY			

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write register Nos. 26, 27, 29, and 2B. (These registers have undetermined values when read.)

Drawing Parameter Control Registers (3)

Register No.	Read/Write	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40 to 47	Reserved																		
48	R	Drawing start pointer	DSPR	DSPX															
49				DSPY															
4A	R	Drawing end pointer	DEPR	DEPX															
4B				DEPY															
4C	R	Drawing address memorize	DRADR	DRADH															
4D				DRADL															R/W
4E	R	Command memorize	CMDR	CMD															
4F to 51	Reserved																		
52	R	Drawing end pointer of SARC	DEPSR	DEPSX															
53				DEPSY															
54 to 57	Reserved																		
58 to FF	Undefined																		

Notes: 1. Shaded bits have undetermined values when read.

2. Do not write to register Nos. 48 to 4E or 52 to 53.

3. Do not read or write register Nos. 40 to 47, 4F to 51, or 54 to FF. (These registers have undetermined values when read.)

4. An execution error occurs if register Nos. 40 to FF are written or register Nos. 58 to FF are read.

Commands (1)

	Mnemonic	Command	Operation Code	Parameters	Words
Line	LINE	Line	1000 0000 0000 000B	Xs, Ys, Xe, Ye	5
	RCT	Rectangle	1000 0010 0000 000B	X_1, Y_1, X_2, Y_2	5
	PLL	Polyline	1000 1000 0000 000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	DPLL	Disjoint Polyline	1000 1010 0000 000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	SPLL	Short Polyline	1001 0010 0000 000B	n, X, Y, {(dX_1, dY_1), ... (dXn, DYn)}	①
	PLG	Polygon	1001 0000 0000 000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	CRCL	Circle	1010 1000 0000 000B	Xc, Yc, A, B	5
	ARC	Arc	1010 1010 0000 000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	ARCC	Arc Close	1011 100CT 0000 000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	SARC	Single-stroke Arc	1011 101C 0000 000B	Xc, Yc, a, b, Xs, Ys, DXe, DYe	9
	DOT	Dot	1001 1000 0000 000B	X, Y	3
Fill	FRCT	Filled Rectangle	1000 0110 P000 000B	X_1, Y_1, X_2, Y_2	5
	FCRCL	Filled Circle	1010 1100 P000 000B	Xc, Yc, A, B	5
	FFAN	Filled Fan	1011 110CT P000 000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	PAINT	Paint	1001 110E P000 000B	Xs, Ys	3
	SEARCH	Search	1000 111IE 0000 000B	Xs, Ys	3
	FTRAP	Filled Trapezoid	1001 0100 PS00 000B	X_1, Y_1, X_2, Y_2, X_3, Y_3, X_4, Y_4, Ys, Ye	11
	FHLINE	Filled Horizontal Line	1000 0100 P000 000B	Y, n, X_1 ... Xn	3+n

Notes: ①: DIR: Search right if DIR = 0, left if DIR = 1
②: $4 + (n/2)\uparrow$
Words: Number of words in command and parameters
B: Breakpoint bit
CT: Sector if CT = 0, segment if CT = 1
P: Tiling pattern if P = 0, solid color fill if P = 1
E: If E = 0, boundary color is color in edge color register
If E = 1, boundary color is color other than color in edge color register
C: Counterclockwise if C = 0, clockwise if C = 1
S: Fill sides if S = 0, do not fill sides if S = 1

Commands (2)

	Mnemonic	Command	Operation Code	Parameters	Words
Text	TEXT	Text	0111 0SD0 0000 000B	X, Y, n, CN_1 ... CNn	4+n
	ATEXT	Append Text	0111 1SD0 0000 000B	n, CN_1 ... CNn	2+n
	TEXTSP	Text with Space	0110 1SD0 0000 000B	X, Y, n, CN_1, DX_1, DY_1 ... CNn, DXn, DYn	4+3n
	ATEXTSP	Append Text with Space	1101 1SD0 0000 000B	n, CN_1, DX_1, DY_1 ... CNn, DXn, DYn	2+3n
	CHR	Character	0110 0SD0 0000 000B	CN	2
Image	COPY	Copy	111③ DSD0 0000 000B	Xs, Ys, DX, DY, Xd, Yd	7
	ZOOM	Zoom	1101 0010 0000 000B	Xs, Ys, LSX, LSY, Xd, Yd, LDX, LDY	9
	ROT	Rotation	1101 0100 0000 000B	Xs, Ys, LSX, LSY, Xd, Yd, LDXx, LDXy, LDYx, LDYy	11
Inter-face	PUT	Put	0101 110M 0000 000B	X, Y, DX, DY, D_1 ... Dn	5+α
	GET	Get	0101 111M 0000 000B	X, Y, DX, DY	5
	ORGD	Origin of Drawing	0000 0110 0000 000B	AH, AL, X, Y	5
	ORGS	Origin of Source	0000 1000 0000 000B	AH, AL, X, Y	5
	ORGP	Origin of Pattern	0000 1010 0000 000B	AH, AL, X, Y	5
	LDPR	Load Parameter Register	0001 1100 0000 000B	RN, AH, AL, n	5
	STPR	Store Parameter Register	0001 1110 0000 000B	RN, AH, AL, n	5
	WPR	Write Parameter Register	0001 0110 0000 000B	RN, D_1 ... Dn, n	3+n
	RPR	Read Parameter Register	0001 1010 0000 000B	RN, n	3

Notes: ③: SSD: Horizontal if SSD = 0; vertical if SSD = 1
Words: Number of words in command and parameters
B: Breakpoint bit
SD: Left-to-right if SD = 00, up if SD = 01 (rotated 90°), right-to-left if SD = 10 (rotated 180°), down if SD = 11 (rotated 270°)
DSD: Right-up if DSD = 000, right-down if DSD = 001, left-up if DSD = 010, left-down if DSD = 011, up-right if DSD = 100, down-right if DSD = 101, up-left if DSD = 110, down-left if DSD = 111
M: Normal transfer if M = 0, convert if M = 1 (PUT—convert binary to color; GET—convert color to binary)
I: No interpolation if I = 0, interpolate if I = 1

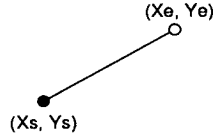
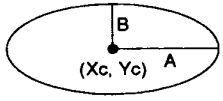
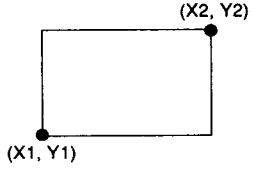
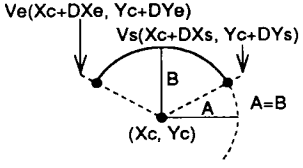
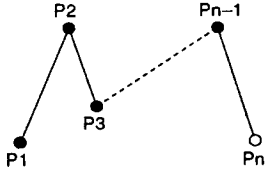
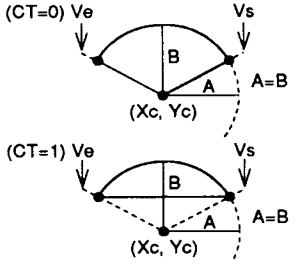
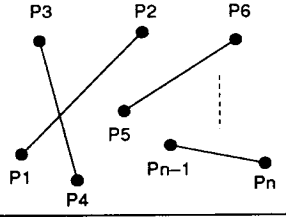
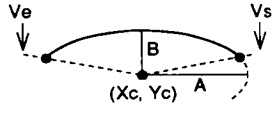
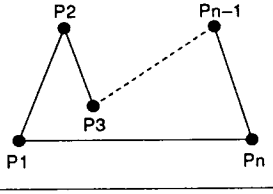
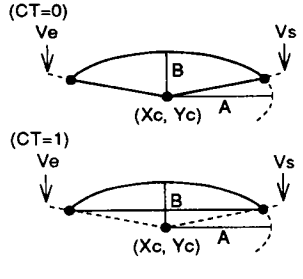
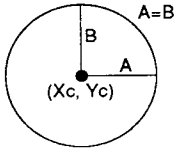
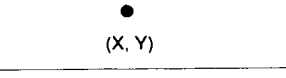
Commands (3)

	Mnemonic	Command	Operation Code				Parameters	Words
Interface	BWT	Block Write	0101	0000	0000	000B	AH, AL, n, $D_1 \cdots D_{2n}$	4+2n
	BRD	Block Read	0101	0010	0000	000B	AH, AL, n	4
	BCOPY	Block Copy	0101	01ID0	0000	000B	ASH, ASL, ADH, ADL, n	6
	DISPON	Display On	0001	0000	0000	000B		1
	DISPOFF	Display Off	0001	0010	0000	000B		1
	NOP	No Operation	0000	0010	0000	000B		1
	ADOUT	Address/Data Out	0000	1100	0000	000B	AH, AL, DH, DL	5
	WDEND	Write DMA End	0000	0100	0000	000B		1
Auxiliary	TERM	Terminator	1001	1010	0000	000B		1
	CLINE	Current Line	1001	0110	0000	000B	Xe, Ye	3
	CHRBGN	Character Begin	0100	1000	0000	000B	X, Y	3
	CHRSPC	Character Space	0100	1010	0000	000B	dX, dY	3
	NOP3	No Operation 3	0000	0000	0000	000B	H'0, H'0	3
	BATCH	Batch	0100	0000	0000	0000	AH, AL	3
	BTEND	Batch End	0100	0010	0000	0000		1

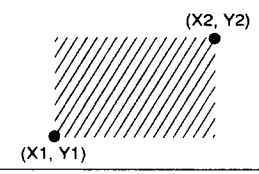
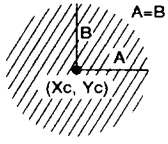
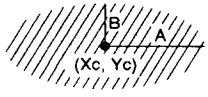
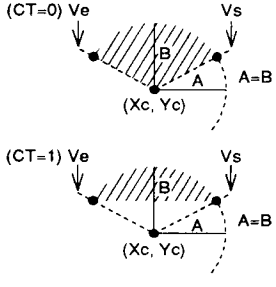
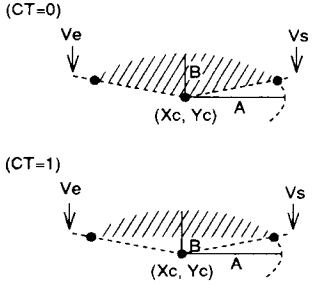
Notes: Words: Number of words in command and parameters
B: Breakpoint bit
ID: Increment if ID = 0, decrement if ID = 1

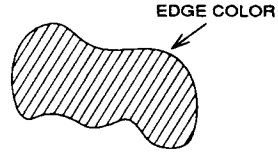
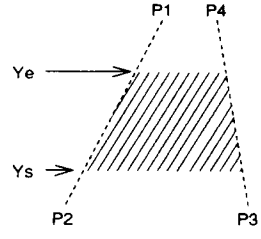
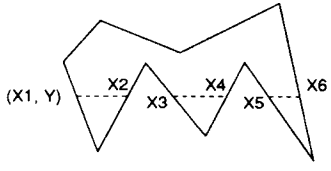
Examples of Principal Drawing Commands

1. Line Drawing Commands

Command	Example	Command	Example
LINE (draw line)		CRCL (draw ellipse)	
RCT (draw rectangle)		ARC (draw circular arc)	
PLL (draw polyline) SPLL (draw polyline with short segments)		ARCC (draw circular sector or segment)	
DPLL (draw disjoint polyline)		ARC (draw elliptical arc)	
PLG (draw polygon)		ARCC (draw elliptical sector or segment)	
CRCL (draw circle)		DOT (draw one dot)	

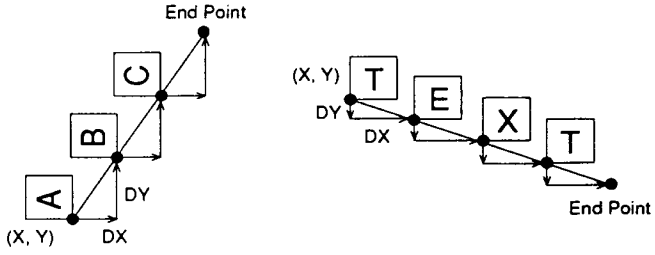
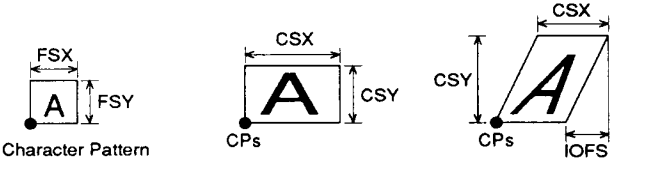
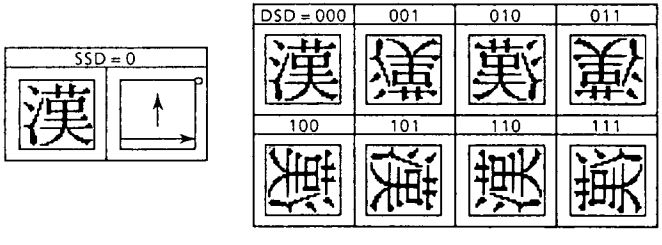
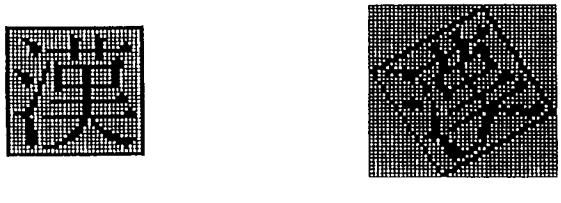
2. Filling Commands

Command	Example
FRCT (draw filled rectangle)	
FCRCL (draw filled circle)	
FCRCL (draw filled ellipse)	
FFAN (draw filled circular sector or segment)	
FFAN (draw filled elliptical sector or segment)	

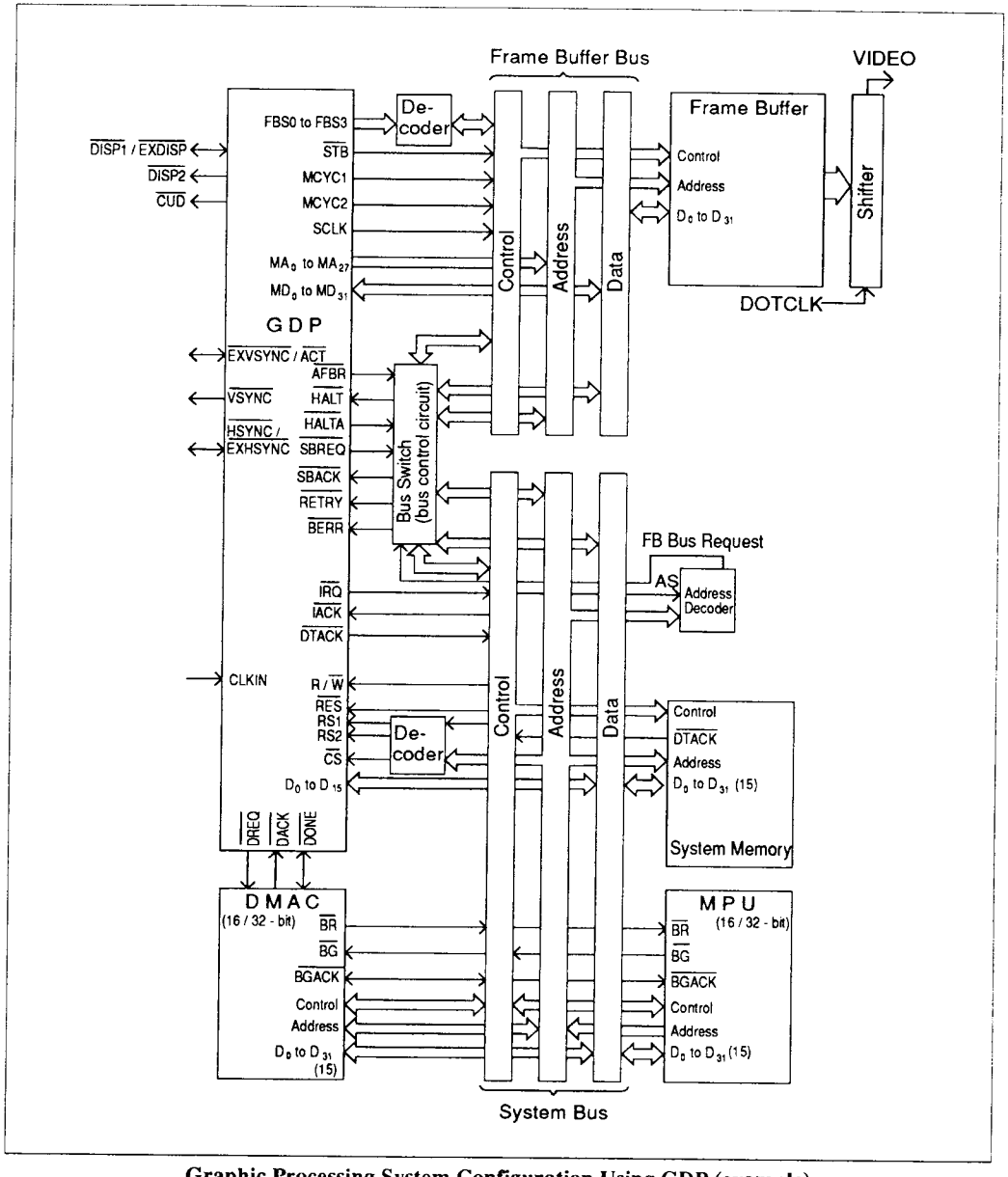
Command	Example
PAINT (fill arbitrary area)	
FTRAP (draw filled trapezoid)	
FHLINE (fill horizontal line segments)	

Pattern (example)

3. Character or Image Drawing Commands

Command	Example
TEXT /ATEXT (draw character string)	
CHR (draw character)	
COPY (copy image data)	
ZOOM (copy with enlargement or shrinking)	
ROT (copy with rotation)	

System Overview



Graphic Processing System Configuration Using GDP (example)

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to +7.0	V
Input Voltage	V_{in}*	−0.3 to V_{CC} +0.3	V
Allowable Output Current	$\|I_O\|$**	5	mA
Total Allowable Output Current	$\|\Sigma I_O\|$**	240	mA
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Based on GND = 0V

** Allowable output current refers to the maximum current that may be sourced or sinked at a single output pin or input/output pin.

*** Total allowable output current refers to the sum of all currents sourced or sinked at all output and input/output pins.

Note: Permanent damage to the GDP chip can result if it is used outside its absolute maximum ratings. The chip should preferably be used in the recommended operating conditions given next. Use in conditions outside the recommended conditions may adversely affect the reliability of the chip.

Recommended Operating Conditions

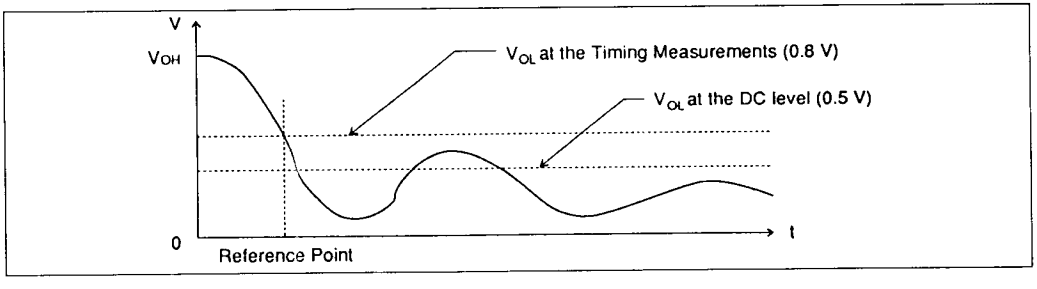
1. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}*	0	—	0.7	V
Input High Voltage	V_{IH}*	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

* Based on GND = 0V

2. Timing Measurements

The output low voltage for timing measurements is 0.8 V. The normal output low voltage remains 0.5 V as listed in the DC characteristics. The high voltage level for timing measurements is V_{CC} − 2.0 V.
(For $\overline{\text{DTACK}}$ measurements the high level is 2.4 V.)



V_{OL} for Timing Measurement

DC Characteristics at V_{CC} = 5.0 V ±5%, GND = 0 V, Ta = 0 to +70°C

Item	Pins	Symbol	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit	Conditions
Input High Voltage	○, △, □	V_{IH}	2.2	V_{CC}	2.2	V_{CC}	V	
Input Low Voltage		V_{IL}	–0.3	0.7	–0.3	0.7		
Input Leakage Current	○	I_{in}	–2.5	2.5	–2.5	2.5	µA	V_{in} = 0 to V_{CC}
Three-State Input Current (Off-State)	△	I_{TSI}	–10	10	–10	10		V_{in} = 0.4 to V_{CC}
Output High Voltage	△, ◇	V_{OH}	V_{CC} –1.0	—	V_{CC} –1.0	—	V	I_{OH} = –400µA
	◎		2.4	—	2.4	—		
Output Low Voltage	△, ◇, ◎	V_{OL}	—	0.5	—	0.5		I_{OL} = 2.2mA
	□, ☆		—	0.5	—	0.5		I_{OL} = 2.5mA
Output Leakage Current (Off-State)		I_{LOD}	—	10	—	10	µA	V_{OH} = V_{CC}
Input Capacitance	△	C_{in}	—	20	—	20	pF	V_{in} = 0V
	○		—	20	—	20		Ta = 25°C
Output Capacitance	□, ☆	C_{out}	—	18	—	18		f = 1.0MHz
Current Dissipation		I_{CC}	—	480	—	380	mA	• Chip not selected • Display on
			—	480	—	380		• During data bus read/write • Display on • During command execution

Notes: ○: Input — $\overline{RES}$, $\overline{CS}$, RS1, RS2, R/$\overline{W}$, $\overline{IACK}$, $\overline{DACK}$, $\overline{HALT}$, $\overline{SBACK}$, $\overline{RETRY}$, $\overline{BERR}$, CLKIN

△: Input/output (including 3-state) — D_0 to D_{15}, $\overline{HSYNC}$/$\overline{EXHSYNC}$, $\overline{EXVSYNC}$/$\overline{ACT}$, $\overline{DISP1}$/$\overline{EXDISP}$, MD_0 to MD_{31}

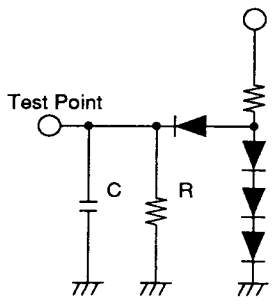
□: Open-drain input/output — $\overline{DONE}$

◇: Output (including 3-state) — $\overline{DREQ}$, $\overline{VSYNC}$, $\overline{DISP2}$, $\overline{CUD}$, MA_0 to MA_{27}, $\overline{STB}$, FBS_0 to FBS_3, $\overline{AFBR}$, $\overline{HALTA}$, $\overline{SBREQ}$, SCLK, MCYC1, MCYC2

◎: Output (3-state) — $\overline{DTACK}$

☆: Open-drain output — $\overline{IRQ}$

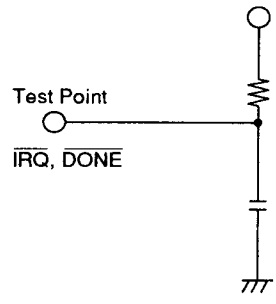
Test Load Circuit A



RL=1.8k Ω
C=40pF
R=10k Ω
All diodes are 1S2074 Ⓗ or equivalent.

Signal
D_0-D_{15}, $\overline{HSYNC}$/$\overline{EXHSYNC}$, $\overline{EXVSYNC}$/$\overline{ACT}$, $\overline{DISP1}$/$\overline{EXDISP}$, MD_0-MD_{31}, $\overline{DTACK}$, $\overline{DREQ}$, $\overline{VSYNC}$, $\overline{DISP2}$, $\overline{CUD}$, MA_0-MA_{27}, $\overline{STB}$, FBS0-FBS3, $\overline{AFBR}$, $\overline{HALTA}$, $\overline{SBREQ}$, SCLK, MCYC1, MCYC2

Test Load Circuit B



RL=1.8k Ω
C=40pF

AC Characteristics at V_{CC} = 5.0 V ± 5%, GND = 0 V, Ta = 0 to +70°C

Clock and Reset Input

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
	Input Clock Frequency	f		4	40	4	32	MHz
1	Clock Cycle Time	t_{cyc}		25	250	32	250	ns
2	Clock "High" Level Pulse Width	t_{PWCH}		8	125	10	125	ns
3	Clock "Low" Level Pulse Width	t_{PWCL}	Fig. 1	8	125	10	125	ns
4	Clock Rise Time	t_{Cr}		–	8	–	8	ns
5	Clock Fall Time	t_{Cf}		–	8	–	8	ns
6	$\overline{RES}$ Input Pulse Width	t_{RESW}		20	–	20	–	t_{cyc}
7	$\overline{RES}$ Hold Time	t_{RESH}	Fig. 2	8	–	12	–	ns
8	$\overline{RES}$ Setup Time	t_{RESS}		4	–	8	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

MPU Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
20	R/$\overline{W}$ Setup Time	t_{RWS}		0	–	0	–	ns
21	R/$\overline{W}$ Hold Time	t_{RWH}		0	–	0	–	ns
22	RS1, RS2 Setup Time	t_{RSS}		0	–	0	–	ns
23	RS1, RS2 Hold Time	t_{RSH}		0	–	0	–	ns
24	$\overline{CS}$ Setup Time	t_{CSS}		30	–	40	–	ns
25	$\overline{CS}$ "High" Level Width	t_{WCSH}		50	–	60	–	ns
26	Data Bus 3 state Recovery Time 1	t_{DBRT1}		0	–	0	–	ns
27	Read Data Access Time	t_{RDAC}		–	45	–	55	ns
28	Read Data Hold Time	t_{RDH}		5	–	5	–	ns
29	Read Data Turn Off Time	t_{RDZ}	Fig. 3	–	45	–	55	ns
30	$\overline{DTACK}$ Delay Time (Z to L)	t_{DTKZL}		–	45	–	55	ns
31	$\overline{DTACK}$ Delay Time (D to L)	t_{DTKDL}	Fig. 4	0	–	0	–	ns
32	$\overline{DTACK}$ Release Time (L to H)	t_{DTKLH}		–	45	–	55	ns
33	$\overline{CS}$ High to $\overline{DTACK}$ High Impedance	t_{CDTKZ}		–	50	–	60	ns
34	MPU Wait Time	t_{MWAT}		0	–	0	–	ns
35	Write Data Setup Time	t_{WDS}		0	–	0	–	ns
36	Write Data Hold Time	t_{WDH}		0	–	0	–	ns
38	$\overline{DACK}$, $\overline{IACK}$ Setup Time to $\overline{CS}$	t_{DICSS}		50	–	60	–	ns
39	$\overline{DACK}$, $\overline{IACK}$ Hold Time to $\overline{CS}$	t_{DICSH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

DMA Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
41	$\overline{\text{DREQ}}$ Delay Time 1	t_{DRQD1}		–	60	–	70	ns
42	$\overline{\text{DREQ}}$ Delay Time 2	t_{DRQD2}		–	60	–	70	ns
46	$\overline{\text{DACK}}$ Setup Time	t_{DAKS}		30	–	40	–	ns
47	$\overline{\text{DACK}}$ "High" Level Width	t_{WDAKH}		50	–	60	–	ns
48	Data Bus 3 state Recovery Time 2	t_{DBRT2}		0	–	0	–	ns
49	DMA Read Data Access Time	t_{DRDAC}		–	45	–	55	ns
50	DMA Read Data Hold Time	t_{DRDH}		5	–	5	–	ns
51	DMA Read Data Turn Off Time	t_{DRDZ}		–	45	–	55	ns
52	DMA $\overline{\text{DTACK}}$ Delay Time (Z to L)	t_{DDTZL}		–	45	–	55	ns
53	DMA $\overline{\text{DTACK}}$ Delay Time (D to L)	t_{DDTDL}	Fig. 5	0	–	0	–	ns
54	DMA $\overline{\text{DTACK}}$ Release Time (L to H)	t_{DDTLH}		–	45	–	55	ns
55	$\overline{\text{DACK}}$ High to $\overline{\text{DTACK}}$ High Impedance	t_{DDTKZ}	Fig. 6	–	50	–	60	ns
56	DMA Wait Time	t_{DWAT}		0	–	0	–	ns
58	$\overline{\text{DONE}}$ Output Delay Time	t_{DND}		–	60	–	70	ns
59	$\overline{\text{DONE}}$ Output Turn Off Time (L to Z)	t_{DNLZ}		–	70	–	80	ns
60	$\overline{\text{DONE}}$ Input Pulse Width	t_{WDNL}		4	–	4	–	t_{cyc}
61	DMA Write Data Setup Time 1	t_{DWDS1}		30	–	40	–	ns
62	DMA Write Data Hold Time 1	t_{DWDH1}		0	–	0	–	ns
65	DMA Write Data Setup Time 2	t_{DWDS2}		0	–	0	–	ns
66	DMA Write Data Hold Time 2	t_{DWDH2}		0	–	0	–	ns
67	$\overline{\text{CS}}$, $\overline{\text{IACK}}$, Setup Time to $\overline{\text{DACK}}$	t_{CIDKS}		50	–	60	–	ns
68	$\overline{\text{CS}}$, $\overline{\text{IACK}}$, Hold Time to $\overline{\text{DACK}}$	t_{CIDKH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Frame Buffer Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
70	SCLK Delay Time 1 (L to H)	t_{SCKD1}		–	25	–	27	ns
71	SCLK Delay Time 2 (H to L)	t_{SCKD2}		–	23	–	27	ns
72	MCYC1, MCYC2 Delay Time from SCLK	t_{MYSD}		0	10	0	15	ns
73	MCYC Phase Difference	t_{MPHS}		40	60	45	80	ns
74	Memory Address Turn On Time	t_{MAZA}		0	–	0	–	ns
75	Memory Address Delay Time	t_{MAD}		0	25	0	25	ns
76	Memory Address Hold Time	t_{MAH}		0	–	0	–	ns
77	Memory Address Turn Off Time	t_{MAAZ}		0	25	0	30	ns
78	FBS Turn On Time	t_{FBSZF}		0	–	0	–	ns
79	FBS Delay Time	t_{FBSD}	Fig. 7	0	20	0	23	ns
80	FBS Hold Time	t_{FBSH}		0	–	0	–	ns
81	FBS Turn Off Time	t_{FBSFZ}	Fig. 8	0	25	0	30	ns
82	MA, FBS, Setup Time 1	t_{MAFBS1}		0	–	0	–	ns
83	$\overline{STB}$ Delay Time	t_{STBD}	Fig. 9	0	19	0	19	ns
84	MA, FBS Hold Time 2	t_{MAFBS2}		0	–	0	–	ns
85	Memory Read Data Setup Time	t_{MRDS}		30	–	30	–	ns
86	Memory Read Data Hold Time	t_{MRDH}		0	–	0	–	ns
87	Memory Write Data Turn On Time	t_{MWDZD}		0	–	0	–	ns
88	Memory Write Data Delay Time	t_{MWDD}		–	25	–	30	ns
89	Memory Write Data Setup Time	t_{MWDS}		0	–	0	–	ns
90	Memory Write Data Hold Time	t_{MWDH}		5	–	5	–	ns
91	Memory Write Data Turn Off Time	t_{MWDDZ}		–	25	–	30	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

System Interface

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
100	$\overline{\text{HALT}}$ Setup Time	t_{HLTS}		25	–	35	–	ns
101	$\overline{\text{HALT}}$ Hold Time	t_{HLTH}		0	–	0	–	ns
102	$\overline{\text{HALTA}}$ Delay Time	t_{HLTD}		0	25	0	30	ns
104	$\overline{\text{AFBR}}$ Delay Time	t_{AFD}		0	20	0	20	ns
105	$\overline{\text{SBREQ}}$ Delay Time	t_{SBRD}	Fig. 10	0	20	0	30	ns
106	$\overline{\text{SBACK}}$ Setup Time	t_{SBKS}		25	–	35	–	ns
107	$\overline{\text{SBACK}}$ Hold Time	t_{SBKH}		0	–	0	–	ns
108	$\overline{\text{RETRY}}$ Setup Time	t_{RTYS}		25	–	35	–	ns
109	$\overline{\text{RETRY}}$ Hold Time	t_{RTYH}		0	–	0	–	ns
110	$\overline{\text{BERR}}$ Setup Time	t_{BERS}		25	–	35	–	ns
111	$\overline{\text{BERR}}$ Hold Time	t_{BERH}		0	–	0	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Display Control Signals and External Synchronization

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
119	MCYC1, MCYC2 Delay Time from CLKIN	t_{MYCKD}		–	33	–	40	ns
120	$\overline{\text{HSYNC}}$ Output Delay Time from CLKIN	t_{HSDCK}		–	45	–	60	ns
121	$\overline{\text{VSYNC}}$ Delay Time from CLKIN	t_{VSDCK}		–	45	–	60	ns
122	$\overline{\text{EXVSYNC}}$ Output Delay Time from CLKIN	t_{EXVDCK}		–	33	–	40	ns
123	$\overline{\text{DISP1}}$, $\overline{\text{DISP2}}$ Output Delay Time from CLKIN	t_{DSPDCK}		–	45	–	60	ns
124	$\overline{\text{CUD}}$ Delay Time from CLKIN	t_{CUDDCK}		–	45	–	60	ns
125	$\overline{\text{EXVSYNC}}$ Output Hold Time from SCLK	t_{EXVHSK}		18	–	25	–	ns
126	$\overline{\text{EXVSYNC}}$ Output Setup Time from SCLK	t_{EXVSSK}		2	–	5	–	ns
127	$\overline{\text{EXVSYNC}}$ Input Pulse Width	t_{WEXV}	Fig. 11	24	–	24	–	t_{cyc}
128	$\overline{\text{EXVSYNC}}$ Input Hold Time from CLKIN	t_{EXVHCK}		12	–	15	–	ns
129	$\overline{\text{EXVSYNC}}$ Input Setup Time from CLKIN	t_{EXVSCK}		12	–	15	–	ns
130	$\overline{\text{EXHSYNC}}$ Input Pulse Width	t_{WEXH}	Fig. 12	24	–	24	–	t_{cyc}
131	$\overline{\text{EXHSYNC}}$ Input Hold Time from CLKIN	t_{EXHHCK}		12	–	15	–	ns
132	$\overline{\text{EXHSYNC}}$ Input Setup Time from CLKIN	t_{EXHSCK}		12	–	15	–	ns
133	$\overline{\text{HSYNC}}$ Output Delay Time from SCLK	t_{HSDSK}		0	25	0	35	ns
134	$\overline{\text{VSYNC}}$ Delay Time from SCLK	t_{VSDSK}		0	25	0	35	ns
135	$\overline{\text{DISP1}}$, $\overline{\text{DISP2}}$ Output Delay Time from SCLK	t_{DSPDSK}		0	25	0	35	ns
136	$\overline{\text{CUD}}$ Delay Time from SCLK	t_{CUDDSK}		0	25	0	35	ns
138	$\overline{\text{EXDISP}}$ Input Setup Time	t_{EXDS}		25	–	30	–	ns
139	$\overline{\text{EXDISP}}$ Input Hold Time	t_{EXDH}		0	–	0	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Interrupts

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
140	$\overline{\text{IRQ}}$ Delay Time 1	t_{IRQ1}		–	60	–	70	ns
141	$\overline{\text{IRQ}}$ Delay Time 2	t_{IRQ2}		–	300	–	300	ns
142	$\overline{\text{IACK}}$ Setup Time	t_{IKS}		30	–	40	–	ns
144	$\overline{\text{IACK}}$ "High" Level Width	t_{WIKH}		50	–	60	–	ns
145	Data Bus 3 state Recovery Time 3	t_{DBRT3}		0	–	0	–	ns
146	Interrupt Vector Delay Time	t_{IVD}		–	45	–	55	ns
147	Interrupt Vector Hold Time	t_{IVH}		5	–	5	–	ns
148	Interrupt Vector Turn Off Time	t_{IVTZ}		–	45	–	55	ns
149	Interrupt $\overline{\text{DTACK}}$ Delay Time (Z to L)	t_{IDTZL}	Fig. 13	–	45	–	55	ns
150	Interrupt $\overline{\text{DTACK}}$ Delay Time (D to L)	t_{IDTDL}		0	–	0	–	ns
151	Interrupt $\overline{\text{DTACK}}$ Release Time (L to H)	t_{IDTLH}		–	45	–	55	ns
152	$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High Impedance	t_{IDTKZ}		–	50	–	60	ns
153	Interrupt Cycle Wait Time	t_{ICWAT}		0	–	0	–	ns
156	$\overline{\text{CS}}$, $\overline{\text{DACK}}$ Setup Time to $\overline{\text{IACK}}$	t_{CDKIS}		50	–	60	–	ns
157	$\overline{\text{CS}}$, $\overline{\text{DACK}}$ Hold Time to $\overline{\text{IACK}}$	t_{CDKIH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Timing Charts

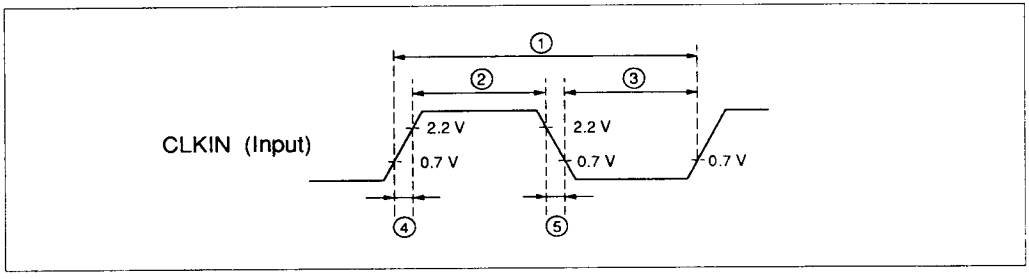


Figure 1. Clock Input (CLKIN) Waveform

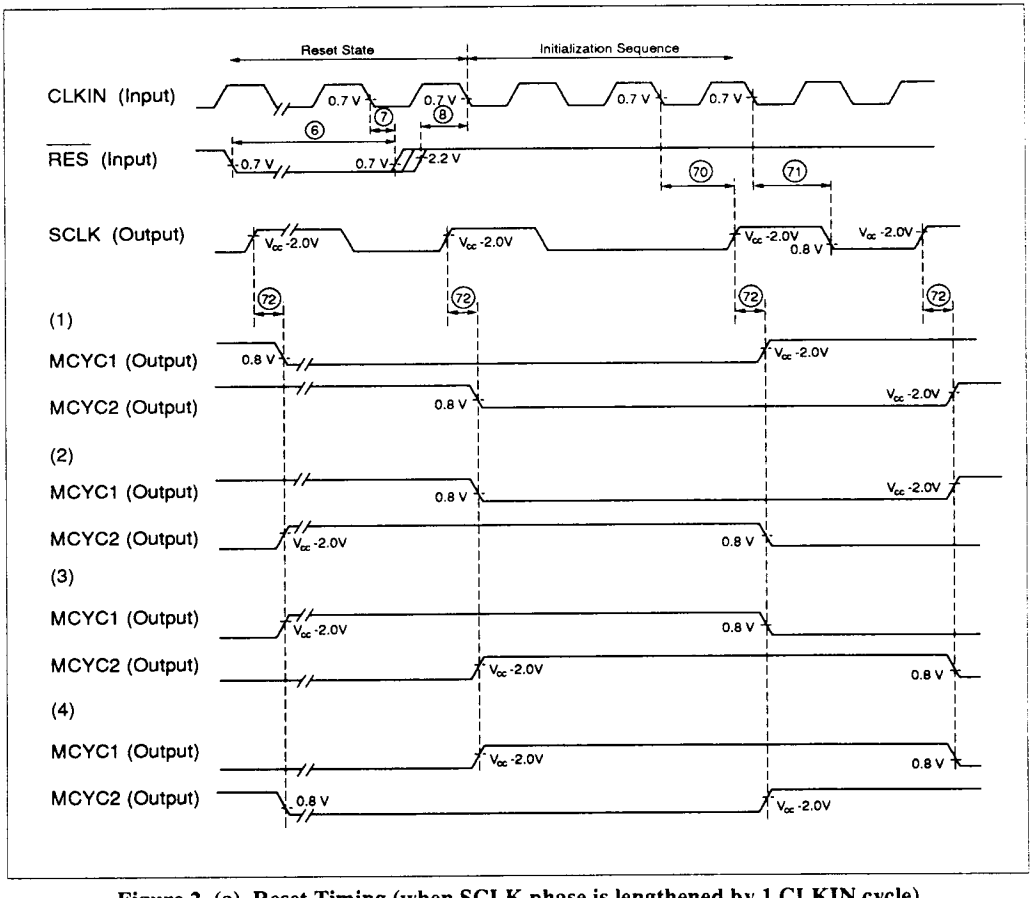


Figure 2. (a) Reset Timing (when SCLK phase is lengthened by 1 CLKIN cycle)

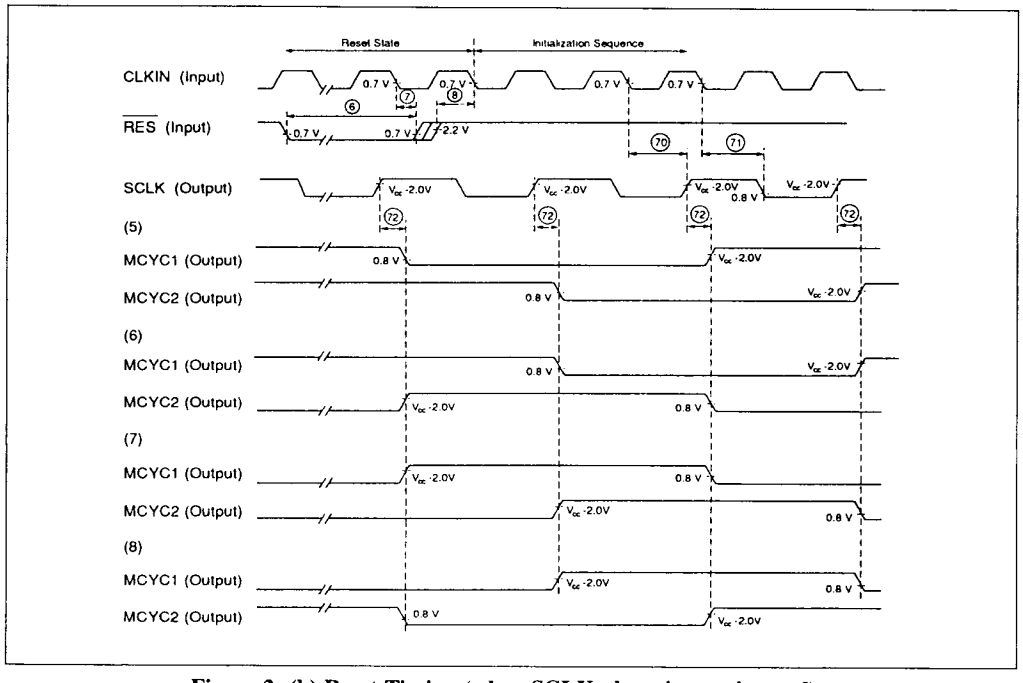


Figure 2. (b) Reset Timing (when SCLK phase is not changed)

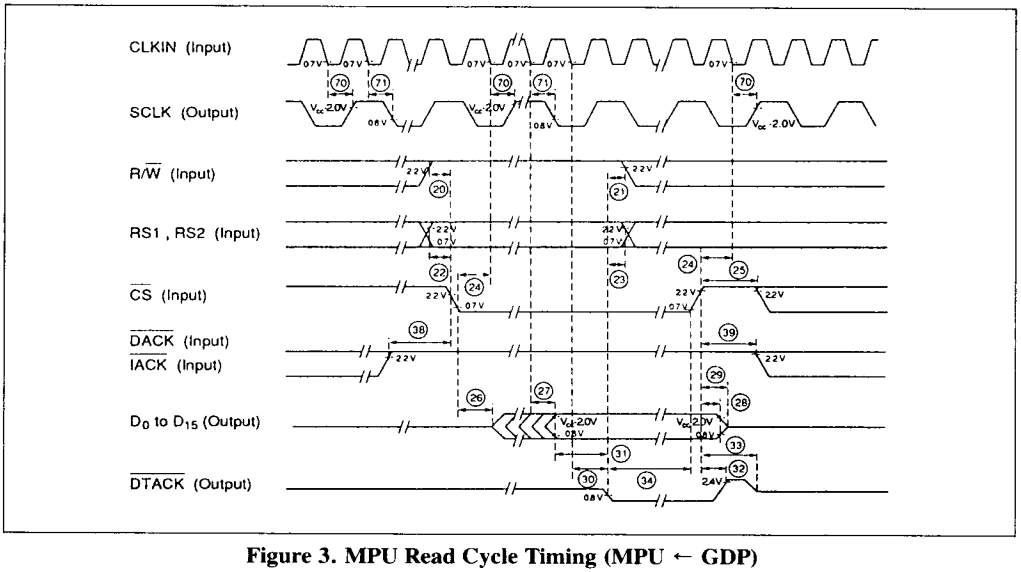


Figure 3. MPU Read Cycle Timing (MPU ← GDP)

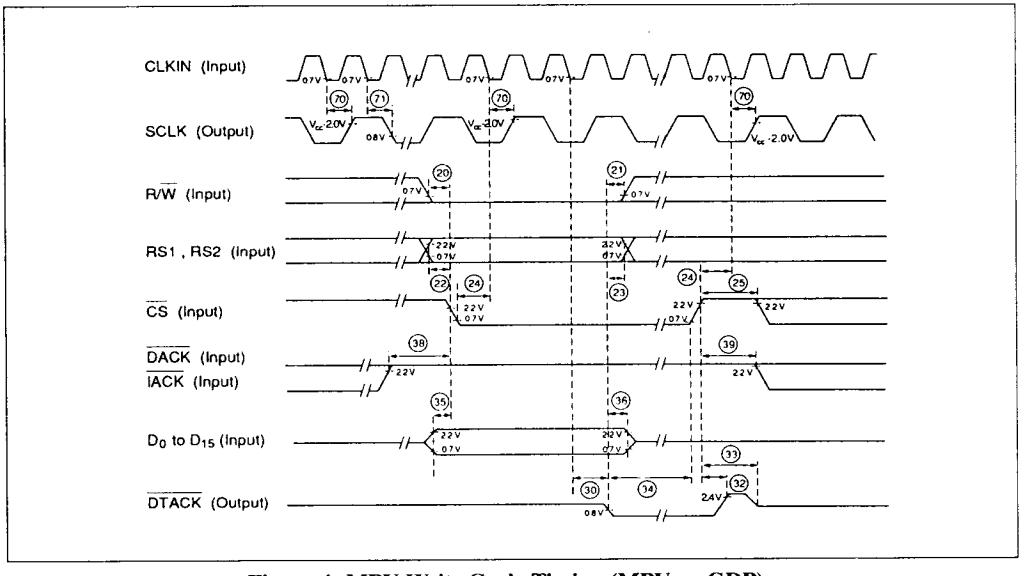


Figure 4. MPU Write Cycle Timing (MPU → GDP)

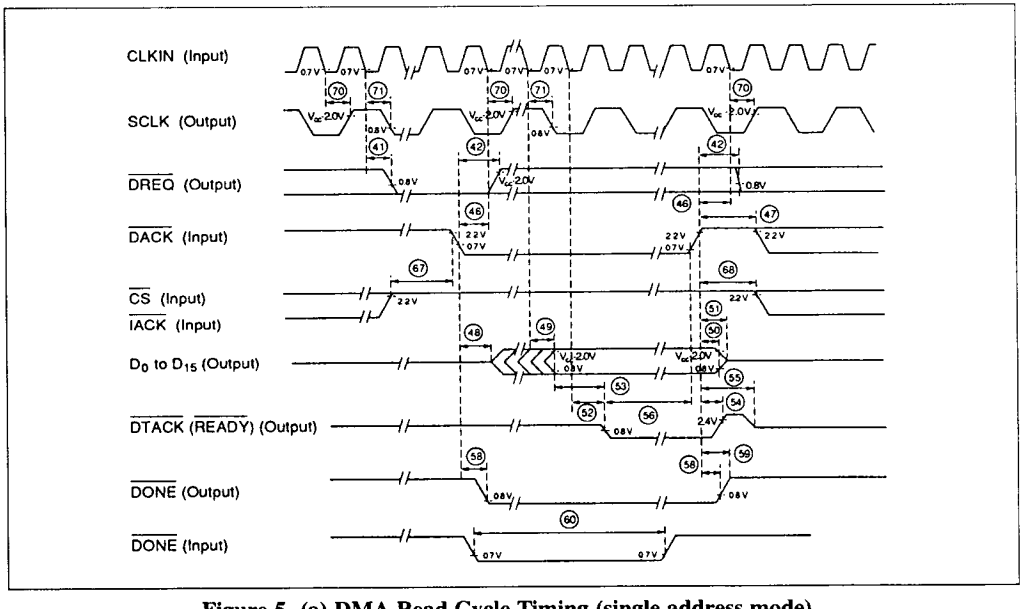


Figure 5. (a) DMA Read Cycle Timing (single address mode)

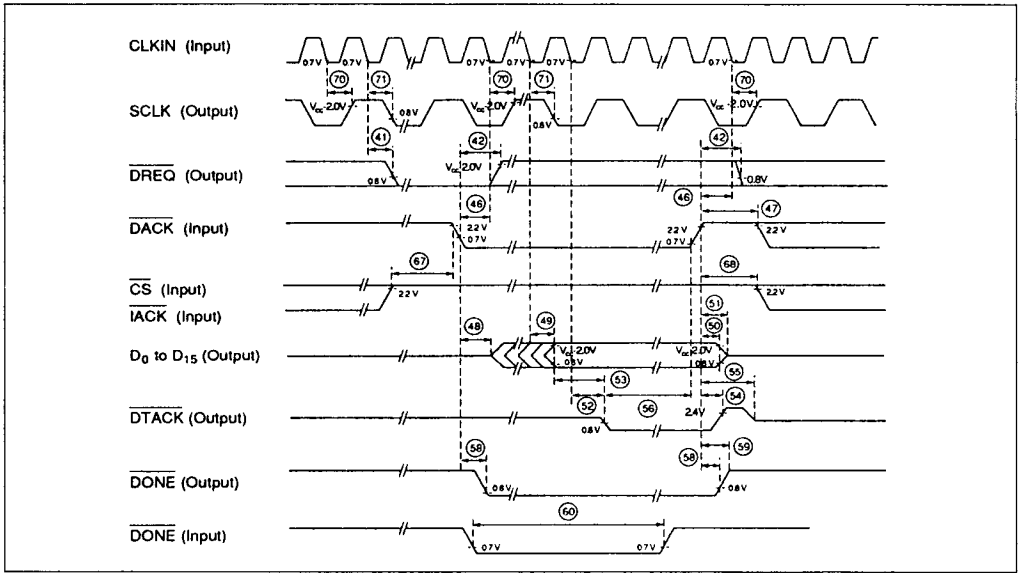


Figure 5. (b) DMA Read Cycle Timing (dual address mode)

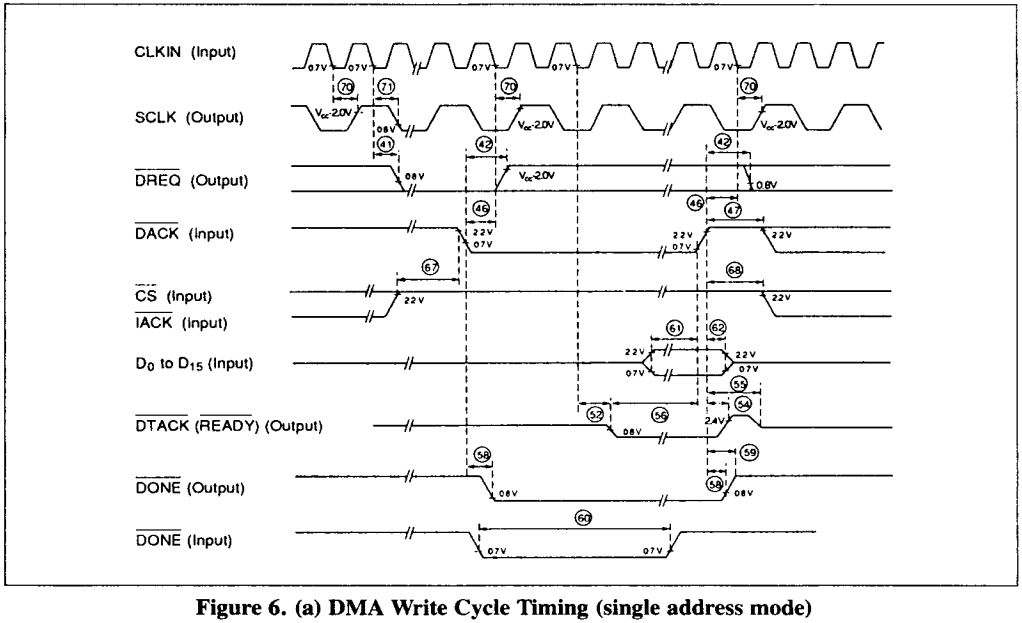


Figure 6. (a) DMA Write Cycle Timing (single address mode)

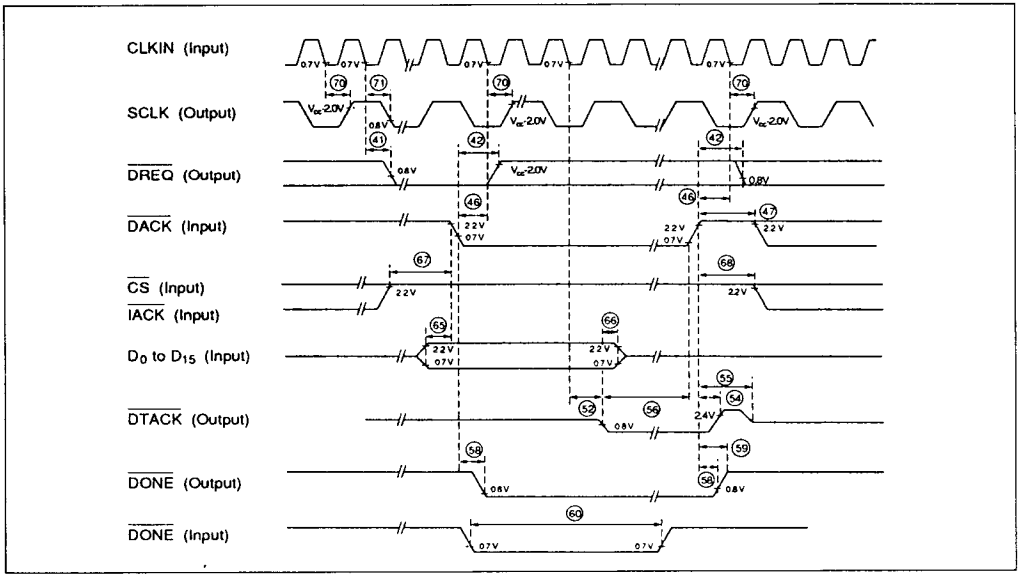


Figure 6. (b) DMA Write Cycle Timing (dual address mode)

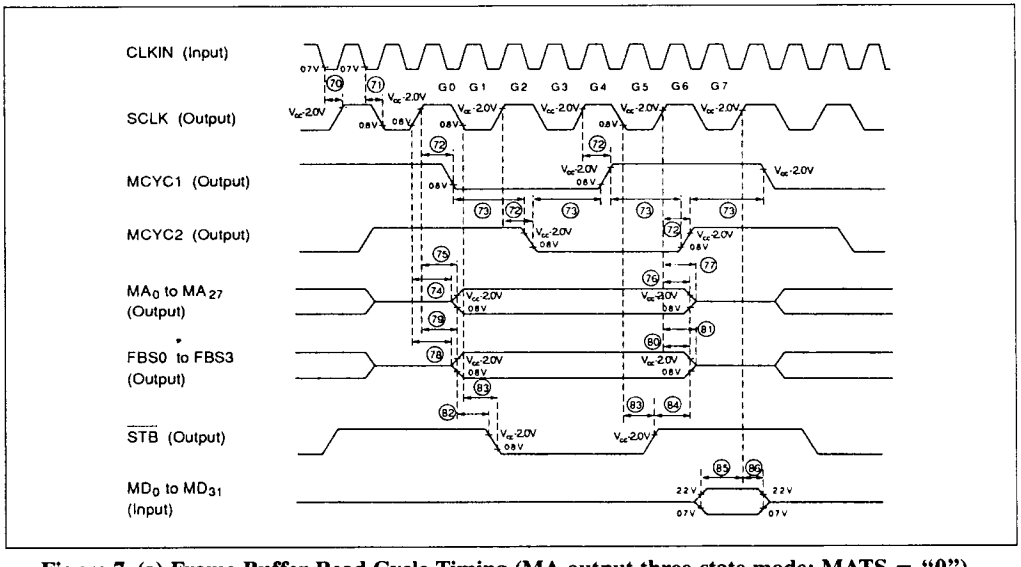


Figure 7. (a) Frame Buffer Read Cycle Timing (MA output three-state mode: MATS = "0")

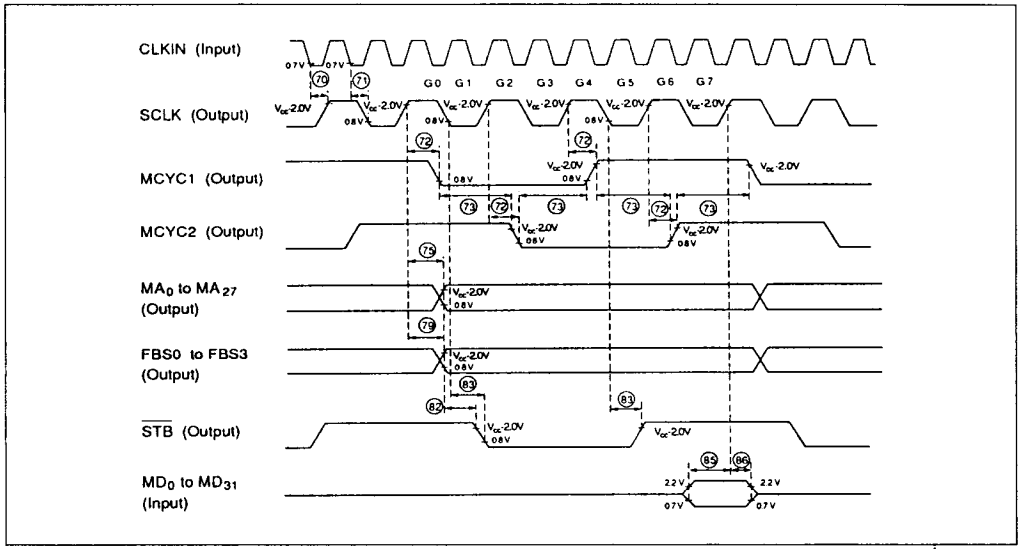


Figure 7. (b) Frame Buffer Read Cycle Timing (MA output non-three-state mode: MATS = "1")

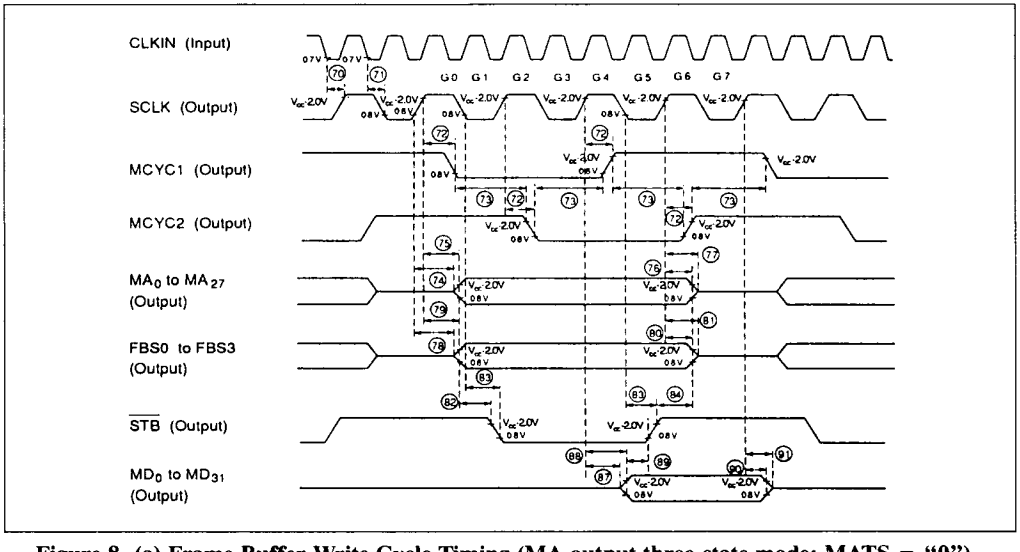


Figure 8. (a) Frame Buffer Write Cycle Timing (MA output three-state mode: MATS = "0")

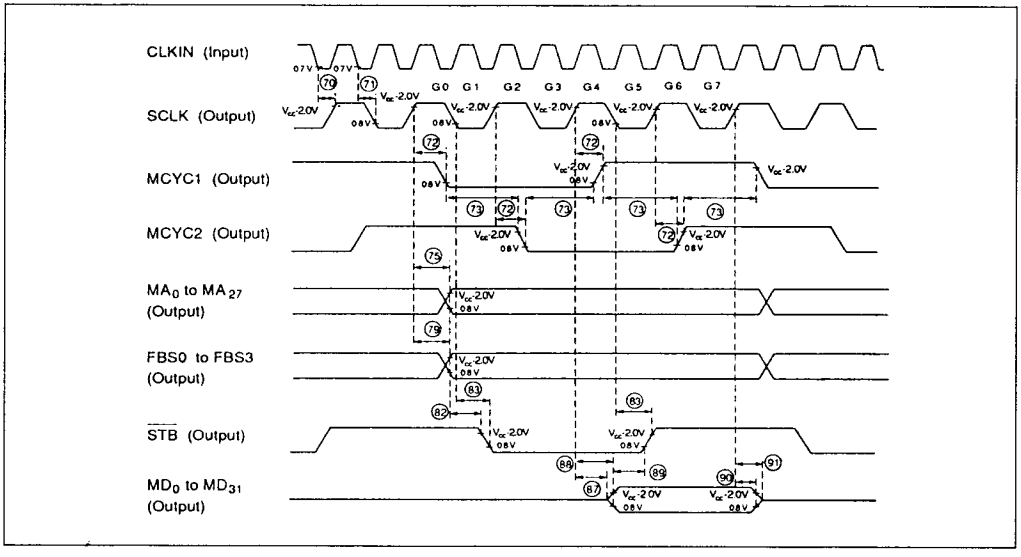


Figure 8. (b) Frame Buffer Write Cycle Timing (MA output non-three-state mode: MATS = "1")

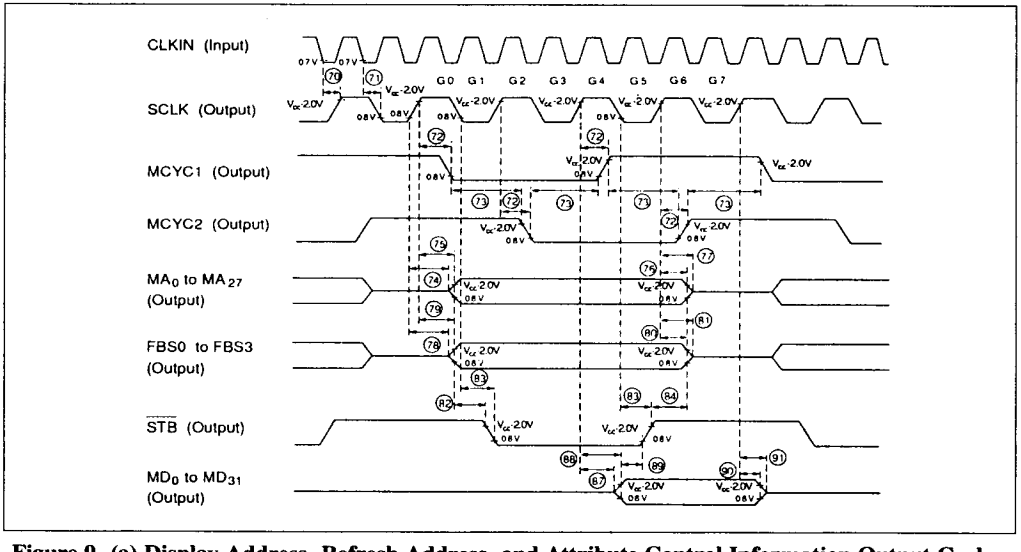


Figure 9. (a) Display Address, Refresh Address, and Attribute Control Information Output Cycle Timing (MA output three-state mode: MATS = "0")

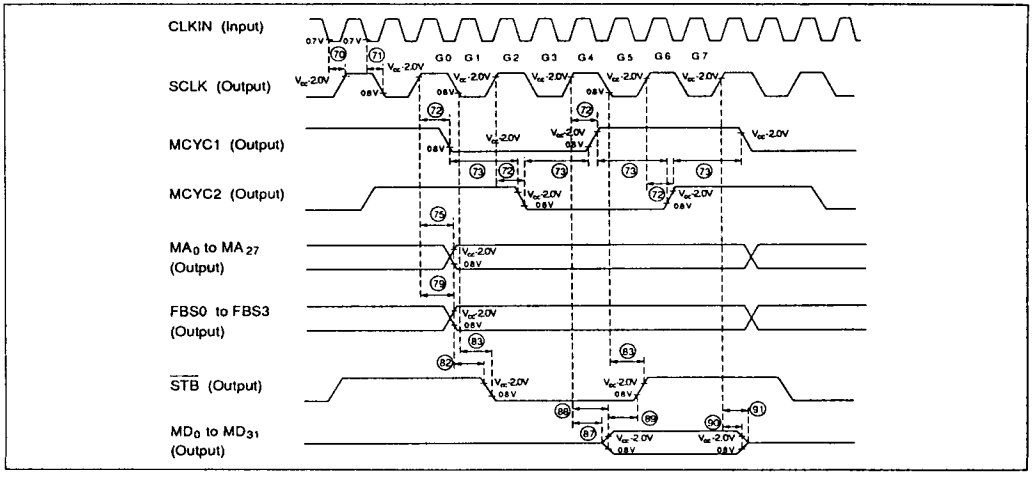


Figure 9. (b) Display Address, Refresh Address, and Attribute Control Information Output Cycle Timing (MA output non-three-state mode: MATS = "1")

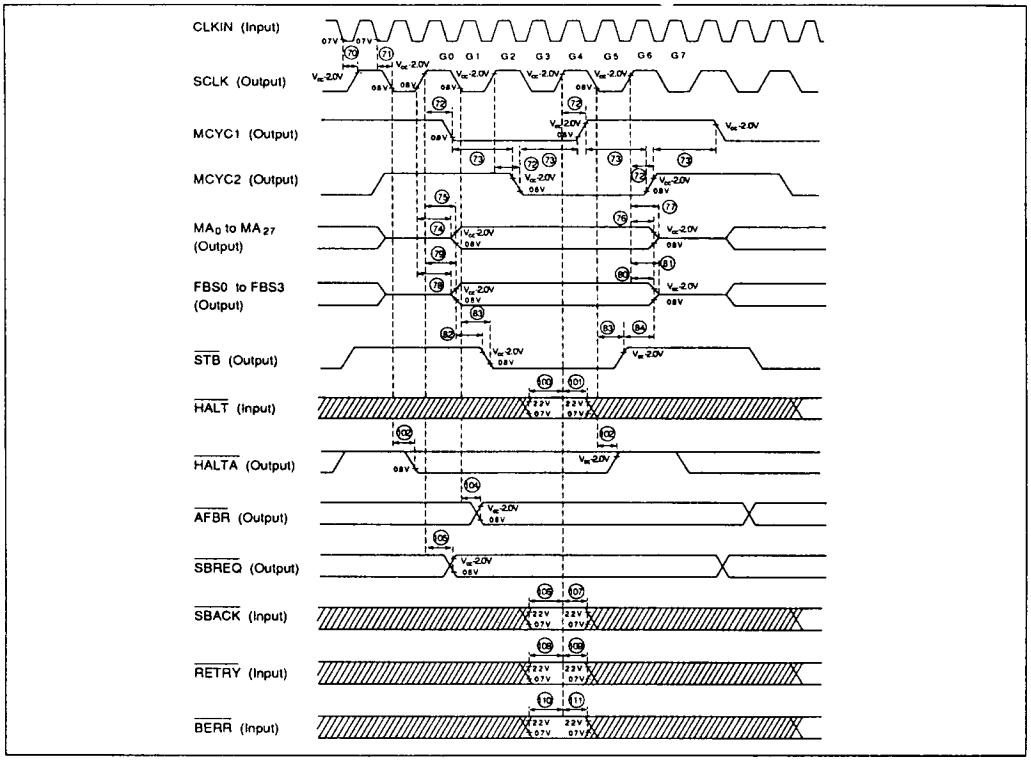


Figure 10. System Interface Timing (MA output three-state mode: MATS = "0")

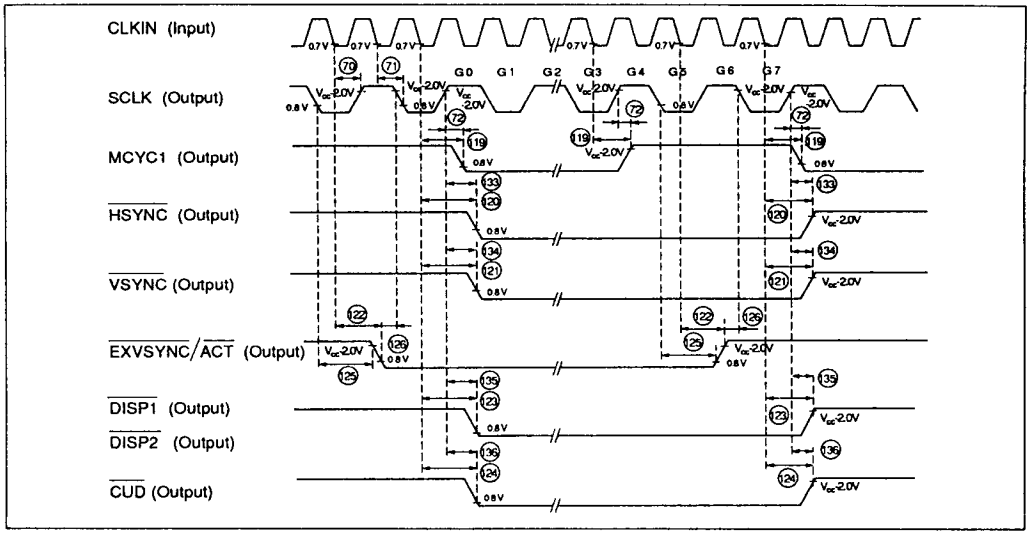


Figure 11 Display Control Signal Output Timing

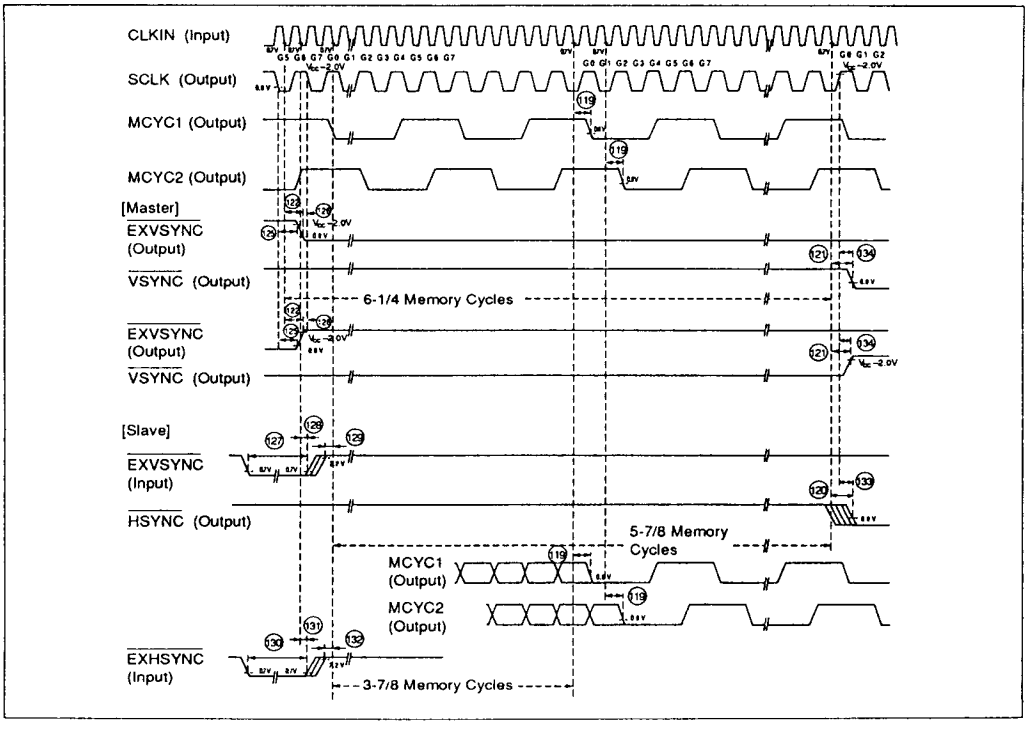


Figure 12. (a) External Synchronization Timing

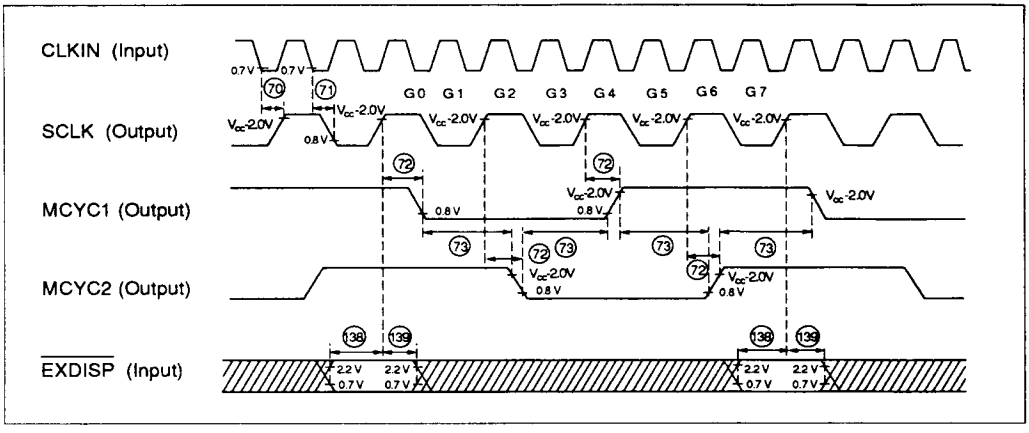


Figure 12. (b) External Synchronization Timing (laser printer mode)

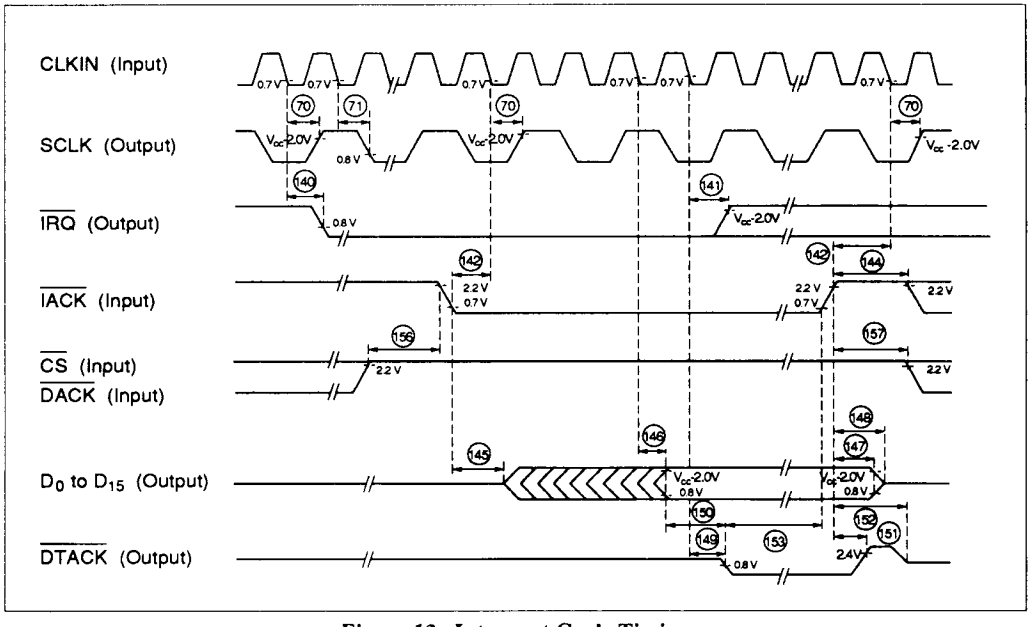


Figure 13. Interrupt Cycle Timing