

HAT2058R/HAT2058RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

HITACHI

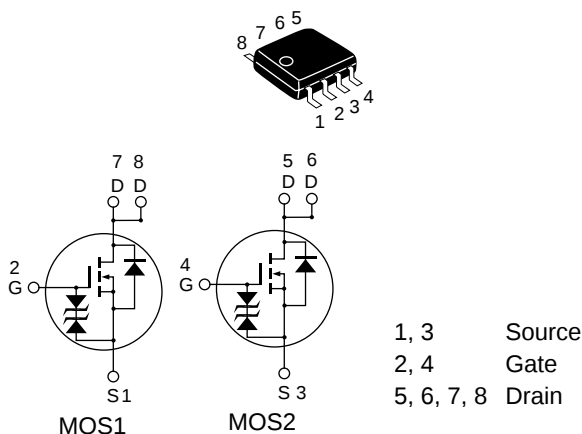
ADE-208-934 (Z)
1st. Edition
Mar. 2001

Features

- Low on-resistance
 - Capable of 4 V gate drive
 - Low drive current
 - High density mounting
 - “J” is for Automotive application
- High temperature D-S leakage guarantee
Avalanche rating

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		HAT2058R	HAT2058RJ	
Drain to source voltage	V _{DSS}	100	100	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	4	4	A
Drain peak current	I _D (pulse) ^{Note1}	32	32	A
Body-drain diode reverse drain current	I _{DR}	4	4	A
Avalanche current	I _{AP} ^{Note4}	—	4	A
Avalanche energy	E _{AR} ^{Note4}	—	1.6	mJ
Channel dissipation	Pch ^{Note2}	2	2	W
	Pch ^{Note3}	3	3	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	−55 to +150	−55 to +150	°C

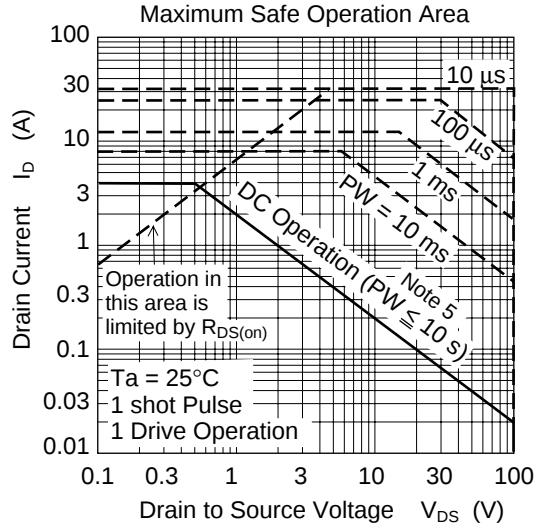
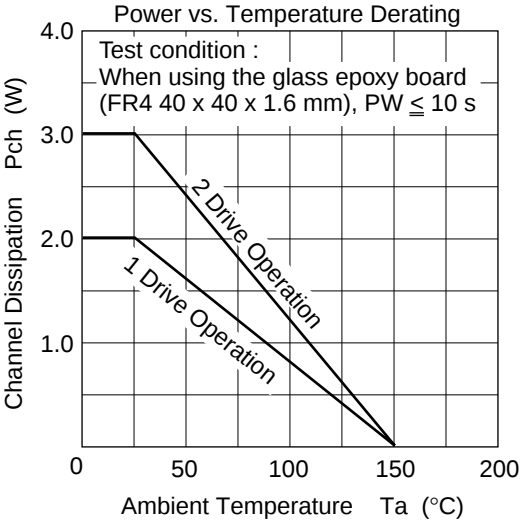
- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics (Ta = 25°C)

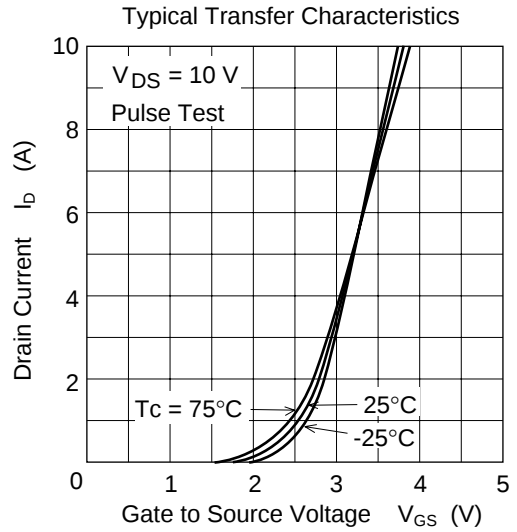
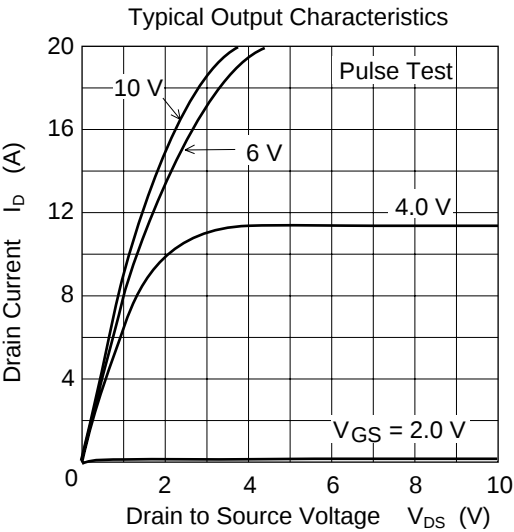
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	HAT2058R	I_{DSS}	—	—	1	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
	HAT2058RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage drain current	HAT2058R	I_{DSS}	—	—	—	μA	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0$ $T_a = 125^\circ\text{C}$
	HAT2058RJ	I_{DSS}	—	—	10	μA	
Gate to source cutoff voltage		I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Static drain to source on state resistance		$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance		$ y_{fs} $	3	5	—	S	$I_D = 2 \text{ A}^{*1}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance		$R_{DS(on)}$	—	120	145	mΩ	$I_D = 2 \text{ A}^{*1}$, $V_{GS} = 10 \text{ V}$
		$R_{DS(on)}$	—	150	180	mΩ	$I_D = 2 \text{ A}^{*1}$, $V_{GS} = 4 \text{ V}$
Input capacitance		C_{iss}	—	420	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$
Output capacitance		C_{oss}	—	180	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance		C_{rss}	—	100	—	pF	
Turn-on delay time		$t_{d(on)}$	—	10	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$ $V_{DD} \cong 30 \text{ V}$
Rise time		t_r	—	30	—	ns	
Turn-off delay time		$t_{d(off)}$	—	110	—	ns	
Fall time		t_f	—	60	—	ns	
Body-drain diode forward voltage		V_{DF}	—	0.85	1.1	V	$I_F = 4 \text{ A}$, $V_{GS} = 0^{*1}$
Body-drain diode reverse recovery time		t_{rr}	—	75	—	ns	$I_F = 4 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse test

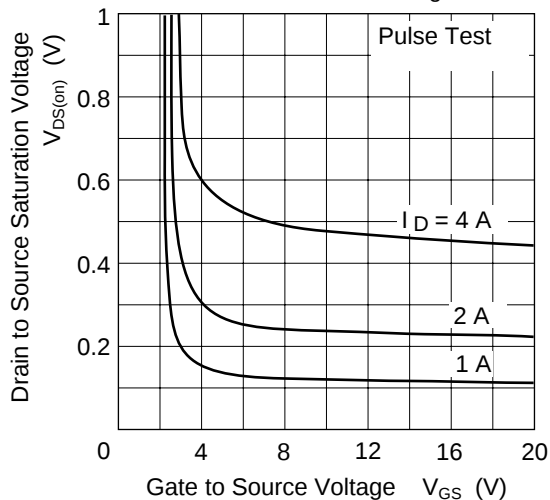
Main Characteristics



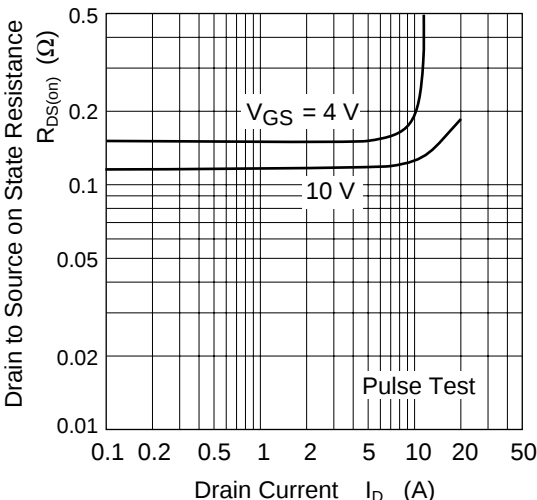
Note 6:
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)



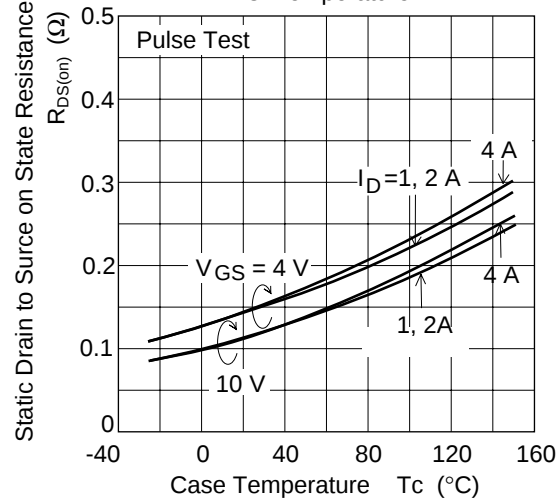
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



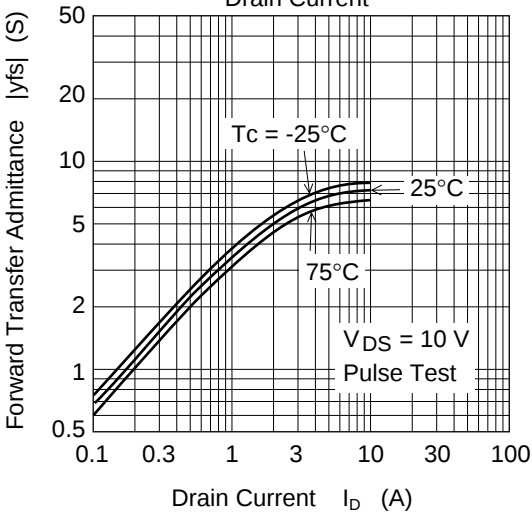
Static Drain to Source on State Resistance
vs. Drain Current

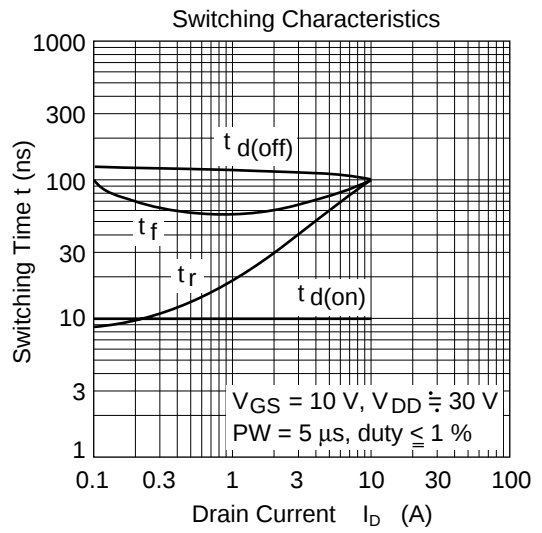
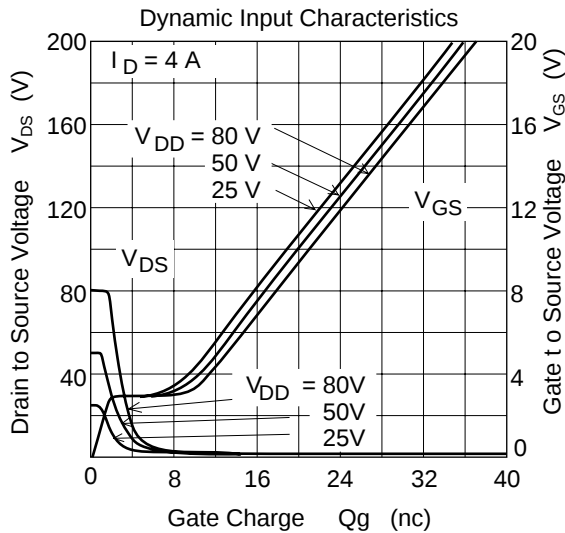
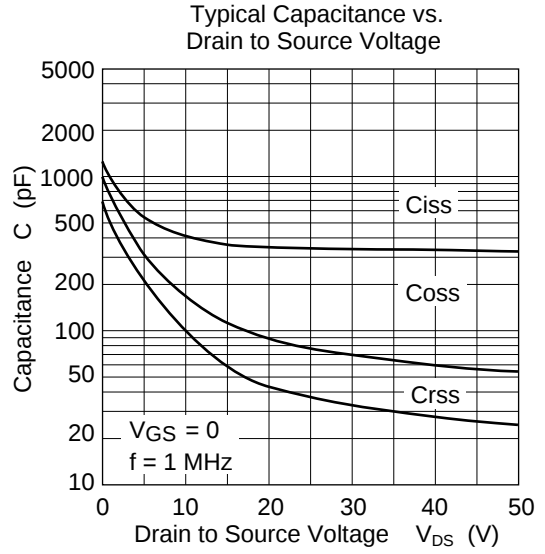
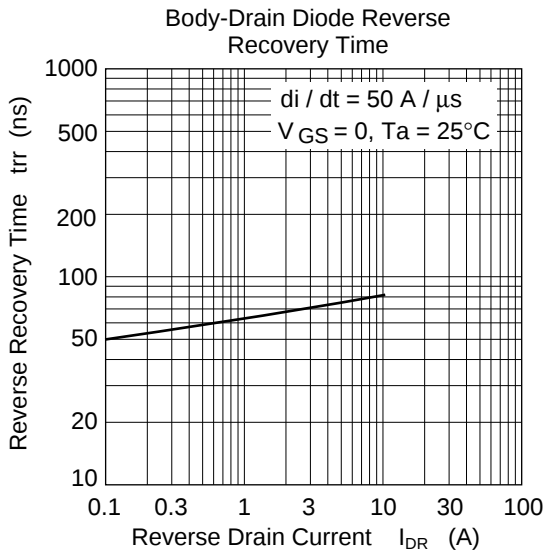


Static Drain to Source on State Resistance
vs. Temperature

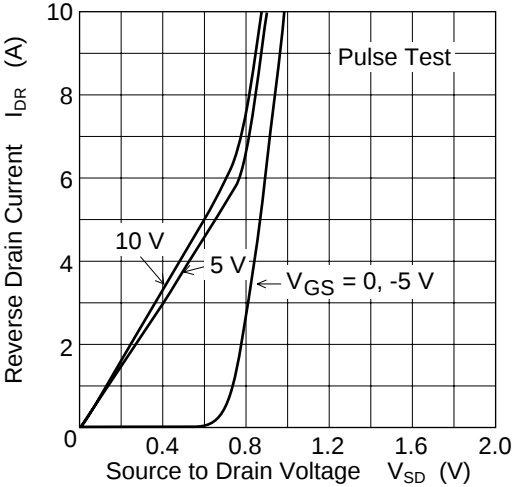


Forward Transfer Admittance vs.
Drain Current

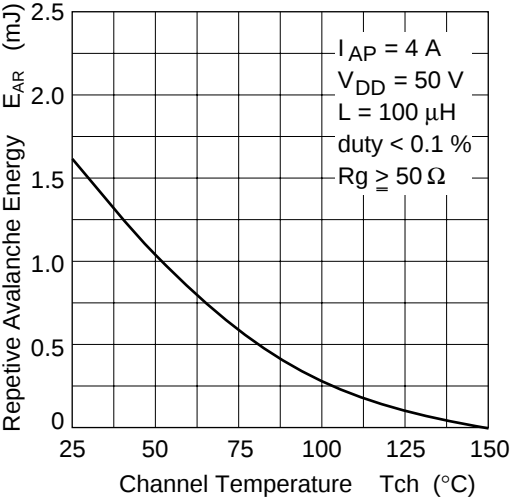




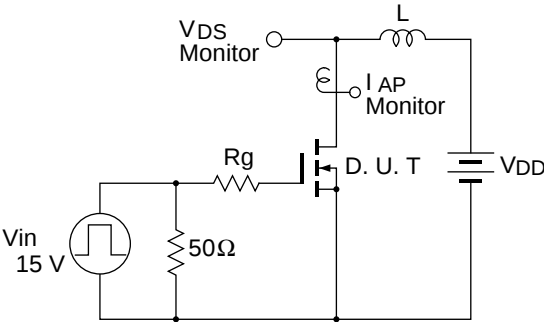
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

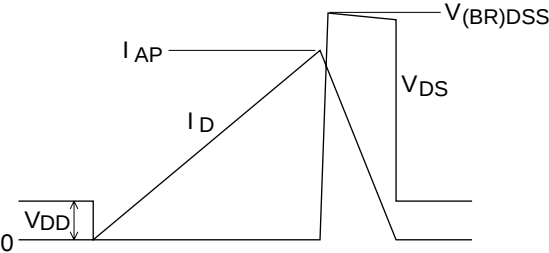


Avalanche Test Circuit

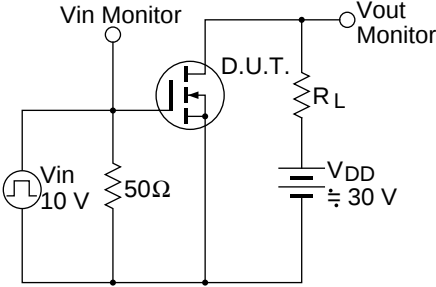


Avalanche Waveform

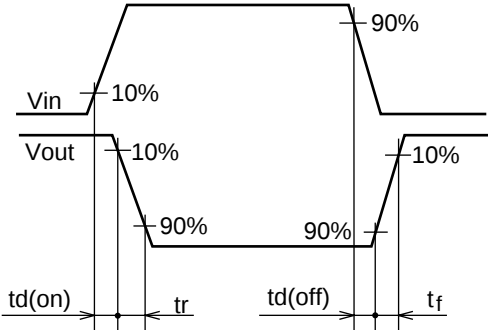
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

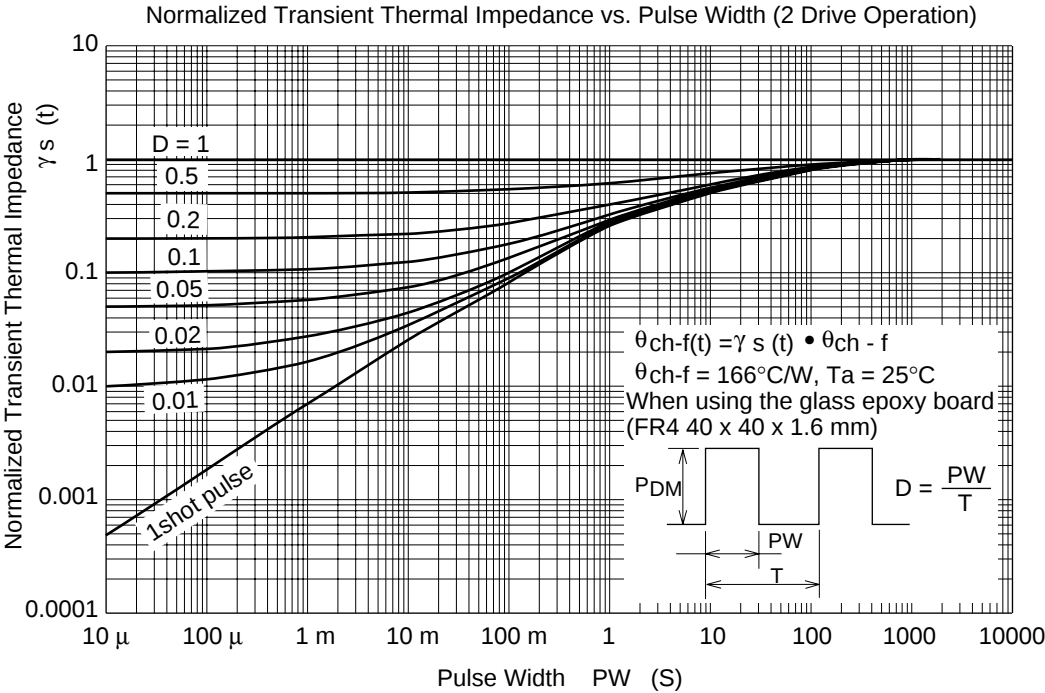
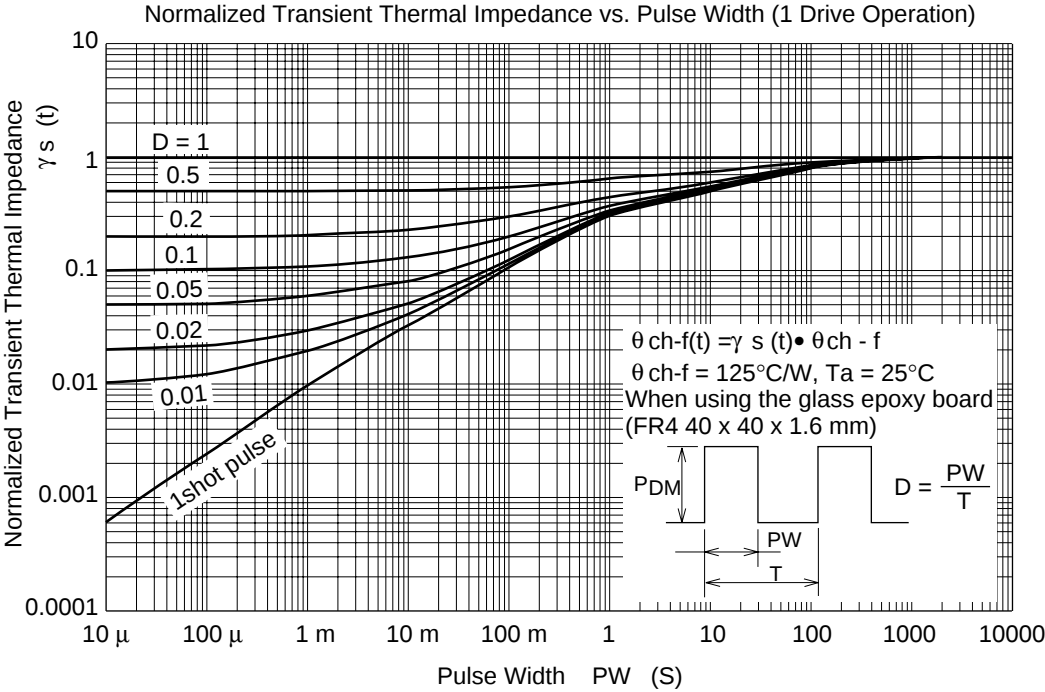


Switching Time Test Circuit



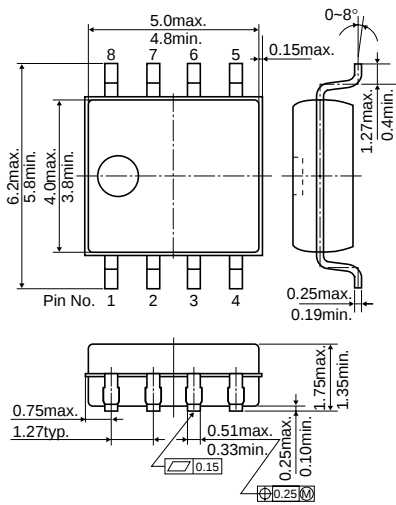
Switching Time Waveform





Package Dimensions

Unit: mm



Hitachi Code	FP-8DA
JEDEC	—
EIAJ	—

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