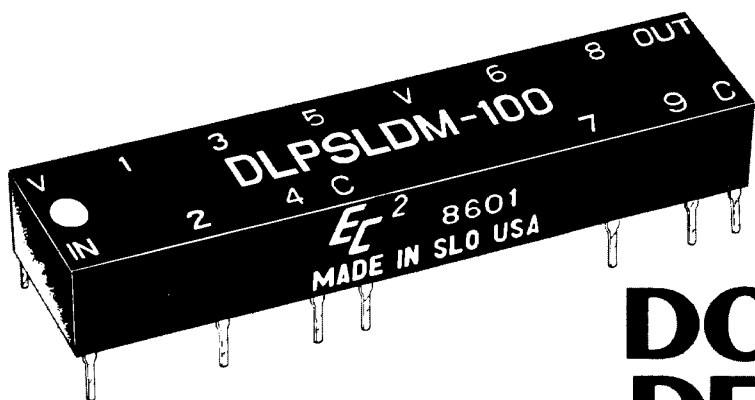


EC²



low profile

T²L

COMPATIBLE DOUBLE LOGIC DELAY MODULE (LOW POWER SCHOTTKY)

- T²L input and outputs
- Delays stable and precise
- 30-pin DIP package (.250 high)
- Available in delays from 100 to 1000ns
- 10% taps — each isolated and with 20 low power Schottky T²L fan-out capacity
- Rise time 8ns maximum

design notes

The "DIP Series" Low Power Schottky Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single 30-pin DIP package. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1.5 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The DLPSLDM is offered in 14 delays from 100 to 1000ns with each module incorporating taps at 10% increments of total delay. Delay tolerances are maintained as shown in the accom-

panying Part Number Table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.3V level on the leading edge. Rise time for all modules is 8ns maximum when measured from 0.8V to 2.0V. Temperature coefficient of delay is approximately +500 ppm/°C over the operating temperature range of 0 to 70°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 20 low power Schottky loads at each tap.

These "DIP Series" modules are packaged in a 30-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive stand off from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

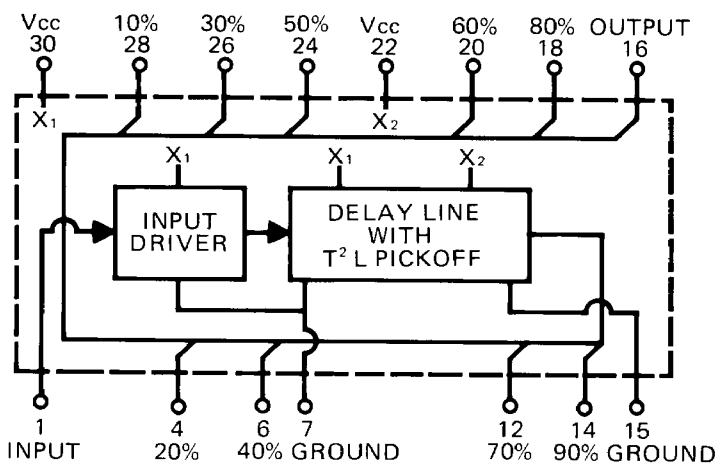
EC²

engineered components company

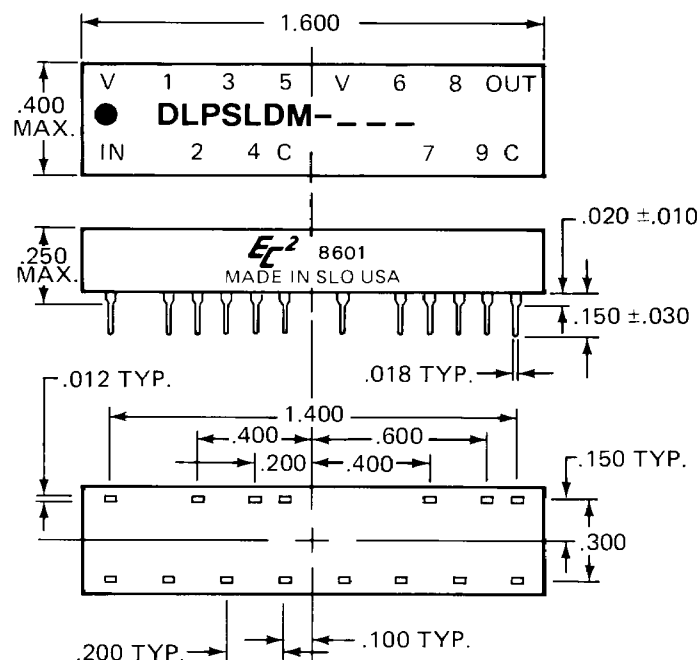
3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121

Phone: (805) 544-3800

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)										
Part Number	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Output
DLPSLDM-100	10 ±1	20 ±1	30 ±1.5	40 ±2	50 ±2	60 ±2.5	70 ±2.5	80 ±3	90 ±3	100 ±3
DLPSLDM-150	15 ±1	30 ±1.5	45 ±2	60 ±2.5	75 ±2.5	90 ±3	105 ±4	120 ±4	135 ±4	150 ±5
DLPSLDM-200	20 ±1	40 ±2	60 ±2.5	80 ±3	100 ±3	120 ±4	140 ±5	160 ±5	180 ±6	200 ±6
DLPSLDM-250	25 ±1.5	50 ±2	75 ±2.5	100 ±3	125 ±4	150 ±5	175 ±5	200 ±6	225 ±7	250 ±8
DLPSLDM-300	30 ±1.5	60 ±2.5	90 ±3	120 ±4	150 ±5	180 ±6	210 ±7	240 ±7	270 ±8	300 ±9
DLPSLDM-350	35 ±1.5	70 ±2.5	105 ±4	140 ±5	175 ±5	210 ±7	245 ±8	280 ±9	315 ±10	350 ±11
DLPSLDM-400	40 ±2	80 ±3	120 ±4	160 ±5	200 ±6	240 ±7	280 ±9	320 ±10	360 ±11	400 ±12
DLPSLDM-450	45 ±2	90 ±3	135 ±4	180 ±6	225 ±7	270 ±8	315 ±10	360 ±11	405 ±12	450 ±14
DLPSLDM-500	50 ±2	100 ±3	150 ±5	200 ±6	250 ±8	300 ±9	350 ±11	400 ±12	450 ±14	500 ±15
DLPSLDM-600	60 ±2.5	120 ±4	180 ±5	240 ±7	300 ±9	360 ±11	420 ±13	480 ±15	540 ±16	600 ±18
DLPSLDM-700	70 ±2.5	140 ±5	210 ±7	280 ±9	350 ±11	420 ±13	490 ±15	560 ±17	630 ±19	700 ±20
DLPSLDM-800	80 ±3	160 ±5	240 ±7	320 ±10	400 ±12	480 ±15	560 ±17	640 ±19	720 ±20	800 ±20
DLPSLDM-900	90 ±3	180 ±6	270 ±8	360 ±11	450 ±14	540 ±16	630 ±19	720 ±20	810 ±20	900 ±22
DLPSLDM-1000	100 ±3	200 ±6	300 ±9	400 ±12	500 ±15	600 ±18	700 ±20	800 ±20	900 ±22	1000 ±22

φ All modules can be operated with a minimum input pulse width of 20% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vcc supply voltage is maintained at 5.0V DC.
3. All units are tested using a low power Schottky toggle-type positive input pulse and one low power Schottky T²L load at the output being tested.
- φ 4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* Vcc supply voltage: 4.75 to 5.25V DC

Vcc supply current:

Constant "0" in 32ma typical

Constant "1" in 6ma typical

Logic 1 input:

Voltage 2V min.; 5.5V max.

Current 2.4V = 20ua max.

5.5V = .1ma max.

Logic 0 input:

Voltage8V max.

Current -.4ma max. (@.4V in)

Logic 1 Voltage out: 2.7V min.

Logic 0 Voltage out:5V max.

Operating temperature range: 0 to 70°C.

Storage temperature: -55 to +125°C.

* Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

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Catalog No. C/021280R