14- & 16-Bit, Hybrid Digital-to-Resolver Converters

AD2S65/AD2S66

FEATURES

- Single Rank Transparent TTL or CMOS Compatible Latched Input Registers With High and Low Byte ENABLE
- Accuracy ±1, ±2 or ±4 Arc Minutes
- Resolution 14- or 16-Bit
- Very Low DC Offset Voltage
- Autonulling Option Available (Extremely Low DC Offset Voltage)
- Output Drive Capability 4.3 mA Peak into Resistive, Inductive or Capacitive Loads
- Low Radius Vector Variation 0.03% (Transformation Ratio)
- ±15 V DC Power Supplies Only
- DC to 2.6 kHz Depending on Option (to 10 kHz with Reduced Accuracy)
- Low Power Dissipation
- 32-Pin Welded Metal Package
- Hermetically Sealed
- Protection Against +200% Overload on Analog Input
- Microprocessor Compatible (8 or 16 Bits)

APPLICATIONS

- Polar to Rectangular Coordinate Conversion
- Missile and Fire Control Systems
- Simulation Systems
- Low Frequency Oscillators
- PPI Displays
- Radar and Navigational Systems
- Avionics
- Axis Rotation
- Flight Instrumentation
- Wrap-Around Resolver-to-Digital Converter Tests
- ATE Systems

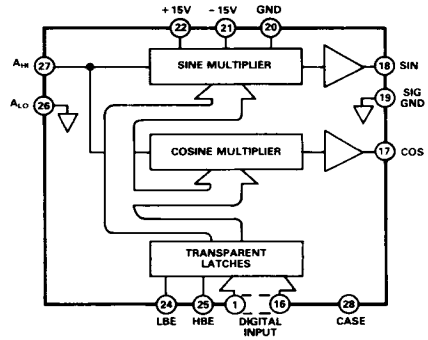
GENERAL DESCRIPTION

The AD2S65 and AD2S66 are hybrid digital-to-resolver converters which accept a 14-bit or 16-bit digital, natural binary input word representing angle, and output sine and cosine voltages.

The AD2S65 and AD2S66 are pin compatible replacements for the previous generation DRC1765 and DRC1766 digital-to-resolver converters, respectively.

The SIN and COS output voltage signals are internally multiplied by the analog input reference voltage, thus the SIN and COS outputs are amplitude modulated at the input reference frequency.

FUNCTIONAL BLOCK DIAGRAM



NOTE: A_{LO}, GND, AND SIG GND ARE INTERNALLY CONNECTED.

The analog input reference voltage can either be dc or ac voltage of frequency up to 10 kHz. For the extremely low dc offset autonulling part, the frequency range is covered by two options, 50 Hz to 2.6 kHz and 360 Hz to 2.6 kHz (both to 10 kHz with reduced accuracy).

The digital input word to the converter is latched with transparent high and low byte ENABLE commands to facilitate easy interface to microprocessor systems. The input latches are TTL and CMOS compatible utilizing components of HCT series.

The devices are available in accuracy grades of ±1, ±2 and ±4 arc minutes. Please see ordering information.

A particularly useful feature of the converters is their low dc output offset voltage (±2.5 mV typ). The autonulling option (see ordering information) offers an extremely low output offset voltage (±0.5 mV typ). The output voltage dc offset remains constant over the frequency range and operating temperature of the converter. The low offset voltage characteristic of this range means that external trim adjustments are not required, particularly important in display and test applications.

The converters have a closed loop bandwidth of 300 kHz and are capable to drive into a load which can be inductive, resistive, capacitive (to the extent of 15 nF) or a combination of above.

A further feature of the converters is that the radius vector variation (Transformation Ratio) is very low at 0.03%. This means that the individual SIN and COS outputs are both independently accurate which is important in coordinate conversion, display applications, simulation and test of resolver-to-digital converters.

AD2S65/AD2S66—SPECIFICATIONS (typical @ +25°C, unless otherwise stated)

Models	AD2S65X1Z	AD2S66X1Z	AD2S65X2Z/X3Z	AD2S66X2Z/X3Z	Comments
DIGITAL INPUT RESOLUTION	**14 Bits (1.3 arc min Per Bit)**	**16 Bits (19 arc sec Per Bit)**	**14 Bits (1.3 arc min Per Bit)**	**16 Bits (19 arc sec Per Bit)**	
DIGITAL INPUT FORMAT	Parallel Natural Binary	*	*	*	TTL and CMOS Compatible
RECOMMENDED ANALOG INPUT (V_{REF})	3.4 Volts rms	*	*	*	
OUTPUT (SINE AND COSINE) WITH RECOMMENDED ANALOG INPUT	6.8 Volts rms	*	*	*	Refer to Gain Section
GAIN[1]	2 ±0.1% N/A N/A	* N/A N/A	N/A 1.98 ±0.1% 1.98 ±0.1%	N/A ** **	Option X1Z dc to 2.6 kHz Option X2Z 50 Hz to 2.6 kHz Option X3Z 360 Hz to 2.6 kHz See Figure 4
OUTPUT TEMPERATURE COEFFICIENT	5 ppm/°C of FSR (typ) 25 ppm/°C of FSR (max)	* *	* *	* *	
ANALOG INPUT FREQUENCY RANGE	dc to 2.6 kHz (dc to 10 kHz With Reduced Accuracy) N/A N/A	* * N/A N/A	N/A N/A 50 Hz to 2.6 kHz 360 Hz to 2.6 kHz (to 10 kHz With Reduced Accuracy)	N/A N/A ** **	Option X1Z Option X2Z Option X3Z
ANALOG INPUT IMPEDANCE	10.2 kΩ	*	*	*	±5% Resistive
ANALOG OUTPUT IMPEDANCE	2 mΩ (typ) 20 mΩ (max)	* *	* *	* *	
ANALOG OFFSET VOLTAGE	**±2.5 mV (typ)** **±12 mV (max)**	* *	**±0.5 (typ)** **±2.5 (max)**	*	
OUTPUT DRIVE CAPABILITY	**4.3 mA peak @ ±10 V peak**	*	*	*	
OUTPUT PROTECTION	Outputs May Be Grounded Indefinitely				
RESPONSE TO A STEP INPUT	20 μs (max) to Within Accuracy of Converter. Any Size Step Input	*	*	*	
VECTOR ACCURACY Radius Error Angular Error	0.03% ±2, ±4 arc min	* ±1, ±2, ±4 arc min	* ±2, ±4 arc min	* ±1, ±2, ±4 arc min	Refer to Frequency Option. See Figure 3
DIGITAL INPUTS (BIT 1–BIT 16) V_{IH} V_{IL}	 2.0 V dc min 0.8 V dc max	*	*	*	+15 V = 15 V dc I_{IH} = 1 μA I_{IL} = 1 μA
DIGITAL INPUTS (ENABLE M, ENABLE L)[2] V_{IH} V_{IL}	 2.0 V dc min 0.8 V dc max	*	*	*	+15 V = 15 V dc I_{IH} = 1.5 μA I_{IL} = 1.5 μA
DIGITAL INPUTS LEAKAGE CURRENT	±1 μA max	*	*	*	+15 V = 15 V dc
DATA SETUP TIME[2] (DATA TO ENABLE M, L)	40 ns min	*	*	*	+15 V = 15 V dc
HOLD TIME (DATA[2] TO ENABLE M, L)	25 ns min	*	*	*	+15 V = 15 V dc
MINIMUM PULSE WIDTH[2] (DATA TO ENABLE M, L)	40 ns min	*	*	*	+15 V = 15 V dc

Models	AD2S65X1Z	AD2S66X1Z	AD2S65X2Z/X3Z	AD2S66X2Z/X3Z	Comments
POWER SUPPLIES					
+15 Volts	**26 mA (typ) 32 mA (max)**	*	*	*	
−15 Volts	**15 mA (typ) 23 mA (max)**	*	*	*	
TEMPERATURE RANGE					
Operating	−55°C to +125°C	*	*	*	Option 4YZ
	0 to +70°C	*	*	*	Option 5YZ
Storage	−65°C to +150°C	*	*	*	
DIMENSIONS	1.75" × 1.1" × 0.225"	*	*	*	
PACKAGE TYPE	32-Pin Bottom Brazed Ceramic T DIP	*	*	*	
WEIGHT	15 Grams (typ)	*	*	*	
	20 Grams (max)	*	*	*	

NOTES
[1]See Figure 4.
[2]ENABLE M enables most significant 8 bits.
ENABLE L enables least significant 6 bits in case of AD2S65, 8 bits in case of AD2S66.
*Specifications same as AD2S65.
**Specifications same as AD2S65AN.
Specifications subject to change without notice.
Specifications shown in **bold face** are tested on all production units at nominal values of power supply, signal voltage and operating frequency.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply
+15 V[2] to GND . . . . . +17 V dc
−15 V[2] to GND . . . . . −17 V dc
Analog Input A_{HI} to A_{LO} (Peak) . . . . . $\pm V_{SUPPLY}$
Common Mode Range . . . . . $\pm V_{SUPPLY}$
Any Logical Input to GND . . . . . −0.4 V dc to +5.5 V dc
Case to GND . . . . . ±20 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
Extended Temperature . . . . . −55°C to +125°C
Commercial Temperature . . . . . 0 to +70°C

NOTES
[1]Absolute maximum ratings are those values beyond which damage to the device may occur.
[2]Correct polarity voltages must be maintained on the +15 V and −15 V pins.

RECOMMENDED OPERATING CONDITIONS

Power Supply
+15 V[1] . . . . . +15 V dc
−15 V[1] . . . . . −15 V dc
Analog Input[2] A_{HI} to A_{LO} . . . . . 3.4 V rms
Analog Input Frequency Range
Option X1Z . . . . . dc to 2.6 kHz
Option X2Z (Autonulling) . . . . . 50 Hz to 2.6 kHz
Option X3Z (Autonulling) . . . . . 360 Hz to 2.6 kHz
Digital Input Format . . . . . Parallel Natural Binary
Operating Temperature Range
Option 4YZ (Extended) . . . . . −55°C to +125°C
Option 5YZ (Commercial) . . . . . 0 to +70°C

NOTES
[1]Power supply tolerance (+15 V, −15 V) ±5%.
[2]The analog input voltage may vary to user's requirements from below 1 V rms to 4.2 V rms in simulation and test applications where the required output voltage is in the range of 2 V rms to 8.4 V rms (11.9 V peak).

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB AD2S65)	0.0220
15	0.0110
16 (LSB AD2S66)	0.0055

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

The power consumption of the AD2S65 and AD2S66 is particularly low by utilizing HCT series latches and only requires ±15 volt power supply rails.

An additional feature of the converters is the extended operating frequency range, dc to 10 kHz for the standard products, 50 Hz, 360 Hz to 10 kHz for the autonulling options; please see the appropriate graphs for accuracy and gain versus frequency.

Separate ENABLE inputs for the high and low bytes facilitate easy interface to any 8- or 16-bit microprocessor system bus.

The converters are housed in a 32-pin DIP solid sidewall hybrid metal package and are hermetically sealed.

MODELS AVAILABLE

The AD2S65 has a resolution of 14 bits (1.3 arc min) and is available with accuracies of ±2 and ±4 arc minutes. The AD2S66 has a resolution of 16 bits (19 arc sec) and is available with accuracies of ±1, ±2 and ±4 arc minutes. Both models operate over the frequency range dc to 2.6 kHz and with reduced accuracy to 10 kHz.

There is the autonulling option available to both models; the accuracies are the same as above, but the operating frequency range is 50 Hz to 2.6 kHz and 360 Hz to 2.6 kHz, both with reduced accuracy to 10 kHz.

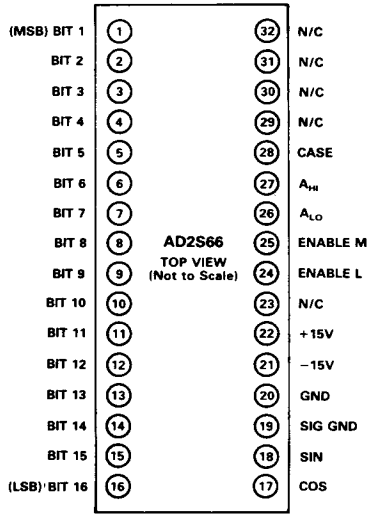
Models are available to operate over the military temperature range (−55°C to +125°C) and also the commercial temperature range (0 to +70°C).

All models are available processed with high reliability screening standards (Suffix B) which receive further levels of testing and screening to ensure high levels of reliability. More information about the option codes is given under the heading Ordering Information.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1–16	Bit 1–16 (AD2S66)	Parallel digital input angle.
1–14	Bit 1–14 (AD2S65)	Bit 15 and Bit 16 are N/C.
17	COS	Cosine signal output.
18	SIN	Sine signal output.
19	SIG GND	Output signals ground connection (0 V).
20	GND	Power supply 0 V connection.
21	−15 V	Main negative power supply.
22	+15 V	Main positive power supply.
23	N/C	No connection.
24	ENABLE L	Input latch enables the 8 (AD2S66) or 6 (AD2S65) least significant bits.
25	ENABLE M	Input latch enables the 8 most significant bits. Logic HI causes the input to appear transparent, the converter output follows the changes on the digital input. Logic LO the converter output will be latched at the level of previous digital input.
26	A_{LO}	Input pin for the reference signal.
27	A_{HI}	Input pin for the reference signal.
28	CASE	Should be connected to 0 V (GND).
29	N/C	No connection.
30	N/C	No connection.
31	N/C	No connection.
32	N/C	No connection.

PIN CONFIGURATION



NOTE: FOR AD2S65, BIT 14 IS LSB. BIT 15 AND BIT 16 ARE NOT CONNECTED.

THEORY OF OPERATION

The analog input reference voltage signal ($V_i \sin \omega t$) applied between A_{HI} (analog input HI) and A_{LO} (analog input LO), is multiplied by both $\sin\theta$ and $\cos\theta$, where θ is the angle represented by the digital input word.

The resultant resolver format output voltages at pins sin and cos are:

$V_O \sin = GV_i \sin \omega t \sin \theta$ (sine output)
$V_O \cos = GV_i \cos \omega t \cos \theta$ (cosine output).

Note: Converter Gain G is typically ×2 (input to output). There is a reduction of 1% due to autonull circuit (see relevant options). Please see specifications section and graphs of gain versus frequency.

All the signal inputs and outputs are with reference to SIG GND (Signal Ground).

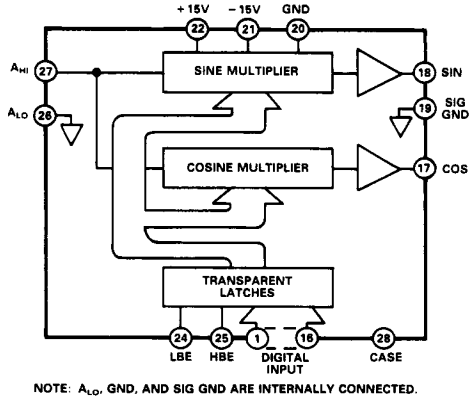


Figure 1. AD2S65/AD2S66 Functional Block Diagram

CONNECTING THE CONVERTER

The connections to the AD2S65 and AD2S66 are very straightforward.

The digital inputs should be connected to the converter using Pins 1 (MSB) through 14 (LSB) in the case of the AD2S65 and through 16 (LSB) in the case of the AD2S66. The format of the digital angular input is shown at the "Bit Weight Table" section.

The digital input control lines should be connected as described under the "Digital Data Input" section.

The analog input reference voltage (V_{REF}, A_{HI} to A_{LO}) should be connected to A_{HI}. It should be noted that this is a single ended amplifier input where A_{LO} is grounded internally (also connected to GND and SIG GND). If it is desired, the V_{REF} signal input can be externally isolated using the STM1680 or 5S72 series of reference input step down transformers.

Alternatively the analog input reference voltage, V_{REF}, can be externally resistively scaled to cater for a wide range of input voltages. Please see the section on "Resistive Input Sealing."

The CASE pin is joined to the case which is isolated and should be connected to a convenient zero potential (GND) point in the system.

The sine and cosine voltage outputs are taken from the SIN and COS pins with SIG GND as the common connection.

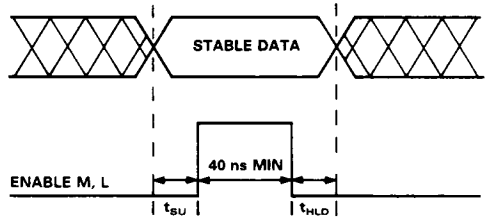
DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches are both CMOS and TTL compatible (type 54HCT373).

The ENABLE M input controls the input of the most significant 8 bits, and the ENABLE L input controls the input of the least significant 6 bits in the case of AD2S65, 8 least significant bits in the case of AD2S66.

A logic HI on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital inputs. When ENABLE M and ENABLE L are taken to a logic LO, the converter output will be latched at the SIN, COS voltage levels (angle) represented by the digital input data at the low going edge of the ENABLE L, M. The SIN, COS voltage outputs will remain constant until the ENABLE L, M are taken to a HI logic state again.

If the latches are not required, ENABLE M and ENABLE L can be left open circuit, as they are internally pulled up by 12.5 kΩ resistors. The timing diagram in Figure 2 illustrates the use of ENABLE M and ENABLE L control inputs.



NOTE: INTERNAL LATCHES ARE TYPE 54HCT373.

Figure 2. Data Transfer Diagram

Internal resistive pull ups are employed only on the ENABLE M, ENABLE L digital inputs and are not necessary for the digital control angular data inputs as the HCT series latches are both TTL and CMOS compatible.

DEGRADATION OF ACCURACY OVER FREQUENCY

The AD2S65 and AD2S66 have guaranteed accuracies as stated in the specifications section from dc to 2.6 kHz and 50 Hz, 360 Hz to 2.6 kHz for the autonull options. However all devices operate satisfactorily to 10 kHz with reduced accuracy.

Figure 3 represents typically the angular accuracy degradation over the range of frequencies dc to 10 kHz for the standard part (Option X1Z) and the autonull parts (Options X2Z and X3Z).

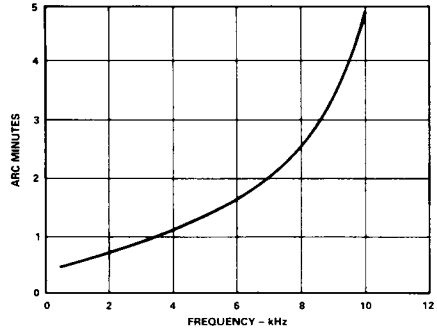


Figure 3. Accuracy vs. Frequency

GAIN VARIATION OVER FREQUENCY

The gain (input to output SIN, COS voltages) of the standard part is ×2 ±0.1% (Option X1Z) over the frequency range dc to 2.6 kHz. As can be seen from Figure 4, the gain at 10 kHz is ×2.02 ±0.1%.

2.6 kHz. From Figure 4 can be seen that the gain for the autonull part is typically ×2 + 0.1% at 10 kHz.

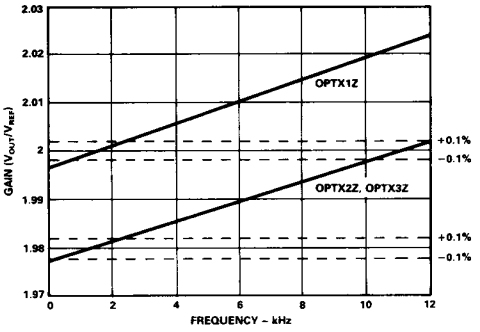


Figure 4. Gain (V_{SIN}, V_{COS}/V_{REF}) vs. Frequency

VECTOR ERRORS AND EFFECTS

The error law used in the converter has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the internal components used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays and resolver-to-digital converter testing.

BANDWIDTH

The dynamic characteristics of the AD2S65 and AD2S66, including the autonulling option, have been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6 kHz, 50 Hz, 360 Hz to 2.6 kHz for the autonulling options. This results in a closed loop bandwidth of 300 kHz.

DEGLITCHING THE CONVERTERS

The AD2S65 and AD2S66 are fundamentally digital to analog converters and can, therefore, produce glitches on the output at the major transition points of the digital angular input. For most applications these glitches can be removed by simple smoothing circuits on the outputs. However, in applications where the smoothing is not an acceptable solution sample and hold amplifiers such as the Analog Devices type AD582 can be used to remove the glitches.

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of input/output voltages.

A resistance of value 3 kΩ per extra volt required (in excess of 3.4 V rms) should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI} to A_{LO}) does not exceed 4.2 V rms (8.4 V rms, 11.9 V peak at SIN, COS outputs) otherwise clipping may occur due to lack of voltage supply headroom for the internal output amplifiers.

The recommended input is 3.4 V rms for a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and therefore the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} input pins.

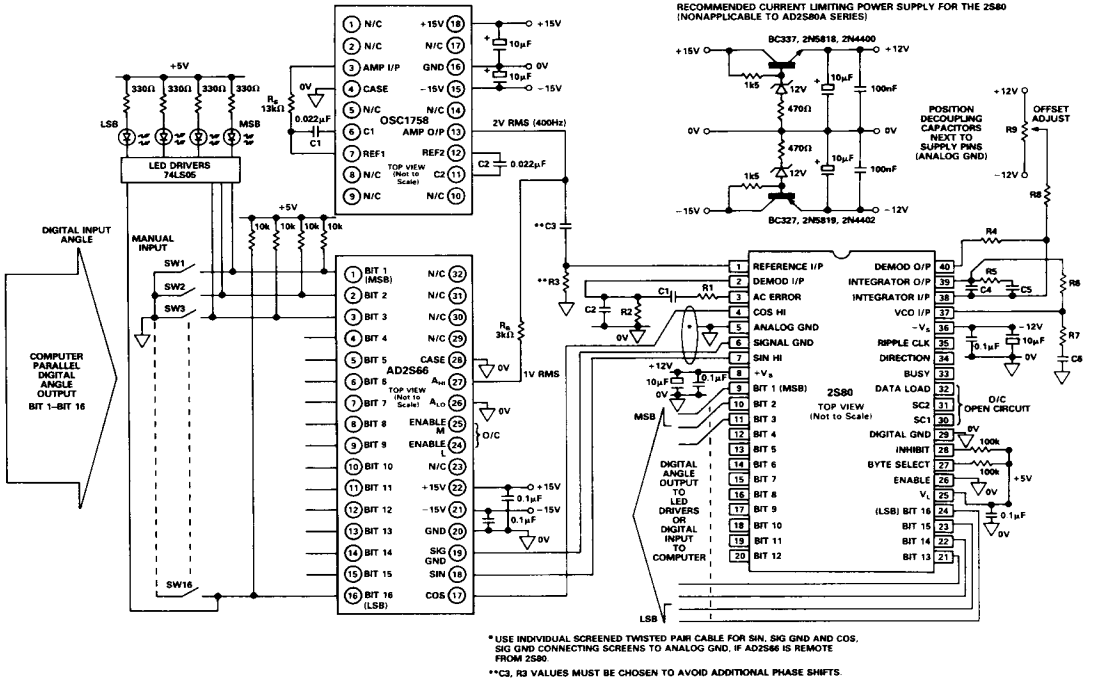


Figure 5. Application Circuit: Resolver-to-Digital Converter (2S80) Testing Using the AD2S66

APPLICATION

The diagram Figure 5 shows a "hookup" for resolver-to-digital converter testing, with the digital-to-resolver converter (AD2S66), power oscillator (OSC1758) and the resolver-to-digital converter (2S80). Using a similar circuit, 2S81, 2S82, 1S20, 1S40, 1S60, 1S24, 1S44, 1S64 and 1S74 R/D converters can be tested.

Current Set Resistor (R_S)

This resistor is used to reduce the voltage output of the oscillator to 2 V rms so it can be used as the reference input to the 2S80.

$$R_S = \frac{37.5 \times 10^3}{V_{OUT\ (rms)}} - 5350\ \Omega$$

for 2 V rms output R_S = 13 k Ohms

Frequency of Oscillation

The frequency of oscillation for the OSC1758 is determined by the two external capacitors, C1 and C2. These should be calculated as follows:

$$C1 = C2 = \frac{1}{F_{OSC} \times 10^5}\ F$$

where F_{OSC} = frequency of oscillation in Hz for 400 Hz frequency C1 = C2 = 0.022 μF.

Decoupling

The DRC and oscillator have internal high frequency decoupling capacitors on the supply lines. However, it is recommended that electrolytic decoupling capacitors are connected close to the hybrid power supply pins. Please see decoupling recommendations in relevant data sheets.

Circuit Description

The OSC1758 generates 2 V rms, of nominal frequency 400 Hz, to be applied at the REFERENCE I/P of the 2S80. The signal is further attenuated by resistor R_B and applied to A_{HI} input of the AD2S66 (V_{REF}) which generates SIN and COS signals, as per digital input angle, at 400 Hz.

The digital input angle can be set either manually by selection of the switches SW1 (MSB) to SW16 (LSB) or by the digital parallel outputs of a computer or by means of a 16-bit counter which consists of 74LS193 and driven by a square wave oscillator. The digital input angle may be displayed, if so desired, by means of LEDs and visually compared with the digital outputs of the 2S80 RDC also displayed by LEDs.

Alternatively, the digital angle position outputs of the 2S80 may be connected to a 16-bit parallel input port of a computer, which can compare digital input angle to digital output angle and compute the error.

2S80 R-to-D Converter External Components

Please consult the appropriate date sheet as the external components which set the dynamic performance characteristics of the converter are user selectable. There is available, on request, PC compatible software to help users select the optimum values of the external components for the desired application.

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217E, Figure 6 shows the MTBF in hours versus case temperature in naval sheltered conditions for AD2S65/AD2S66.

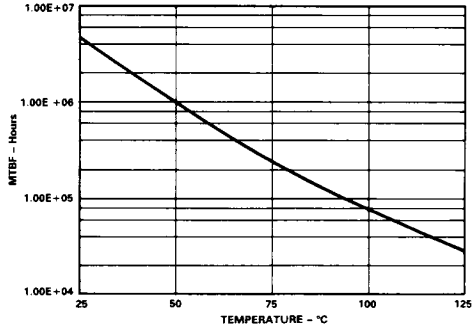


Figure 6. AD2S65/AD2S66 MTBF Curve

OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The DRC1745 (14 bit) and DRC1746 (16 bit) are hybrid resolver-to-digital converters with internal power amplifiers capable of driving a 2 VA load.

The STM1683 series are output transformers used in conjunction with the DRC1745 and DRC1746, operate over the frequency range of 360 Hz to 2.6 kHz and can be Scott T connected to provide all the standard synchro output formats over the frequency range dc to 2.6 kHz.

The 2S80 and 2S82 are monolithic, variable resolution 10-, 12-, 14- and 16-bit tracking resolver-to-digital converters that feature user selectable dynamic performance and operate over the reference frequency range 50 Hz to 20 kHz, with accuracies of ±2, ±4, ±8 arc min (2S80 and 2S82) and 22 arc min (2S82).

The 2S81 is a low cost, monolithic tracking resolver-to-digital converter with fixed 12-bit resolution, user selectable dynamic performance over the frequency range 50 Hz to 20 kHz and accuracy 30 arc min.

The AD2S75 is a transformer isolated universal synchro and resolver pin programmable interface. All standard synchro and resolver signal and reference voltages are accepted and transformed to 2 V rms, resolver format signals for use with the 2S80 series monolithic resolver-to-digital converters.

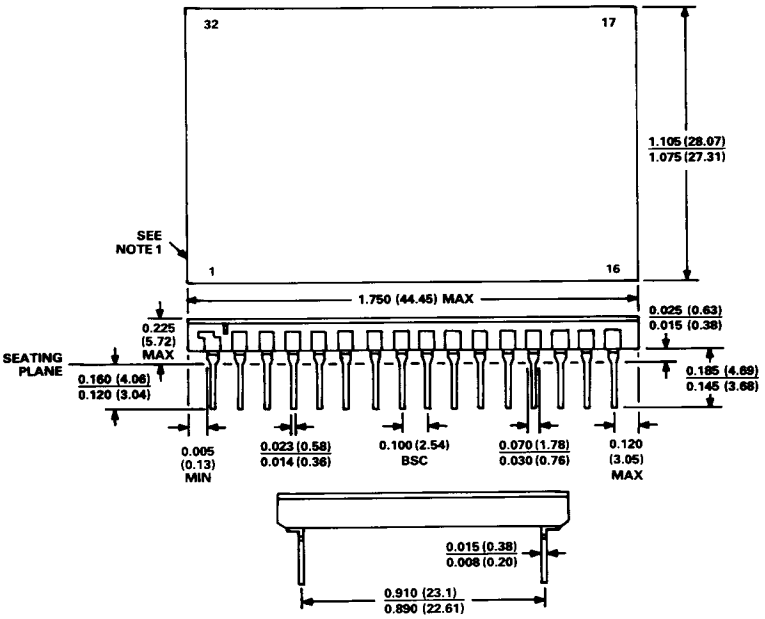
The 1740 series are hybrid 14- or 12-bit continuous tracking synchro or resolver-to-digital converters featuring internal microtransformers for signal isolation.

The OSC1758 is an excitation oscillator for supplying reference signals to synchros, resolvers and Inductosyns* and associated converters.

*Inductosyn is a registered trademark of Farrand Industries, Inc.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.

AD2S6N/ X Y Z B

- B — High-Rel Processing (Applicable X = 4)
- Z = 1 ±1 arc min Accuracy (AD2S66 Only)
- Z = 2 ±2 arc min Accuracy
- Z = 4 ±4 arc min Accuracy
- Y = 1 Bandwidth dc–2.6 kHz
- Y = 2 Bandwidth 50 Hz–2.6 kHz (Autonull Option)
- Y = 3 Bandwidth 360 Hz–2.6 kHz (Autonull Option)
- X = 4 −55°C to +125°C Operating Temperature Range
- X = 5 0 to +70°C Operating Temperature Range
- AD2S65 = 14-Bit Resolution, Accuracy Z = ±2, ±4 arc min
- AD2S66 = 16-Bit Resolution, Accuracy Z = ±1, ±2, ±4 arc min