REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30			
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-02-28

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 1 MEG X 16 DRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96743**

SHEET 1 OF 30

DESC FORM 193
JUL 94

9004708 0019719 078

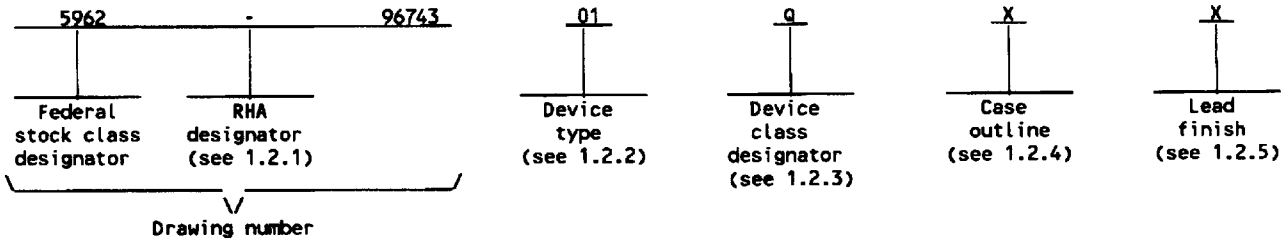
5962-E335-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	416160-80	1 MEG-word by 16-bit DRAM, 32 ms refresh	80 ns
02	416160-70	1 MEG-word by 16-bit DRAM, 32 ms refresh	70 ns
03	418160-80	1 MEG-word by 16-bit DRAM, 8 ms refresh	80 ns
04	418160-70	1 MEG-word by 16-bit DRAM, 8 ms refresh	70 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	50	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Voltage range on V_{CC}	-1 V dc to +7 V dc
Voltage range on any pin	-1 V dc to +7 V dc
Short circuit output current	+50 mA
Maximum power dissipation (P_D)	1 W
Operating free-air temperature range T_A	-55°C to +125°C
Storage temperature range T_{stg}	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values in this drawing are with respect to V_{SS}.

Thermal resistance, junction-to-case (θ_{JC})	
Case outline X	5°C/W 3/
Junction temperature (T_J) 4/	+175°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Supply voltage (V_{SS})	0 V dc
High-level input voltage (V_{IH})	+2.4 V dc minimum to +6.5 V dc maximum
Low-level input voltage (V_{IL}) 5/	-1.0 V dc minimum to +0.8 V dc maximum
Transition time (t_T)	3 ns minimum to 30 ns maximum
Operating free-air temperature range (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3/ When the thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this drawing for logic voltage levels only.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	I_{OH} = -5 mA, V_{IL} = 0.8 V V_{IH} = 2.4 V	1,2,3	All	2.4		V
Low-level output voltage	V_{OL}	I_{OL} = 4.2 mA, V_{IL} = 0.8 V V_{IH} = 2.4 V	1,2,3	All		0.4	V
Input leakage current	I_I	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}	1,2,3	All		±10	µA
Output leakage current	I_O	V_{CC} = 5.5 V, $\overline{CASx}$ high, V_O = 0 V to V_{CC}	1,2,3	All		±10	µA
Average operating power supply current (Random read or write cycle)	I_{CC1}	V_{CC} = 5.5 V, Minimum cycle time, outputs open Measured with a maximum of one address change while $\overline{RAS}$ = 0.8 V	1,2,3	01		70	mA
				02		80	
				03		170	
				04		180	
Standby power supply current	I_{CC2}	V_{CC} = 5.5 V After one memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high TTL V_{IH} = 2.4 V	1,2,3	All		2	mA
		CMOS $V_{IH} = V_{CC}$-0.2 V	1,2,3	All		1	
Average operating power supply current ($\overline{RAS}$ only refresh, or CBR)	I_{CC3}	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CASx}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CASx}$ low (CBR) Measured with a maximum of one address change while $\overline{RAS}$ = 0.8 V	1,2,3	01		70	mA
				02		80	
				03		170	
				04		180	
Average operating power supply current (Page mode)	I_{CC4}	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CASx}$ cycling, outputs open Measured with a maximum of one address change while $\overline{CASx}$ = 2.4 V	1,2,3	01		70	mA
				02		80	
				03		170	
				04		180	
Standby power supply current (outputs enabled)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CASx}$ = V_{IL}, Data out is enabled, outputs open Measured with a maximum of one address change while $\overline{CASx}$ = 2.4 V	1,2,3	All		5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance, address inputs A0-A11	$C_{i(A)}$	f = 1 MHz, See 4.4.1e, Bias on pins under test = 0 V, all other pins are open T_A = 25°C	4	All		8	pF
Input capacitance, $\overline{OE}$	$C_{i(OE)}$		4	All		8	pF
Input capacitance, $\overline{CASx}$ and $\overline{RAS}$	$C_{i(RC)}$		4	All		8	pF
Input capacitance, $\overline{W}$	$C_{i(W)}$		4	All		8	pF
Output capacitance	C_O		4	All		10	pF
Functionals		See 4.4.1c	7,8A,8B	All			
Access time from column address	t_{AA}	See figures 4 and 5 1/ 2/	9,10,11	01,03		40	ns
				02,04		35	
Access time from $\overline{CASx}$ low	t_{CAC}		9,10,11	01,03		20	ns
				02,04		18	
Access time from column precharge	t_{CPA}		9,10,11	01,03		45	ns
				02,04		40	
Access time from $\overline{RAS}$ low	t_{RAC}		9,10,11	01,03		80	ns
				02,04		70	
Access time from $\overline{OE}$ low	t_{OEA}		9,10,11	01,03		20	ns
				02,04		18	
Output disable time after $\overline{CASx}$ high 3/	t_{OFF}		9,10,11	01,03		20	ns
				02,04		18	
Output disable time after $\overline{OE}$ high 3/	t_{OEZ}		9,10,11	01,03		20	ns
				02,04		18	
Cycle time, read 2/	t_{RC}		9,10,11	01,03	150		ns
				02,04	130		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Cycle time, write 2/	t_{WC}	See figures 4 and 5 1/ 2/	9,10,11	01,03	150		ns
				02,04	130		
Cycle time, read-write 2/	t_{RWC}		9,10,11	01,03	205		ns
				02,04	181		
Cycle time, page-mode read or write 2/ 4/	t_{PC}		9,10,11	01,03	50		ns
				02,04	45		
Cycle time, page-mode read-write 2/	t_{PRWC}		9,10,11	01,03	105		ns
				02,04	96		
Pulse duration, page mode, $\overline{RAS}$ low 5/	t_{RASP}		9,10,11	01,03	80		ns
				02,04	70		
				All		100	µs
Pulse duration, non-page-mode, $\overline{RAS}$ low 5/	t_{RAS}		9,10,11	01,03	80		ns
				02,04	70		
				All		10	µs
Pulse duration, $\overline{CASx}$ low 6/	t_{CAS}		9,10,11	01,03	20		ns
				02,04	18		
				All		10	µs
Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}		9,10,11	01,03	60		ns
				02,04	50		
Pulse duration, $\overline{W}$ low	t_{WP}		9,10,11	All	10		ns
Setup time, column address before $\overline{CASx}$ low	t_{ASC}		9,10,11	All	0		ns
Setup time, row address before $\overline{RAS}$ low	t_{ASR}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, data 7/	t_{DS}	(See figures 4 and 5) 1/ 2/	9,10,11	All	0		ns
Setup time, $\overline{W}$ high before $\overline{CASx}$ low	t_{RCS}		9,10,11	All	0		ns
Setup time, $\overline{W}$ low before $\overline{CASx}$ high	t_{CWL}		9,10,11	01,03	20		ns
				02,04	18		
Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}		9,10,11	01,03	20		ns
				02,04	18		
Setup time, $\overline{W}$ low before $\overline{CASx}$ low (Early-write operation only)	t_{WCS}		9,10,11	All	0		ns
Hold time, column address after $\overline{CASx}$ low	t_{CAH}		9,10,11	All	15		ns
Hold time, data 7/	t_{DH}		9,10,11	All	15		ns
Hold time, row address after $\overline{RAS}$ low	t_{RAH}		9,10,11	All	10		ns
Hold time, $\overline{W}$ high after $\overline{CASx}$ high 8/	t_{RCH}		9,10,11	All	0		ns
Hold time, $\overline{W}$ high after $\overline{RAS}$ high 8/	t_{RRH}		9,10,11	All	0		ns
Hold time, $\overline{W}$ low after $\overline{CASx}$ low (Early-write operation only)	t_{WCH}		9,10,11	All	15		ns
Hold time, $\overline{CASx}$ low to $\overline{CASx}$ high	t_{CLCH}		9,10,11	All	5		ns
Hold time, $\overline{RAS}$ high from $\overline{CASx}$ precharge	t_{RHCP}		9,10,11	01,03	45		ns
				02,04	40		
Hold time, $\overline{OE}$ command	t_{OEH}		9,10,11	01,03	20		ns
				02,04	18		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	t_{ROH}	See figures 4 and 5 1/ 2/	9,10,11	All	10		ns
Delay time, $\overline{CASx}$ high (precharge)	t_{CP}		9,10,11	All	10		ns
Delay time, column address to $\overline{W}$ low (Read-write operation only)	t_{AWD}		9,10,11	01,03	70		ns
				02,04	63		
Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high (CBR refresh only)	t_{CHR}		9,10,11	All	10		ns
Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low	t_{CRP}		9,10,11	All	5		ns
Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high	t_{CSH}		9,10,11	01,03	80		ns
				02,04	70		
Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (CBR refresh only)	t_{CSR}		9,10,11	All	5		ns
Delay time, $\overline{CASx}$ low to $\overline{W}$ low (Read-write operation only)	t_{CWD}		9,10,11	01,03	50		ns
				02,04	46		
Delay time, $\overline{OE}$ to data	t_{OED}		9,10,11	01,03	20		ns
				02,04	18		
Delay time, $\overline{RAS}$ low to column address 9/	t_{RAD}		9,10,11	01,03	15	40	ns
				02,04	15	35	
Delay time, column address to $\overline{RAS}$ high	t_{RAL}		9,10,11	01,03	40		ns
				02,04	35		
Delay time, column address to $\overline{CASx}$ high	t_{CAL}		9,10,11	01,03	40		ns
				02,04	35		
Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low 9/	t_{RCD}		9,10,11	01,03	20	60	ns
				02,04	20	52	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low	t_{RPC}	See figures 4 and 5 1/ 2/	9,10,11	All	0		ns
Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high	t_{RSH}		9,10,11	01,03	20		ns
				02,04	18		
Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	t_{RWD}		9,10,11	01,03	110		ns
				02,04	98		
Delay time, $\overline{W}$ low after $\overline{CASx}$ precharge (read-write operation only)	t_{CPW}		9,10,11	01,03	75		ns
				02,04	68		
Refresh time interval	t_{REF}		9,10,11	01,02		32	ms
				03,04		8	

1/ An initial pause of 200 µs is required after power-up followed by a minimum of 8 initialization cycles after full V_{CC} level is achieved. The 8 initialization cycles need to be $\overline{RAS}$ only refresh or CBR to assure proper device operation. The 8 initialization cycles should be repeated any time the refresh requirement is exceeded.

2/ All cycle times assume transition time t_T = 5 ns, referenced to V_{IH} (min) and V_{IL} (max).

3/ t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled (high impedance) by bringing either $\overline{OE}$ or $\overline{CASx}$ high.

4/ To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

5/ In a read-write cycle, t_{RWD} and t_{RWL} must be observed.

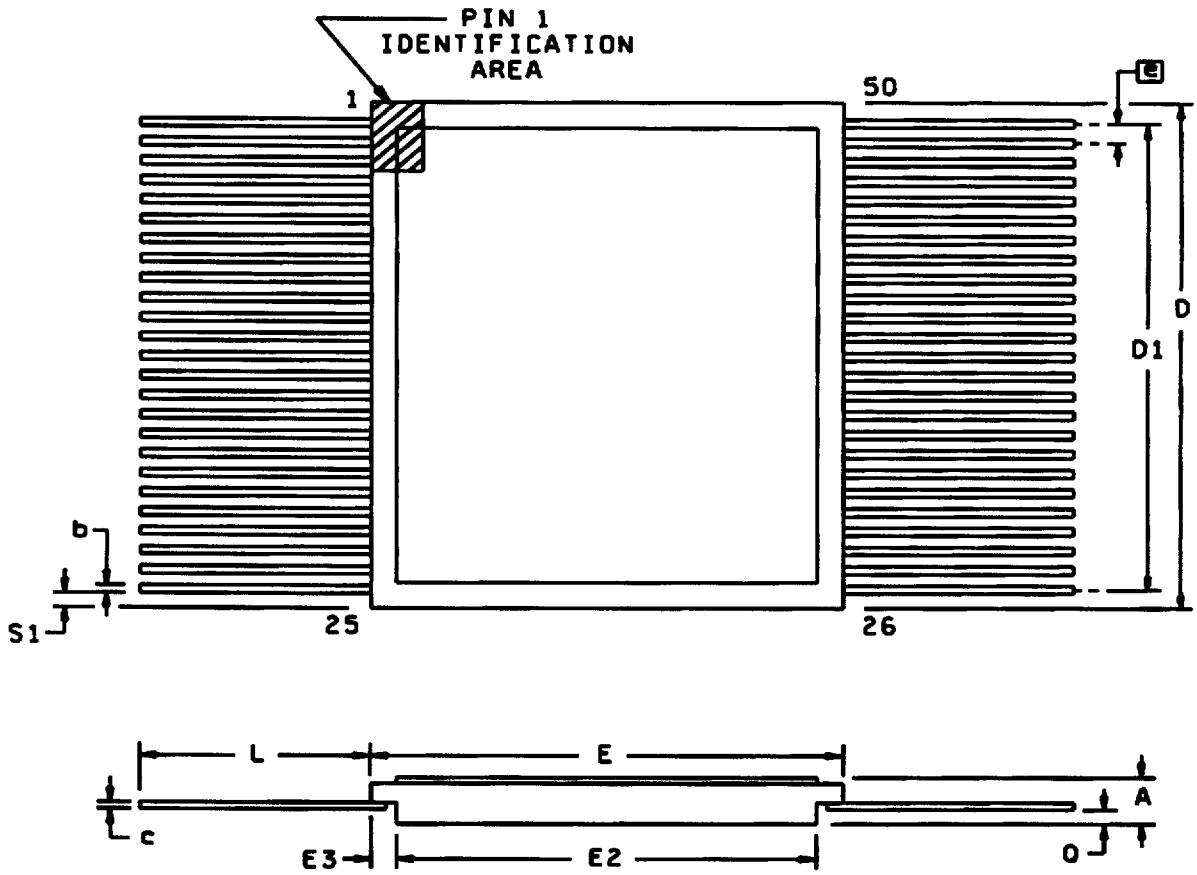
6/ In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

7/ Referenced to the later of $\overline{CASx}$ or $\overline{W}$ in write operations.

8/ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

9/ Maximum value specified only to guarantee access time.

Case X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.80	3.55	.110	.140
b	0.30	0.50	.012	.020
c	0.10	0.23	.004	.009
D	20.60	21.40	.811	.842
D1	18.95	19.45	.746	.766
E	16.10	16.90	.634	.665
E2	14.10	14.90	.555	.587
E3	0.76	---	.030	---
e	0.80 BSC		.031 BSC	
L	6.35	9.40	.250	.370
Q	0.66	---	.026	---
S1	0.38	---	.015	---

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline.

Device types	01, 02, 03, and 04		
Case outlines	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	26	V_{SS}
2	DQ0	27	A4
3	DQ1	28	A5
4	DQ2	29	A6
5	DQ3	30	A7
6	V_{CC}	31	A8
7	DQ4	32	A9
8	DQ5	33	$\overline{OE}$
9	DQ6	34	$\overline{CASU}$
10	DQ7	35	$\overline{CASL}$
11	NC	36	NC
12	NC	37	NC
13	NC	38	NC
14	NC	39	NC
15	NC	40	NC
16	NC	41	DQ8
17	$\overline{W}$	42	DQ9
18	$\overline{RAS}$	43	DQ10
19	A11 1/	44	DQ11
20	A10 1/	45	V_{SS}
21	A0	46	DQ12
22	A1	47	DQ13
23	A2	48	DQ14
24	A3	49	DQ15
25	V_{CC}	50	V_{SS}

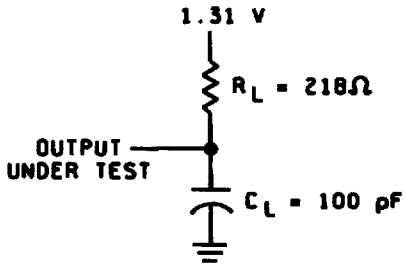
1/ A10 and A11 are NC for devices 03 and 04.

FIGURE 2. Terminal connections.

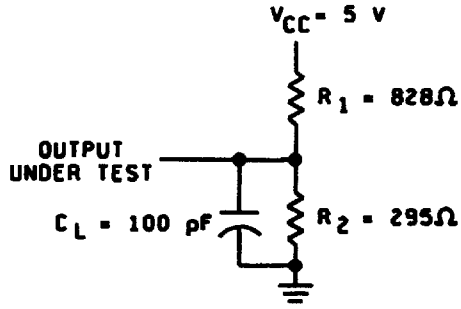
Operation	Inputs						Input/Output	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	D	Q
Read	ACT	ACT	NAC	ACT	APD	APD	NAC	VLD
Write (early write)	ACT	ACT	ACT	DNC	APD	APD	APD	ILD
Write (late write)	ACT	ACT	ACT	NAC	APD	APD	APD	ILD
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN
Hidden refresh (read)	ACT	ACT	NAC	ACT	APD	APD	NAC	VLD
Hidden refresh (write)	ACT	ACT	ACT	DNC	APD	APD	APD	DNC
CAS before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN
Standby	NAC	NAC	DNC	DNC	DNC	DNC	DNC	OPN

ACT = active
NAC = nonactive
DNC = don't care
VLD = valid
ILD = invalid
APD = applied
OPN = open

FIGURE 3. Truth table.



(a) LOAD CIRCUIT

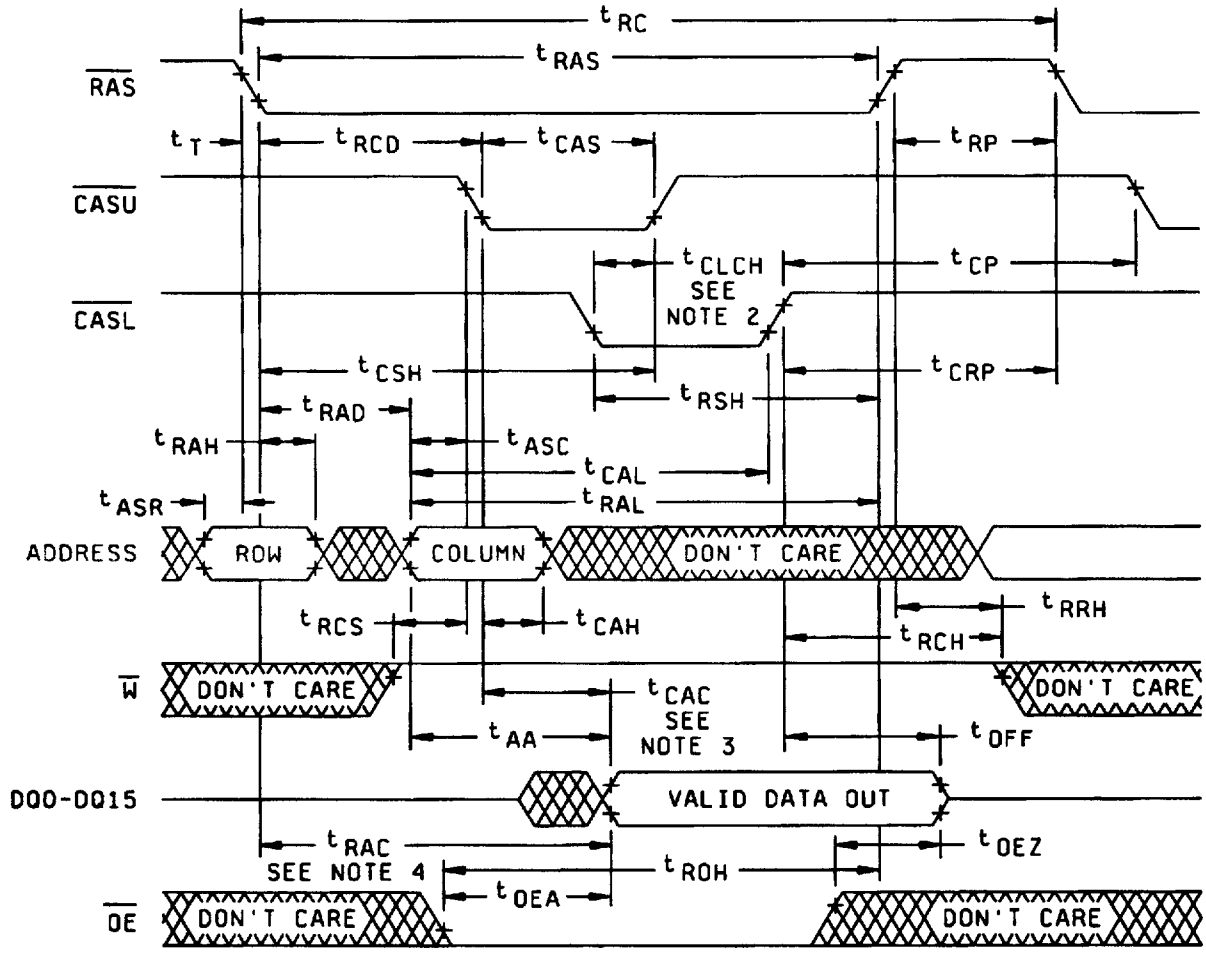


(b) ALTERNATE LOAD CIRCUIT

NOTE: The ac timing parameters are specified with reference to the minimum valid high-level voltage and the maximum valid low-level voltage for each signal. This corresponds to 2.4 V and 0.8 V for inputs; 2.4 V and 0.4 V for outputs with the given load circuit.

FIGURE 4. Load circuit and voltage waveforms.

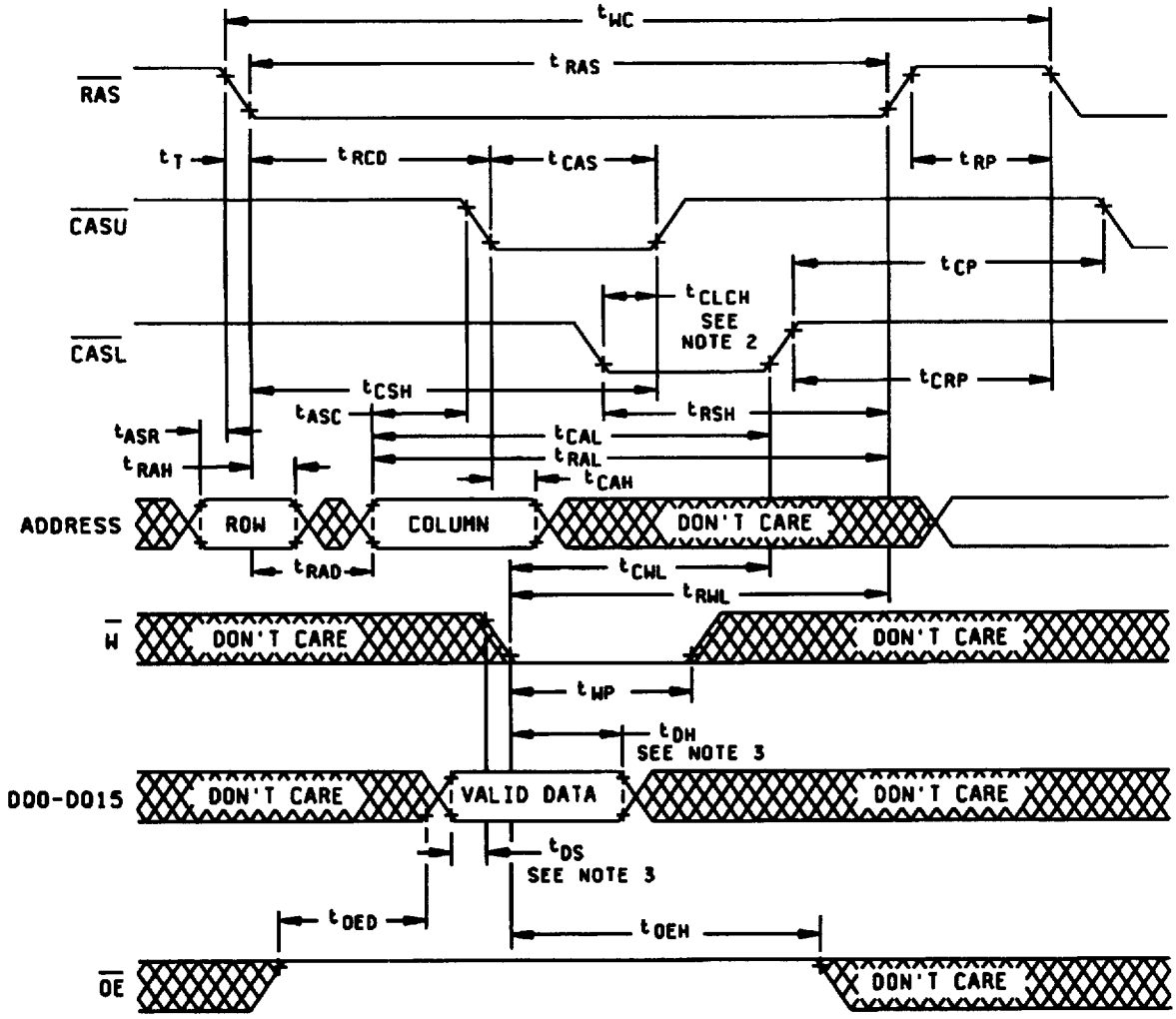
READ CYCLE
SEE NOTE 1



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
3. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
4. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

FIGURE 5. Timing waveforms.

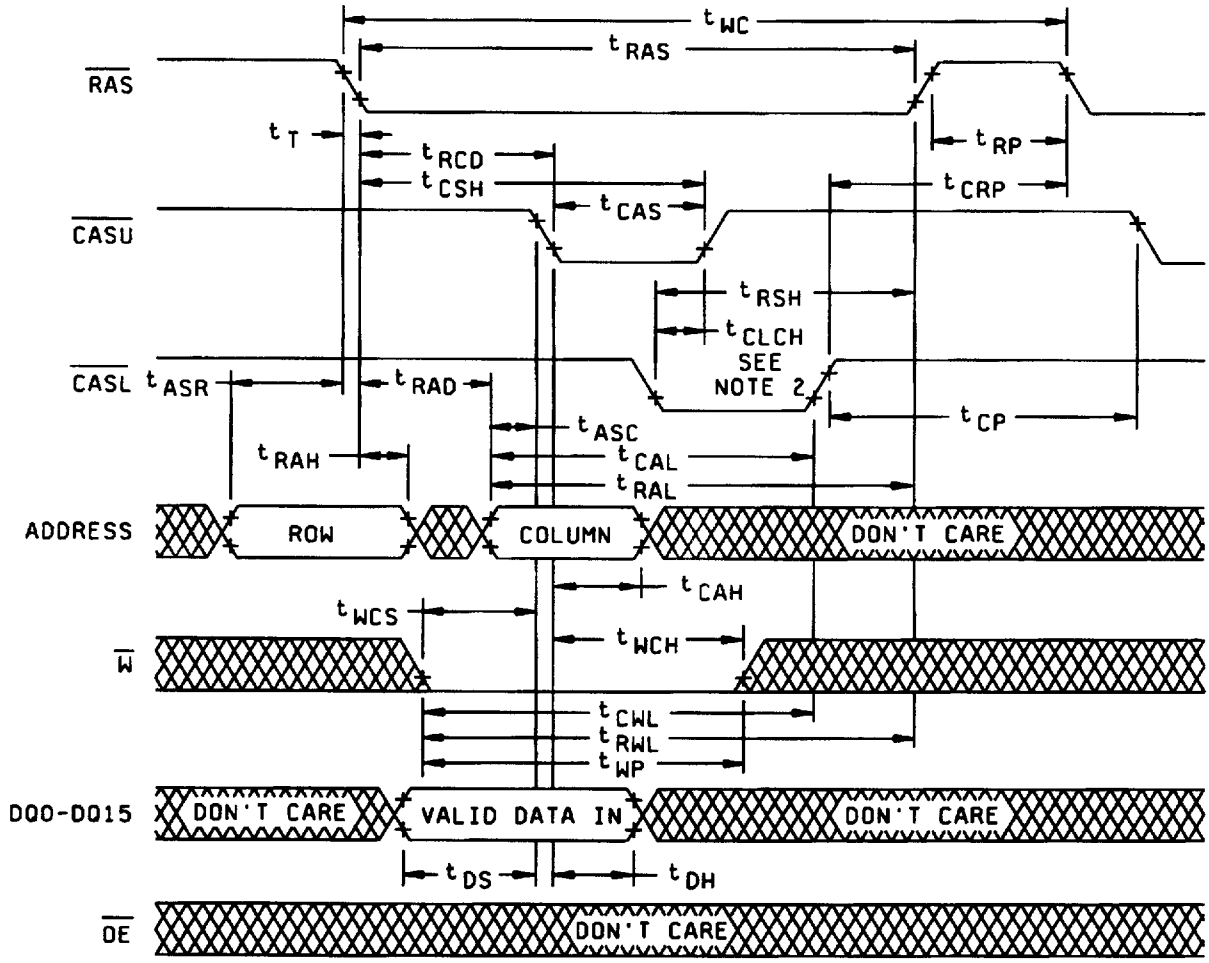
WRITE CYCLE
SEE NOTE 1



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
3. Referenced to the first $\overline{CASx}$ or $\overline{W}$, whichever occurs last.

FIGURE 5. Timing waveforms - Continued.

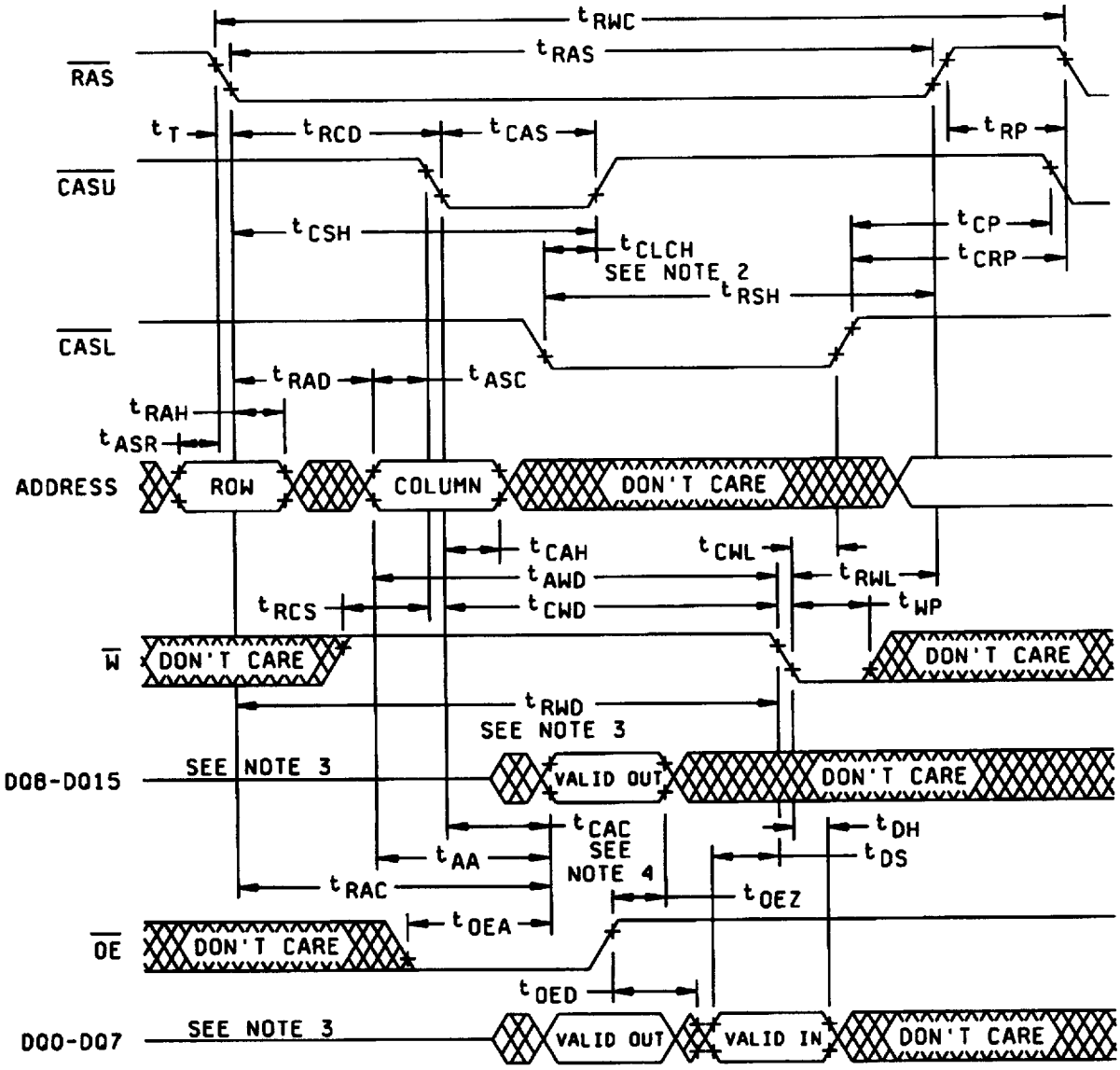
EARLY-WRITE-CYCLE
SEE NOTE 1



NOTES:
1. CASx order is arbitrary.
2. To hold the address latched by the first CASx going low, the parameter t_{CLCH} must be met.

FIGURE 5. Timing waveforms - Continued.

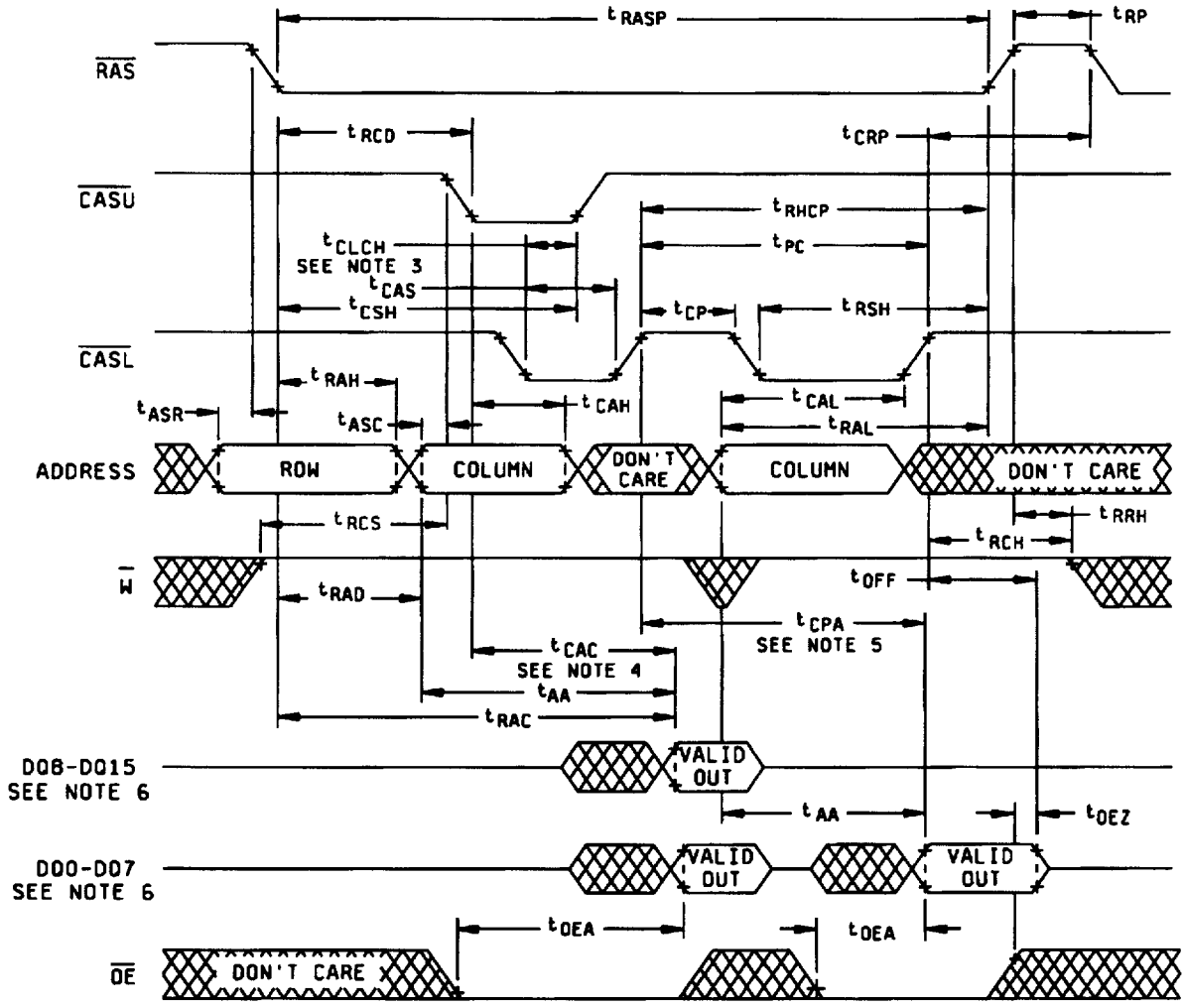
READ-MODIFY-WRITE-CYCLE
SEE NOTE 1



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
3. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
4. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.

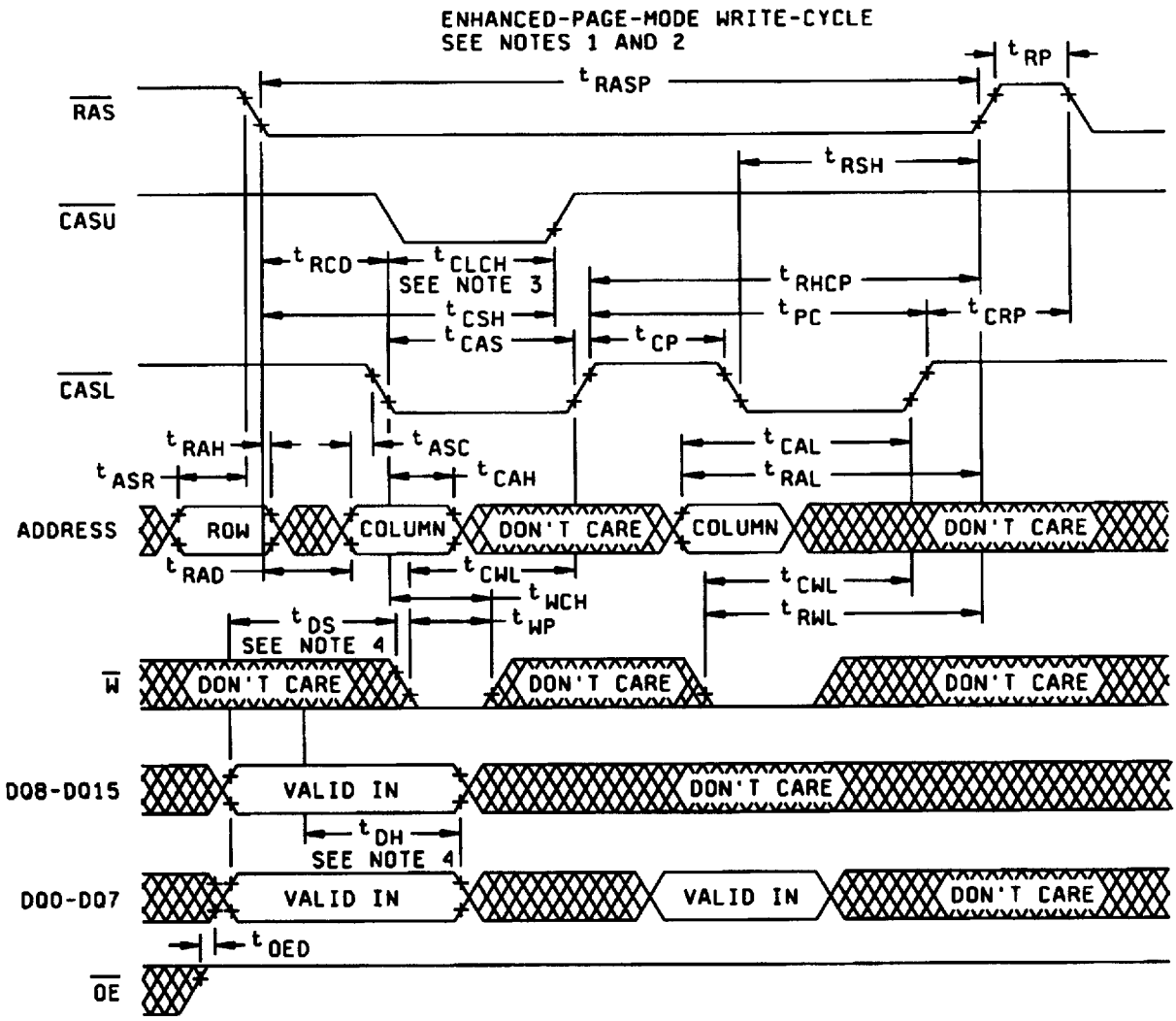
FIGURE 5. Timing waveforms - Continued.

ENHANCED-PAGE-MODE READ-CYCLE
SEE NOTES 1 AND 2



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
3. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
4. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
5. Access time is t_{CPA} or t_{AA} dependent.
6. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

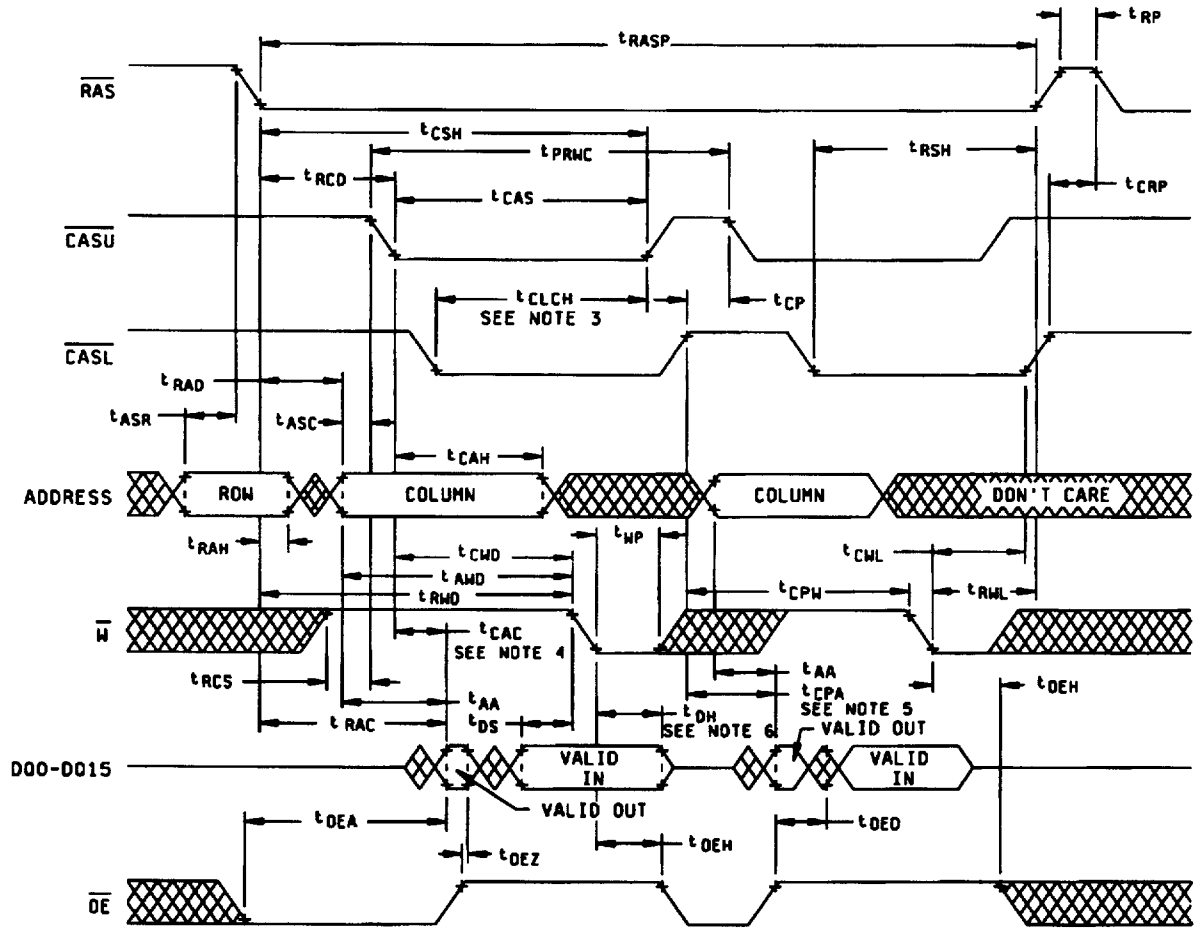
FIGURE 5. Timing waveforms - Continued.



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write-timing specifications are not violated.
3. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
4. Referenced to the first $\overline{CASx}$ or $\overline{W}$, whichever occurs last.

FIGURE 5. Timing waveforms - Continued.

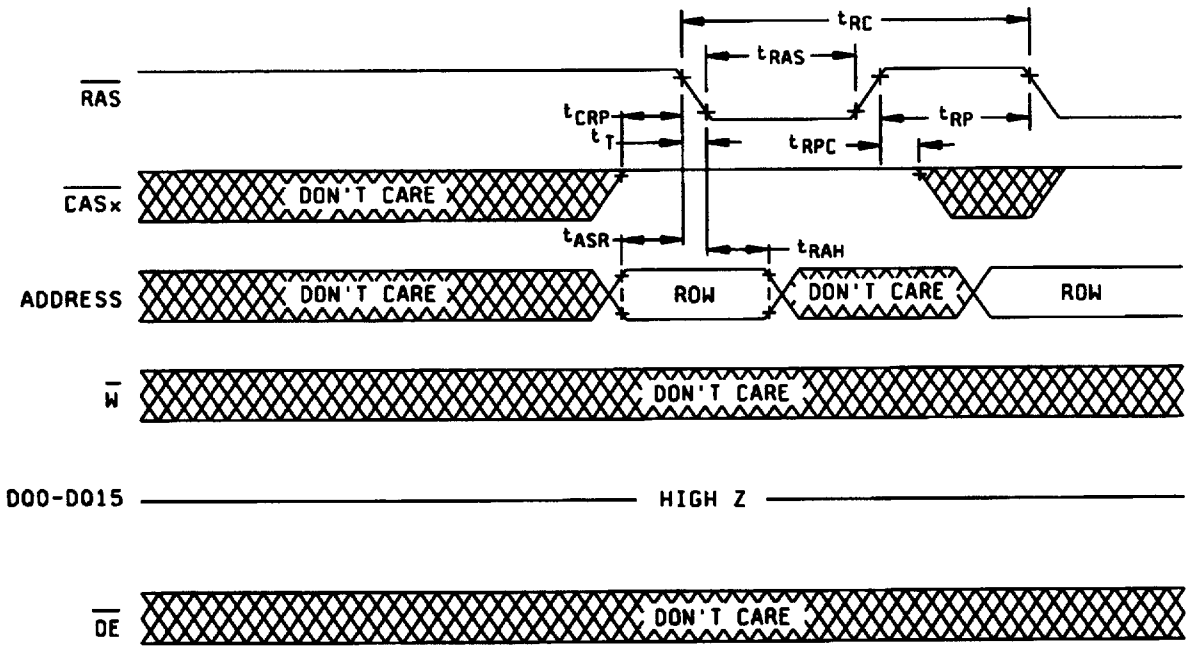
ENHANCED-PAGE-MODE READ-MODIFY-WRITE-CYCLE
SEE NOTES 1 AND 2



NOTES:
1. $\overline{CASx}$ order is arbitrary.
2. A read or write cycle can be mixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
3. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
4. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
5. Access time is t_{CPA} or t_{AA} dependent.
6. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

FIGURE 5. Timing waveforms - Continued.

RAS-ONLY REFRESH-CYCLE
SEE NOTE



NOTE: All $\overline{CASx}$ must be high.

FIGURE 5. Timing waveforms - Continued.

HIDDEN-REFRESH-CYCLE

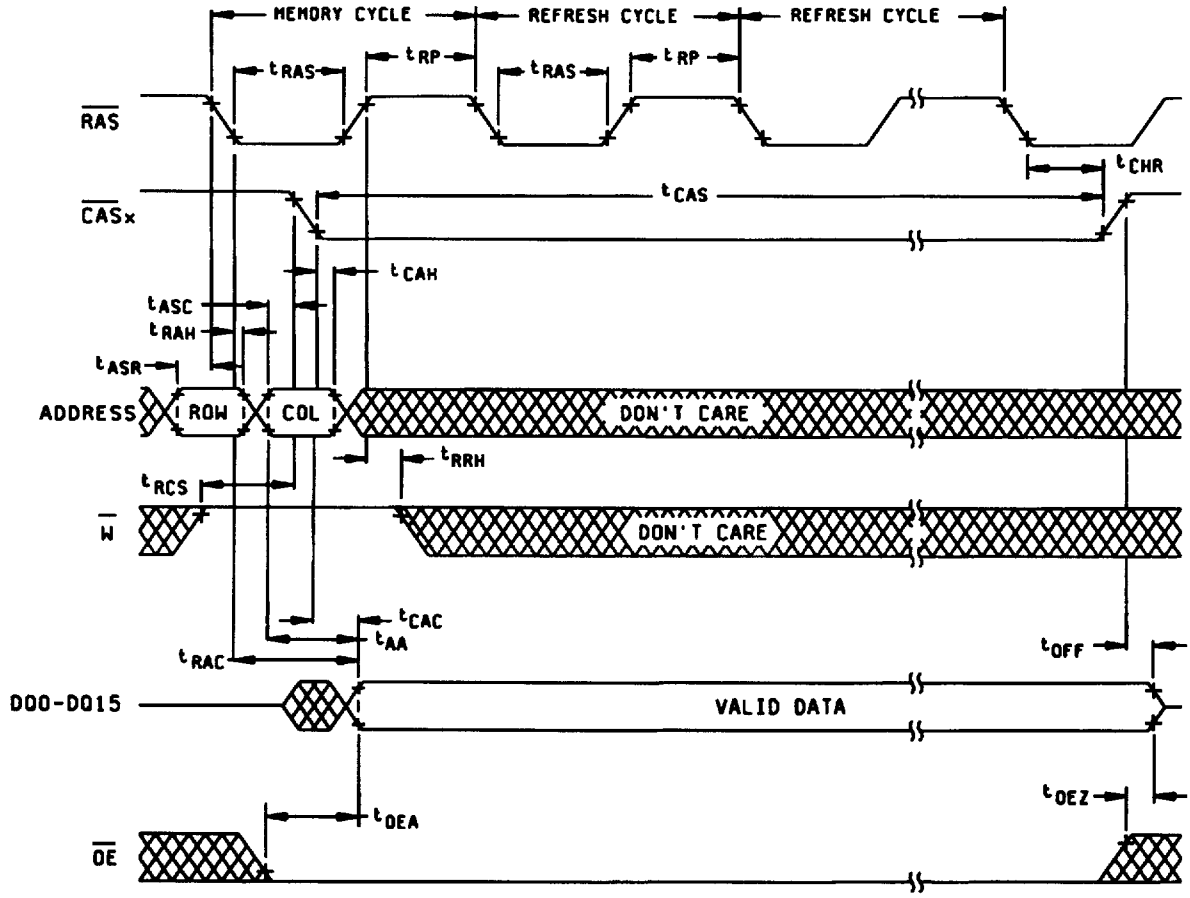
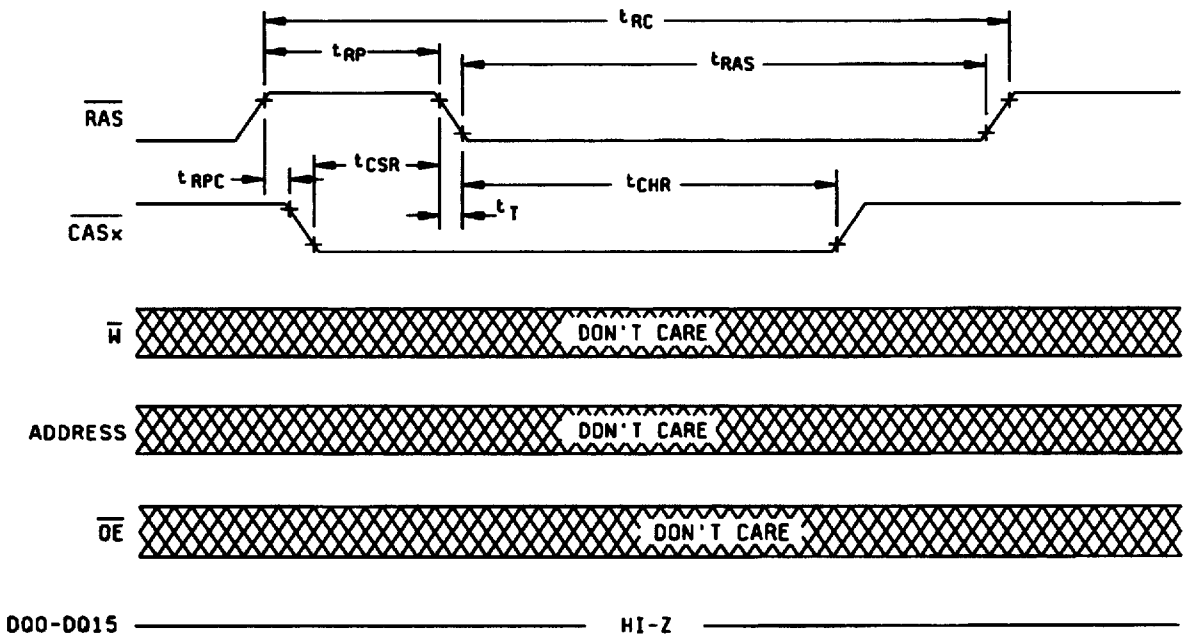


FIGURE 5. Timing waveforms - Continued.

AUTOMATIC xCBR REFRESH-CYCLE
SEE NOTE



NOTE: Any $\overline{CASx}$ can be used.

FIGURE 5. Timing waveforms - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device classes Q and V, performance of delta limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition A or D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high

T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
V_{SS}	Ground zero voltage potential.
V_{IC}	Positive input clamp voltage
O/V	Latch-up over-voltage
O/I	Latch-up over-current
A0-A11	Address inputs
DQ0-DQ11	Data In/Data Out
$\overline{CASL}$	Lower Column-Address Strobe
$\overline{CASU}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance (t_{OFF}). This pattern verifies the output buffer switches to high impedance (three-state) within the specified t_{OFF} after the rise of CAS. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise CAS and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after t_{OFF} delay.

30.2 Algorithm B (pattern 2).

30.2.1 V_{CC} slew). This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with V_{CC} at 5.0 V.
Step 3: Change V_{CC} to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change V_{CC} to 4.5 V.
Step 7: Read memory with background data complement.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause t_{REF} (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2 through 4 with data complement.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 2 and 3 using data complement.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with background data using Page mode cycle.
Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
Step 5: Repeat steps 2 through 4 for remaining memory locations.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause for t_{REF} (stop all clocks).
Step 4: Perform 4096 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles for device types 01 and 02 and 1024 for device types 03 and 04, while attempting to modify data.
Step 5: Read memory with background data.

30.8 Algorithm H (pattern 8).

30.8.1 $\overline{\text{RAS}}$-only refresh test. This test is used to verify the functionality of the $\overline{\text{RAS}}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause for t_{REF} (stop all clocks).
Step 4: Perform 4096 $\overline{\text{RAS}}$-only cycles for device types 01 and 02 and 1024 for device types 03 and 04, while attempting to modify data.
Step 5: Read memory with background data.