REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15																			

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
RAJESH PITHADIA

CHECKED BY
KENNETH RICE

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
93-03-25

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT,MEMORY, DIGITAL, CMOS UV ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-89469**

SHEET 1 OF 15

DESC FORM 193
JUL 91

5962-E646-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001245 429

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89469	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Propagation delay
01		2100 gate UV EPLD	45 ns

1.2.2 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GQCC1-J68	68	"J" lead chip carrier package 2/
Y	CMGA15-PN	68	Pin grid array package 2/ 3/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Maximum power dissipation	2 W 5/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines X and Y	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C
Endurance	25 erase/write cycles (minimum)
Data retention	10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Inactive for new design.
4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, C, or D (see 4.3 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_I	$V_{IN} = V_{CC}$ or GND (at $V_{CC} = V_{CC}$ max)	1, 2, 3	All	-10	+10	µA
Three-state output off current	I_{OZ}	$V_{OUT} = V_{CC}$ or GND (at $V_{CC} = V_{CC}$ max)	1, 2, 3	All	-10	+10	µA
Low level input voltage	V_{IL}		1, 2, 3	All	-0.3	0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC}+ 0.3	V
Low level output voltage 2/	V_{OL}	I_{OL} = +4.0 mA (at $V_{CC} = V_{CC}$ min), V_{IH} = 3.0 V, V_{IL} = 0.0 V	1, 2, 3	All		0.45	V
High level TTL output voltage 2/	V_{OH}(TTL)	I_{OH} = -4.0 mA (at $V_{CC} = V_{CC}$ min)	1, 2, 3	All	2.4		V
High level CMOS output voltage 2/	V_{OH}(CMOS)	I_{OH} = -2.0 mA (at $V_{CC} = V_{CC}$ min) V_{IH} = 3.0 V, V_{IL} = 0.0 V	1, 2, 3	All	3.84		V
V_{CC} supply current (standby, non-TURBO) 2/	I_{CC1}	$V_{IN} = 0$ V or V_{CC}	1, 2, 3	All		900	µA
V_{CC} supply current (active, non-TURBO) 2/ 3/	I_{CC2}	$V_{IN} = 0$ V or V_{CC}, f = 1 MHz	1, 2, 3	All		40	mA
V_{CC} supply current (active, TURBO) 2/ 3/	I_{CC3}	$V_{IN} = 0$ V or V_{CC}, $f = f_{MAX}$	1, 2, 3	All		275	mA
Input capacitance 2/	C_{IN}	V_{IN} = 0 V dc, f = 1.0 MHz measured from pin to V_{SS} See 4.3.1c	4	All		20	pF
Output capacitance 2/	C_{OUT}	V_{OUT} = 0 V dc, f = 1.0 MHz measured from pin to V_{SS} See 4.3.1c	4	All		20	pF
Clock pin capacitance 2/	C_{CLK}	V_{IN} = 0 V dc, f = 1.0 MHz measured from pin to V_{SS} See 4.3.1c	4	All		25	pF
Clock/V_{PP} pin capacitance 2/	C_{VPP}	V_{OUT} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} See 4.3.1c	4	All		160	pF
Functional tests		See 4.3.1d	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input to nonregistered output	t_{PD1}	CL = 35 pF	9,10,11	All		45	ns
I/O input to nonregistered output	t_{PD2}		9,10,11	All		55	ns
Input to output enable 4/ 5/	t_{PZX}		9,10,11	All		45	ns
Input to output disable 2/ 4/ 5/	t_{PXZ}	CL = 5 pF output change = 500 mV	9,10,11	All		45	ns
Asynchronous output clear time 4/ 5/	t_{CLR}	CL = 35 pF	9,10,11	All		50	ns
I/O input buffer delay	t_{IO}		9,10,11	All		5	ns
Maximum frequency (1/tSU) 4/ 5/ 6/ 7/	f_{MAX1}		9,10,11	All	33.3		MHz
Input setup time 4/ 5/	t_{SU}		9,10,11	All	30		ns
Input hold time 4/	t_H		9,10,11	All	0		ns
Clock high time	t_{CH}		9,10,11	All	15		ns
Clock low time	t_{CL}		9,10,11	All	15		ns
Clock to output delay time 5/	t_{CO1}		9,10,11	All		25	ns
Minimum clock period (tSU + tCO1) (register output feedback to register input-external path) 8/	t_{P2}		9,10,11	All		55	ns
Minimum clock period (register output feedback to register input-internal path) 5/	t_{CNT}		9,10,11	All		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC}$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal maximum frequency (1/tCNT) 9/	f_{MAX2}		9,10,11	All	22.2		MHz
Asynchronous input setup time 4/ 5/	t_{ASU}	CL = 35 pF	9,10,11	All	13		ns
Asynchronous input hold time 4/ 5/	t_{AH}	CL = 35 pF	9,10,11	All	18		ns
Asynchronous clock low time 4/ 5/	t_{ACL}	CL = 35 pF	9,10,11	All	18		ns
Asynchronous clock high time 4/ 5/	t_{ACH}	CL = 35 pF	9,10,11	All	18		ns
Asynchronous clock to output delay 4/ 5/	t_{ACO1}	CL = 35 pF	9,10,11	All		50	ns
Asynchronous minimum clock period (register output feedback to register input-internal path) 5/	t_{ACNT}		9,10,11	All		45	ns
Asynchronous internal maximum frequency (1/tACNT) 9/	f_{MAX3}		9,10,11	All	22.2		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Screening and characterization of ac delay parameters are conducted at 10 MHz or less. Figure 3 shows the output loading circuit and figure 4 shows the timing diagram.

2/ May not be tested, but shall be guaranteed to the limits specified in table I.

3/ Tested using a data pattern specified by the device manufacturer, which has been correlated to four independent 12-bit counters and no output loading.

4/ All array-dependent delays are specified for an XOR pattern. This pattern involves two product terms and two pure inputs with all other product terms in the macrocell held low by one EPROM pull-down. Other patterns may result in longer delays than those specified. Delays involving only one product term, such as tPXZ, are specified for an "XOR-like" pattern which involves one pure input switching at a time, and the single product term. All tested parameters may not be tested on all macro cells.

5/ When the TURBO bit is not set, a non-TURBO adder of 30 ns maximum (40 ns for t_{ASU}) shall apply. Parameters may not be tested in non-TURBO condition, but shall be guaranteed to the limits specified in table I. Non-TURBO mode devices require one input or I/O transition to guarantee entering correct power-up state.

6/ f_{MAX} represents the highest clock frequency for pipelined data.

7/ May not be tested, but shall be guaranteed to the limits of t_{SU} specified in table I

8/ May not be tested, but shall be guaranteed to the limits of t_{SU} and t_{CO1} specified in table I.

9/ May not be tested, but shall be guaranteed to the limits of t_{CNT} and t_{ACNT} specified in table I.

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number 1/	Terminal symbol	Terminal number 1/	Terminal symbol
1	GND	35	GND
2	I/O	36	I/O
3	I/O	37	I/O
4	I/O	38	I/O
5	I/O	39	I/O
6	I/O	40	I/O
7	I/O	41	I/O
8	I/O	42	I/O
9	I/O	43	I/O
10	I/O	44	I/O
11	I/O	45	I/O
12	I/O	46	I/O
13	I/O	47	I/O
14	I	48	I
15	I	49	I
16	I	50	I
17	CLK1/I	51	CLK3/I
18	V_{CC}	52	V_{CC}
19	CLK2/I	53	CLK4/I
20	I	54	I
21	I	55	I
22	I	56	I
23	I/O	57	I/O
24	I/O	58	I/O
25	I/O	59	I/O
26	I/O	60	I/O
27	I/O	61	I/O
28	I/O	62	I/O
29	I/O	63	I/O
30	I/O	64	I/O
31	I/O	65	I/O
32	I/O	66	I/O
33	I/O	67	I/O
34	I/O	68	I/O

1/ Terminal numbers are referenced to the electrical pin one.

Case outline Y

1	2	3	4	5	6	7	8	9	10	11	
	I/O	I/O	I	CLK1/I	CLK2/I	I	I/O	I/O	I/O		L
I/O	I/O	I/O	I	I	V_{CC}	I	I/O	I/O	I/O	I/O	K
I/O	I/O								I/O	I/O	J
I/O	I/O								I/O	I/O	H
I/O	I/O								I/O	I/O	G
I/O	GND								GND	I/O	F
I/O	I/O								I/O	I/O	E
I/O	I/O								I/O	I/O	D
I/O	I/O	1/							I/O	I/O	C
I/O	I/O	I/O	I	I	V_{CC}	I	I	I/O	I/O	I/O	B
	I/O	I/O	I/O	I	CLK4/I	CLK3/I	I	I/O	I/O		A
1	2	3	4	5	6	7	8	9	10	11	

BOTTOM VIEW

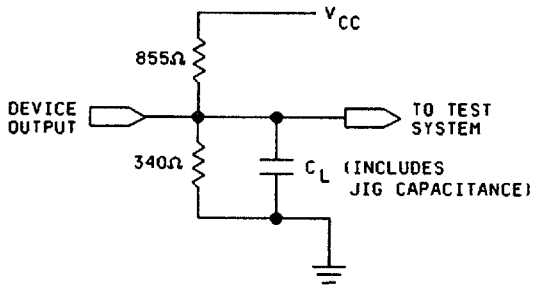
1/ Reference mark

FIGURE 1. Terminal connections - Continued.

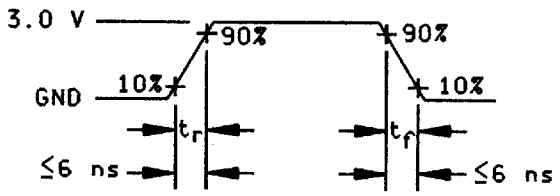
Truth table		
Input pins		Output pins
CP/I	I	I/O
X	X	Z

NOTES:
1. X = Don't care.
2. Z = High impedance.

FIGURE 2. Truth table.



Input pulses

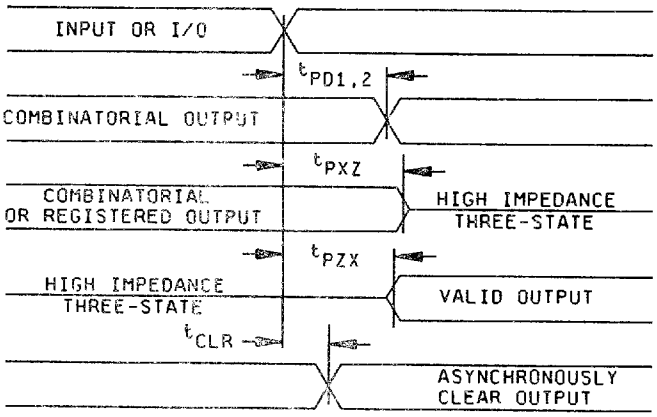


AC test conditions

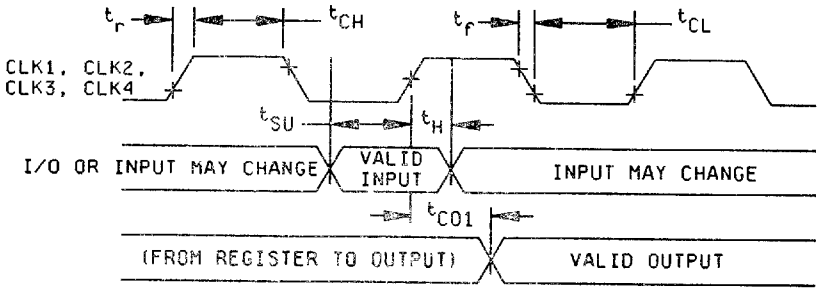
Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 6 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

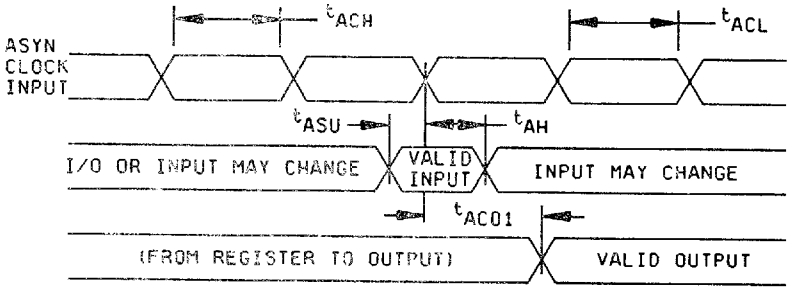
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE



NOTE: t_{ACL}, t_{CL}, t_{ACH}, and t_{CH} timings are specified at 0.3 V and 2.7 V respectively.

All other timings are at 1.5 V.

FIGURE 4. Timing waveforms.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPLD's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.5 herein) to the specified pattern or erased (see 4.4 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

a. All devices selected for testing shall be programmed in accordance with 3.2.3.1 herein.

b. Verify pattern (see 3.10.3).

c. Erase (see 3.10.1).

d. Verify pattern erasure (see 3.10.3).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

Margin test method .

(1) Program a minimum of 95 percent of the total number of cells, including the slowest programming cell (see 3.10.2).

(2) Bake, unbiased, for 72 hours at +140°C minimum, or equivalent time and temperature implied by an activation energy of 0.4 eV.

(3) Perform electrical test (see 4.2b) at +25°C including a margin test at Vm = 5.6 V and loose timing (i.e., 1 μs).

(4) Erase (see 3.10.1).

(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.10.2).

(6) Perform electrical test (see 4.2b) at +25°C including a margin test at Vm = 5.6 V and loose timing (i.e., 1 μs).

(7) Erase (see 3.10.1).

(8) Perform burn-in (see 4.2a).

(9) Perform electrical test (see 4.2b) at +25°C including a margin test at Vm = 5.6 V and loose timing (i.e., 1 μs).

(10) Perform electrical tests at T_C = +125°C.

(11) Perform electrical tests at T_C = -55°C.

(12) Erase (see 3.10.1).

(13) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial characterization and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. See 4/ of table II.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8A, 8B,9
Group A test requirements (method 5005)	1,2,3,4**,7, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroup 7 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed in accordance with 3.2.3.1 herein. After completion of testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 30 Ws/cm^2. The erasure time with this dosage is approximately 45 minutes using a ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 1000 Ws/cm^2 (1 day at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.