REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Recommended operating condition, changed high level input voltage from 2.0 V to 2.3 V. Deleted pin numbers configuration from device type 03, 6.6 pin description section. Changes to terminal connections on figure 2. Editorial changes throughout.	92-02-12	

REV	A	A	A	A															
SHEET	35	36	37	38															
REV				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS														
REV	A	A	A	A				A						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Todd Creek

CHECKED BY
Ray Monnin

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
29 MARCH 1988

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER NMOS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88566
A	67268	

SHEET 1

DESC FORM 193
JUL 91

5962-E128

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88566	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2681	Dual asynchronous receiver/transmitter (DUART)
02	2681	Dual asynchronous receiver/transmitter (DUART) with 7-bit input and 8-bit output ports
03	68681	Dual asynchronous receiver/transmitter (DUART)

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	See figure 1(52-lead, 1.330" x .660" x .100"), flat package
U	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1 W
Lead temperature (soldering, 5 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Q, U	see MIL-M-38510, appendix C
Case Y	20°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (logic inputs)(V_{IH}):	
Devices 01, 02, and 03	2.3 V dc
Device 03 (pin X1/CLK only)	4.0 V dc
Low level input voltage (logic inputs)(V_{IL})	0.8 V dc
Maximum high level output current (I_{OH})	-400 µA
Maximum low level output current (I_{OL})	2.4 mA
Case operating temperature range (T_C)	-55°C to +125°C

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}		All	1,2,3		0.8	V
Input high voltage (except X1/CLK)	V_{IH}		All	1,2,3	2.3		V
Input high voltage (X1/CLK)	V_{IH}		All	1,2,3	4.0		V
Output low voltage	V_{OL}	$I_{OL} = 2.4$ mA	All	1,2,3		0.4	V
Output high voltage (except open collector outputs)	V_{OH}	$I_{OH} = -400\ \mu A$	All	1,2,3	2.7		V
Input leakage current	I_{IL}	$V_I = 0$ V to V_{CC}	All	1,2,3	-10	10	µA
Data bus three-state leakage current	I_{OZL}, I_{OZH}	$V_O = 0.4$ V to V_{CC}	All	1,2,3	-10	10	µA
X1/CLK low input current	I_{IL} (XI)	$V_I = 0$ V, X2 grounded	01,02	1,2,3	-4.0	0.0	mA
			03	1,2,3	-1.0		
		$V_I = 0$ V, X2 floated	All	1,2,3	-3.0	0.0	mA
X1/CLK high input current	I_{IH} (XI)	$V_I = V_{CC}$, X2 grounded	All	1,2,3	-1.0	1.0	mA
		$V_I = V_{CC}$, X2 floated	All	1,2,3	0.0	10.0	mA
X2 low input current	I_{IL} (X2)	$V_I = 0$ V, X1/CLK floated	All	1,2,3	-100	0.0	µA
X2 high input current	I_{IH} (X2)	$V_I = V_{CC}$, X1/CLK floated	All	1,2,3	-0.0	100	µA
Open collector output leakage current	I_{OH}	$V_O = 0.4$ V to V_{CC}	All	1,2,3	-10	10	µA
Power supply current	I_{CC}	$V_{CC} = 5.5$ V, $T_C = +25°C$ and $+125°C$	All	1,2		150	mA
		$V_{CC} = 5.5$ V, $T_C = -55°C$	All	3		175	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits Min	Limits Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\ V$, $F_C = 1\ MHz$, See 4.3.1c	All	4		20	pF
Functional testing		See 4.3.1d	All	7,8			
Reset pulse width	t_{RES}	See figure 4	01,02	9,10,11	1.0		µs
A0-A3 setup time to RDN, WRN low	t_{AS}	See figure 5 4/	01,02	9,10,11	10		ns
A0-A3 hold time from RDN, WRN high	t_{AH}		01,02	9,10,11	0		ns
CEN setup time to RDN, WND low	t_{CS}		01,02	9,10,11	0		ns
CEN hold time from RDN, WRN high	t_{CH}		01,02	9,10,11	0		ns
WRN, RDN pulse width	t_{RW}		01,02	9,10,11	225		ns
Data valid after RDN low	t_{DD}		01,02	9,10,11		175	ns
Data bus floating after RDN high	t_{DF}		01,02	9,10,11		100	ns
Data setup time before WRN high	t_{DS}		01,02	9,10,11	100		ns
Data hold time after WRN high	t_{DH}		01,02	9,10,11	20		ns
High time between READS and/ or WRITES 5/ 6/	t_{RWD}		01,02	9,10,11	200		ns
Port input setup time before RDN low	t_{PS}	See figure 6 4/	01,02	9,10,11	0		ns
Port input hold time after RDN high	t_{PH}		01,02	9,10,11	0		ns
Port output valid after WRN high	t_{PD}		01,02	9,10,11		400	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits Min	Limits Max	Unit
INTRN (or OP3-OP7 when used as interrupts) negated from:		See figure 7					
Read RHR (RxRDY/FFULL interrupt)	t_{IR1}		01,02	9,10,11		300	ns
Write THR (TxRDY interrupt)	t_{IR2}		01,02	9,10,11		300	ns
Reset command (delta break interrupt)	t_{IR3}		01,02	9,10,11		300	ns
Stop C/T command (counter interrupt)	t_{IR4}		01,02	9,10,11		300	ns
Read IPCR (input port change interrupt)	t_{IR5}		01,02	9,10,11		300	ns
Write IMR (clear of interrupt mask bit)	t_{IR6}		01,02	9,10,11		300	ns
X1/CLK high or low time	t_{CLK}	See figure 8	01,02	9,10,11	100		ns
X1/CLK frequency	f_{CLK}		01,02	9,10,11	2.0	4.0	MHz
CTCLK (IP2) high or low time	t_{CTC}		01,02	9,10,11	100		ns
CTCLK (IP2) frequency	f_{CTC}		01,02	9,10,11	0	4.0	MHz
RxC high or low time	t_{RX}		01,02	9,10,11	220		ns
RxC frequency (16X)	f_{RX}		01,02	9,10,11	0	2.0	MHz
RxC frequency (1X)	f_{RX}		01,02	9,10,11	0	1.0	MHz
TxC high or low time	t_{TX}		01,02	9,10,11	220		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits Min	Limits Max	Unit
TxC frequency (16X)	f_{TX}	See figure 8	01,02	9,10,11	0	2.0	MHz
TxC frequency (1X)	f_{TX}		01,02	9,10,11	0	1.0	MHz
TxD output delay from TxC low	t_{TXD}	See figure 9	01,02	9,10,11		350	ns
Output delay from TxC low to TxD data output	t_{TCS}		01,02	9,10,11	0	150	ns
RxD data setup time to RxC high	t_{RXS}	See figure 10	01,02	9,10,11	240		ns
RxD data hold time from RxC high	t_{RXH}		01,02	9,10,11	200		ns
RESETN pulse width	t_{RES}	See figure 11	03	9,10,11	1.0		µs
A1-A4 setup to CSN low	t_{AS}	See figures 12, 13, 14	03	9,10,11	10		ns
A1-A4 hold time from CSN high	t_{AH}		03	9,10,11	0		ns
R/WN setup time to CSN high	t_{RWS}		03	9,10,11	0		ns
R/WN holdup time to CSN high	t_{RWH}		03	9,10,11	0		ns
CSN high pulse width 7/	t_{CSW}		03	9,10,11	160		ns
CSN or IACKN high from 8/ DTACKN low	t_{CSD}		03	9,10,11	20		ns
Data valid from CSN or IACKN low	t_{DD}		03	9,10,11		175	ns
Data bus floating from CSN or IACKN high	t_{DF}		03	9,10,11		100	ns
Data setup time to CLK high	t_{DS}		03	9,10,11	100		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits		Unit
					Min	Max	
Data hold time from CSN high	t_{DH}	See figures 12, 13, 14	03	9,10,11	0		ns
DTACKN low from read data	t_{DAL}		03	9,10,11	0		ns
DTACKN low (read cycle) from CLK high	t_{DCR}		03	9,10,11		125	ns
DTACKN low (write cycle) from CLK high	t_{DCW}		03	9,10,11		125	ns
DTACKN high from CSN or IACKN high	t_{DAH}	See figures 12, 13, 14	03	9,10,11		100	ns
DTACKN high impedance from CSN or IACKN high	t_{DAT}		03	9,10,11		125	ns
CSN or IACKN setup time 9/ to clock high	t_{CSC}		03	9,10,11	90		ns
Port input setup to CSN low	t_{PS}	See figure 15	03	9,10,11	0		ns
Port input hold time CSN high	t_{PH}		03	9,10,11	0		ns
Port output valid from CSN high	t_{PD}		03	9,10,11		400	ns
INTRN, or OP3-OP7 when used as interrupts, negated from:		See figure 16					
Read RHR (RxRDY/FFULL interrupts)	t_{IR1}		03	9,10,11		300	ns
Write THR (TxRDY interrupt)	t_{IR2}		03	9,10,11		300	ns
Reset command (delta break interrupt)	t_{IR3}		03	9,10,11		300	ns
Stop C/T command (counter interrupt)	t_{IR4}		03	9,10,11		300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5$ V ±10% unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits		Unit
					Min	Max	
Read IPCR (input port change interrupt)	t_{IR5}	See figure 16	03	9,10,11		300	ns
Write IMR (clear of interrupt mask bit)	t_{IR6}		03	9,10,11		300	ns
X1/CLK high or low time	t_{CLK}	See figure 17	03	9,10,11	100		ns
X1/CLK frequency	f_{CLK}		03	9,10,11	2.0	4.0	MHz
CTCLK high or low time	t_{CTC}		03	9,10,11	100		ns
CTCLK frequency	f_{CTC}		03	9,10,11	0	4.0	MHz
RxC high or low time	t_{RX}		03	9,10,11	220		ns
RxC frequency (16X)	f_{RX}		03	9,10,11	0	2.0	MHz
RxC frequency (1X)	f_{RX}		03	9,10,11	0	1.0	MHz
TxC high or low time	t_{TX}		03	9,10,11	220		ns
TxC frequency (16X)	f_{TX}		03	9,10,11	0	2.0	MHz
TxC frequency (1X)	f_{TX}		03	9,10,11	0	1.0	MHz
TxD output delay from TxC low	t_{TXD}	See figure 18	03	9,10,11		350	ns
Output delay from TxC low to TxD data output	t_{TCS}		03	9,10,11		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5$ V ±10% unless otherwise specified 1/ 2/ 3/	Device types	Group A sub-groups	Limits Min	Limits Max	Unit
RxD data setup time to RxC high	t_{RXS}	See figure 19	03	9,10,11	240		ns
RxD data hold time from RxC high	t_{RXH}		03	9,10,11	200		ns

1/ Parameters are valid over specified temperature range. All test to be performed using worst-case test conditions unless otherwise specified

2/ All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4 V and 2.4 V with a transition time of < 20 ns. For X1/CLK this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.8 V and 2.3 V as appropriate.

3/ Test condition for outputs: C_L = 150 pF tied to ground, except interrupt outputs. Test condition for interrupt outputs: C_L = 50 pF tied to ground, R_L = 2.7 kΩ to V_{CC}.

4/ Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the "strobing" input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are AND'ed internally. As a consequence the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

5/ If CEN is used as the "strobing" input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.

6/ Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

7/ This specification will impose maximum 68000 CPU CLK to 6 MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

8/ This specification imposed a lower bound on CSN and IACKN low, guaranteeing that it will be low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.

9/ This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.

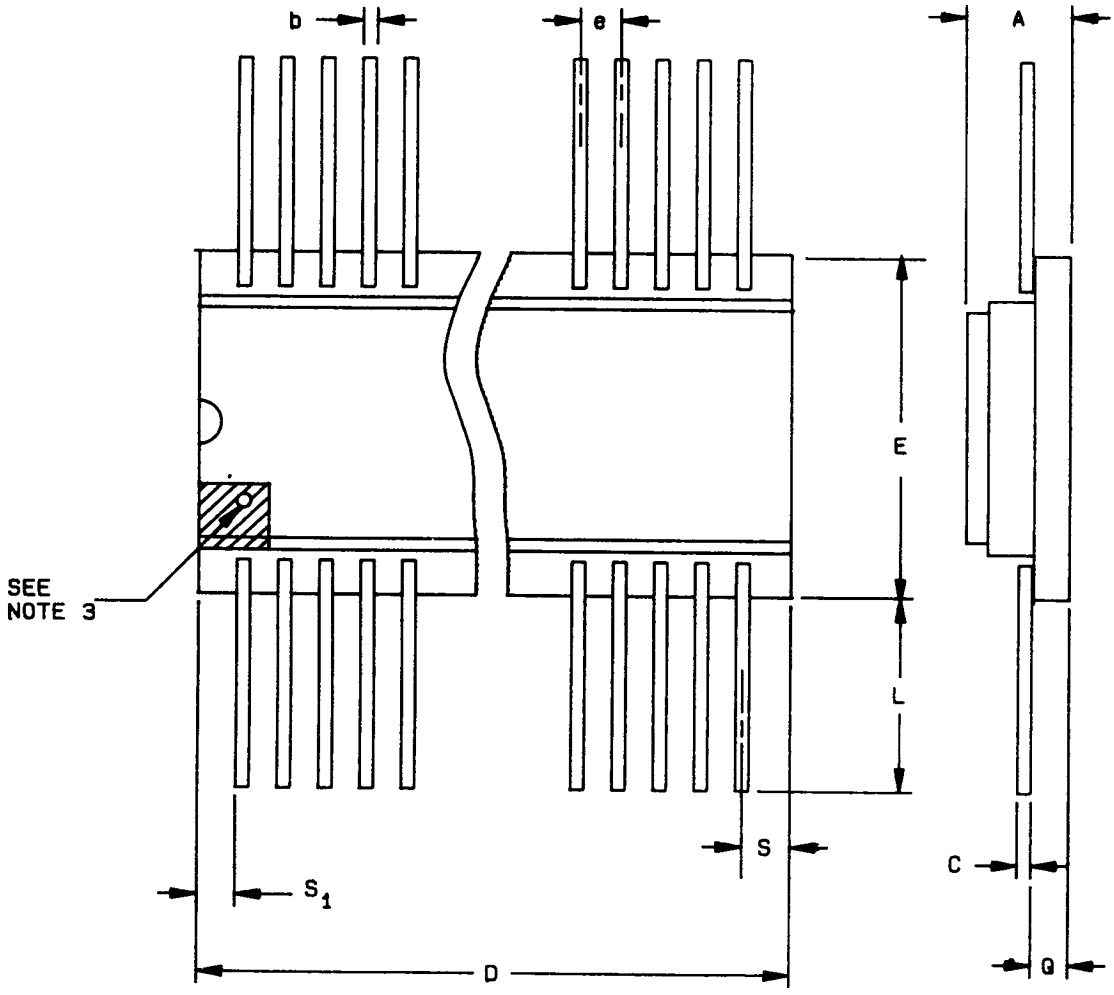


FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88566
		REVISION LEVEL	SHEET 11

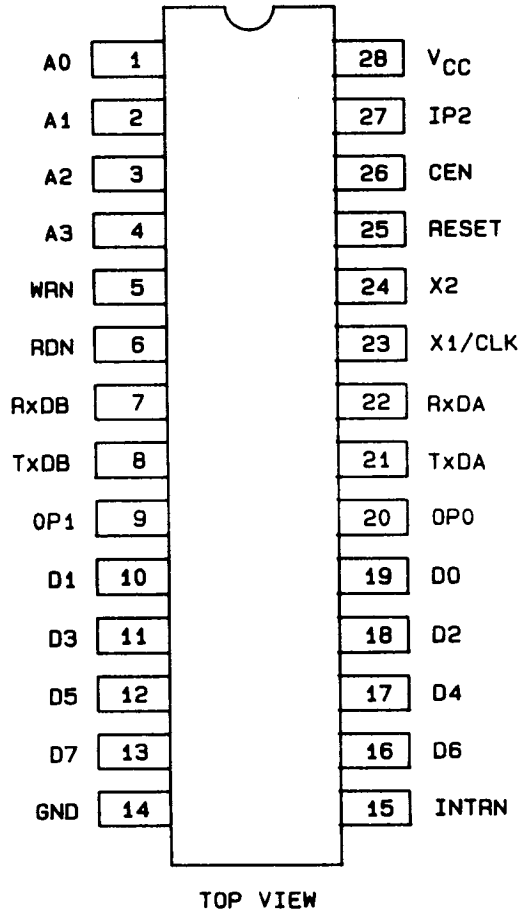
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.100	1.14	2.54	
b	.015	.023	0.38	0.58	7
c	.008	.012	0.20	0.30	7
D	---	1.330	---	33.78	4
E	.620	.660	15.75	16.76	
E_1	---	---	---	---	
e	.050 BSC		1.27 BSC		5
L	.250	.370	6.35	9.40	
Q	.054	.066	1.37	1.68	6
S	---	.045	---	1.14	
S_1	.005	---	0.13	---	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. A pin 1 tab (enlargement) is located within the shaded area shown and adjacent to the package body. Other pin numbers proceed sequentially from pin 1 counterclockwise (as viewed from the top of the device).
4. This dimension allows to off center lid, meniscus, and glass overrun.
5. The reference pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline is located within ±.005 (0.13 mm) of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured at the point of exit of the lead body.
7. All leads increase maximum limit by .003 (0.08 mm) measured at the crest of major flats, when lead finish A or B is applied.

FIGURE 1. Case outline Y - Continued.

Device type 01

Case outline X

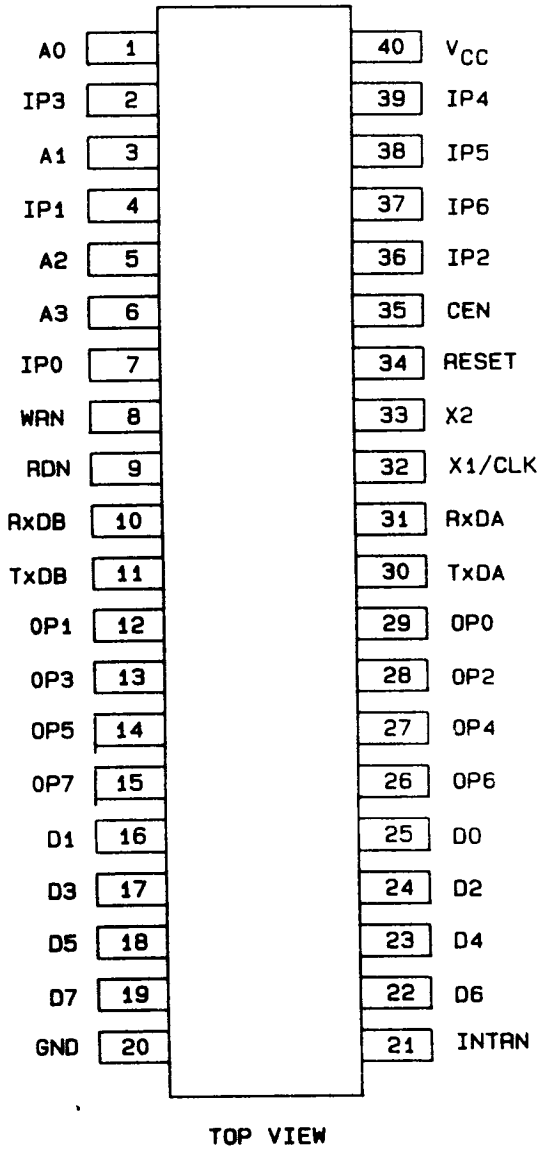


TOP VIEW

FIGURE 2. Terminal connections.

Device type 02

Case outline Q



TOP VIEW

FIGURE 2. Terminal connections - Continued.

Device type 02

Case outline Y

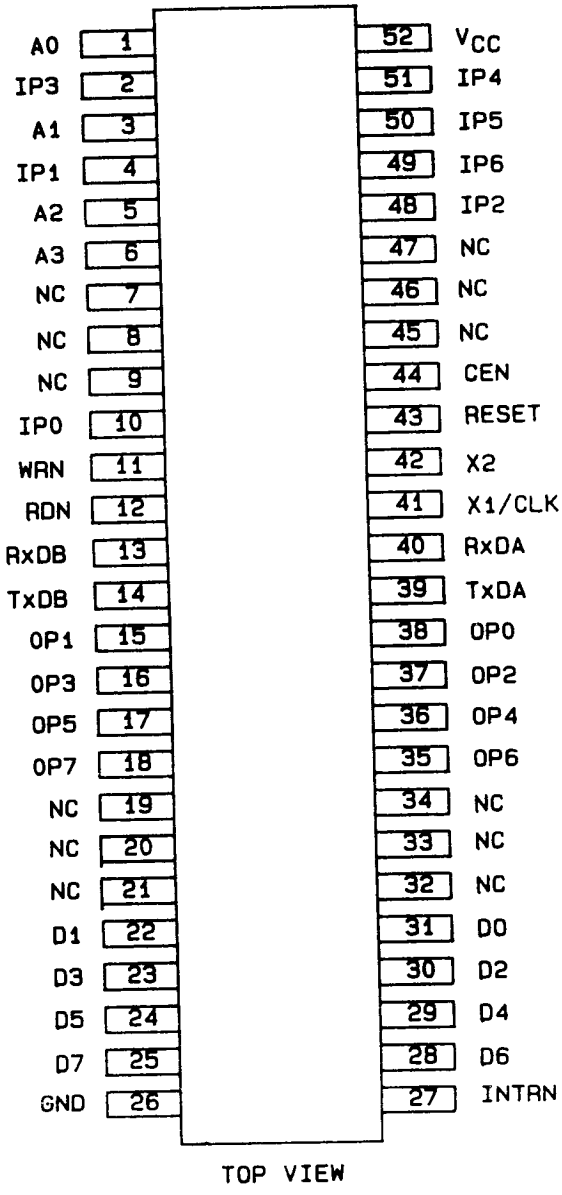
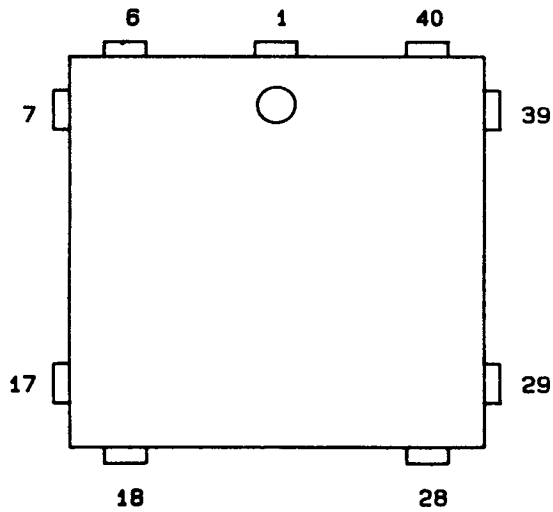


FIGURE 2. Terminal connections - Continued.

Device type 02

Case outline U

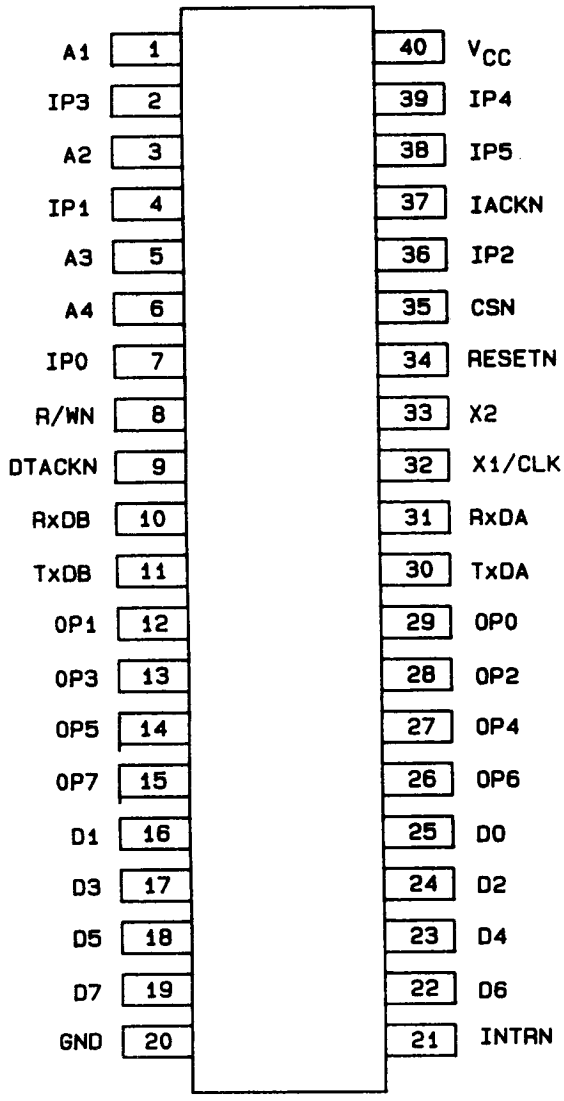


Pin	Function	Pin	Function
1.	NC	23.	NC
2.	A0	24.	INTRN
3.	IP3	25.	D6
4.	A1	26.	D4
5.	IP1	27.	D2
6.	A2	28.	D0
7.	A3	29.	OP6
8.	IP0	30.	OP4
9.	WRN	31.	OP2
10.	RDN	32.	OP0
11.	RxDB	33.	TxDA
12.	NC	34.	NC
13.	TxDB	35.	RxDA
14.	OP1	36.	X1/CLK
15.	OP3	37.	X2
16.	OP5	38.	RESET
17.	OP7	39.	CEN
18.	D1	40.	IP2
19.	D3	41.	IP6
20.	D5	42.	IP5
21.	D7	43.	IP4
22.	GND	44.	V_{CC}

FIGURE 2. Terminal connections - Continued.

Device type 03

Case outline Q

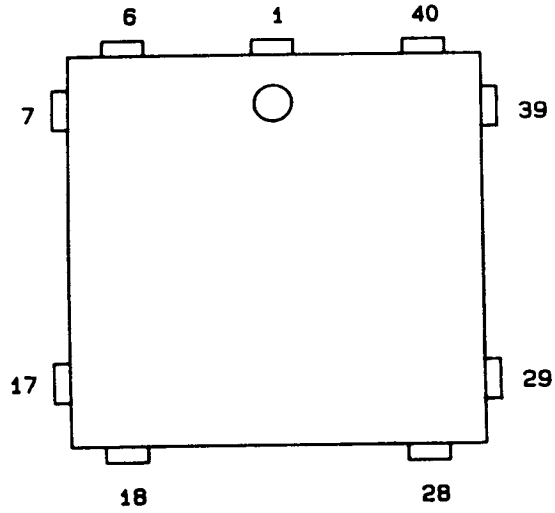


TOP VIEW

FIGURE 2. Terminal connections - Continued.

Device type 03

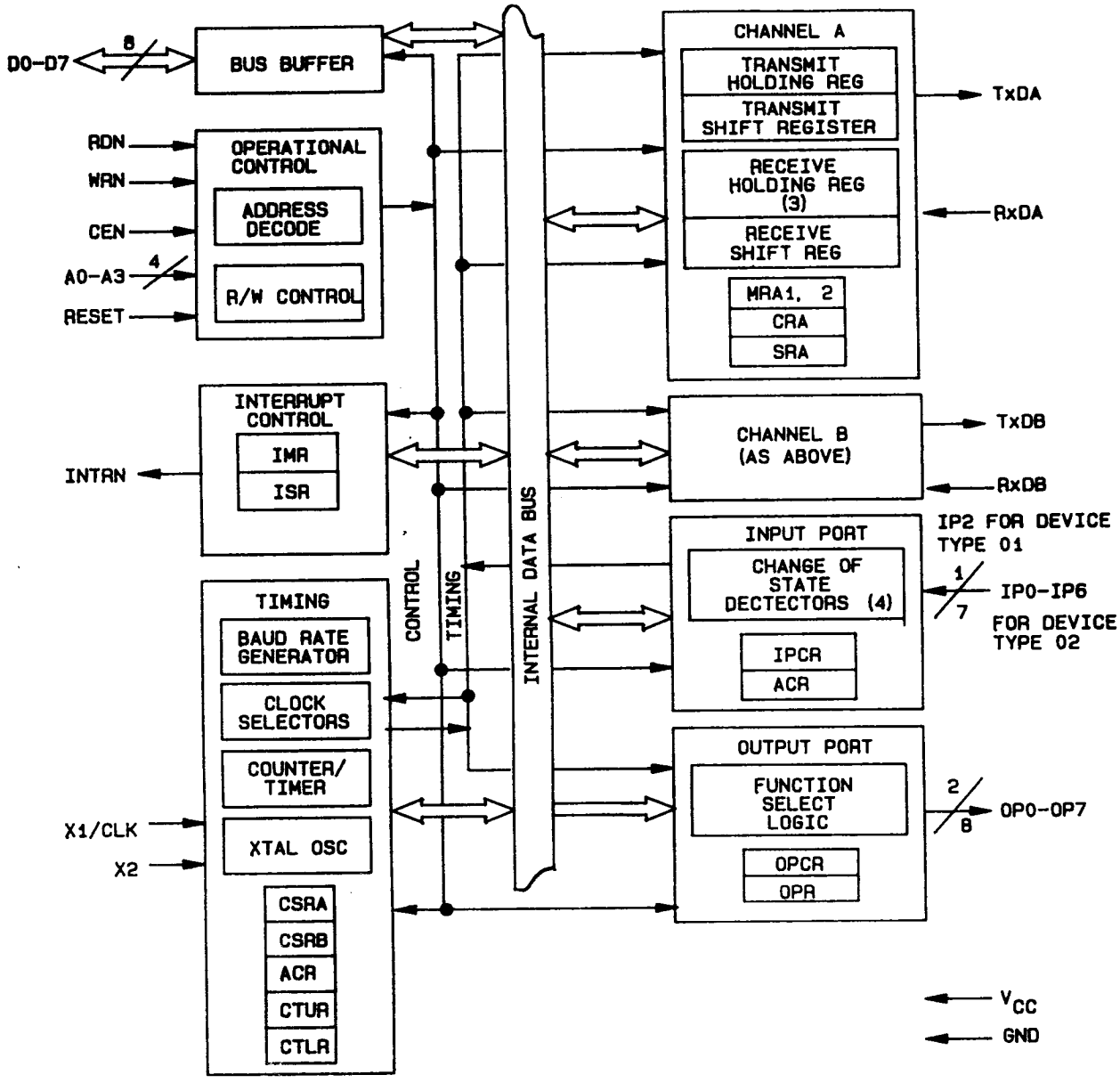
Case outline U



Pin	Function	Pin	Function
1.	NC	23.	NC
2.	A1	24.	INTRN
3.	IP3	25.	D6
4.	A2	26.	D4
5.	IP1	27.	D2
6.	A3	28.	D0
7.	A4	29.	OP6
8.	IP0	30.	OP4
9.	R/WN	31.	OP2
10.	DTACKN	32.	OP0
11.	RxDB	33.	TxDA
12.	NC	34.	NC
13.	TxDB	35.	RxDA
14.	OP1	36.	X1/CLK
15.	OP3	37.	X2
16.	OP5	38.	RESETN
17.	OP7	39.	CSN
18.	D1	40.	IP2
19.	D3	41.	IACKN
20.	D5	42.	IP5
21.	D7	43.	IP4
22.	GND	44.	V_{CC}

FIGURE 2. Terminal connections - Continued.

Device types 01 and 02



NOTE: Device type 01 does not have 7-bit input port and 8-bit output port (see 6.6 pin descriptions).

FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88566
		REVISION LEVEL A	SHEET 19

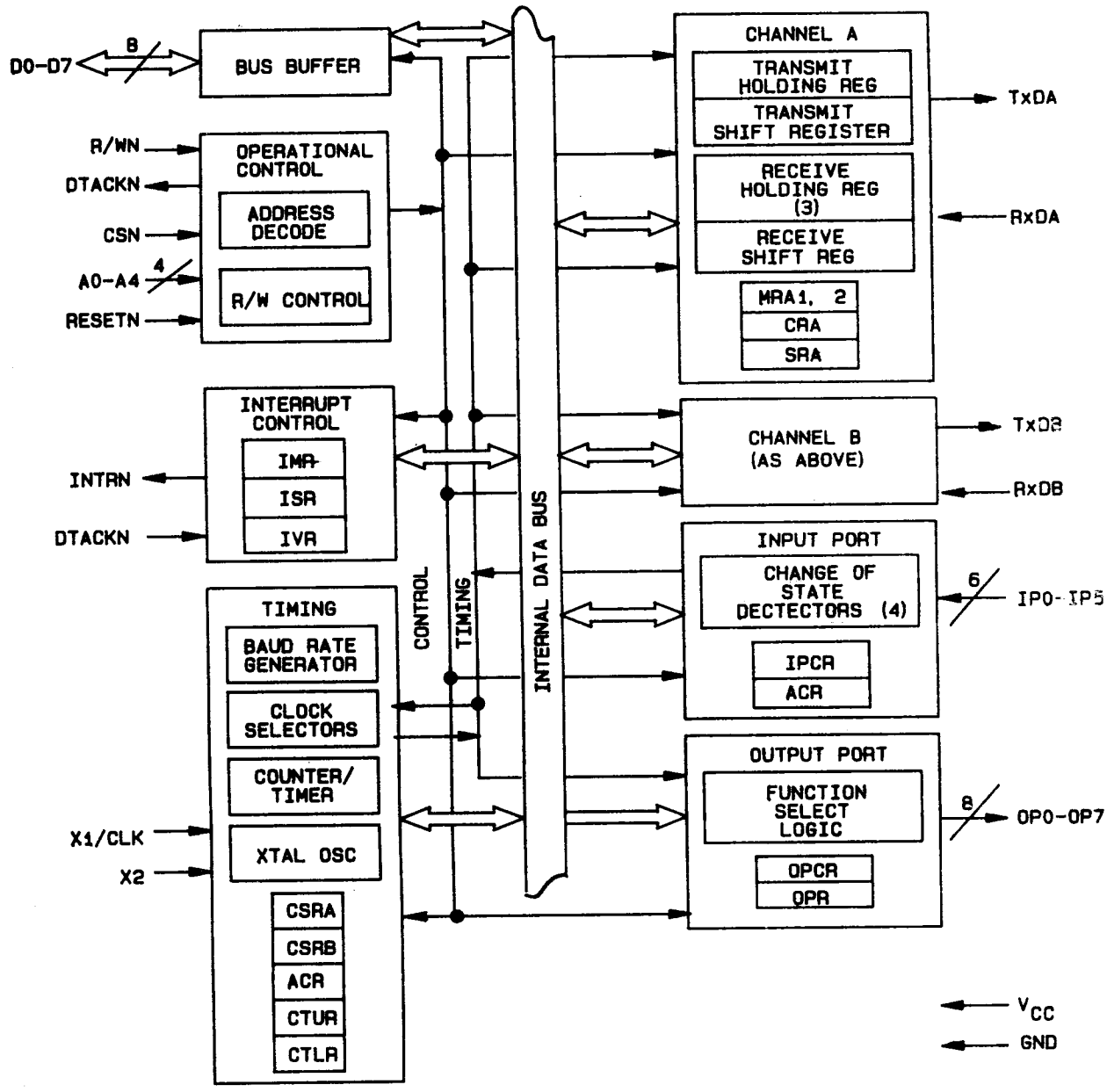


FIGURE 3. Block diagram - Continued.

FIGURE 4. Reset timing.

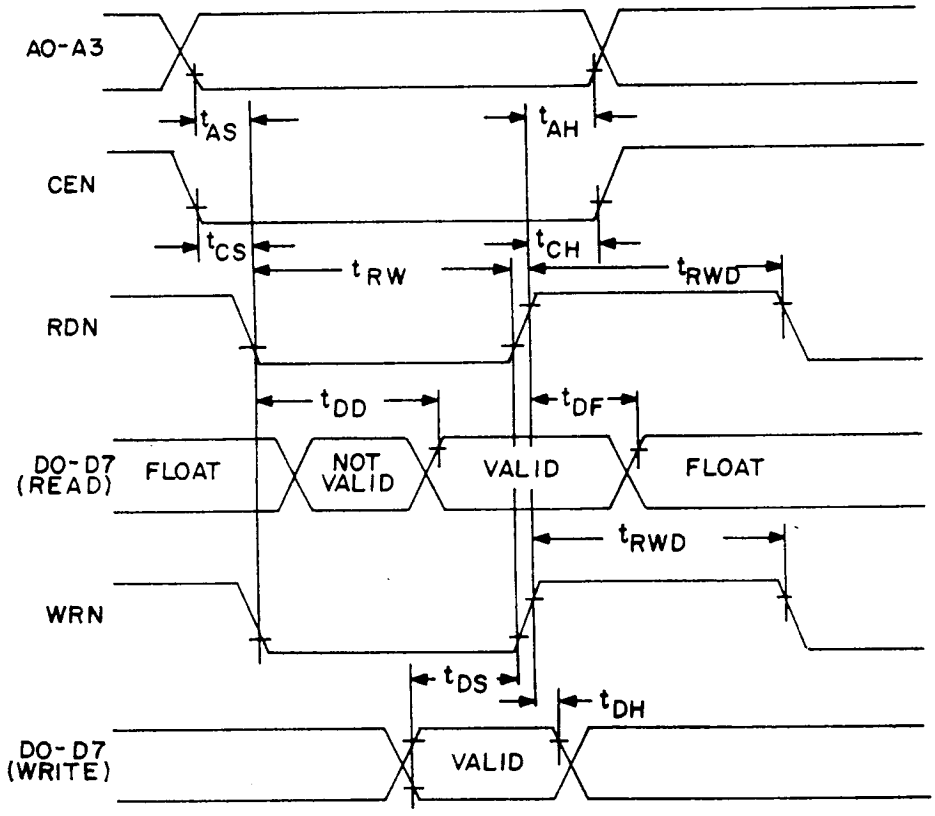


FIGURE 5. Bus timing.

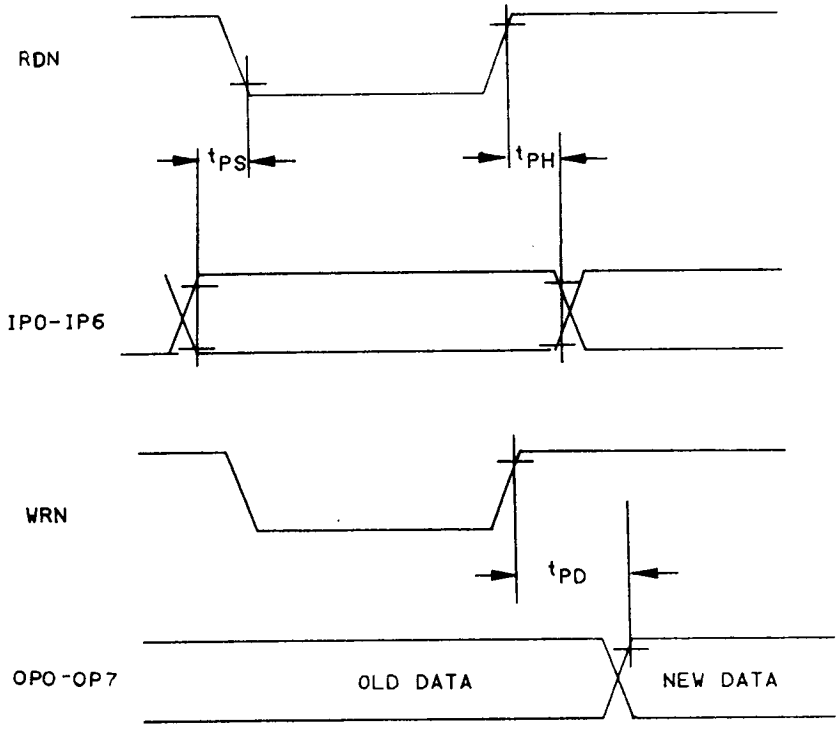
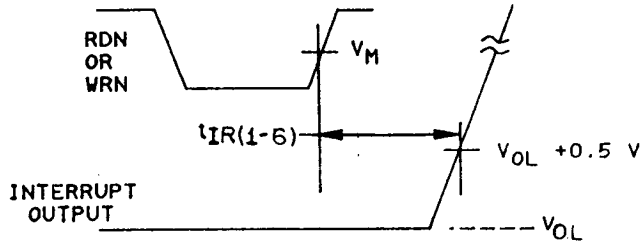
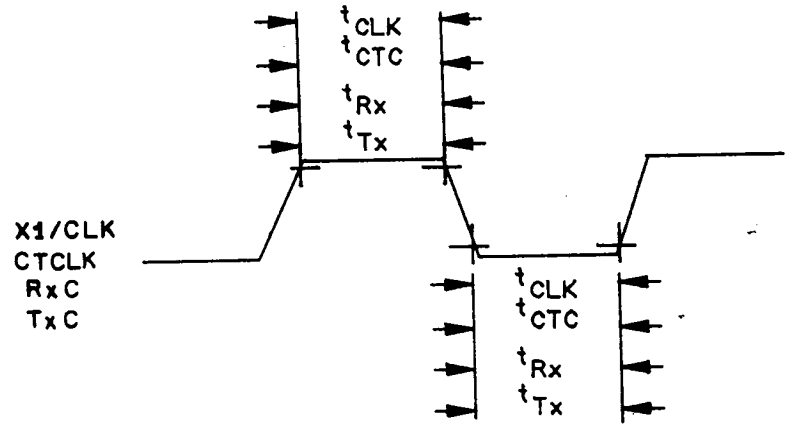


FIGURE 6. Port timing.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of the response is referenced from the midpoint of the switching signal. V_M to a point 0.5 V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuity and test environment are pronounced and can greatly affect the resultant measurement.

FIGURE 7. Interrupt timing.



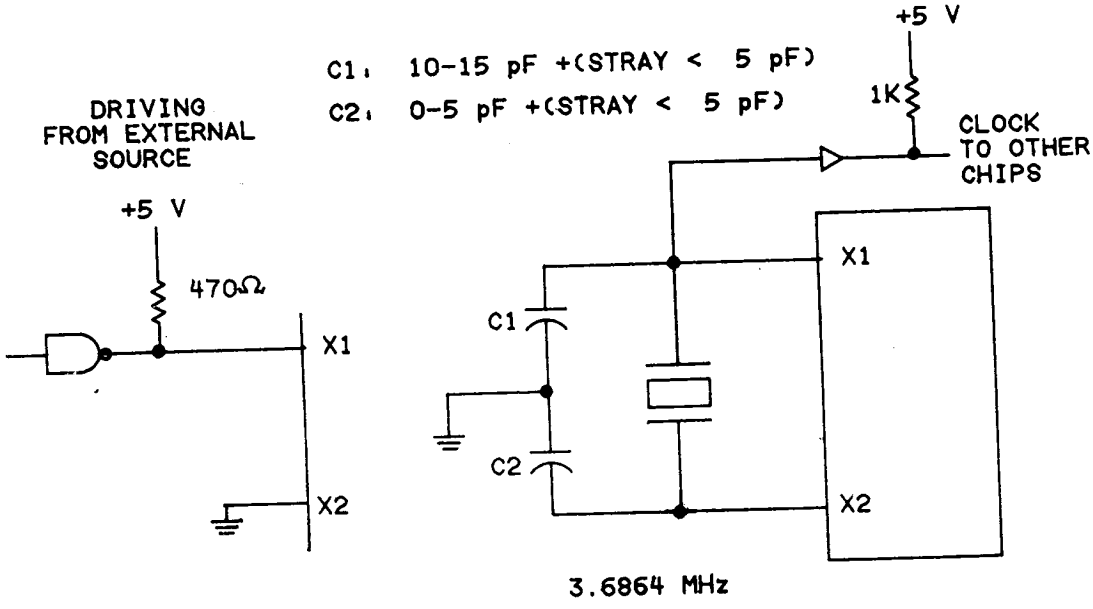


FIGURE 8. Clock timing.

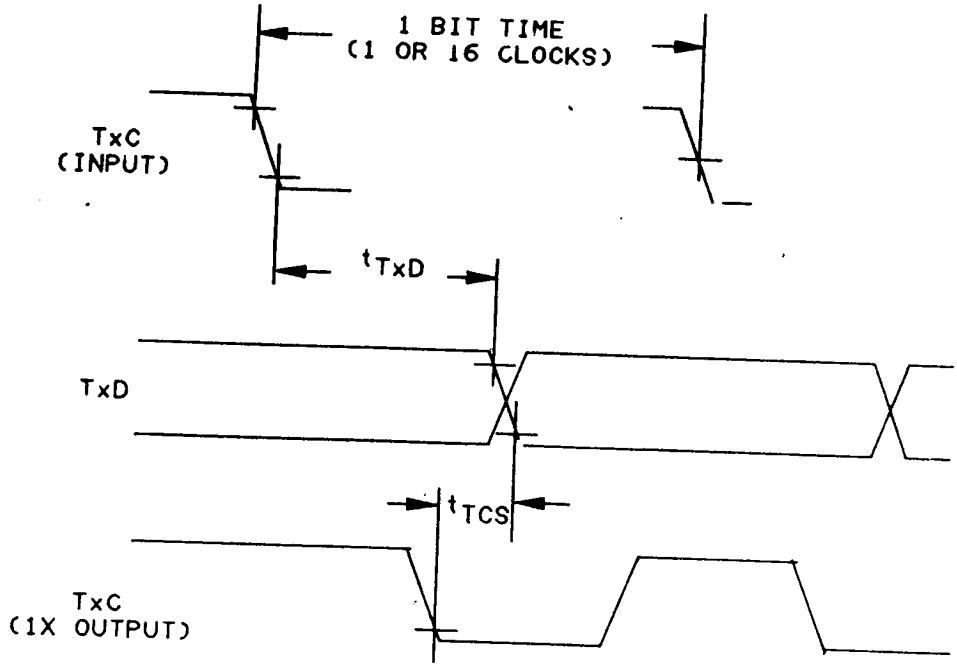


FIGURE 9. Transmitter timing.

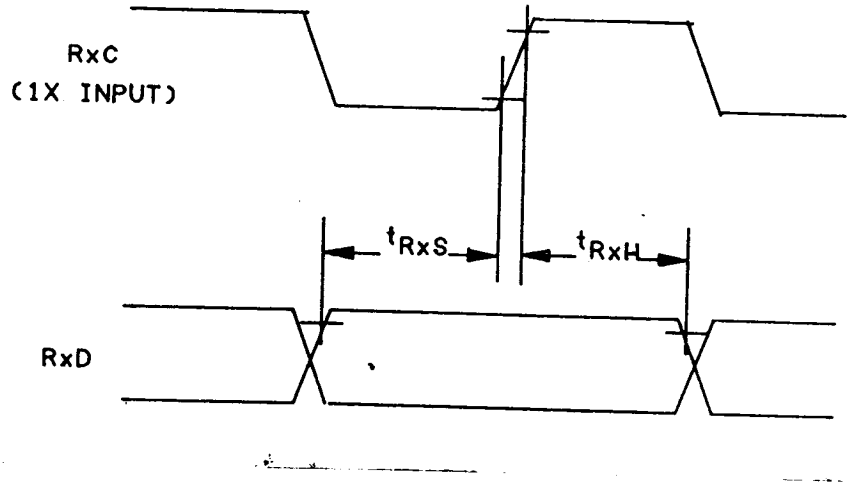


FIGURE 10. Receiver timing.

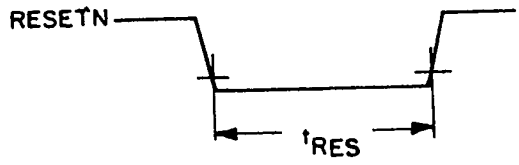


FIGURE 11. Reset timing.

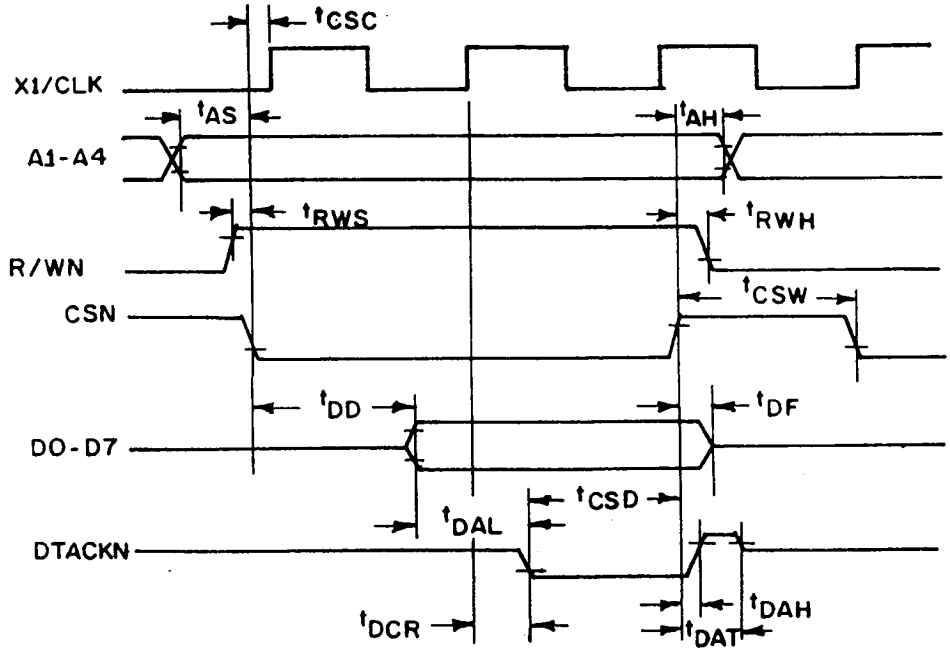


FIGURE 12. Bus timing (read cycle).

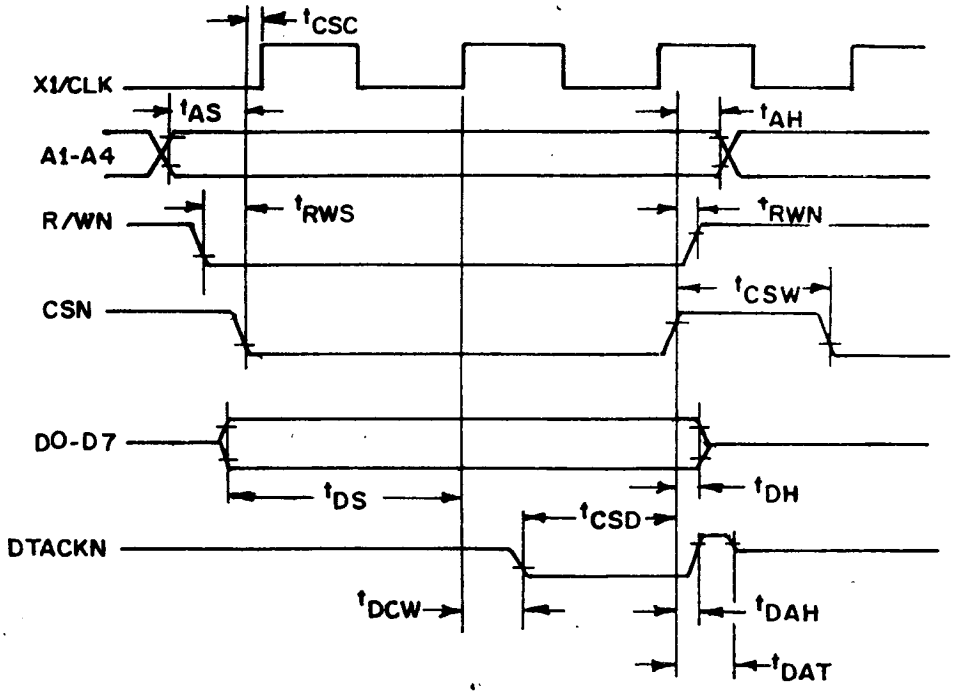


FIGURE 13. Bus timing (write cycle).

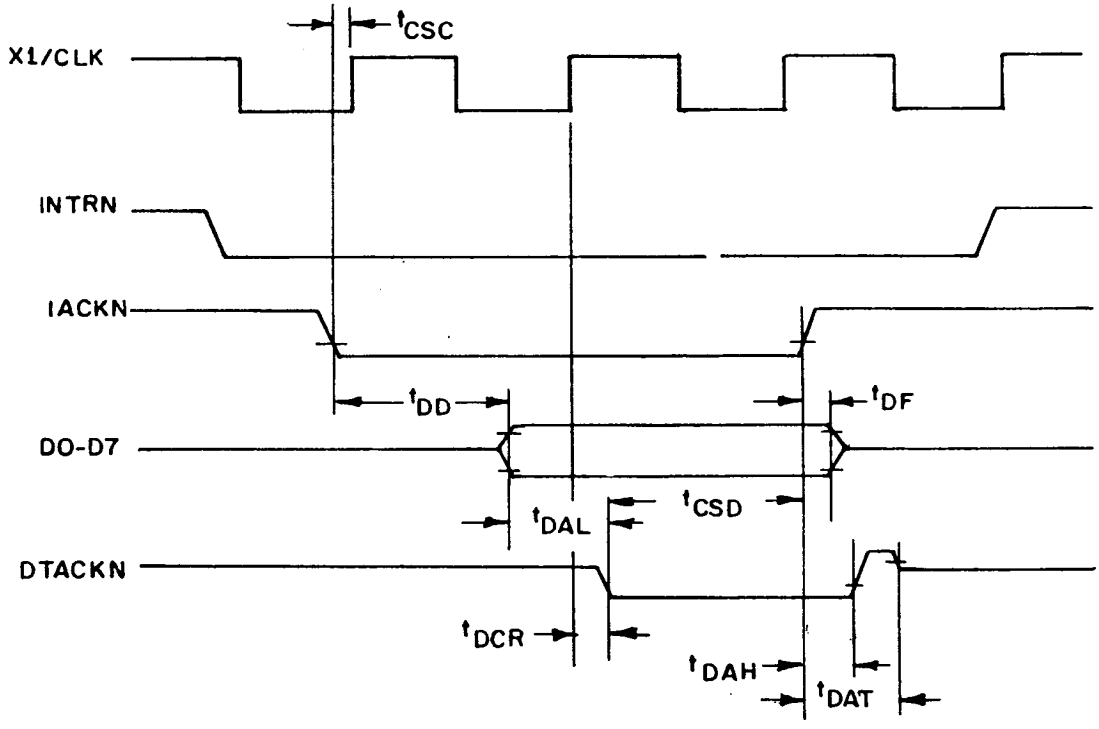


FIGURE 14. Interrupt cycle timing.

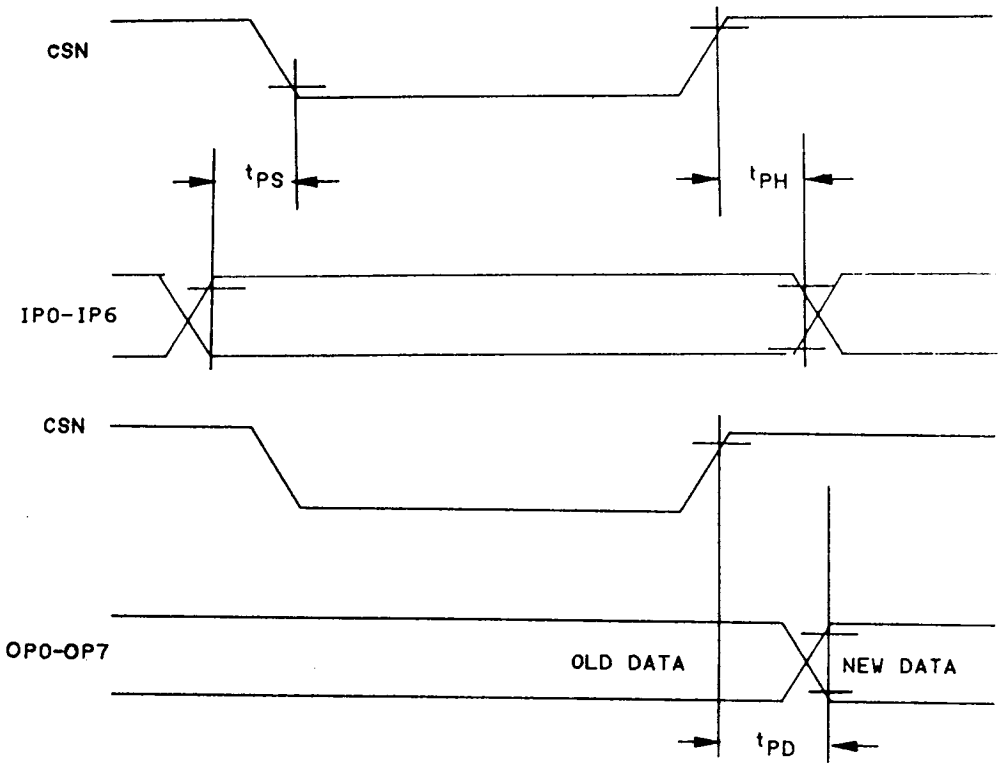
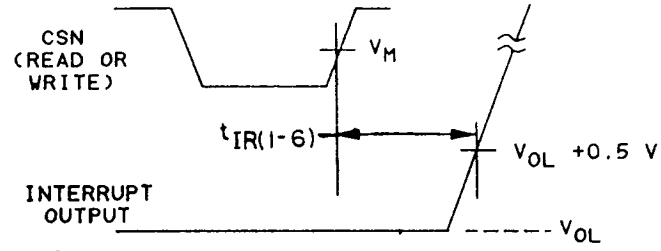


FIGURE 15. Port timing.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of the response is referenced from the midpoint of the switching signal. V_M to a point 0.5 V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuity and test environment are pronounced and can greatly affect the resultant measurement.

FIGURE 16. Interrupt timing.

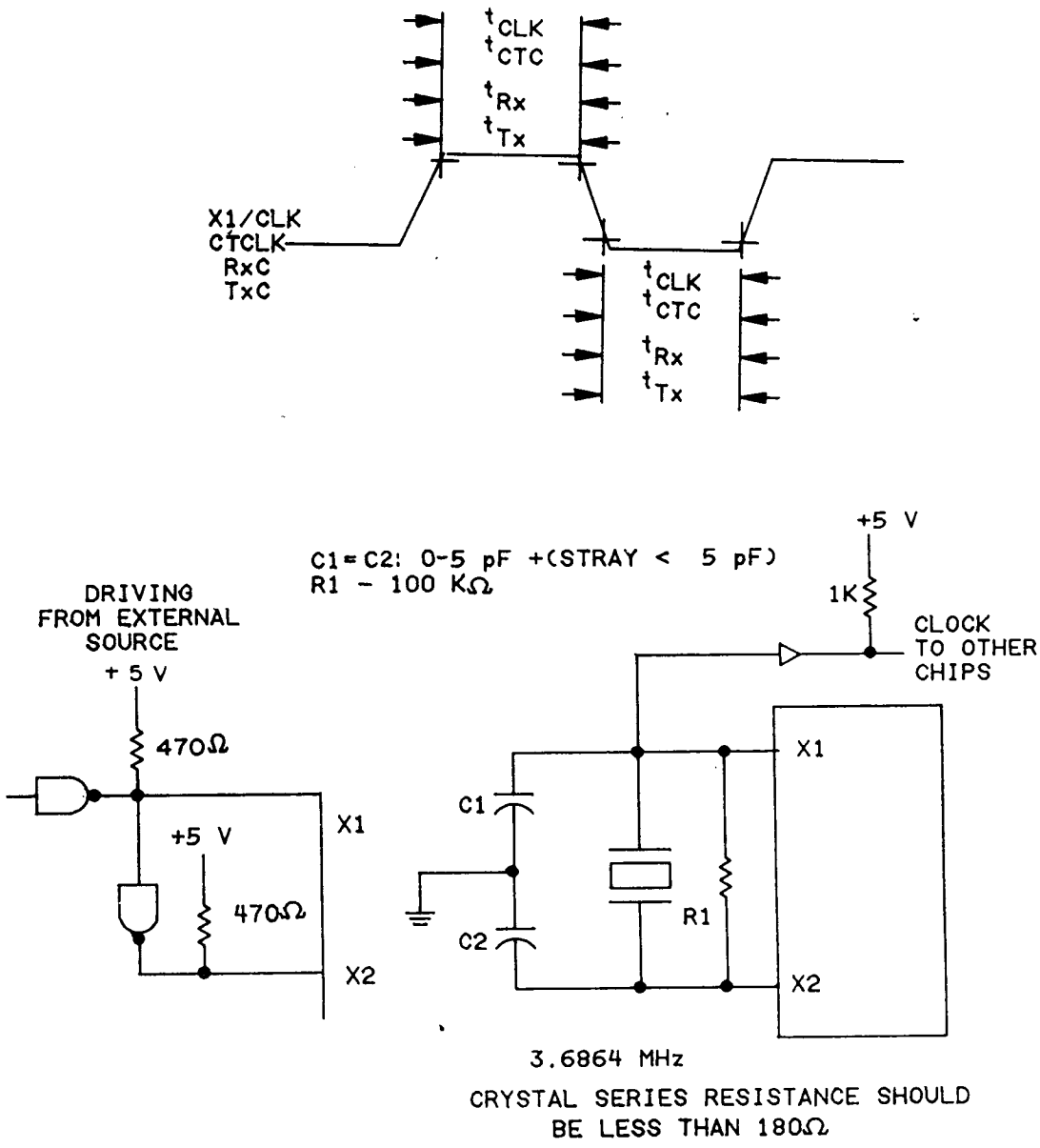


FIGURE 17. Clock timing.

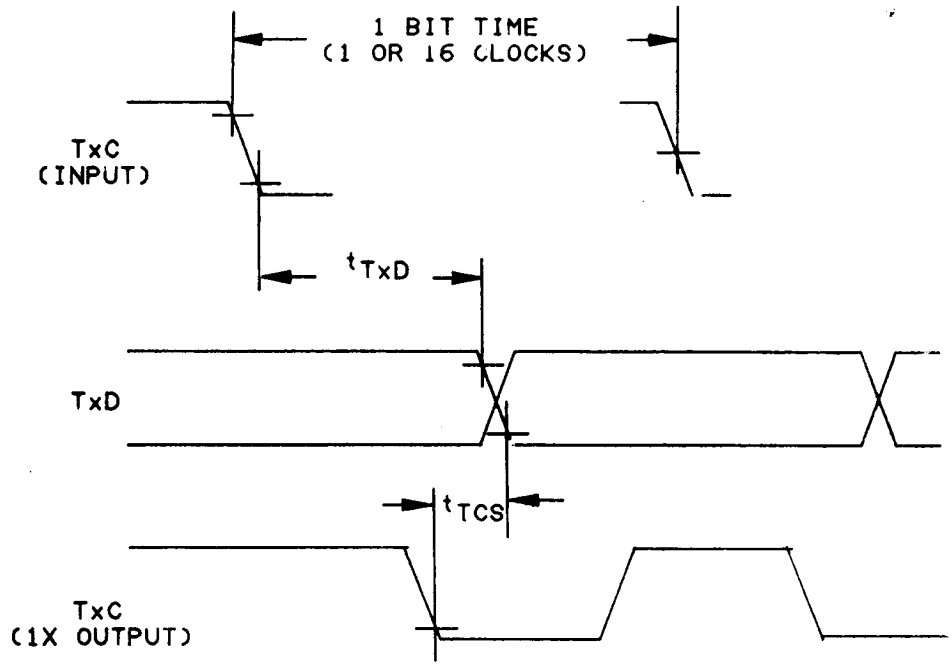


FIGURE 18. Transmitter timing.

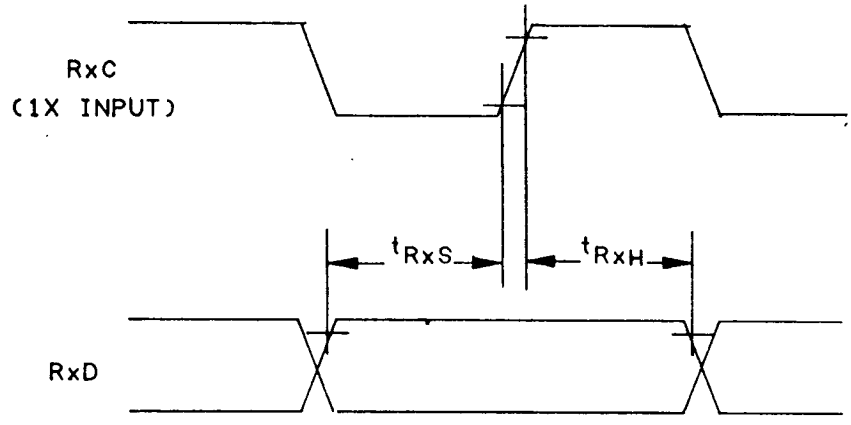


FIGURE 19. Receiver timing.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved source of supply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

1/ Any subgroup at the same temperature may be combined using a multifunction tester.

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Pin descriptions for device types 01 and 02.

Mnemonic	Package Number of pins 28 (Device 01)	40 (Device 02)	44 (Device 02)	52 (Device 02)	Type	Name and function
D0-D7	X	X	X	X	I/O	DATA BUS: Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	X	I	CHIP ENABLE: Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When high, places the D0-D7 lines in three-state condition.
WRN	X	X	X	X	I	WRITE STROBE: When low and CEN is also low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	X	I	READ STROBE: When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	X	I	ADDRESS INPUTS: Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	X	I	RESET: A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	X	O	Interrupt Request: Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	X	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 8).

6.6 Pin descriptions for device types 01 and 02 - Continued.

Mnemonic	Package Number of pins 28 (Device 01)	40 (Device 02)	44 (Device 02)	52 (Device 02)	Type	Name and function
X2	X	X	X	X		Crystal 2: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 8).
RxDA	X	X	X	X	I	Channel A Receiver Serial Data input: The least significant bit is received first. "Mark" is high, "space" is low.
RxDB	X	X	X	X	I	Channel B Receiver Serial Data input: The least significant bit is received first. "Mark" is high, "space" is low.
TxDA	X	X	X	X	O	Channel A transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "Mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
TxDB	X	X	X	X	O	Channel B Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "Mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
OP0	X	X	X	X	O	Output 0: General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated automatically on receive or transmit.
OP1	X	X	X	X	O	Output 1: General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated automatically on receive or transmit.
OP2		X	X	X	O	Output 2: General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3		X	X	X	O	Output 3: General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4		X	X	X	O	Output 4: General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5		X	X	X	O	Output 5: General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6		X	X	X	O	Output 6: General purpose output, or channel A open drain, active low, TxRDYA output.
OP7		X	X	X	O	Output 7: General purpose output, or channel B open drain, active low, TxRDYB output.

6.6 Pin descriptions for device types 01 and 02 - Continued.

Mnemonic	Package: Number of pins 28	40	44	52 — Device 01	02	02	02	Type	Name and function
IP0		X	X	X				I	Input 0: General purpose input, or channel A clear to send active low input (CTSAN).
IP1		X	X	X				I	Input 1: General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X	X	X				I	Input 2: General purpose input, or counter/timer external clock input.
IP3		X	X	X				I	Input 3: General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4		X	X	X				I	Input 4: General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5		X	X	X				I	Input 5: General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6		X	X	X				I	Input 6: General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	X				I	Power supply: +5 V supply input.
GND	X	X	X	X				I	Ground.

6.6 Pin descriptions for device type 03.

Mnemonic	Pin no.	Type	Name and function
D0-D7	25,16,24,17 23,18,22,19	I/O	DATA BUS: Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	CHIP SELECT: Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN and A1-A4 inputs. When high, places the D0-D7 lines in the three-state condition.
R/WN	8	I	READ/WRITE: A high input indicates a read cycle and a low input indicated a write cycle, when a cycle is initiated by assertion of the CSN input.
A1-A4	1,3,5,6	I	Address inputs: Selects the DUART internal registers and ports for read/write operations.
RESETN	34	I	Reset: A low clears internal registers (SRA,SRB,IMR,ISR,OPR, OPCR), initializes the IVR to hex OF, puts OP0-OP7 in the high state, stops the counter/timer, and puts channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
DTACKN	9	O	Data Transfer Acknowledge: Three-state active low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	Interrupt Request: Active low, open drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	Interrupt Acknowledge: Active low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 17).
X2	33	I	Crystal 2: Connection for other side of the crystal. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 17). If an external clock is used, this pin should be grounded.
RxDA	31	I	Channel A Receiver Serial Data input: The least significant bit is received first. "Mark" is high, "space" is low.

6.6 Pin descriptions for device type 03 - Continued.

Mnemonic	Type	Name and function
RxDB	I	Channel B Receiver Serial Data input: The least significant bit is received first. "Mark" is high, "space" is low.
TxDA	O	Channel A Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
TxDB	O	Channel B Transmitter Serial Data Output: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle, or when operating in local loopback mode. "Mark" is high, "space" is low.
OP0	O	Output 0: General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated automatically on receive or transmit.
OP1	O	Output 1: General purpose output or channel B request to send (RTSBN, active low). Can be deactivated automatically on receive or transmit.
OP2	O	Output 2: General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	Output 3: General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	Output 4: General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	O	Output 5: General purpose output or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	O	Output 6: General purpose output or channel A open drain, active low, TxRDYA output.
OP7	O	Output 7: General purpose output or channel B open drain, active low, TxRDYB output.
IP0	I	Input 0: General purpose input, or channel A clear to send active low input (CTSAN).
IP1	I	Input 1: General purpose input, or channel B clear to send active low input (CTSBN).
IP2	I	Input 2: General purpose input, or channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

6.6 Pin descriptions for device type 03 - Continued.

Mnemonic	Type	Name and function
IP3	I	Input 3: General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	Input 4: General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	Input 5: General purpose input, or channel A transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	I	Power supply: +5 V supply input.
GND	I	Ground.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.