REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 04, 05 and 06. Correct I_{OS} limits in table I. Correct figure 1. Update boilerplate. Editorial changes throughout.	93-06-18	M. L. Poelking

REV																			
SHEET																			
REV	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY GREG A. PITZ

CHECKED BY RAY MONNIN

APPROVED BY MICHAEL FRYE

DRAWING APPROVAL DATE 88-08-24

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS 16 x 16 MULTIPLIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
B	67268	**5962-86873**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-86873	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	7C516-42, 7216L40	16 x 16 multiplier	42 ns
02	7C516-55, 7216L55	16 x 16 multiplier	55 ns
03	7C516-75, 7216L75	16 x 16 multiplier	75 ns
04	7C516-30, 7216L30	16 x 16 multiplier	30 ns
05	7216L25	16 x 16 multiplier	25 ns
06	7216L20	16 x 16 multiplier	20 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP1-T64	64	Dual-in-line package
Y	CQCC1-N68	68	Square chip carrier
Z 1/	CMGA15-PN	68	Pin grid array
U	See figure 1	64	Quad flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to +7.0 V dc
DC output current	10 mA
Maximum power dissipation 3/	1.2 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, and Z	See MIL-STD-1835
Case U	30°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc to 6.0 V dc
Input low voltage (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Inactive for new design.
2/ Stress above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade the performance and affect reliability.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Input/output data formats. The input/output data formats shall be as specified on figure 3.

3.2.4 Block diagram(s). The block diagram(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5 \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA	1,2,3	All	2.4		V
Ouput low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	1,2,3	All		0.4	V
Input high voltage	V_{IH}		1,2,3	All	2.0		V
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V, GND $\le V_{IN} \le V_{CC}$	1,2,3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, $\overline{OE}$ = 2.0 V	1,2,3	All	-25	+25	µA
Output short circuit 2/ current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	1,2,3	All	-3		mA
Supply current 3/ (quiescent)	I_{CC1}	V_{CC} = 5.5 V, $V_{IH} \le V_{IN} \le V_{CC}$ or GND $\le V_{IN} \le V_{IL}$, $\overline{OE}$ = high	1,2,3	All		50	mA
Supply current 3/ (quiescent)	I_{CC2}	V_{CC} = 5.5 V, V_{CC} - 0.2 $\le V_{IN} \le V_{CC}$ or GND $\le V_{IN} \le$ 0.2 V, $\overline{OE}$ = high	1,2,3	All		25	mA
Supply current 3/ (dynamic)	I_{CC3}	V_{CC} = 5.5 V, fCLK = 10 MHz, $\overline{OE}$ = high, V_{IN} = 0.0 to 3.0 V	1,2,3	All		110	mA
Input capacitance	C_{IN}	f = 1.0 MHz, T_C = 25°C, V_{CC} = 5.0 V, See 4.3.1c; V_{IN} = 0.0 V	4	All		10	pF
	C_{OUT}	V_{OUT} = 0.0 V				12	
Functional testing		See 4.3.1d	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5 \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Unclocked multiply time	t_{MUC}	See figure 5	9,10,11	01 02 03 04 05 06		65 75 100 43 38 30	ns
Clocked multiply time	t_{MC}			01 02 03 04 05 06		42 55 75 30 25 20	
Setup time X_i, Y_i, RND, TCX and TCY	t_S			01 02 03 04,05 06	15 20 25 12 11		
Hold time X_i, Y_i, RND, TCX and TCY	t_H			01-03 04,05 06	3 2 1		
Clock pulse width (high, low)	t_{PWH} t_{PWL}			01 02 03 04,05 06	15 25 30 10 9		
$\overline{\text{MSPSEL}}$ to product out	t_{PDSEL}			01 02 03 04,05 06		25 30 35 20 18	
Output clock to P	t_{PDP}			01,02 03 04,05 06		30 35 20 18	
Output clock to Y	t_{PDY}			01,02 03 04,05 06		30 40 20 18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5 \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{OEP}$, $\overline{OEL}$ disable time	t_{PHZ} t_{PLZ}	See figure 5	9,10,11	01 02 03 04 05 06		25 31 36 20 18 15	ns
$\overline{OEP}$, $\overline{OEL}$ enable time	t_{PZH} t_{PZL}			01 02 03 04 05 06		25 30 40 20 18 15	
Clock low hold time 4/ CLKX, Y relative to CLKM, L	t_{HCL}			All	0		

1/ Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 40 pF load capacitance.

2/ For test purposes, not more than 1 output should be tested at a time. Duration of the short circuit should not be more than 1 second. Guaranteed, if not tested, to the specified limits.

3/ Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC}(ac), where I_{CC}(ac) = (8 mA/MHz) x clock frequency.

4/ To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

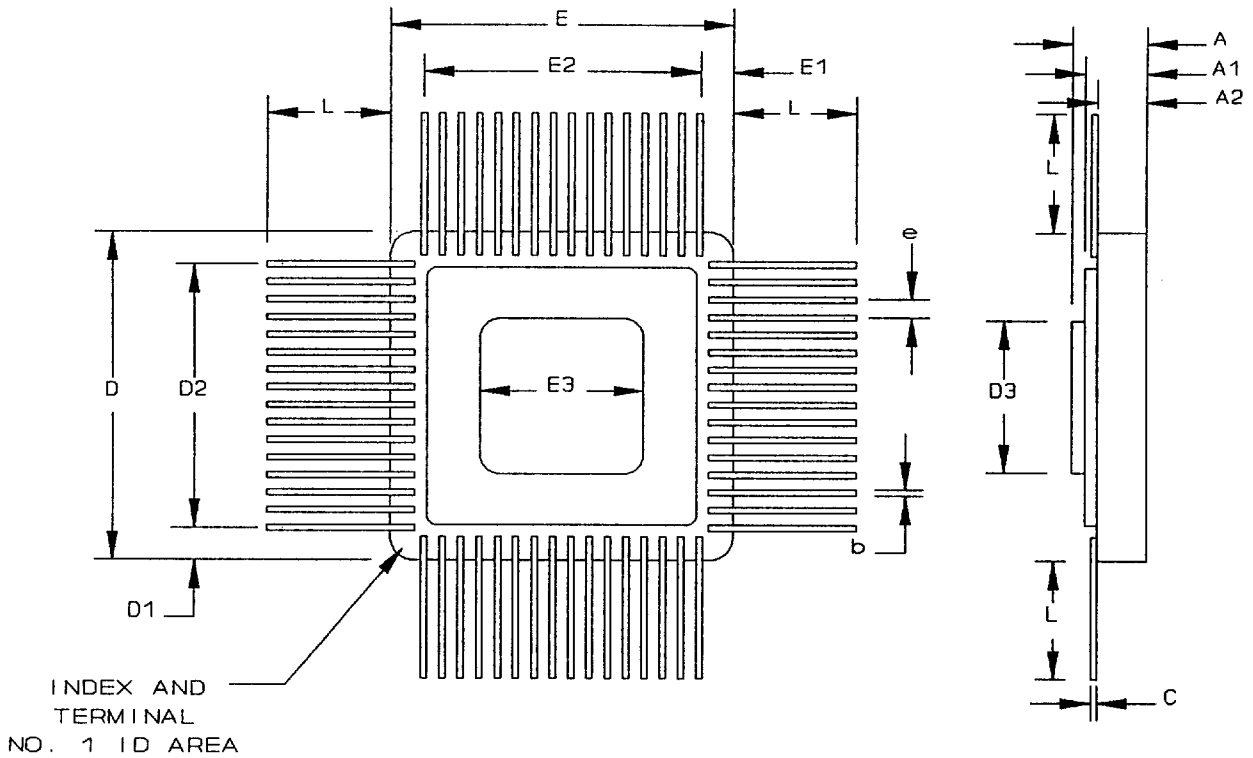
3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

CASE U



Symbol	Min	Max	Symbol	Min	Max	Symbol	Min	Max
A	.070	.090	D1	.075 REF		E2	.750 BSC	
A1	.060	.078	D2	.750 BSC		E3	.505	.535
A2	.030	.045	D3	.505	.535	L	.350	.450
b	.016	.020	e	.050 BSC		ND	16	
C	.009	.012	E	.885	.915	NE	16	
D	.885	.915	E1	.075 REF				

NOTES:
1. All dimensions are in inches unless otherwise specified.
2. BSC = basic pin spacing between centers.

FIGURE 1. Case outlines

CASE X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	X_4	17	P_8 Y_8	33	P_8 P_{24}	49	V_{CC}
2	X_3	18	P_9 Y_9	34	P_9 P_{25}	50	TCY
3	X_2	19	P_{10} Y_{10}	35	P_{10} P_{26}	51	TCX
4	X_1	20	P_{11} Y_{11}	36	P_{11} P_{27}	52	RND
5	X_0	21	P_{12} Y_{12}	37	P_{12} P_{28}	53	CLKX
6	OEL	22	P_{13} Y_{13}	38	P_{13} P_{29}	54	X_{15}
7	CLKL	23	P_{14} Y_{14}	39	P_{14} P_{30}	55	X_{14}
8	CLKY	24	P_{15} Y_{15}	40	P_{15} P_{31}	56	X_{13}
9	P_0 Y_0	25	P_0 P_{16}	41	CLKM	57	X_{12}
10	P_1 Y_1	26	P_1 P_{17}	42	OEP	58	X_{11}
11	P_2 Y_2	27	P_2 P_{18}	43	FA	59	X_{10}
12	P_3 Y_3	28	P_3 P_{19}	44	FT	60	X_9
13	P_4 Y_4	29	P_4 P_{20}	45	MSPSEL	61	X_8
14	P_5 Y_5	30	P_5 P_{21}	46	GND	62	X_7
15	P_6 Y_6	31	P_6 P_{22}	47	GND	63	X_6
16	P_7 Y_7	32	P_7 P_{23}	48	V_{CC}	64	X_5

NOTE: $\overline{\text{OEL}}$, $\overline{\text{OEP}}$ and $\overline{\text{MSPSEL}}$ are active low.

FIGURE 2. TERMINAL CONNECTIONS.

CASE Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	18	P_7 Y_{23}	35	P_7 P_7	52	X_5
2	GND	19	P_6 Y_{22}	36	P_6 P_6	53	X_6
3	GND	20	P_5 Y_{21}	37	P_5 P_5	54	X_7
4	MSPSEL	21	P_4 Y_{20}	38	P_4 P_4	55	X_8
5	FT	22	P_3 Y_{19}	39	P_3 P_3	56	X_9
6	FA	23	P_2 Y_{18}	40	P_2 P_2	57	X_{10}
7	OEP	24	P_1 Y_{17}	41	P_1 Y_1	58	X_{11}
8	CLKM	25	P_0 Y_{16}	42	P_0 Y_0	59	X_{12}
9	NC	26	NC	43	NC	60	NC
10	P_{15} P_{31}	27	P_{15} P_{15}	44	CLKY	61	X_{13}
11	P_{14} Y_{30}	28	P_{14} P_{14}	45	CLKL	62	X_{14}
12	P_{13} Y_{29}	29	P_{13} P_{13}	46	OEL	63	X_{15}
13	P_{12} Y_{28}	30	P_{12} P_{12}	47	X_0	64	CLKX
14	P_{11} Y_{27}	31	P_{11} P_{11}	48	X_1	65	RND
15	P_{10} Y_{26}	32	P_{10} P_{10}	49	X_2	66	TCX
16	P_9 Y_{25}	33	P_9 P_9	50	X_3	67	TCY
17	P_8 Y_{24}	34	P_8 P_8	51	X_4	68	V_{CC}

NOTES: $\overline{\text{MSPSEL}}$, $\overline{\text{OEP}}$ and $\overline{\text{OEL}}$ are active low.
NC = No connect.

FIGURE 2. TERMINAL CONNECTIONS - Continued.

CASE U

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{15} P_{31}	17	P_{15} Y_{15}	33	CLKY	49	X_{13}
2	P_{14} P_{30}	18	P_{14} Y_{14}	34	CLKL	50	X_{14}
3	P_{13} P_{29}	19	P_{13} Y_{13}	35	OEL	51	X_{15}
4	P_{12} P_{28}	20	P_{12} P_{12}	36	X_0	52	CLKX
5	P_{11} P_{27}	21	P_{11} Y_{11}	37	X_1	53	RND
6	P_{10} P_{26}	22	P_{10} Y_{10}	38	X_2	54	TCX
7	P_9 P_{25}	23	P_9 Y_9	39	X_3	55	TCY
8	P_8 P_{24}	24	P_8 Y_8	40	X_4	56	V_{CC}
9	P_7 P_{23}	25	P_7 Y_7	41	X_5	57	V_{CC}
10	P_6 P_{22}	26	P_6 Y_6	42	X_6	58	GND
11	P_5 P_{21}	27	P_5 Y_5	43	X_7	59	GND
12	P_4 P_{20}	28	P_4 Y_4	44	X_8	60	MSPSEL
13	P_3 P_{19}	29	P_3 Y_3	45	X_9	61	FT
14	P_2 P_{18}	30	P_2 Y_2	46	X_{10}	62	FA
15	P_1 P_{17}	31	P_1 Y_1	47	X_{11}	63	OEP
16	P_0 P_{16}	32	P_0 Y_0	48	X_{12}	64	CLKM

NOTE: $\overline{\text{OEL}}$, $\overline{\text{OEP}}$ and $\overline{\text{MSPSEL}}$ are active low.

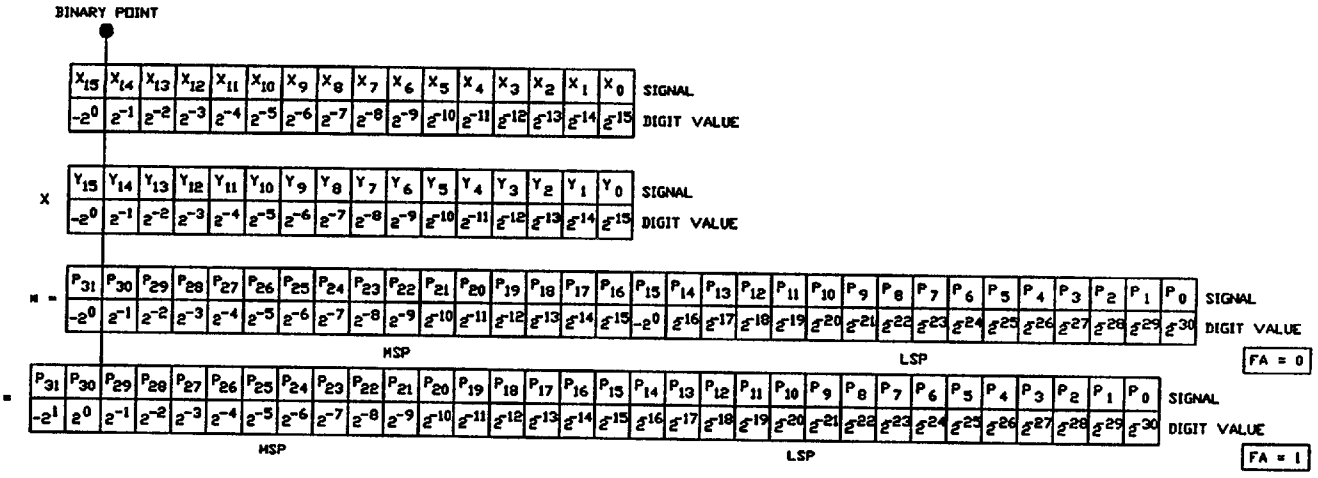
FIGURE 2. TERMINAL CONNECTIONS - Continued.

CASE Z

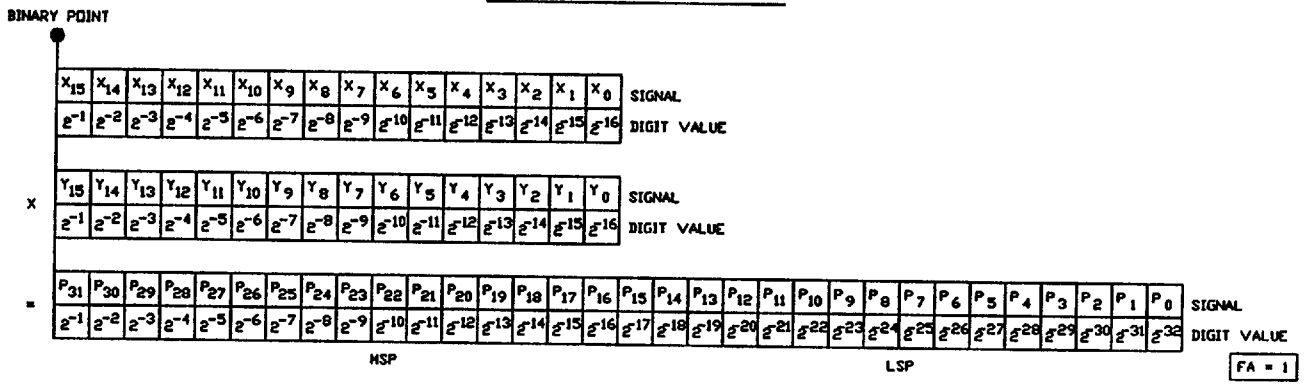
	NC	X_{13}	X_{15}	RND	TCY	V_{CC}	GND	FT	OEP	
X_{11}	X_{12}	X_{14}	CLKX	TCX	V_{CC}	GND	MSPSEL	FA	CLKM	NC
X_9	X_{10}								P_{30} P_{14}	P_{31} P_{15}
X_7	X_8								P_{28} P_{12}	P_{29} P_{13}
X_5	X_6								P_{26} P_{10}	P_{27} P_{11}
X_3	X_4				TOP VIEW				P_{24} P_8	P_{25} P_9
X_1	X_2								P_{22} P_6	P_{23} P_7
OEL	X_0								P_{20} P_4	P_{21} P_5
CLKY	CLKL								P_{18} P_2	P_{19} P_3
NC	Y_0 P_0	Y_2 P_2	Y_4 P_4	Y_6 P_6	Y_8 P_8	Y_{10} P_{10}	Y_{12} P_{12}	Y_{14} P_{14}	P_{16} P_0	P_{17} P_1
	Y_1 P_1	Y_3 P_3	Y_5 P_5	Y_7 P_7	Y_9 P_9	Y_{11} P_{11}	Y_{13} P_{13}	Y_{15} P_{15}	NC	

NOTES: $\overline{\text{OEL}}$, $\overline{\text{OEP}}$ and $\overline{\text{MSPSEL}}$ are active low.
NC = No connect

FIGURE 2. TERMINAL CONNECTIONS - Continued.



Fractional Two's Complement Notation



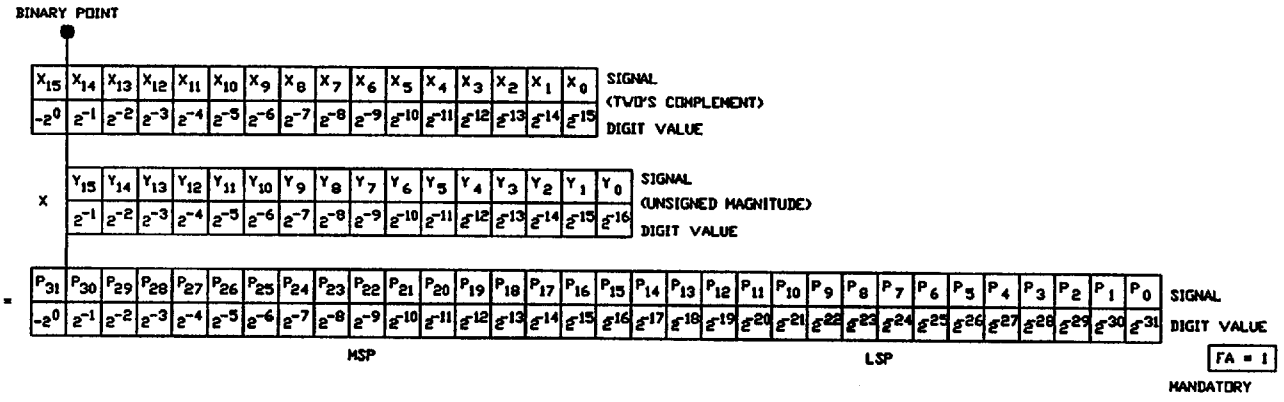
Fractional Unsigned Magnitude Notation

FIGURE 3. INPUT/OUTPUT DATA FORMATS.

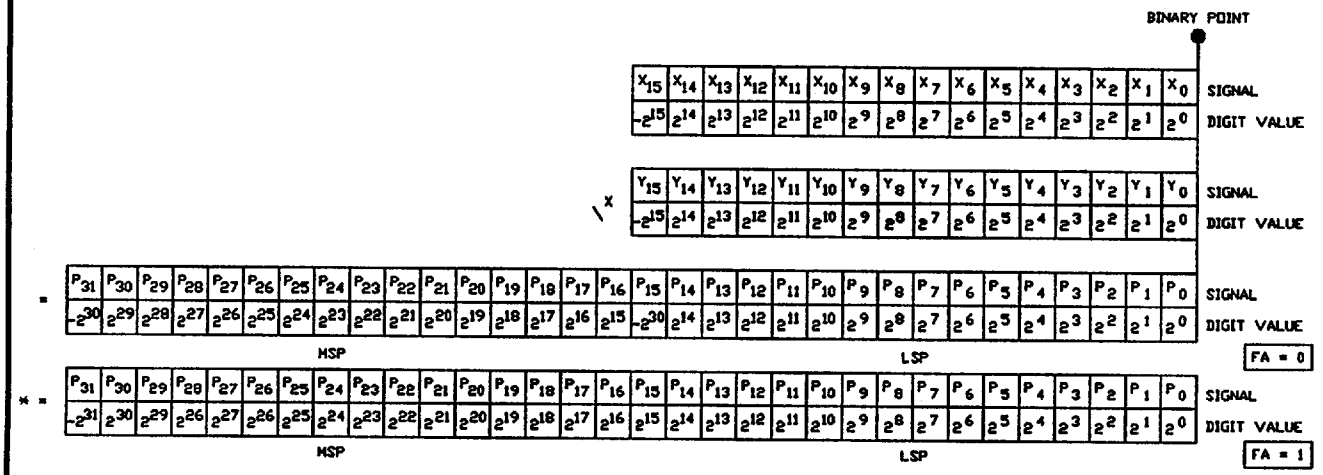
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86873
		REVISION LEVEL A	SHEET 12

DESC FORM 193A
JUL 91

9004708 0010611 780



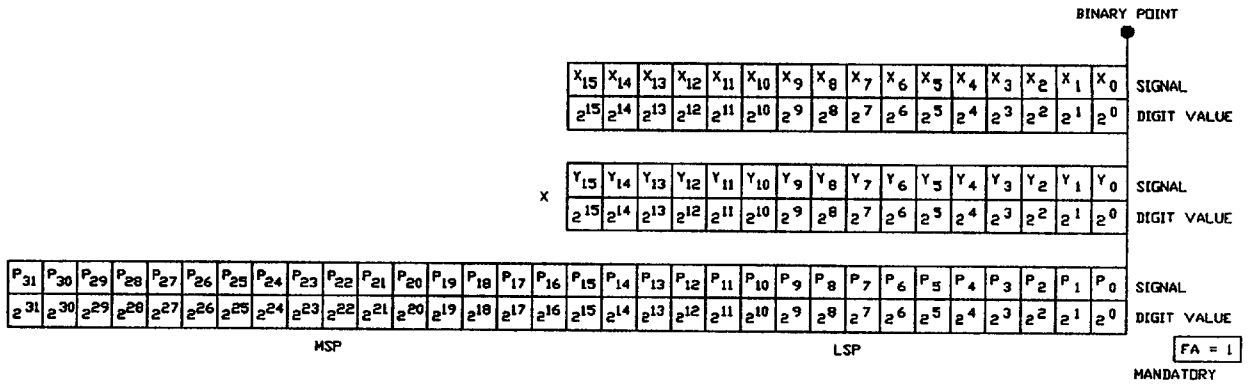
Fractional Mixed Mode Notation



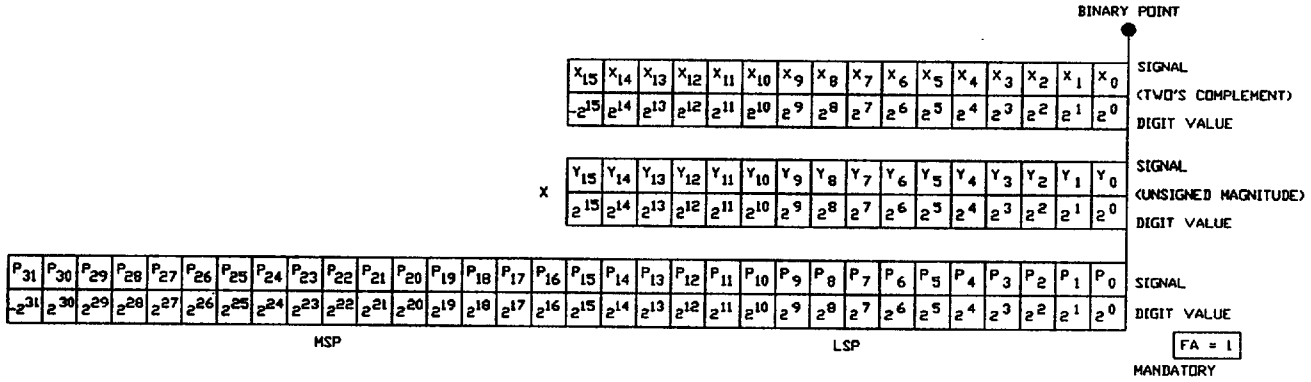
Integer Two's Complement Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

FIGURE 3. INPUT/OUTPUT DATA FORMATS - Continued.



Integer Unsigned Magnitude Notation



Integer Mixed Mode Notation

FIGURE 3. INPUT/OUTPUT DATA FORMATS - Continued.

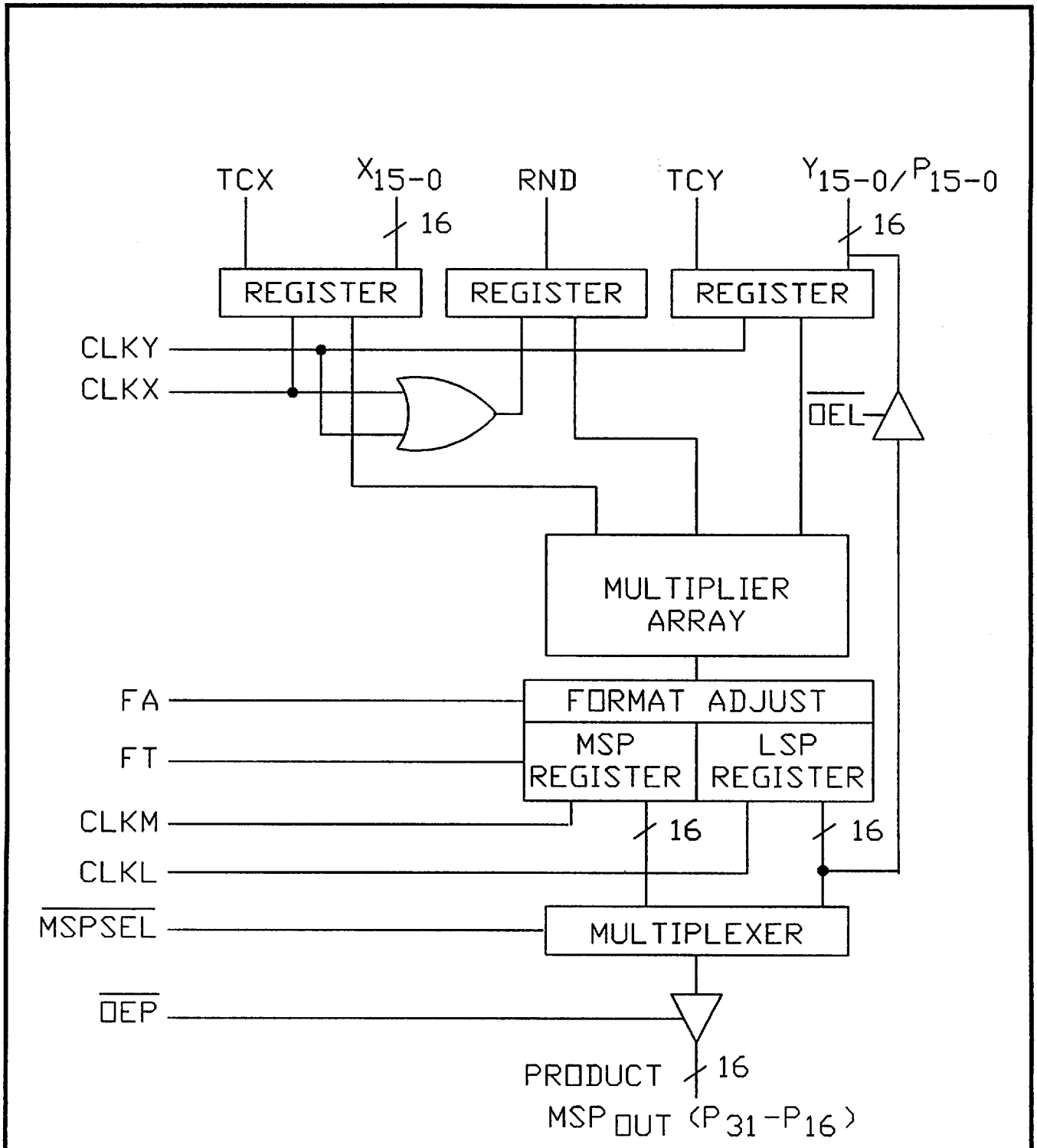
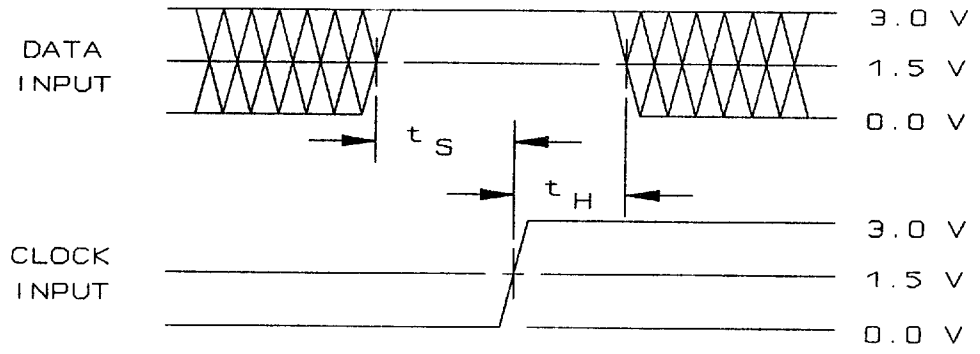


FIGURE 4. BLOCK DIAGRAM.

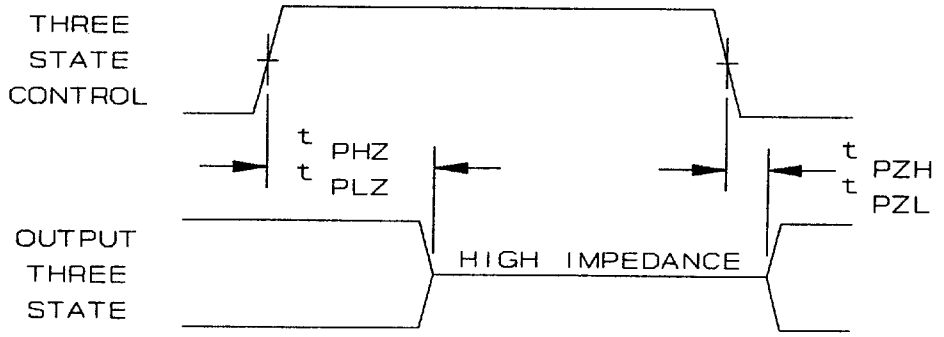
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86873
		REVISION LEVEL A	SHEET 15

Set-up and hold time



NOTE: Diagram shown for HIGH data only.
Output transition may be opposite sense.

Three-state control timing diagram



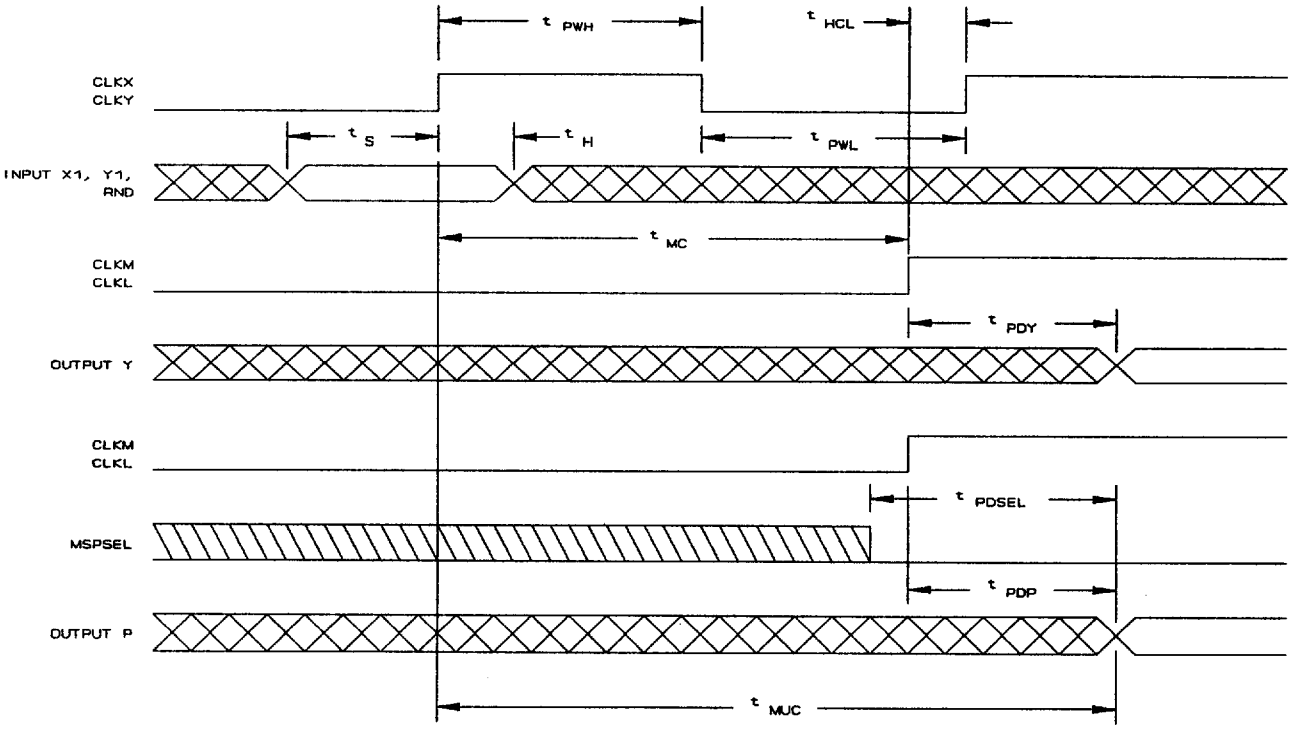
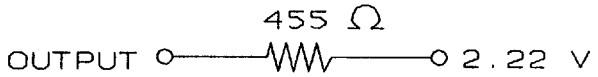
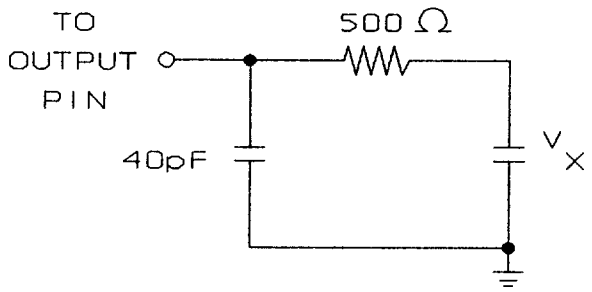


FIGURE 5. WAVEFORMS AND TEST CIRCUITS - Continued.

THEVENIN EQUIVALENT



Load A. Normal outputs.



Load B. Output three state Delay load (V_X = 0 V or 2.6 V, or equivalent)

AC TEST CONDITIONS	
Input pulse levels	GND to 3.0V
Input rise/fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V

FIGURE 5. WAVEFORMS AND TEST CIRCUITS - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the functionality of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Pin descriptions.

Pin	I/O	Description
X_{15-0}	I	X input data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	Y input/LSP output data. This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y input port may be multiplexed with the LSP output (P_{15-0}).
P_{31-16} (P_{15-0})	O	Output data. This 16-bit port may carry either the MSP (P_{31-16}) or the LSP (P_{15-0}).
FT	I	The MSP and LSP registers are made transparent (asynchronous operation) if FT is high.
FA	I	Format adjust control. If FA is high, a full 32-bit product is output. If FA is low, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be high for two's complement integer, unsigned magnitude, and mixed mode multiplication.
$\overline{\text{MSPSEL}}$	I	Output multiplexer control. When $\overline{\text{MSPSEL}}$ is low the MSP is available for output at the MSP output port, and the LSP is available at the Y input/LSP output port. When $\overline{\text{MSPSEL}}$ is high, the LSP is available at both ports (above) and the MSP is not available.

6.6 Pin descriptions - Continued.

RND	I	Round control. When RND is high, a one is added to the MSB of the LSP. This position is dependent on the FA control; FA = high means RND adds to the 2^{-15} bit (P_{15}), FA = low means RND adds to the 2^{-16} bit (P_{14}).
TCX	I	Two's complement control X. X input data are interpreted as two's complemented when TCX is high. TCX low means the data are interpreted as unsigned magnitude.
TCY	I	Two's complement control Y. Y input data are interpreted as two's complement when TCY is high. TCY low means the data are interpreted as unsigned magnitude.
$\overline{OEP}$	I	P_{31-16}/P_{15-0} output port three state control. When $\overline{OEP}$ is low, the output port is enabled; when $\overline{OEP}$ is high, the drivers are in a high impedance state.
$\overline{OEL}$	I	Y-in/P_{15-0} port three state control. When $\overline{OEL}$ is low, the timeshared port is enabled for LSP output. When $\overline{OEL}$ is high, the output drivers are in a high impedance state. This is required for Y input.
CLKX	I	X register clock. X input data and TCX are latched in at the rising edge of CLKX.
CLKY	I	Y register clock. Y input data and TCY are latched in at the rising edge of CLKY.
CLKM	I	MSP register clock. The most significant product (MSP) is latched in at the MSP register at the rising edge of CLKM.
CLKL	I	LSP register clock. The least significant product (LSP) is latched in at the LSP register at the rising edge of CLKL.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.